Static Timing Analysis using PrimeTime

Lab Manual

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1. Lab 01 - PrimeTime Flow

Objective : *To be familiar with Prime Time and understand how to read and analyze setup/hold reports*

Working Directory : /home/<user_name>/PD_Labs/PT/Lab01
Relevant Files & Directories :

Lab01	: current working directory
common_setup.tcl	: multi tool shared setup file
pt_shell.tcl	: tool specific PrimeTime setup file.
pt_scripts	: Run file directory
pt.tcl	: Run file
.synopys_pt.setup	: Automatically read PT setup file
orca_savesession	: Saved Session directory
RUN.tcl	: Run script for orca_savesession

Learning outcomes:

- ✓ How to create a session for later usage
- ✓ How to restore a saved session
- ✓ How to validate a restored session
- ✓ Understanding the basic PrimeTime flow
- ✓ To understand how to read and understand the timing reports.

1.1 Task 1 : Restore a PrimeTime Session

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Invoke PrimeTime from the lab1 directory.

```
PT_Labs]$ cd Lab01/
Lab01]$ pt_shell
```

✓ Restore a previously saved PrimeTime session. This step will read in the design netlist, libraries, and constraints. The design is now ready for analysis.

- Note: The orca_savesession below is a Unix directory.
- Note: The orca_savesession can be recreated, if needed, using:

```
pt_shell -f RUN.tcl | tee -i run.log
```

- Note: Any PARA-124 Errors during the execution of RUN.tcl (within the parasitics_command.log file) can be safely ignored for the purpose of our labs.
- Note: Prime Time supports command, option, variable and file completion. Type a few letters and then hit the tab key.

```
pt_shell> restore_session orca_savesession
```

✓ Generate coverage analysis report

```
pt_shell> report_analyis_coverage
```

- **Question 1 :** What is the name of the design under analysis?

  ……
  ……
  ……

- **Question 2 :** How many setup and hold violations does ORCA have?

  ……
  ……
  ……

✓ Generate global timing report

```
pt_shell> report_global_timing
```

- **Question 3 :** How many reg-reg setup and hold violations are there?

  ……
  ……
  ……

1.2 Task 2 : Explore some helpful commands

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Execute the following three history short cut commands:

```
pt_shell> history
pt_shell> !!
pt_shell> !2
```

- **Question 4 :** Describe the difference between the last two history commands above.

  ……
  ……
  ……

✓ Use up and down arrows to scroll through the history event list as an alternative to the previous step. Type the following to see all the available key bindings (in the default emacs editing mode).

```
pt_shell> list_key_bindings
```

✓ Explore the page mode alias; execute the following command, which will generate a report that scrolls off the screen.

```
pt_shell> report_timing -group [get_path_group *]
```

✓ Turn on the page mode

```
pt_shell> page_on
pt_shell> !rep
```

✓ Use the space bar and Enter keys to page through a long report. Quit from a long report in page mode by typing "g*. If you want to turn off page mode, use the command alias page off.

✓ Find the command to restore a PrimeTime session and then display help information on this command.

```
pt_shell> help restore*
pt_shell> view man restore_session
pt_shell> restore_session -help
```

- **Note :** The following is an alternative way to display syntax help

```
pt_shell> help -v restore_session
```

- **Question 5 :** From the last command above. does the command restore session accent switches?.

……
……
……

✓ The time unit in PrimeTime is determined by the main technology library. To find the time unit for ORCA, first list all libraries in memory.

- **Note :** The * in the following report indicates the main library.

```
pt_shell> list_lib
```

✓ Generate a report for the main library which will state the time unit.

- **Note :** Use copy and paste to avoid mistyping the lib name. The time unit is at the very top of the report.

```
pt_shell> report_lib cb13fs120_tsmc_max
```

- **Question 6 :** What is the time unit used for timing reports (as well as all other reports) for the ORCA design?

……
……
……

- **Note :** Do not forget to use "q" to quit from a long report in page mode and return to the pt_shell prompt without reading the entire report.

✓ Display units used by the current design.

```
pt_shell> report_units
```

1.3 Task 3 : Validate an Existing PrimeTime Session

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions. In this task, you will validate the inputs that have been read into Prime Time: the current design and libraries, the back annotation and constraints.

✓ Verify that the current design is your top-level module: ORCA.

```
pt_shell> current_design
```

✓ Compare the unix paths of the libraries to what has been read into Prime Time.

```
pt_shell> printvar search_path
pt shell> printvar link_path
pt shell> list_libraries
```

- **Question 7 :** Have the 4 libraries in the link_path been successfully read into PrimeTime?

  ……
  ……
  ……

- **Question 8 :** Which library defines the defaults for time units, operating conditions, and other delay calculation information?

  ……
  ……
  ……

- **Question 9 :** What time unit is used?

  ……
  ……
  ……

✓ Verify that the nets are completely annotated..

```
pt_shell> report_annotated_parasitics
```

- **Question 10 :** Are there any nets that are not annotated?

  ……
  ……
  ……

- **Question 11 :** What option to report_annotated_parasitics would be good to use as a 'next step' in debugging the missing nets?

  ……
  ……
  ……

✓ Verify that the design is completely constrained.

```
pt_shell> check_timing
```

- **Question 12 :** What option to check_timing would be good to use as a 'next step' in debugging the missing constraints?

  ……
  ……
  ……

✓ Verify that the checks in your cells are completely exercised; look at possible causes for your findings.

```
pt_shell> report_analysis_coverage
pt_shell> report_case_analysis
```

- **Question 13 :** Is it logical that many of your timing checks are untested?

  ……
  ……
  ……

✓ Quit PrimeTime.

```
pt_shell> quit
```

1.4 Task 4 : Execute the Run Script and Analyze the run

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Execute the run script logging the results to the log file run. log.

```
Lab01]$ pt_shell -f ./pt_scripts/pt.tcl | tee -i run.log
```

- **Question 14 :** Were there any errors during the execution of the run script?

  ……
  ……
  ……

✓ If there are any errors, address these first before moving on to the next step.

✓ Evaluate your log file. With a text editor, open your log file. Search for the update timing messages (UITE-214), **`print_message_info`** output, and the exit output. Then, in your **`profile`** directory, examine the file **`tcl_profile_sorted_by_cpu_time`**.

- **Question 15 :** What step required the most CPU time?

  ……
  ……
  ……

- **Question 16 :** What commands were causing UITE-214 messages?

  ……
  ……
  ……

- **Question 17 :** Can any of the timing updates be avoided?

  ……
  ……
  ……

- **Question 18 :** Why might the exit command output be a good place to start before reviewing your log file?

  ……
  ……
  ……

1.5 Task 5 : Analyze STA Reports

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions. Generate and interpret two STA reports for setup and hold for SYS_CLK.

✓ Invoke PrimeTime and restore the session that you saved in the previous task.

```
Lab01]$ pt_shell
pt_shell> restore_session my_savesession
```

✓ Execute the following to display the clocks in ORCA:.

```
pt_shell> report_clock
```

- **Question 19 :** How many clocks are in ORCA?

  ……
  ……
  ……

✓ Create a single, "short" timing report for setup for the clock SYS_CLK. Use command-line expansion (the tab key) to expand both the command AND the options **-group** and **-path**.

```
pt_shell> report_timing -group SYS_CLK -path short
```

- **Note :** The lines containing the data path cells and their delays are removed from the data arrival section making this report.

- **Note :** The above command generates a report for setup by default.

- **Question 20 :** There are at least 4 clues that this report is for setup and not for hold. How many can you identify?

  ……
  ……
  ……

- **Question 21 :** Identify the instance names of the start and end point flip-flops.

  ……
  ……
  ……

- **Question 22 :** The clock skew for this timing path is 0.511ns; which two lines in the report can you use to calculate this?

  ……
  ……
  ……

- **Question 23 :** How does this clock skew affect slack (i.e. does the clock skew help or hurt slack)?

  ……
  ……
  ……

- **Question 24 :** How large is the violation in comparison to the clock period?

  ……
  ……
  ……

✓ Generate a timing report for hold time.
The following is a short cut that will execute the last command in history starting with the letters **"rep"** and add the switch **-delay min** (which will generate a report for hold time).

```
pt_shell> !rep -delay min
```

- **Question 25 :** There are at least 4 clues that indicate this is a hold report and not a setup report. How many can you find?

  ……
  ……
  ……

- **Question 26 :** How does the clock skew in this hold report affect slack (i.e. does the clock skew help or hurt slack)?

  ……
  ……
  ……

✓ Quit PrimeTime.

```
pt_shell> quit
```

2. Lab 02 - writing constraints and validating them

Objective : *To understand how to validate the constraints and how to interpret constraints in a timing report*

Working Directory : /home/<user_name>/PD_Labs/PT/Lab02
Relevant Files & Directories :
Lab02 : current working directory
.synopys_pt.setup : Automatically read PT setup file
orca_savesession : Saved Session directory
RUN.tcl : Run script for orca_savesession

Learning outcomes:

- ✓ How to validate the constraints for constraint completeness
- ✓ How to validate the constraints for untested timing checks
- ✓ How to interpret the timing constraints

2.1 Task 1 : Validate Constraints

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

- ✓ Invoke PrimeTime from the lab2 directory and restore a previously saved PrimeTime session using the orca_savesession directory.
  - Note: The orca_savesession can be recreated, if needed, using:

```
pt shell - RUN.tcl | tee -i run. log
```

  - Note: Any PARA-124 Errors during the execution of RUN.tcl can be safely ignored for the purpose of our labs.

- ✓ Check for constraint completeness.

```
pt_shell> check_timing -verbose
```

  - **Question 1 :** Are all registers in the design clocked?

    ……
    ……
    ……

  - **Question 2 :** Are there any missing constraints? Can you explain?

    ……
    ……
    ……

✓ Check for the untested timing checks in the design

```
pt_shell> report_analysis_coverage
```

- **Question 3 :** Nearly two thirds of the setup/hold checks are untested! - What are the 2 causes?

  ……
  ……
  ……

- **Question 4 :** Why are there unexercised min_pulse_width checks?

  ……
  ……
  ……

- **Question 5 :** How many output delay constraints are there for setup and for hold and are these constraints met or violated?

  ……
  ……
  ……

2.2 Task 2 : Analyse Timing Report for Input Delay Constraint

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Generate a report for the input delay constraints applied to the port **`pad[0]`**.

```
pt_shell> report_port -input_delay pad[0]
```

- **Question 6 :** What are the min and max arrival times to pad [0] ?

  ……
  ……
  ……

- **Question 7 :** What is the name of the external start point clock constraining pad [0]?

  ……
  ……
  ……

✓ Generate a timing report for setup starting at the port **`pad[0]`**. Answer the following questions using this report. Use your job aid labelled "timing reports" for help recalling the appropriate switch for report_timing.

- **Question 8 :** Which lines in the timing report did you use to ensure the reported path starts at the port pad [01 and is for setup?

  ……
  ……
  ……

- **Question 9 :** List all user specified constraints in this timing report.

  ……
  ……
  ……

- **Question 10 :** Where must the clock latency be included for the start point clock PCI_CLK?

  ……
  ……
  ……

- **Question 11 :** Describe the direction of the port pad [0] (i.e. is it an input, output or inout port)

  ……
  ……
  ……

- **Question 12 :** Describe the end point of this timing path (i.e. is it an output port or an internal flip-flop).

  ……
  ……
  ……

✓ Generate a new report from the same port pad [0] for setup, which also shows the details of the calculated clock network delay. Use the job aid labelled "timing reports" for help recalling the appropriate switch for report timing. Remember to take advantage of history commands.

- **Question 13 :** How large is the clock source latency versus the clock network latency for the end point clock PCI CLK?

  ……
  ……
  ……

- **Question 14 :** Where has the clock PCI CLK been defined (the clock definition point)?

  ……
  ……
  ……

✓ Generate a report starting at the port pad [0) for hold time.

- **Question 15 :** Does the value of the input external delay constraint match your expectations?

  ……
  ……
  ……

2.3 Task 3 : Analyse Timing Report for Output Delay Constraint

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Generate a report for the output delay constraints applied to the port `pad[0]`.

- **Question 16 :** What are the min and max output delay constraints for this port?

  ……
  ……
  ……

- **Question 17 :** How will the negative min output delay constraint be applied to this port (i.e. will it impose a positive or negative hold requirement)?

  ……
  ……
  ……

- **Question 18 :** What is the name of the external end point clock constraining this port?

  ……
  ……
  ……

✓ Generate a "short timing report ending at the port pad [0] for hold time.

- **Question 19 :** Describe the start point of this timing path (i.e. is it an input port or an internal flip-flop).

  ……
  ……
  ……

- **Question 20 :** Does the path group for this timing path match your expectations?

  ……
  ……
  ……

- **Question 21 :** Does the "data required time" match your expectations?

  ……
  ……
  ……

✓ Optionally, apply the following constraint which will impose a positive output delay constraint for hold on pad [0] and then re-execute the steps in this task to see the affect.

```
pt_shell> set_output_delay -min 1.0 -clock PCI_CLK pad[0]
```

✓ Quit PrimeTime.

.

3. Lab 03 – Generating Timing Reports and analysing them

Objective : *To understand how to generate timing reports and how to understand how to analyzing them.*

Working Directory : /home/<user_name> PD_Labs/PT/Lab03
Relevant Files & Directories :
Lab03 : current working directory
.synopys_pt.setup : Automatically read PT setup file
orca_savesession : Saved Session directory
RUN.tcl : Run script for orca_savesession

Learning outcomes:

- ✓ How to generate summary report for the violations
- ✓ How to analyze the timing reports for setup and hold
- ✓ How to apply the switches to timing report commands
- ✓ How to identify the clock cycle paths

3.1 Task 1 : Setup PrimeTime for Lab3

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

- ✓ Invoke Prime Time from the lab3 reports workshop lab directory. Restore the PrimeTime session using the orca_savesession directory.
  - Note: The orca_savesession can be recreated, if needed, using:

```
pt shell - RUN.tcl | tee -i run. log
```

  - Note: Any PARA-124 Errors during the execution of RUN.tcl can be safely ignored for the purpose of our labs.

- ✓ Find the variable that controls the significant digits for many reports and set it to 4 significant digits. (Hint: aa significant].
  - **Question 1 :** What is this variable's default value? [Hint: man page]

……..
……..
……..

3.2 Task 2 : Generate Summary Reports

Instructions : Follow the below instructions.

- ✓ Answer the following questions by generating the appropriate summary reports:
  - **Question 2 :** Identify the top five setup violations with the worst slack. The required details are me endpoint names and the slack.

    ……
    ……
    ……
  - **Question 3 :** List the 2 clock domains that have violating setup timing paths, and the 5 clock domains that have violating hold timing paths (ORCA has 6 clock domains in total).

    ……
    ……
    ……
  - **Question 4 :** Identify how many hold violations are on input paths, how many on output paths, and how many are register-to-register violations.

    ……
    ……
    ……
- ✓ Generate a report for the worst slack for setup to each bit of a 16-bit bus ending at the output ports sd_DQ (0] to sd_DQ [15] (the output ports are all constrained by a single clock, SD DDR CLK).
  - **Question 5 :** List the end point with the largest margin (the best slack).

    ……
    ……
    ……
- ✓ Generate a high-level overview of the quality of the design.
  - **Question 6 :** Which clock group has the highest number of violating paths?

    ……
    ……
    ……

3.3 Task 3 : Analyse Timing Reports for Setup and Hold

Instructions : Follow the below instructions.

- ✓ Turn Page Mode on.
- ✓ Execute the following command to generate a timing report for PCI CLK:

```
pt_shell> report_timing -group PCI_CLK
```

- **Question 7 :** Does this timing path meet or violate timing?

  ……
  ……
  ……

- **Question 8 :** What type of timing path is this - internal flip-flop to flip-flop, input, or output timing path?.

  ……
  ……
  ……

- ✓ Generate a timing report for hold time for the same clock group PCI_CLK.

```
pt_shell> report_timing -group PCI_CLK -delay min
```

- **Question 9 :** What type of timing path is this - internal flip-flop to flip-flop, input, or output timing path?

  ……
  ……
  ……

- **Question 10 :** How many cells are on the data path of this timing path?

  ……
  ……
  ……

- **Question 11 :** The cell delays used are rise delays. Offer one reason why this would result in a worse slack for hold than using fall delays?

  ……
  ……
  ……

- ✓ In the next step, you will continue to explore and confirm your answer for the above question.

- **Question 12 :** What additional information do you need to confirm your answer for the above question?

  ……
  ……
  ……

✓ Generate another timing report for the same timing path for hold time but with a fall transition at the end point (instead of a rise transition). Use copy and paste to avoid mistyping the end point and start point pin names. Use the job aid labelled "timing reports" to find the appropriate switches for report_timing.

- **Question 13 :** Which lines in this report did you use to confirm that the correct path has been reported?

  ……
  ……
  ……

- **Question 14 :** Was the guess correct - the faster fall delays results in a faster data arrival time but a smaller hold time requirement and thus a better slack?

  ……
  ……
  ……

3.4 Task 4 : Apply the Correct Timing Report Switches

Instructions : Follow the below instructions.

✓ Answer the following questions by experimenting and exploring in Prime Time. Use the job aid labelled "timing reports" for help identifying the appropriate commands and switches.:

- **Question 15 :** Write the command to generate a single timing report for each path group for setup.

  ……
  ……
  ……

- **Question 16 :** Write the command to generate a single timing report for setup for each path group which has a violation..

  ……
  ……
  ……

- **Question 17 :** What are the names of the two path groups that have violating timing paths in ORCA (the answer will come from the result of the previous question)?

  ……
  ……
  ……

- **Question 18 :** Write the command to generate a timing report with the worst slack for setup to any output port constrained by the clock PCI_CLK.

  ……
  ……
  ……

- **Question 19 :** There are a few latches in ORCA; write the command to identify the data pins of these latches.

  ……
  ……
  ……

- **Question 20 :** Write the command to generate a timing report for hold to the D pin of the latched_cik_en_reg latches.

  ……
  ……
  ……

3.5 Task 5 : Identify Half-Clock Cycle Paths

Instructions : The clock SDRAM_CLK constrains many half clock cycle paths in ORCA (i.e. it constrains paths from a falling edge triggered flip-flop to a rising edge triggered flip-flop and vice versa). These paths must be carefully monitored for various reasons (e.g. the duty cycle of SDRAM_CLK is not yet well defined or for analysis of the clock skew)..

✓ Execute the following command to report the clock period for SDRAM CLK and use this information to answer the following questions:

```
pt_shell> report_clock SDRAM_CLK
```

- **Question 21 :** Given that the first number under the waveform column is the first rising edge for the clock SDRAM CLK and the second number is the falling edge - what duty cycle has been defined for this clock?

  ……
  ……
  ……

- **Question 22 :** Describe the specific clock edges that will be used in a timing report for setup for a timing path constrained by the rising edge of SDRAM_CLK to the falling edge of SDRAM_CLK.

  ……
  ……
  ……

- **Question 23 :** For this same timing path, describe the specific clock edges that will be used in a timing report for hold timing checks.

  ……
  ……
  ……

✓ Confirm the information in the following table by generating the appropriate timing reports for the half clock cycle timing paths constrained by the clock SDRAM_CLK.

Launch Clock Edge	Capture clock edge	Worst Setup Slack	Launch clock edge	Capture clock edge	Worst Hold Slack
Rise 0ns	Fall 3.75ns	0.680ns	Rise 7.5ns	Fall 3.75ns	3.558ns
Fall 3.75ns	Rise 7.50ns	0.635ns	Fall 3.75ns	Rise 0ns	3.514ns

- **Question 24 :** Which switch is useful for generating the worst 10 timing reports for each of these half clock cycle timing paths?

  ……
  ……
  ……

- **Question 25 :** Why does PrimeTime report "no constrained paths?" (hint. the options PrimeTime is using are shown immediately following the report timing command).

  ……
  ……
  ……

- **Question 23 :** What additional option must you use to report the worst 10 timing paths?

  ……
  ……
  ……

✓ Quit PrimeTime.

4. Lab 04 - Constraining multiple clocks

Objective : *To understand how to PrimeTime commands to gather information about the design clocks and use the GUI for another view of the design clocks.*

Working Directory : /home/<user_name> PD_Labs/PT/Lab04
Relevant Files & Directories :

Lab04	: current working directory
.synopys_pt.setup	: Automatically read PT setup file
orca_savesession	: Saved Session directory
orca_savesession_violations	: Saved ORCA Session with an issue
RUN.tcl	: Run script for ORCA
scripts/orca_pt_variables.tcl	: Run script for ORCA

Learning outcomes:

- ✓ How to use PT commands to get the information of clocks
- ✓ How to use GUI to view the design clocks

4.1 Task 1 : Get to Know the Design Clocks

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

- ✓ Make sure your current directory is Lab04.
- ✓ Invoke PrimeTime (pt_shell) and restore the session saved in orca_savesession.
  - **Question 1 :** How many clocks are in this design and how many of these are generated?

    ……
    ……
    ……
  - **Question 2 :** Which input ports have defined, master clocks?

    ……
    ……
    ……
  - **Question 3 :** Which output ports have defined, outgoing clocks?

    ……
    ……
    ……

- **Question 4 :** Are the clocks propagated or ideal?

  ……
  ……
  ……

- **Question 5 :** Which 3 clock pairs have constrained timing paths?

  ……
  ……
  ……

4.2 Task 2 : Use the GUI to Report Clock Relationships

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Start the GUI by executing the following command.

```
pt_shell> start_gui
```

- **Note :** The original pt_shell session is still running in the terminal window. You can keep the GUI open and use either the shell or the GUI interface as appropriate to the desired tasks.

✓ Look at clock domain crossings: Open the "clock domain matrix" from the pull-down menu: Clock → Clock Analyzer.

The ClockAnalyzer window that opens (expand if needed by clicking on the plus signs to the left of the clocks) should match the information from check timing when reporting the clock crossings in the design. Mouse over the blocks in the matrix to see information on what type of false paths exist. It is sometimes easier to digest this information as a graphical matrix table in comparison to the text output from.

```
pt_shell> check_timing -override clock_crossing -verbose
```

The left part of the window lists each master clock and any generated clocks that are created from each master clock..

- **Question 6 :** What is the master clock for SYS_2x_CLK?

  ……
  ……
  ……

- **Question 7 :** SYS_2x_CLK is defined on which pin/port (its "source")? (note: you may have to drag the clock matrix out of the way, exposing more columns of information about the clocks)

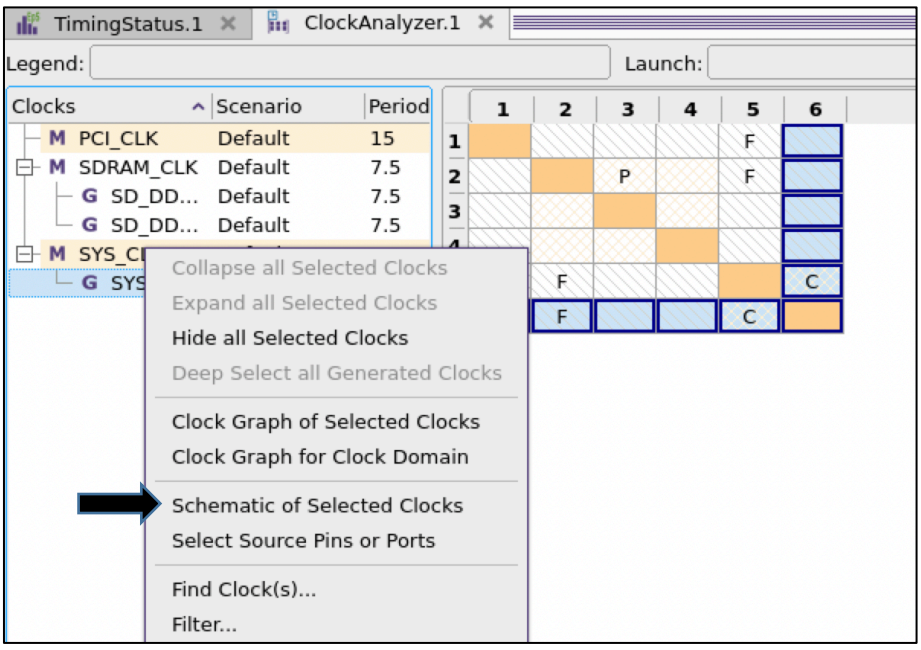
  ……
  ……
  ……

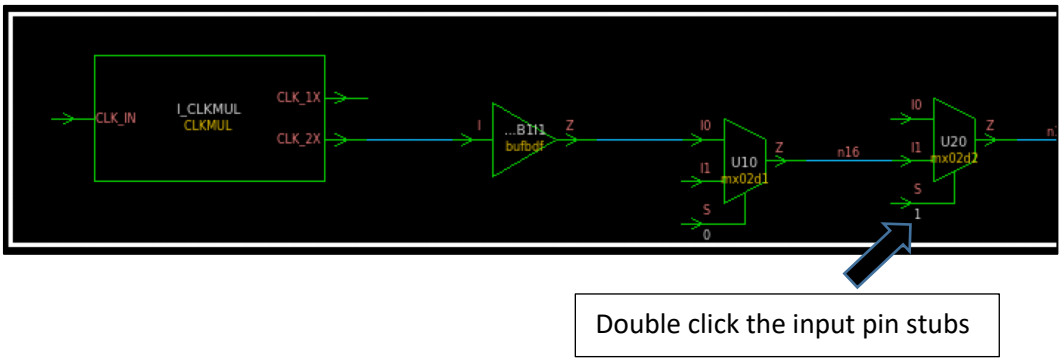
- **Question 8 :** The master clock for SYS 2x CLK is defined on which pin/port?

  ……
  ……
  ……

✓ Explore in more detail by displaying the clock schematic for SYS_2x_CLK: select the clock, then right mouse button + Schematic of Selected Clocks. Expand the fan-in for the schematic for the MUX called I_CLOCK_GEN/U20 [Hint: To locate/highlight U20, use Select → By Name] by double-clicking the input stubs, as shown in the following screen captures.

✓ Continue the double clicks until the fain is exhausted [Example: an input port has been reached]





Double click the input pin stubs

- **Question 9 :** What port is connected to the select pin of the MUX I_CLOCK_GEN/U20?

  ……
  ……
  ……

- **Question 10 :** Does seeing the schematic give you insight into the clocking scheme for test?

  ……
  ……
  ……

✓ Explore clock relationships with the abstract clock graph: Close the schematic window, then, on the Top Level window, select Clock → Clock Graph for All Clocks. If necessary, display a toolbar next to the schematic by pressing the F8 key. Display various elements by checking the toolbar and pressing Apply.

✓ Find a pair of muxed clocks: In the Abstract Clock Graph toolbar, select Mux and click Apply.

✓ In the Abstract Clock Graph, find instance I_CLOCK_GEN/U10 of mx02d1. [Hint: To locate/highlight U10, use Select → By Name].

- **Question 11 :** What clocks drive I_CLOCK_GEN/U10?

  ……
  ……
  ……

✓ In From the clock graph window, 'zoom into' an interesting object by displaying a schematic for it: Select I_CLOCK_GEN/U10, then Schematic → Schematic View.

- **Question 12 :** What port drives the select line to I_CLOCK_GEN/U10?

  ……
  ……
  ……

✓ Go back to the Abstract Clock Graph.

- **Question 13 :** From the abstract clock graph window, is it possible to open and display the same clock schematic for SYS_2x_CLK you displayed in the clock analyzer [Right Click on SYS_2X_CLK and find the option?

  ……
  ……
  ……

- ✓ Close the Clock Analyzer window by clicking on the small "X" in its upper right corner.
- ✓ Close the Clock Schematic and Clock Analyzer windows by clicking on the small "X" in the upper right corner.

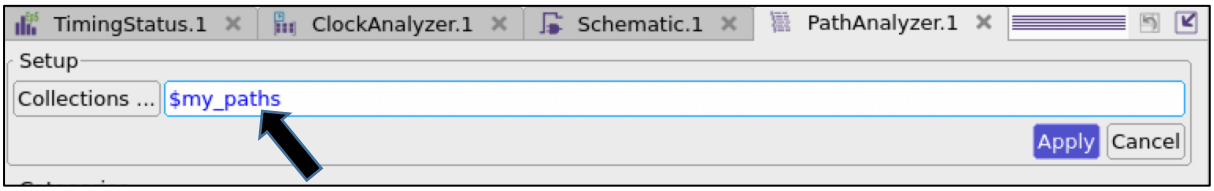
4.3 Task 3 : Use the GUI to explore detail of timing paths

Instructions : Investigate paths between launch and capture clocks - in this case. you will look at network latency for the launch and capture paths clocked by SYS_CLK.

- ✓ Propagate all the clocks to have the clock network delays calculated by Primetime before examining paths, by executing these commands in the shell, which remains open behind the GUI (this will take a minute or so to complete). Tell PrimeTime to save the arrival times for all pins (this is what you will examine. Then, define a collection of timing paths to examine.

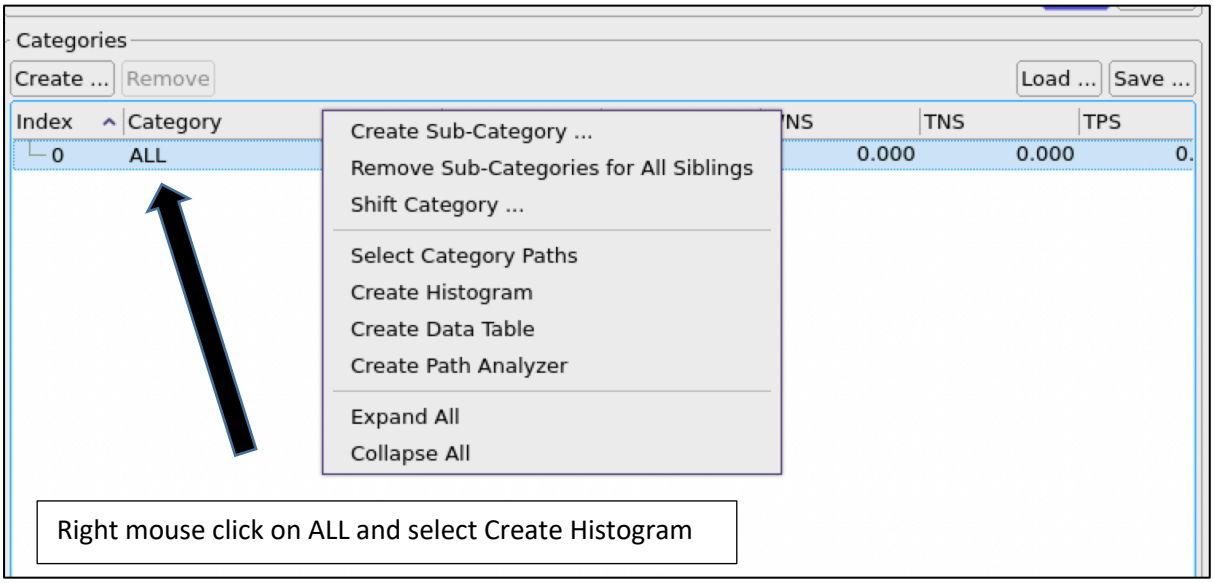
```
pt_shell> set_propadated_clock [all_clocks]
pt_shell> set timing_save_pin_arrival_and_slack true
pt_shell> update_timing
pt_shell> set my_paths [get_timing_paths -max 10 -group
                  SYS_CLK -path full_clock_expanded]
```

- ✓ Enter your collection of violating paths from the pull-down menu Timing → Path Analyzer.

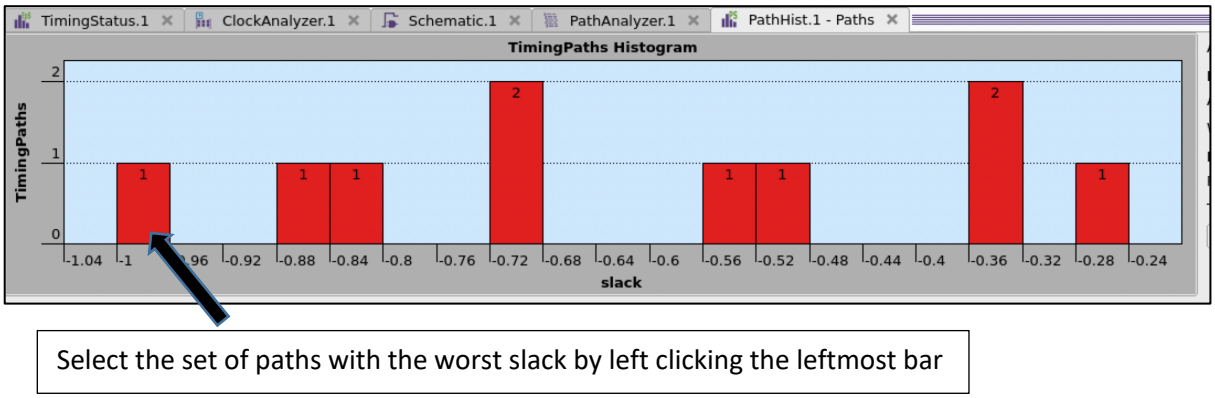


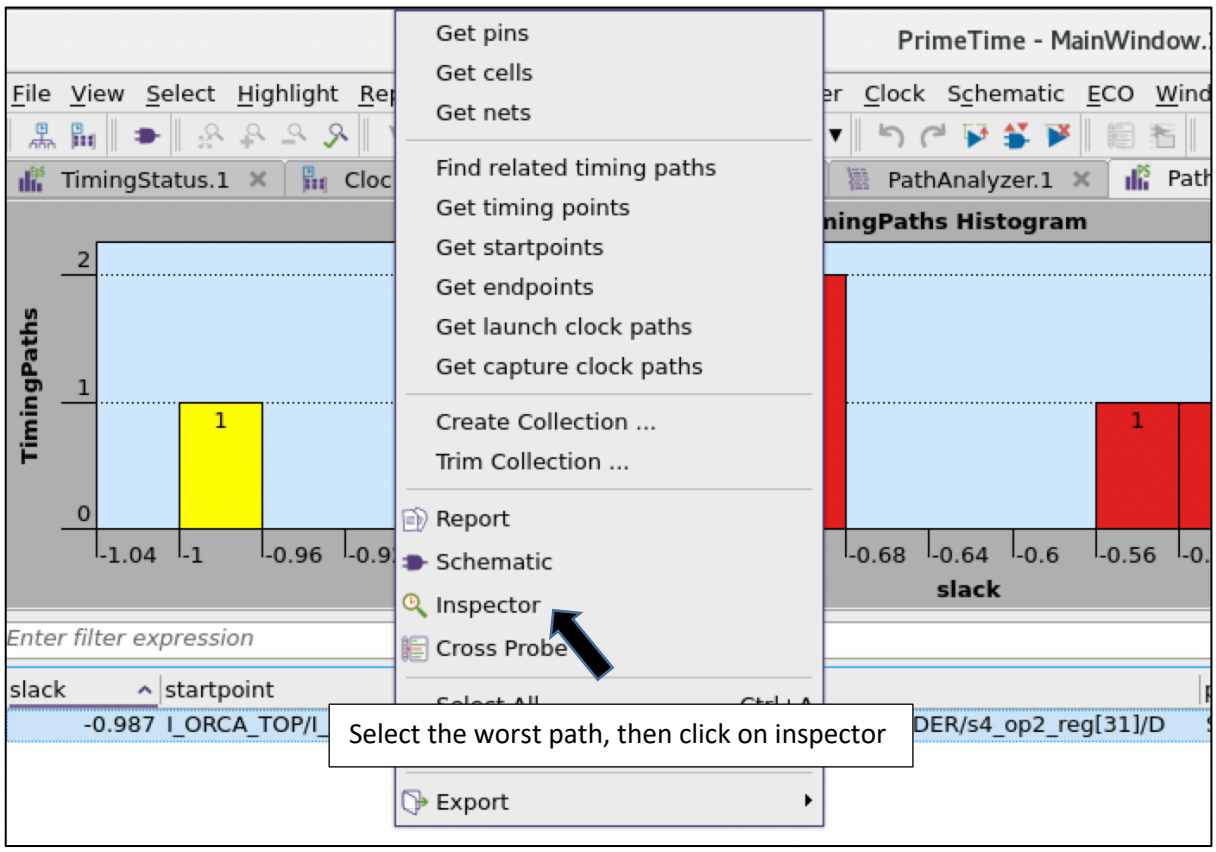
Enter your collection of timing paths and click on apply

✓ Bring up a histogram of your ten timing paths.

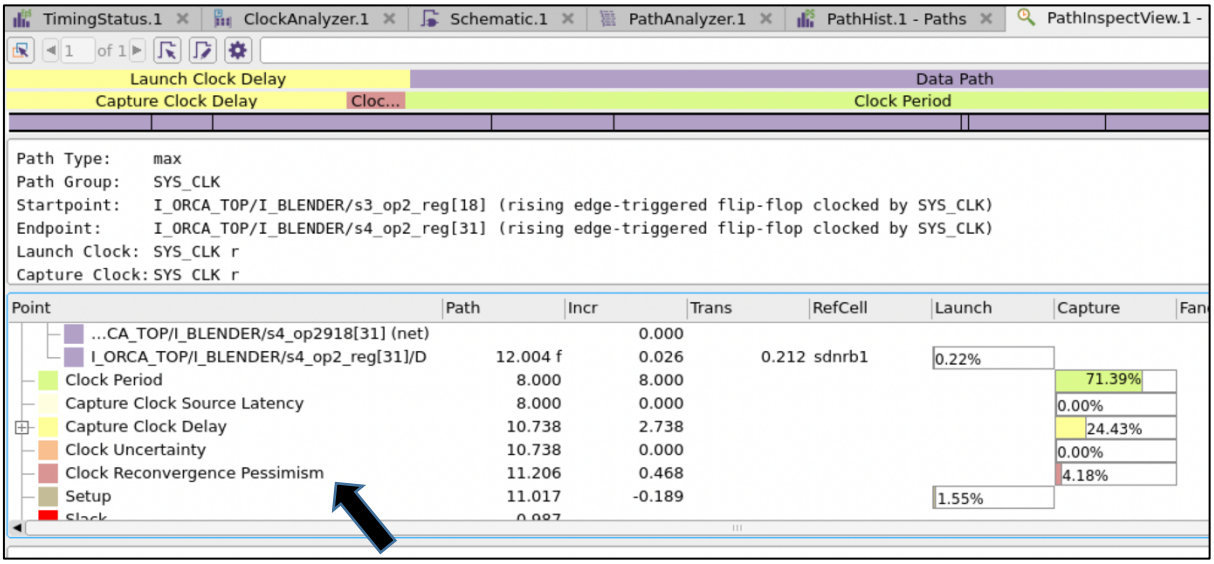


✓ From the histogram, bring up the Path Inspector on a selected path.





✓ In the Path Inspector, examine clock reconvergence pessimism: In the data required and data arrival section, scroll down until you find CRP. Then, scroll across until you find the percent of delay for the CRP.



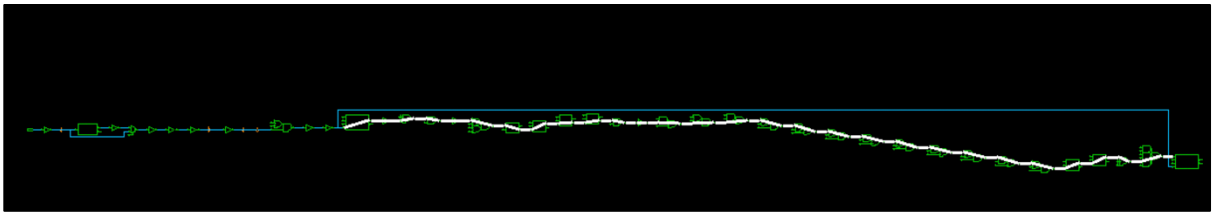
- **Question 14 :** What percent of the capture delay comes from CRP?

  ……
  ……
  ……

- **Question 15 :** Is this percent representative of all designs?

  ……
  ……
  ……

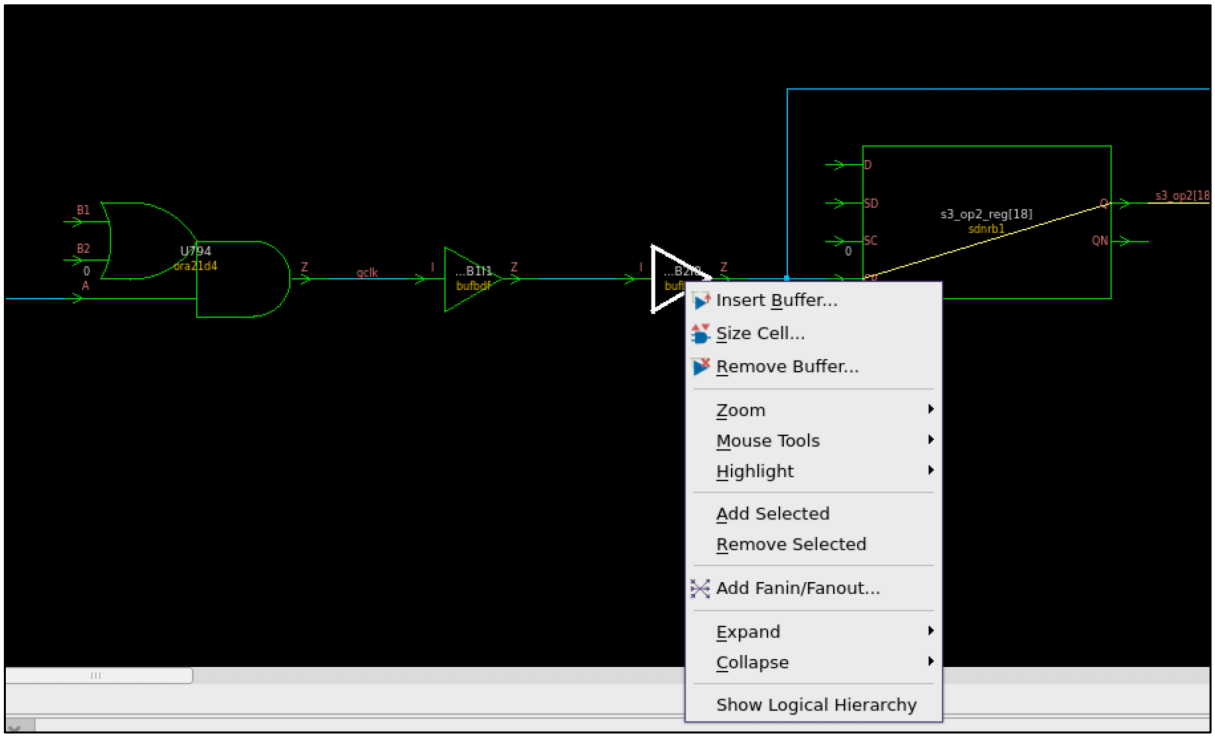
✓ Look at a schematic of the path by clicking on the Path Schematic tab on the bottom of the path inspector window.



✓ In the schematic window, find the CRP (clock reconvergence pessimism) point. This is the last pin before the launch and capture paths diverge.

- **Note :** Mouse "gestures" or "strokes" are available for easier zooming: While pressing the middle mouse button drag the cursor vertically for 'zoom full'; Drag diagonally up across an object to zoom in, and down across an object to zoom out.

✓ To see arrival times on this pin, if necessary, you may have to first 'expand the pin's buffer. (PrimeTime may 'collapse' buffer trees into a single buffer).



✓ View the arrival times (and any other attributes of interest) by selecting the output pin of the buffer just before the register, then by selecting View → Property [and by changing the list from being the default "Basic" to the "Application"].

- **Question 16 :** How wide is the arrival window for thee buffer output pin?

  ……
  ……
  ……

- **Question 17 :** Does this match what we saw earlier in the data arrival data required section of the path inspector?

  ……
  ……
  ……

✓ Examine the path waveform: Click on the Waveform tab at the bottom of the Path Inspector window.

- **Question 18 :** What can you add to the waveforms by clicking the right mouse button in the waveform window?

  ……
  ……
  ……

✓ Close the GUI while keeping the original pt_shell session going in the terminal window.

```
pt_shell> stop_gui (In the pt_shell window)
or
File -> Close GUI (in the main GUI window)
```

✓ Exit PrimeTime

4.4 Task 4 : Report a False Violation

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ Bring up PrimeTime and restore the saved session orca_savesession_violations

✓ Determine the number and type of timing violations in ORCA:

```
pt_shell> report_analysis_coverage
```

- **Question 19 :** How many, and what kind of violations does ORCA have?

  ……
  ……
  ……

✓ Generate a "short" timing report for the worst slack for an out_setup timing checks

- **Question 20 :** How will you identify the endpoint port which has the worst slack for out_setup (use the job aid labeled "Timing Reports" for help recalling the two appropriate switches)?

  ……
  ……
  ……

- **Question 21 :** Which clocks (launch and capture are involved in this violation?

  ……
  ……
  ……

- **Note :** From task 1, you know that SD_DDR_CLK is a generated clock defined at an output port. The purpose of defining outgoing clocks is that Prime Time calculates source latency for this clock and include this latency as part of the data required time.

✓ Look at the data required time section of the timing report from the last step and notice that no clock latency is reported. Confirm this with the following command:

```
# This report will return nothing as Primetime
has not calculated source latency for SD_DDR_CLK

pt_shell> report_clock -skew SD_DDR_CLK
```

- **Question 22 :** Why has PrimeTime not calculated source latency for the outgoing clock SD DDR CLK?

  ……
  ……
  ……

- **Note :** After speaking with the designer, it turns out there was a miscommunication. The designer was expecting you to turn on a variable that will propagate all clocks!

✓ There is a variable that can be used to make all clocks propagated. Use the Tel procedure a to help you identify the appropriate variable:

```
aa propagate
```

- **Question 23 :** What is the name of this variable?

  ……
  ……
  ……

- **Question 24 :** Using a man page, explain what this variable will do?

  ……
  ……
  ……

✓ Use the man page for check_timing to find the name of the additional check that will flag all ideal clocks. The following command opens the man page in a pop-up window with a scroll bar that simplifies viewing long reports.:

```
pt_shell> vman check_timing
```

- **Note :** The above command is an allas created in the synopsys_pt.setup file. It uses a command called view that is available on SolvNetPlus, Doc Id 000006678.

- **Note :** The alias vman will not work if the "wish" executable, the main executable in the Tk package, is not installed and made available in your lab environment

- **Question 25 :** How will you modify check timing to add a check to validate that all clocks are propagated?

  ……
  ……
  ……

✓ Quit PrimeTime

4.5 Task 5 : Re-Execute the Run Script to reduce violation

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ You are provided with the file . /scripts/orca_pt_variables.tcl that will accomplish the following two things.

- Adds to the default checks performed by check timing the check that will flag ideal clocks.
- All created clocks will be created as propagated clocks.

✓ Execute the run script. /RUN.tcl from the lab4 clocks Unix directory. Log the results to the log file run.log.:

```
Lab04]$ pt shell - RUN.tcl | tee -i run.log
```

✓ Invoke PrimeTime and restore the newly saved session in the Unix directory orca_savesession

✓ Use the appropriate commands to confirm the information below:

- The out_setup violations have been reduced.
- All clocks are propagated.
- Execute check_timing to confirm it is performing its default checks in addition to the check for ideal clocks
- The source latency is now calculated for SD_DDR_CLK.
- The timing report to sd_DQ [3] includes this calculated source latency.
- There will be additional violations (more setup violations as well as out_hold violations) that you can ignore.

✓ Quit Prime Time.

5. Lab 05 – Additional Constraints

Objective : *To understand how to add additional constraints apply user specified annotated delays to explore time borrowing with latches.*

Working Directory : /home/<user_name>PD_Labs/PT/Lab05
Relevant Files & Directories :
Lab04 : current working directory
.synopys_pt.setup : Automatically read PT setup file
orca_savesession : Saved Session directory
logs/ : log files from run script
RUN.tcl : Run script for ORCA

Learning outcomes:

- ✓ How to apply user specified annotated delays.
- ✓ How to debug PTE-070 messages

5.1 Task 1 : Debug PTE-070 Information Messages

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

- ✓ Invoke PrimeTime from the lab5 additional Unix directory.

```
Lab04]$ pt shell - RUN.tcl | tee -i run.log
```

- ✓ Shown below is the full message regarding a non-unate path on the clock network. In the next step, you will be asked to generate a timing report through this pin. In order to copy and paste and avoid typos - either find this message in the log file from another terminal window or use the Uni command grep from within PrimeTime as shown.

```
# From ./ run. log
Information: A non-unate path in clock
network detected.
Propagating both inverting and noninverting
senses of clock 'SDRAM CLK' from pin
'I _ORCA_ TOP/I_SDRAM_IF/sd mux dq_out_0/Z'.
(PTB-070)
```

```
pt_shell> sh grep -A1 -B 1 PTE-070 run.log
```

- **Note :** The command sh (or alternatively exec) allows you to execute Unix commands from within the PrimeTime shell.

✓ Generate a timing report for setup through the above pin and answer the following questions.

```
pt_shell> report_timing -input -through <through pin>
```

- **Question 1 :** Which lines in the timing report did you use to validate it is for setup and the timing path start point is the source for the clock SDRAM CLK?

  ……
  ……
  ……

- **Question 2 :** How does this timing report confirm that the pin in the warning above is on a data path (i.e. a clock source being used and constrained as a data path) and not on a clock path?

  ……
  ……
  ……

- **Question 3 :** Which sense is propagated through the above pin (i.e. positive unate or negative unate)? Look for a small arrow in the timing report which will locate the specific pin of interest.

  ……
  ……
  ……

✓ Generate at least one additional timing report to show the use of a negative unate timing arc through the pin of interest.

- **Question 4 :** Which lines in the timing report did you use to validate it is for setup, the timing path start point is the source for the clock SDRAM_CLK and that the timing arc is negative unate for the pin of interest?

  ……
  ……
  ……

✓ Do not quit PrimeTime.

5.2 Task 2 : Explore Time Borrow and Latches

Instructions : Follow the below instructions and answer the given questions based on your observations after the execution of the relevant instructions.

✓ There is only one latch in this design. Use the following commands to find it. Take advantage of command and option completion with the tab key.

```
pt shell> all_registers -level_sensitive
pt_shell> !! -clock_pin
pt_shell> all_registers -level_sensitive -data_pins
```

- **Question 5 :** What is the name of the clock pin for this latch?

  ……
  ……
  ……

- **Question 6 :** What are the names of the three data pins?

  ……
  ……
  ……

✓ Generate a timing report starting at the latch for setup time (be specific by using the clock pin as the start point and not just the cell name!). This lab will refer to this timing report as "path segment #2*. The function of this latch in the ORCA design is to generate a clock gating signal to turn on and off the clock SYS_CLK.

- **Question 7 :** Describe how you know this latch is not experiencing time borrow from the previous stage?

  ……
  ……
  ……

✓ Generate a timing report for the previous stage (this lab will refer to this timing report as "path segment #1*). Use the D input pin of the latch as the end point of this timing path.

- **Question 8 :** How much more time can path segment #1 take before it would start borrowing time from path segment #2?

  ……
  ……
  ……

✓ Force path segment #1 to borrow time from path segment #2 by annotating a net delay of 4ns as shown below:

```
# Use cut and paste to avoid typos on the pin name

pt_shell> set_annotated_delay -net 4 \
          -to _ORCA_TOP/I_BLENDER/latched_clk_en_reg/D
```

✓ Generate the timing report for path segment #1 again (take advantage of the up and down arrows to scroll through the history event list).

- **Question 9 :** How much time is path segment #1 borrowing from path segment #2?

  ……
  ……
  ……

- **Question 10 :** What is the slack for path segment #1?

  ……
  ……
  ……

✓ Re-generate the timing report for path segment #2.

- **Note :** The start point of the timing path will now be the D pin of the latch (not the clock pin as used before because you are interested in reporting the timing path that includes time borrow.

```
pt_shell> report_timing -from \
    I_ORCA_TOP/I_BLENDER/latched_clk_en_reg/D
```

- **Question 11 :** Does the time given to path segment #1 now match your expectations?

  ……
  ……
  ……

✓ Change the latch behaviour for transparency; that is, make it transparent when data arrives between the opening and closing edges of the cock.

```
pt_shell> set_app_var timing_enable_through_paths true
```

✓ Repeat your timing report to the latch D pin. Notice that, even though the latch is transparent, you can still specify the D pin as an endpoint.

```
pt_shell> report_timing -to \
    I_ORCA_TOP/I_BLENDER/latched_clk_en_reg/D
```

- **Question 12 :** What is the start point?

  ……
  ……
  ……

✓ Do a timing report FROM the start point you just identified.

```
pt_shell> report_timing -from \
    I_ORCA_TOP/I_PARSER/blender_clk_en_reg/CP
```

- **Question 13 :** What is the path endpoint?

  ……
  ……
  ……

- **Question 14 :** What are the transparency open and close edges?

  ……
  ……
  ……

- **Question 15 :** Did data arrive between them?

  ……
  ……
  ……

- **Question 16 :** Was there time borrowing?

  ……
  ……
  ……

- **Question 17 :** Was the slack positive?

  ……
  ……
  ……

✓ Quit PrimeTime.