

SAED 14nm FinFET EDUCATIONAL DESIGN KIT

SAED_EDK14_FinFET

DATABOOK



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1. Introduction

This specification describes the basic technical requirements of the SAED_EDK14_FINFET Educational Design Kit (EDK).

1.1. Goal of EDK development

SAED_EDK14_FINFET will be designed to be free from intellectual property restrictions EDK and will be anticipated for the use in educational purposes aimed at training highly qualified specialists in the area of microelectronics in:

- SYNOPSYS Customer Education Services
- SYNOPSYS Global Technical Services
- Universities included in SYNOPSYS University Program

SAED_EDK14_FINFET is foreseen to support the trainees to better master:

- Advanced design methodologies
- Capabilities of SYNOPSYS tools.

For the use of EDK it is assumed that European or North American bundle of SYNOPSYS EDA tools is available to trainees.

SAED_EDK14_FINFET will be anticipated for designing different integrated circuits by the application of 14nm_FinFET technology and SYNOPSYS EDA tools.

1.2. Peculiarities of Low Power Design

During the development of SAED_EDK14_FINFET the possibility to apply state-of-the-art methods of low power design should be considered which are described in the [1,2].

1.3. Content of EDK

The content of SAED_EDK14_FINFET is shown in Table 1.1.

Table 1.1. Content of SAED_EDK14_FINFET

N	Name	Description
2	SAED_EDK14_FINFET_CORE	Digital Standard Cell Library
3	SAED_EDK14_FINFET_IO_STD	I/O Standard Cell Library (Wire-bond and Flip-Chip versions)
4	SAED_EDK14_FINFET_IO_SP	I/O Special Cell Library (Wire-bond and Flip-Chip versions)
5	SAED_EDK14_FINFET_RAM	Set of Memories
6	SAED_EDK14_FINFET_PLL	Phase Locked Loop
9	SAED_EDK14_FINFET_ChipTop	ChipTop processor's reference design
11	SAED_EDK14_FINFET_OpenSPARC	OpenSPARC processor's reference design

1.4. Methodology of getting technological files

For design of SAED14nm FinFET Educational Design Kit, abstract technology, simulation models will be generated recalling as a primary model the Predictive Technology Model (PTM) developed by the Nanoscale Integration and Modeling Group (NIMO) of Arizona State University (ASU) (<http://ptm.asu.edu/>). The initial version of the model will be specified using FinFET device characteristics of [3, 4] item from open sources.

Layout design rules for SAED14nm_FinFET educational, abstract technology should be obtained by considering lithography requirements and restrictions for 14nm FinFET technology. Parasitics extraction deck will be formed using the models of parasitics estimation developed by NIMO group of ASU. Double patterning rules and also 14nm advanced rules supported by Synopsys IC Compiler Zroute router will be added.

Digital Standard Cell Library SAED_EDK14_FINFET_CORE will be built using SAED14nm FinFET technology. The library will be created aimed at optimizing the main characteristics of designed integrated circuits by its help. The library will include typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library will contain all the cells which are required for different styles of low power designs (multi-voltage, power gating, clock gating, multi-threshold, etc.).

I/O Standard Cell Library SAED_EDK14_FINFET_IO_STD will be built using SAED14nm FinFET technology. The library will include typical I/O cells which are necessary for integrated circuits design for educational purposes.

I/O Special Cell Library SAED_EDK14_FINFET_IO_SP will be built using SAED14nm FinFET technology according to specifications of corresponding special I/Os. The library will include commonly used special I/O cells.

Both Standard and Special I/O Cell Libraries will be developed in both wire-bond and flip chip versions enabling advanced designs in educational environment.

Set of Memories SAED_EDK14_FINFET_RAM will be built using SAED14nm FinFET technology. The set will include several RAMs of not large sizes which are necessary for integrated circuits design for educational purposes.

OpenSPARC Megacells SAED_EDK14_FINFET_RAM_OS will be designed using SAED14nm FinFET technology according to specification of OpenSPARC processor.

Phase Locked Loop SAED_EDK14_FINFET_PLL will be designed using SAED14nm FinFET technology and will be used for integrated circuits design for educational purposes.

ChipTop is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design (.v, .sdc, .tcl, .upf), all setup (.setup) and other files needed to design the processor. ChipTop processor design must be created by all well known low-power techniques (multi voltage, power gating, clock gating, multi threshold, .etc) to be possible to compare all design versions in university environment.

ORCA is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design files (.v, .sdc, .tcl, .upf) and all setup files (.setup) needed to design the processor.

Leon3 is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design files (.v, .sdc, .tcl, .upf) and all setup files (.setup) needed to design the processor. Leon3 processor design must be created by all well known low-power techniques (multi voltage, power gating, clock gating, multi threshold) to be possible to compare all design versions in university environment.

OpenSPARC is a reference processor design which helps to get introduced to Synopsys design flow. It contains both design files (.v, .sdc, .tcl, .upf) and all setup files (.setup) needed to design the processor.

2. Digital Standard Cell Library SAED_EDK14_FINFET_CORE

2.1. Introduction

The SAED_EDK14_FINFET_CORE Digital Standard Cell Library will be built using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V design rules. The library will be created aimed at optimizing the main characteristics of designed integrated circuits by its help. The library will include typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library will contain all the cells which are required for different styles of low power (multi-voltage, power gating, clock gating, multi-threshold, etc.) designs. Those are the following: Isolation Cells, Level Shifters, Retention Flip-Flops, Always-on Buffers and Power Gating Cells. In order to implement multi-threshold low power techniques High-Vt(HVT), Low-Vt(LVT), Super Low-Vt(SLVT) and Regular-Vt(RVT) versions of the Library will be created. The presence of all these cells will provide the support of integrated circuits design with different core voltages to minimize dynamic and leakage power. Compiling the cell list has been based on the analysis of different educational designs.

2.2. General Information

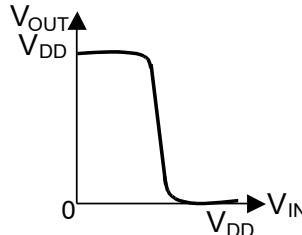
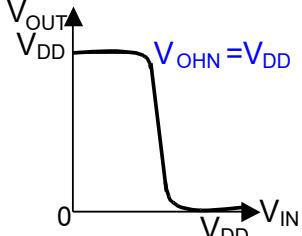
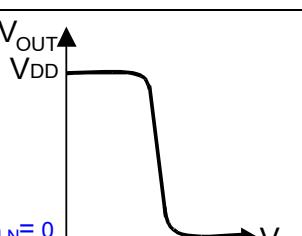
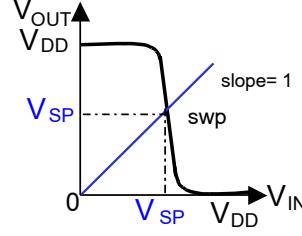
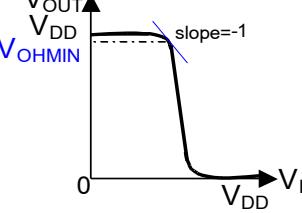
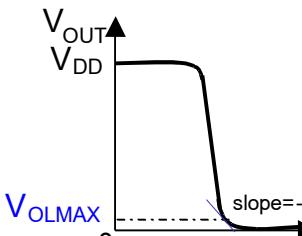
The used symbols of logic elements' states are shown in Table 2.1.

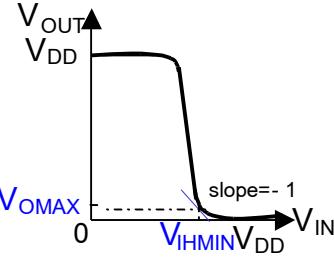
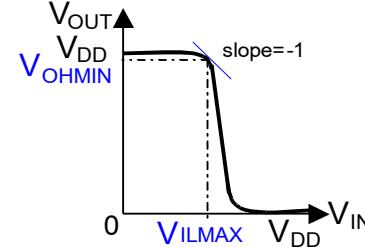
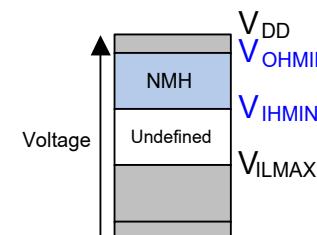
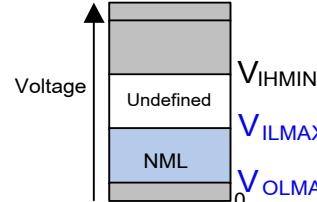
Table 2.1. Symbols of logic elements' states

Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIGH Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

DC parameters and measurement conditions of the elements included in SAED_EDK14_FINFET_CORE Digital Standard Cell Library are shown in Table 2.2.

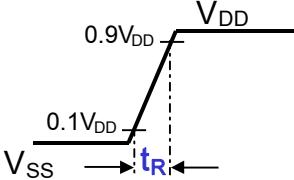
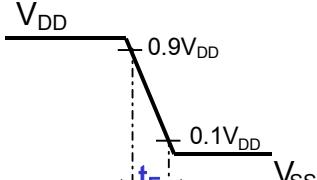
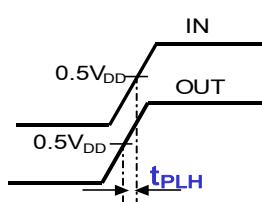
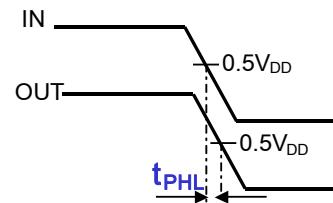
Table 2.2. DC Parameters and measurement conditions of digital cells

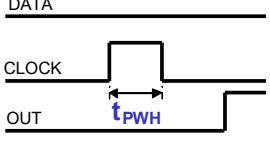
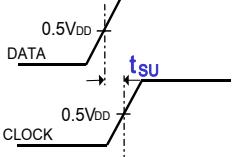
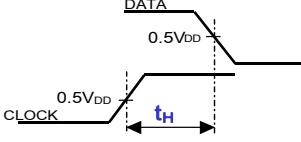
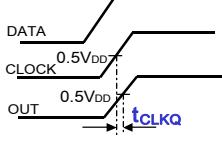
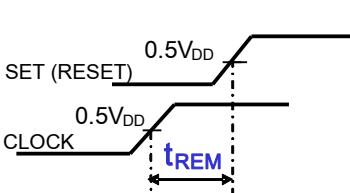
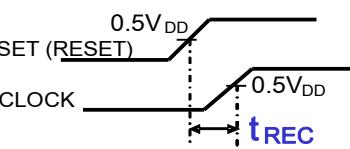
No	Parameter	Unit	Symbol	Figure	Definition
1	Voltage Transfer Characteristic	-	VTC		DC functional dependence between input and output voltages.
2	Output high level voltage (nominal)	V	$V_{OHN}=V_{DD}$		Output high voltage at nominal condition, usually equals to V_{DD}
3	Output low level voltage (nominal)	V	$V_{OLN}=0$ ($V_{OLN}=V_{SS}$)		Output low voltage at nominal condition, usually $V_{OLN}=0$
4	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT}=V_{IN}$
5	Output high level minimum voltage	V	V_{OHMIN}		Highest output voltage at slope= -1.
6	Output low level maximum voltage	V	V_{OLMAX}		Lowest output voltage at slope= -1

No	Parameter	Unit	Symbol	Figure	Definition
7	Input minimum high voltage	V	V_{IHMIN}		Highest input voltage at slope = -1
8	Input maximum low voltage	V	V_{ILMAX}		Lowest input voltage at slope = -1
9	High state noise margin	V	$NMH = V_{OHMIN} - V_{IHMIN}$		The maximum input noise voltage which does not change the output state when its value is subtracted from the input high level voltage
10	Low state noise margin	V	$NML = V_{ILMAX} - V_{OLMAX}$		The maximum input noise voltage which does not change the output state when added to the input low level voltage
11	Static leakage current consumption at output on high state	uA	I_{LEAKH}	None	The current consumed when the output is high
		uA	I_{LEAKL}	None	The current consumed when the output is low
12	Leakage power consumption (dissipation) at output	pW	$P_{LEAKH} = V_{DD} \times I_{LEAKH}$	None	The power consumed when the output is high
		pW	$P_{LEAKL} = V_{DD} \times I_{LEAKL}$	None	The power consumed when the output is low

AC parameters and measurement conditions of the elements included in SAED_EDK14_FINFET_CORE Digital Standard Cell Library are shown in Table 2.3.

Table 2.3. AC Parameters and measurement conditions of digital cells

No	Parameter	Unit	Symbol	Figure	Definition
1	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from kV_{DD} to $(1-k)V_{DD}$ value. Usually $k=0.1$ (also possible $k=0.2, 0.3$, etc)
2	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to kV_{DD} value. Usually $k=0.1$ (also possible $k=0.2, 0.3$, etc)
3	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low
5	Average supply current	uA	$I_{V_{DD}AVG} = \frac{1}{T} \int_0^T I_{V_{DD}}(t) dt$	None	The power supply current average value for a period (T)
6	Supply peak current	uA	$I_{V_{DD}PEAK} = \max(I_{V_{DD}}(t))$ $t \in [0; T]$	None	The peak value of power supply current within one period (T)
7	Dynamic power dissipation	pW	$P_{DISDYN} = I_{V_{DD}AVG} \times V_{DD}$	None	The average power consumed from the power supply
8	Power-delay product	nJ	$PD = P_{DISDYN} \times \max(t_{PHL}, t_{PLH})$	None	The product of consumed power and the largest propagation delay
9	Energy-delay product	nJs	$ED = PD \times \max(t_{PHL}, t_{PLH})$	None	The product of PD and the largest propagation delay
10	Switching fall power	nJ	$P_{SWF} = (C_{LOAD} + C_{OUT F}) \times V_{DD}^2 / 2$	None	The energy dissipated on a fall transition. ($C_{OUT F}$ is the output fall capacitance)
11	Switching rise power	nJ	$P_{SWR} = (C_{LOAD} + C_{OUT R}) \times V_{DD}^2 / 2$	None	The energy dissipated on a rise transition. ($C_{OUT R}$ is the output rise capacitance)

No	Parameter	Unit	Symbol	Figure	Definition
12	Minimum clock pulse (only for flip-flops or latches)	ns	t_{PWH} (t_{PWL})		The time interval during which the clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch
13	Setup time (only for flip-flops or latches)	ns	t_{SU}		The minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs
14	Hold time (only for flip-flops or latches)	ns	t_H		The minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred
15	Clock-to-output time (only for flip-flops or latches)	ns	t_{CLKQ}		The amount of time that takes the output signal to change after clock's active edge is applied
16	Removal time (only for flip-flops or latches with asynchronous Set or Reset).	ns	t_{REM}		The minimum time in which the asynchronous Set or Reset pin to a flip-flop or latch must remain enabled after the active edge of the clock has occurred
17	Recovery time (only for flip-flops and latches with asynchronous Set or Reset)	ns	t_{REC}		The minimum time in which Set or Reset must be held stable after being deasserted before next active edge of the clock occurs
18	From high to Z-state entry time, (only for tri-state output cells)	ns	t_{HZ}	None	The amount of time that takes the output to change from high to Z-state after control signal is applied
19	From low to Z-state entry time, (only for tri-state output cells)	ns	t_{LZ}	None	The amount of time that takes the output to change from low to Z-state after control signal is applied
20	From Z to high-state exit time (only for tri-state output cells)	ns	t_{ZH}	None	The amount of time that takes the output to change from Z to high-state after control signal is applied

No	Parameter	Unit	Symbol	Figure	Definition
21	From Z to low-state exit time (only for tri-state output cells)	ns	t_{ZL}	None	The amount of time that takes the output to change from Z to low-state after control signal is applied
22	Input pin capacitance	pF	C_{IN}	None	Defines the capacitance between input pin and VSS pin
23	Maximum capacitance	pF	C_{MAX}	None	Defines the maximum total capacitive load that an output pin can drive

2.3. NXT Architecture

In designs using NXT architecture, the preferred routing direction for M2 is parallel to the cell power/ground (P/G) rails. This routing direction is conventionally referred to as “horizontal”. The preferred routing direction for M1 is horizontal if the particular cell architecture has a M1 power/ground rail, and vertical otherwise. The preferred routing directions in the cell layouts naturally extend to routing at the block and chip level as well.

Preferred routing directions for SAED standard cell library are horizontal for M1 and M2, vertical for M3, and alternating horizontal and vertical thereafter. This is conventionally referred to as the HHVH routing scheme.

One of the advantages of the NXT routing architecture is that there are many M2 tracks that can access the M1 pins on a given cell. This enhances the ability of a routing tool to connect to these pins, since M2 is the primary layer used by routers to approach M1 cell pins. Improving pin access in this way minimizes congestion in the vicinity of a cell, since the router is no longer restricted to a single M2 track when connecting to a given pin.

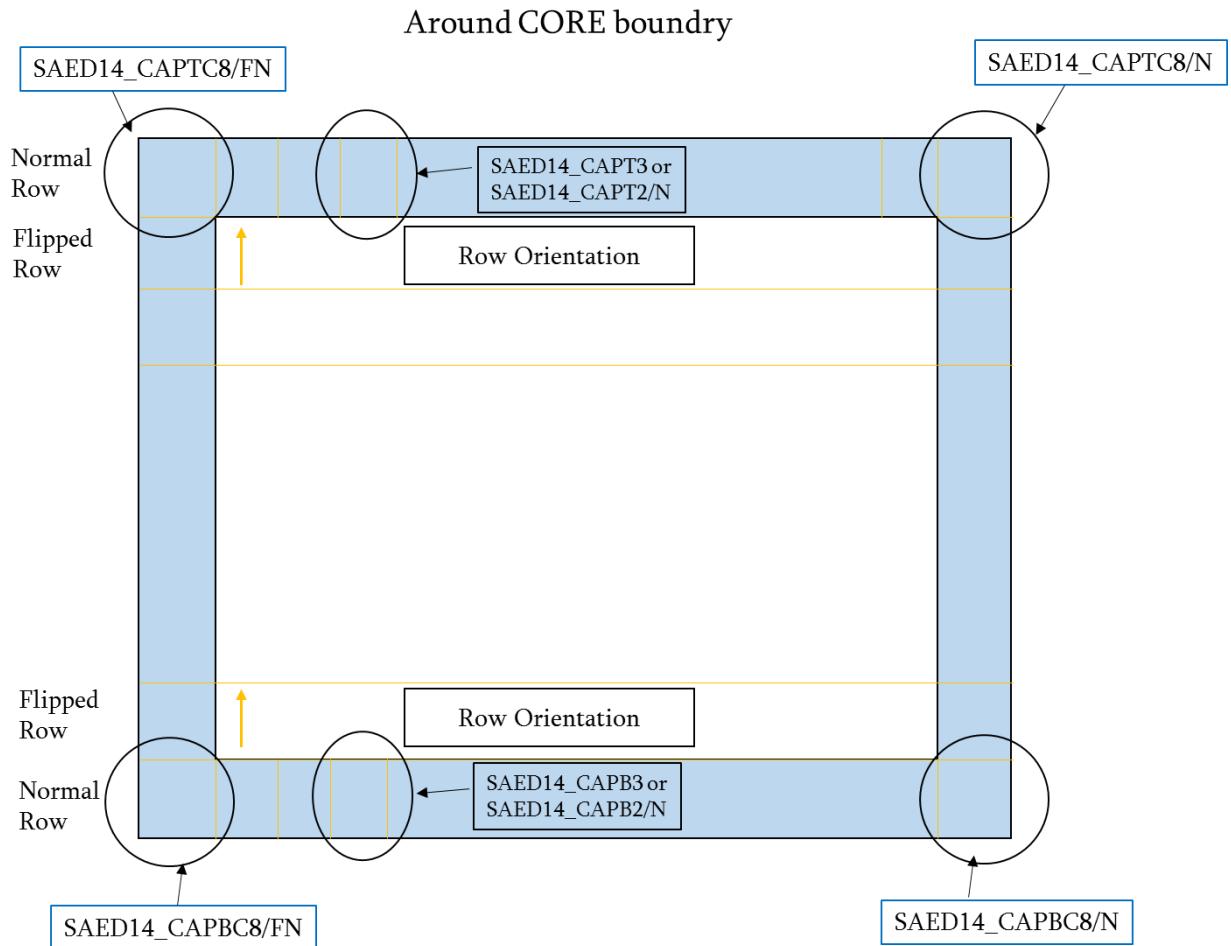
2.4. Floorplanning and Placement

2.4.1. Core to Die Boundary Distance

- The core to die boundary needs to be a multiple of 45nm.
- Fin pitch is 45nm.
- All the IP blocks/macros on the chip should follow the alignment with the Fin pitch.

Outside corner cells

- a. top_right_corner_cell
- b. bottom_right_corner_cell
- c. top_left_corner_cell
- d. bottom_left_corner_cell



2.4.2. Boundary Cell Insertion

Emerging node technologies require additional types of corner and endcap cells for DFM and DRC fixing. The new **insert_boundary_cell** command provides capabilities for various new boundary cell insertion requirements and technologies. Designers have to insert boundary cells in floorplan stage, otherwise the design rule and DFM issues will be difficult to resolve after physical design is complete.

With **insert_boundary_cell** command, IC Compiler can insert additional types of corner and endcap cells.

2.5. ECO cells

At present, a typical ECO design flow would be to allocate space to unconnected spare cells during design layout, when the space is available. While implementing the ECO changes to the design, the spare cells are connected to complete the design netlist change.

The ECO library allows designers much more flexibility in their ECO changes.

2.5.1. Preparing Design for an ECO Change

In order to implement design changes with the ECO library, all empty space remaining in the original design after placement with the saed14 library should be populated with the ECO base filler cell wherever possible. The remaining empty sites are then populated with filler cells from the saed14 library as appropriate. This ECO base filler cell is included in saed14 library.

2.6. Operating conditions

SAED_EDK14_FINFET_CORE Digital Standard Cell Library specification is given for 0.8V operation. The used process technology will be SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V, but only the 1P1M option will be used.

The operating conditions of SAED_EDK14_FINFET_CORE Digital Standard Cell Library are shown in Table 2.4.

Table 2.4. Operating conditions

Parameter	Min	Typ	Max	Units
Power Supply (VDD) range	0.72	0.8	0.88	V
Operating Temperature range	-40	+25	+125	°C
Operating Frequency (F)	-	1	-	GHz

2.7. Definition of input signal slope, standard load and drive strengths

Preliminary value for the slope of input signal edges will be determined from the given operating frequency (F=1 GHz) using the following formula:

$$T_{isl} = \frac{1}{(10 \div 20) \cdot F}$$

The result thus obtained is preliminary and may be revised after specifying the inverter's sizes.

Standard load (C_{sl}) will be selected as the input pin capacitance of INVX_1 cell. The INVX_1 cell itself will be tuned to drive 4 standard loads.

Table 2.5. Definition of drive strength

Drive Strength	Cell Load
X_0.5	0.5x C_{sl}
X_0.75	0.75x C_{sl}
X_1	1x C_{sl}
X_2	2x C_{sl}
X_3	3x C_{sl}
X_4	4x C_{sl}
X_8	8x C_{sl}
X_12	12x C_{sl}
X_16	16x C_{sl}
X_24	24x C_{sl}
X_32	32x C_{sl}

2.8. AC Characteristics

2.8.1. Characterization corners

Composite Current Source (CCS) modeling technology will be applied for characterization to meet the contemporary methods of low power design. The application of that technology will support timing, noise, and power analyses simultaneously with consideration of the relevant nanometer dependencies. It will allow meeting the requirements of variation-aware analysis. The characterization results will be given for 18 process/voltage/temperature (PVT) conditions shown in Table 2.6., and The Level Shifters will be characterized for the following corners:

Table 2.6. Base Characterization Corners

#	Corner Name/ Library Name Suffix	Process (NFIN proc. – PFIN proc.)	Power Supply (V)	Temperature (°C)
Normal Voltage Operating Conditions				
1.	tt0p8v25c	Typical - Typical	0.8	25
2.	tt0p8v125c	Typical - Typical	0.8	125
3.	tt0p8vm40c	Typical – Typical	0.8	-40
4.	ss0p72v25c	Slow - Slow	0.72	25
5.	ss0p72v125c	Slow - Slow	0.72	125
6.	ss0p72vm40c	Slow - Slow	0.72	-40
7.	ff0p88v25c	Fast - Fast	0.88	25
8.	ff0p88v125c	Fast - Fast	0.88	125
9.	ff0p88vm40c	Fast - Fast	0.88	-40
Low Voltage Operating Conditions				
10.	tt0p6v25c	Typical – Typical	0.65	25
11.	tt0p6v125c	Typical – Typical	0.65	125
12.	tt0p6vm40c	Typical – Typical	0.65	-40
13.	ss0p6v25c	Slow - Slow	0.6	25
14.	ss0p6v125c	Slow - Slow	0.6	125
15.	ss0p6vm40c	Slow - Slow	0.6	-40
16.	ff0p7v25c	Fast - Fast	0.7	25
17.	ff0p7v125c	Fast – Fast	0.7	125
18.	ff0p7vm40c	Fast – Fast	0.7	-40

Table 2.7. Multi-VDD characterization corners for high-low level shifters

#	Corner Name/ Library Name Suffix	Process (NFIN proc. – PFIN proc.)	Power Supply1 (V)	Power Supply2 (V)	Temp. (°C)
1.	dlvl_ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	125
2.	dlvl_ff0p88v125c_i0p7v	Fast-Fast	0.88	0.7	125
3.	dlvl_ff0p7v125c_i0p7v	Fast-Fast	0.7	0.7	125
4.	dlvl_ff0p88v25c_i0p88v	Fast-Fast	0.88	0.88	25
5.	dlvl_ff0p88v25c_i0p7v	Fast-Fast	0.88	0.7	25
6.	dlvl_ff0p7v25c_i0p7v	Fast-Fast	0.7	0.7	25
7.	dlvl_ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	-40
8.	dlvl_ff0p88v125c_i0p7v	Fast-Fast	0.88	0.7	-40
9.	dlvl_ff0p7v125c_i0p7v	Fast-Fast	0.7	0.7	-40
10.	dlvl_tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	125
11.	dlvl_tt0p8v125c_i0p65v	Typical-Typical	0.8	0.65	125
12.	dlvl_tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	125
13.	dlvl_tt0p8v25c_i0p8v	Typical-Typical	0.8	0.8	25
14.	dlvl_tt0p8v25c_i0p65v	Typical-Typical	0.8	0.65	25
15.	dlvl_tt0p65v25c_i0p65v	Typical-Typical	0.65	0.65	25
16.	dlvl_tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	-40
17.	dlvl_tt0p8v125c_i0p65v	Typical-Typical	0.8	0.65	-40
18.	dlvl_tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	-40
19.	dlvl_ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	125
20.	dlvl_ss0p72v125c_i0p6v	Slow-Slow	0.72	0.6	125
21.	dlvl_ss0p6v125c_i0p6v	Slow-Slow	0.6	0.6	125
22.	dlvl_ss0p72v25c_i0p72v	Slow-Slow	0.72	0.72	25
23.	dlvl_ss0p72v25c_i0p6v	Slow-Slow	0.72	0.6	25
24.	dlvl_ss0p6v25c_i0p6v	Slow-Slow	0.6	0.6	25
25.	dlvl_ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	-40
26.	dlvl_ss0p72v125c_i0p6v	Slow-Slow	0.72	0.6	-40
27.	dlvl_ss0p6v125c_i0p6v	Slow-Slow	0.6	0.6	-40

Table 2.8. Multi-VDD characterization corners for low-high level shifters

#	Corner Name/ Library Name Suffix	Process (NMOS proc. – PMOS proc.)	Power Supply1 (V)	Power Supply2 (V)	Temp. (°C)
1.	ulvl_ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	125
2.	ulvl_ff0p7v125c_i0p88v	Fast-Fast	0.7	0.88	125
3.	ulvl_ff0p7v125c_i0p7v	Fast-Fast	0.7	0.7	125
4.	ulvl_ff0p88v25c_i0p88v	Fast-Fast	0.88	0.88	25
5.	ulvl_ff0p7v25c_i0p88v	Fast-Fast	0.7	0.88	25
6.	ulvl_ff0p7v25c_i0p7v	Fast-Fast	0.7	0.7	25
7.	ulvl_ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	-40
8.	ulvl_ff0p7v125c_i0p88v	Fast-Fast	0.7	0.88	-40
9.	ulvl_ff0p7v125c_i0p7v	Fast-Fast	0.7	0.7	-40
10.	ulvl_tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	125
11.	ulvl_tt0p65v125c_i0p8v	Typical-Typical	0.65	0.8	125
12.	ulvl_tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	125
13.	ulvl_tt0p8v25c_i0p8v	Typical-Typical	0.8	0.8	25
14.	ulvl_tt0p65v25c_i0p8v	Typical-Typical	0.65	0.8	25
15.	ulvl_tt0p65v25c_i0p65v	Typical-Typical	0.65	0.65	25
16.	ulvl_tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	-40
17.	ulvl_tt0p65v125c_i0p8v	Typical-Typical	0.65	0.8	-40

#	Corner Name/ Library Name Suffix	Process (NMOS proc. – PMOS proc.)	Power Supply1 (V)	Power Supply2 (V)	Temp. (°C)
18.	ulvl_tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	-40
19.	ulvl_ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	125
20.	ulvl_ss0p6v125c_i0p72v	Slow-Slow	0.6	0.72	125
21.	ulvl_ss0p6v125c_i0p6v	Slow-Slow	0.6	0.6	125
22.	ulvl_ss0p72v25c_i0p72v	Slow-Slow	0.72	0.72	25
23.	ulvl_ss0p6v25c_i0p72v	Slow-Slow	0.6	0.72	25
24.	ulvl_ss0p6v25c_i0p6v	Slow-Slow	0.6	0.6	25
25.	ulvl_ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	-40
26.	ulvl_ss0p6v125c_i0p72v	Slow-Slow	0.6	0.72	-40
27.	ulvl_ss0p6v125c_i0p6v	Slow-Slow	0.6	0.6	-40

2.8.2. The values of Output Load and Input Slope

Characterization should be realized for 7 different values of Output Load and 7 different values of Input Slope shown in Table 2.9.

Table 2.9. The values to be used for characterization

Parameter	Value						
Output Load	0	0.5*C _{sl}	1*C _{sl}	2*C _{sl}	4*C _{sl}	8*C _{sl}	16*C _{sl}
Input Slope (ns)	0.2*T _{isl}	0.4*T _{isl}	0.8*T _{isl}	1.6*T _{isl}	3.2*T _{isl}	6.4*T _{isl}	12.8*T _{isl}

The calculation of Setup/Hold times should be realized for 3 different values of Data and Input Slopes shown in Table 2.10.

Table 2.10. The used values for calculating Setup/Hold Times

Parameter	Slope Values (ns)		
Data Input Slope	0.5*T _{isl}	1*T _{isl}	5*T _{isl}
Clock Input Slope	0.5*T _{isl}	1*T _{isl}	5*T _{isl}

2.9. Digital Standard Library Cells List

SAED_EDK14_FINFET_CORE Digital Standard Cell Library will contain 1437 cells, with regular, low and hight threshold voltages, 5748 in total. The list of cells is shown in Table 2.11. Cells will be prefixed according to threshold level SAEDRVT_*, SAEDLVT_*, SAEDSLVT_*, SAEDHVT_* for regular, low, superlow and hight threshold voltages accordingly (i.e. library will include 4 "INV_1" cells: SAEDRVT14_INV_1, SAEDLVT14_INV_1, SAEDSLVT14_INV_1, SAEDHVT14_INV_1).

2.9.1. Naming Conventions

Cell Naming Syntax

<prefix>_<baseName>[_<extension>][_<drive>]

<prefix>

This is a prefix identifying the type of library the cell is a part of as well as the V_t corner.

<baseName>

This is an alphanumeric string conveying the function in commonly used form.

<extension>

This optional extension to the name appears where the general function of the cell is the same but the specific implementation requires a unique topology or other consideration.

<drive>

This optional suffix gives the drive strength, the driving capability of the cell, in the number format.

Examples

A cell with the name

SAED14_INV_S_1

is a standard cell Symmetric rise/fall slew time inverter with a 1x drive strength.

Architecture Decoder

This section presents the cell naming codes that are used to define the architecture with the help of a decoder. The cell architecture syntax is as follows:

<Architecture&VT>_<Function>_<Variant>_<Drive>

- Variant is optional field
- T - tapered variant (input closest to output is made faster by increasing size of devices closer to supply)
- CT - Clock Tree cell
- D - density variant

- G - GateArray style sizing, max P/N size devices used for all elements of circuit (for 2-stage circuits this implies a 1:2 stage gain also)
- S - symmetric rise/fall
- F - Fast version of circuit

2.9.2. Digital standard library cell list

Table 2.11. Digital Standard Library Cells List

Cell name	Cell Description	Driver option
Inverters, Buffers		
SAED14_BUF_*	Non-inverting buffer	1, 10, 12, 16, 1.5, 2, 20, 3, 4, 6, 8
SAED14_BUF_CDC_*	Non-inverting buffer	2, 4
SAED14_BUF_ECO_*	Non-inverting buffer	1, 2, 3, 4, 6, 7, 8
SAED14_BUF_S_*	Symmetric rise/fall delay buffer	0.5, 0.75, 1, 10, 12, 16, 1.5, 2, 20, 3, 4, 6, 8
SAED14_BUF_UCDC_*	Non-inverting buffer	0.5, 1
SAED14_BUF_U_*	Non-inverting buffer	0.5, 0.75
SAED14_DELPROGS4_*	Delay buffer	12, 16, 4, 6, 8
SAED14_DELPROGS4_Y2_*	Delay buffer	24
SAED14_DELPROGS9_V1_*	Delay buffer	4
SAED14_DELPROGS9_V2_*	Delay buffer	4
SAED14_DEL_R2V1_*	Delay buffer	1, 2
SAED14_DEL_R2V2_*	Delay buffer	1, 2
SAED14_DEL_R2V3_*	Delay buffer	1, 2
SAED14_DEL_L4D100_*	Delay buffer	1, 2
SAED14_CLKSPLT_*	Clock Splitter	1, 8
SAED14_INV_*	Inverter	0.5, 0.75, 1, 10, 12, 16, 1.5, 2, 20, 3, 4, 6, 8
SAED14_INV_ECO_*	Inverter	1, 2, 3, 4, 6, 8
SAED14_INV_S_*	Symmetric rise/fall slew time inverter	0.5, 0.75, 1, 10, 12, 16, 1.5, 2, 20, 3, 4, 5, 6, 7, 8, 9
Logic Gates		
SAED14_AN2B_MM_*	2-Input AND (A inverted input), symmetric rise/fall	1, 12, 16, 2, 20, 4, 6, 8
SAED14_AN2_*	2-Input AND	0.5, 0.75, 1, 2, 4, 8
SAED14_AN2_ECO_*	2-Input AND	2
SAED14_AN2_MM_*	2-Input AND, symmetric rise/fall	0.5, 1, 12, 16, 2, 20, 3, 4, 6, 8
SAED14_AN3_*	3-Input AND	0.5, 0.75, 1, 2, 4, 8
SAED14_AN3_ECO_*	3-Input AND	1
SAED14_AN4_*	4-Input AND	0.5, 0.75, 1, 2, 4, 8
SAED14_AN4_ECO_*	4-Input AND	2
SAED14_ND2B_*	2-Input NAND (A inverted input)	0.75, 1, 1.5, 2, 4
SAED14_ND2B_U_*	2-Input NAND (A inverted input)	0.5
SAED14_ND2_*	2-Input NAND	0.5, 1, 16, 1.5, 2, 3,

Cell name	Cell Description	Driver option
		4, 5, 6, 8
SAED14_ND2_CDC_*	2-Input NAND	0.5, 1, 2, 4
SAED14_ND2_ECO_*	2-Input NAND	1, 2
SAED14_ND2_MM_*	2-Input NAND, symmetric rise/fall	0.5, 1, 10, 12, 16, 2, 3, 4, 6, 8
SAED14_ND3B_*	3-Input NAND (A inverted input)	0.5, 0.75, 1, 2, 4
SAED14_ND3_*	3-Input NAND	0.5, 0.75, 1, 2, 3, 4, 8
SAED14_ND3_ECO_*	3-Input NAND	1
SAED14_ND4_*	4-Input NAND	0.5, 0.75, 1, 2, 3, 4, 8
SAED14_NR2B_*	2-Input NOR (A inverted input)	0.75, 1, 1.5, 2, 4
SAED14_NR2B_U_*	2-Input NOR (A inverted input)	0.5
SAED14_NR2_*	2-Input NOR	0.5, 1, 16, 1.5, 2, 3, 4, 5, 6, 8
SAED14_NR2_ECO_*	2-Input NOR	1, 2
SAED14_NR2_MM_*	Symmetric rise/fall time 2-input NOR	0.5, 1, 10, 12, 16, 2, 3, 4, 6, 8
SAED14_NR3B_*	3-Input NOR (A inverted input)	0.75, 1, 1.5, 2, 4
SAED14_NR3B_U_*	3-Input NOR (A inverted input)	0.5
SAED14_NR3_*	3-Input NOR	0.5, 0.75, 1, 2, 3, 4, 8
SAED14_NR3_ECO_*	3-Input NOR	1
SAED14_NR4_*	4-Input NOR	0.75, 2
SAED14_OR2_*	2-Input OR	0.5, 0.75, 1, 2, 4
SAED14_OR2_ECO_*	2-Input OR	2
SAED14_OR2_MM_*	2-Input OR, symmetric rise/fall	0.5, 0.75, 1, 12, 16, 1.5, 2, 20, 3, 4, 6, 8
SAED14_OR3_*	3-Input OR	0.5, 0.75, 1, 2, 4
SAED14_OR4_*	4-Input OR	1, 2
SAED14_EN2_*	2-Input exclusive NOR	0.5, 1, 1.5, 2, 3, 4
SAED14_EN2_ECO_*	2-Input exclusive NOR	1
SAED14_EN2_V1_*	2-Input exclusive NOR	0.75, 1.5
SAED14_EN3_*	3-Input exclusive NOR	1, 2, 3
SAED14_EN3_U_*	3-Input exclusive NOR	0.5
SAED14_EN4_M_*	4-Input exclusive NOR	1
SAED14_EN4_*	4-Input exclusive NOR	2, 4
SAED14_EN4_U_*	4-Input exclusive NOR	0.5
SAED14_EO2_*	2-Input exclusive OR	0.5, 1, 1.5, 2, 3, 4
SAED14_EO2_ECO_*	2-Input exclusive OR	1
SAED14_EO2_MM_*	2-Input exclusive OR, symmetric rise/fall	0.5, 1, 2, 4
SAED14_EO2_V1_*	2-Input exclusive OR	0.75, 1.5
SAED14_EO3_*	3-Input exclusive OR	0.5, 1, 2, 4
SAED14_EO4_*	4-Input exclusive OR	1, 2, 4

Cell name	Cell Description	Driver option
SAED14_EO4_U_*	4-Input exclusive OR	0.5
Complex Logic Gates		
SAED14_AO21B_*	One 2-input AND into 2-input OR with inverted B	0.5, 1, 2, 4
SAED14_AO21_*	One 2-input AND into 2-input OR	1, 2, 4
SAED14_AO21_ECO_*	One 2-input AND into 2-input OR	1
SAED14_AO21_U_*	One 2-input AND into 2-input OR	0.5
SAED14_AO221_*	Two 2-input ANDs into 3 input OR	0.5, 1, 2, 4
SAED14_AO222_*	Three 2-input ANDs into 3-input OR	1, 2, 4
SAED14_AO222_U_*	Three 2-input ANDs into 3-input OR	0.5
SAED14_AO22_*	Two 2-input ANDs into 2-input OR	0.5, 0.75, 1, 2, 4
SAED14_AO2BB2_*	One 2-input NOR, and one 2-input AND, into a 2-input OR	0.5, 1, 2, 4
SAED14_AO2BB2_V1_*	One 2-input NOR, and one 2-input AND, into a 2-input OR	0.5, 0.75, 1, 2, 4
SAED14_AO31_*	One 3-input AND into 2-input OR	1, 2, 4
SAED14_AO31_U_*	One 3-input AND into 2-input OR	0.5
SAED14_AO32_*	One 3-input AND one 2-input AND into 2-input OR	1, 2, 4
SAED14_AO32_U_*	One 3-input AND one 2-input AND into 2-input OR	0.5
SAED14_AO33_*	Two 3-input ANDs into a 2-input OR	1, 2, 4
SAED14_AO33_U_*	Two 3-input ANDs into a 2-input OR	0.5
SAED14_AOI211_*	One 2-input AND into 3-input NOR	0.5, 1, 2, 4
SAED14_AOI21_*	One 2-input AND into 2-input NOR	0.5, 0.75, 1, 1.5, 2, 3, 4, 6, 8
SAED14_AOI21_ECO_*	One 2-input AND into 2-input NOR	1
SAED14_AOI21_V1_*	One 2-input AND into 2-input NOR	4, 6, 8
SAED14_AOI221_*	Two 2-input ANDs into 3-input NOR	0.5, 1, 2, 4
SAED14_AOI222_*	Three 2-input ANDs into 3-input NOR	0.5, 1, 2, 4
SAED14_AOI22_*	Two 2-input ANDs into 2-input NOR	0.5, 0.75, 1, 1.5, 2, 3, 4, 6
SAED14_AOI22_ECO_*	Two 2-input ANDs into 2-input NOR	1
SAED14_AOI31_*	One 3-input AND into 2-input NOR	0.5, 0.75, 1, 2, 4
SAED14_AOI31_ECO_*	One 3-input AND into 2-input NOR	1
SAED14_AOI32_*	3-input AND and 2-input AND into 2-input NOR	0.5, 0.75, 1, 2, 4
SAED14_AOI33_*	Two 3-input ANDs into a 2-input NOR	0.5, 0.75, 1, 2, 4
SAED14_AOI311_*	One 3-input AND into 3-input NOR	0.5, 0.75, 1, 2, 4
SAED14_OA21B_*	One 2-input OR into 2-input AND	1, 2, 4
SAED14_OA21_MM_*	One 2-input OR into 2-input AND, symmetric rise/fall	1, 2, 4, 6
SAED14_OA21_U_*	One 2-input OR into 2-input AND	0.5
SAED14_OA211_*	One 2-input OR into 3-input AND	1, 2, 4
SAED14_OA211_U_*	One 2-input OR into 3-input AND	0.5
SAED14_OA22_*	Two 2-input ORs into 2-input AND	0.75, 1, 2, 4
SAED14_OA22_U_*	Two 2-input ORs into 2-input AND	0.5

Cell name	Cell Description	Driver option
SAED14_OA2BB2_*	One 2-input OR with inverted inputs + 2-input OR into 2-input AND	0.5, 1, 2, 4
SAED14_OA2BB2_V1_*	One 2-input OR with inverted inputs + 2-input OR into 2-input AND	0.5, 0.75, 1, 2, 4
SAED14_OA221_*	Two 2-input ORs into 3-input AND	1, 2, 4
SAED14_OA221_U_*	Two 2-input ORs into 3-input AND	0.5
SAED14_OA222_*	Three 2-input ORs into a 3-input AND	1, 2, 4
SAED14_OA222_U_*	Three 2-input ORs into a 3-input AND	0.5
SAED14_OA31_*	One 3-input OR into 2-input AND	1, 1.5, 2, 4
SAED14_OA31_U_*	One 3-input OR into 2-input AND	0.5
SAED14_OA32_*	One 3-input OR + one 2-input OR into 2-input AND	0.75, 1, 2, 4
SAED14_OA32_U_*	One 3-input OR + one 2-input OR into 2-input AND	0.5
SAED14_OA33_*	Two 3-input ORs into a 2-input AND	1, 2, 4
SAED14_OA33_U_*	Two 3-input ORs into a 2-input AND	0.5
SAED14_OAI211_*	One 2-input OR into 3-input NAND	0.5, 1, 2, 4
SAED14_OAI21_*	One 2-input OR into 2-input NAND	0.5, 0.75, 1, 1.5, 2, 3, 4
SAED14_OAI21_V1_*	One 2-input OR into 2-input NAND	4, 6, 8
SAED14_OAI221_*	Two 2-input ORs into 3-input NAND	0.5, 1, 2, 4
SAED14_OAI222_*	Three 2-input ORs into 3-input NAND	0.5, 1, 2, 4
SAED14_OAI22_*	Two 2-input ORs into 2-input NAND	0.5, 0.75, 1, 1.5, 2, 3, 4
SAED14_OAI311_*	3-input OR into 3-input NAND	0.5, 0.75, 1, 2, 4
SAED14_OAI31_*	3-input OR into 2-input NAND	0.5, 0.75, 1, 2, 4
SAED14_OAI32_*	3-input OR and 2-input OR into 2-input NAND	0.5, 0.75, 1, 2, 4
Multiplexers		
SAED14_MUX2_*	2-1 multiplexer	1, 1.5, 2, 4
SAED14_MUX2_ECO_*	2-1 multiplexer	1, 2
SAED14_MUX2_MM_*	2-1 multiplexer, symmetric S to X rise/fall	0.5, 1, 2, 4
SAED14_MUX2_U_*	2-1 multiplexer	0.5
SAED14_MUXI2_*	2-1 multiplexer with inverted output	0.5, 1, 2, 4
SAED14_MUXI2_B_*	2-1 multiplexer with inverted output	1
SAED14_MUXI2_ECO_*	2-1 multiplexer with inverted output	1, 2
SAED14_MUXI2_U_*	2-1 multiplexer with inverted output	0.5
SAED14_MUX3_V1M_*	3-1 multiplexer	0.5, 1, 2, 4
SAED14_MUXI3_*	3-1 multiplexer with inverted output	0.5, 1, 2, 4
SAED14_MUX4_V1M_*	4-1 multiplexer	1, 2, 4
SAED14_MUX4_V1U_*	4-1 multiplexer	0.5
SAED14_MUXI4_*	4-1 multiplexer with inverted output	1, 2, 4
SAED14_MUXI4_U_*	4-1 multiplexer with inverted output	0.5
Decoders		
SAED14_ADDF_V1_*	Full adder	0.5, 1, 2
SAED14_ADDF_V2_*	Full adder	0.5, 1, 2

Cell name	Cell Description	Driver option
SAED14_ADDH_*	Half adder	0.5, 1, 2, 4
D Flip-Flops		
SAED14_FDPQB_V2LP_*	D-Flip Flop, pos-edge triggered, qn-only	0.5, 1, 2
SAED14_FDPQB_V2_*	D-Flip Flop, pos-edge triggered, qn-only	1, 2, 4, 8
SAED14_FDPQB_V3_*	D-Flip Flop, pos-edge triggered, qn-only	1, 2, 4, 8
SAED14_FDPQ_V2ECO_*	D-Flip Flop, pos-edge triggered, q-only	1
SAED14_FDPQ_V2_*	D-Flip Flop, pos-edge triggered, q-only	1, 6, 8
SAED14_FDPQ_V3_*	D-Flip Flop, pos-edge triggered, q-only	1, 2, 4
SAED14_FDPRBQ_V2LP_*	D-Flip Flop, pos-edge triggered, □ lo-async-clear, q-only	0.5, 1, 2
SAED14_FDPRBQ_V2_*	D-Flip Flop, pos-edge triggered, □ lo-async-clear, q-only	0.5, 1, 2, 4
SAED14_FDPRBSBQ_V2_*	D-Flip Flop pos-edge triggered, □ lo-async-clear/set, q-only	0.5, 1, 2, 4
SAED14_FDPRB_V3_*	D-Flip Flop, pos-edge triggered, lo-async-clear	2
SAED14_FDPSBQ_*	D-Flip Flop pos-edge triggered, lo-async-set, q-only	0.5, 1, 2, 4
SAED14_FDPSQB_*	D-Flip Flop pos-edge triggered, hi-async-set qn-only	2
SAED14_FDPSYNSBQ_V2_*	D-Flip Flop, pos-edge triggered, syn active low set, q-only	0.5, 1, 2, 4
SAED14_FDPS_V3_*	D-Flip Flop pos-edge triggered, hi-async-set	2
SAED14_FDP_V2LP_*	D-Flip Flop, pos-edge triggered	0.5, 1, 2
SAED14_FDP_V2_*	D-Flip Flop, pos-edge triggered	0.5, 1, 2, 4
SAED14_LSCRLDpq4_*	D-Flip Flop, pos Edge Live/Slave(Zero pin) Retention, clamp high	1, 2
Scan D Flip-Flops		
SAED14_FSDNQ_V3_*	D-Flip Flop w/scan, neg-edge triggered, q-only	1, 2, 4
SAED14_FSDN_V2_*	D-Flip Flop w/scan, neg-edge triggered	0.5, 1, 2, 4
SAED14_FSDPMQ_*	D-Flip Flop w/scan, pos-edge triggered, □ 2-to-1 muxed data inputs, q-only	0.5, 1, 2, 4
SAED14_FSDPMQ_LP_*	D-Flip Flop w/scan, pos-edge triggered, □ 2-to-1 muxed data inputs, q-only	0.5, 1, 2
SAED14_FSDPQB_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, □ qn-only	0.5, 1, 2
SAED14_FSDPQB_V2_*	D-Flip Flop w/scan, pos-edge triggered, qn-only	0.5, 1, 2, 4, 8
SAED14_FSDPQB_V3_*	D-Flip Flop w/scan, pos-edge triggered, □ qn-only	1, 2, 4, 8
SAED14_FSDPQ_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, □ q-only	0.5, 1, 2
SAED14_FSDPQ_V2_*	D-Flip Flop w/scan, pos-edge triggered	0.5, 1, 2, 4

Cell name	Cell Description	Driver option
	triggered, \square q-only	
SAED14_FSDPQ_V3_*	D-Flip Flop w/scan, pos-edge triggered, \square q-only	1, 2, 4
SAED14_FSDPRBQ_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-async-clear, q-only	0.5, 1, 2
SAED14_FSDPRBQ_V2_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-async-clear, q-only	0.5, 1, 2, 4
SAED14_FSDPRBQ_V3_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-async-clear, q-only	1, 2, 4
SAED14_FSDPRBSBQ_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-async-clear/set, q-only	0.5, 1, 2
SAED14_FSDPRBSBQ_V2_*	D-Flip Flop w/scan, pos-edge triggered, lo-async-clear/set, q-only	0.5, 1, 2, 4
SAED14_FSDPSBQ_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, lo-async-/set, q-only	0.5, 1, 2
SAED14_FSDPSBQ_V2_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-async-/set, q-only	0.5, 1, 2, 4
SAED14_FSDPSYNRBQ_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, syn-active low reset, q-only	0.5, 1, 2
SAED14_FSDPSYNRBQ_V2_*	D-Flip Flop w/scan, pos-edge triggered, \square syn-active low reset, q-only	0.5, 1, 2, 4
SAED14_FSDPSYNRBQ_V3_*	D-Flip Flop w/scan, pos-edge triggered, \square syn-active low reset, q-only	1, 2, 4
SAED14_FSDPSYNSBQ_V2LP_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-sync-/set, q-only	0.5, 1, 2
SAED14_FSDPSYNSBQ_V2_*	D-Flip Flop w/scan, pos-edge triggered, \square lo-sync-/set, q-only	0.5, 1, 2, 4
SAED14_FSDP_V2LP_*	D-Flip Flop w/scan, pos-edge triggered	0.5, 1, 2
SAED14_FSDP_V2_*	D-Flip Flop w/scan, pos-edge triggered	0.5, 1, 2, 4
Latches		
SAED14_LDCKNR2PQ_*	D-latch, 2-to-1 nor clock inputs, q-only	5
SAED14_LDND2NQ_*	2-to-1 nand data inputs latch, neg-gate, \square q-only	1, 2, 4
SAED14_LDNQOR2_*	D-latch with input as the nor of two enable signals, neg-gate, q-only	1, 2, 4
SAED14_LDNQ_*	D-latch, neg-gate, q-only	1, 2, 3, 4, 5, 6, 8
SAED14_LDNQ_U_*	D-latch, neg-gate, q-only	0.5
SAED14_LDNQ_V1_*	D-latch, neg-gate, q-only	1, 2, 4
SAED14_LDNR2PQ_*	2-to-1 nor data inputs latch, pos-gate, q-only	1, 2, 4
SAED14_LDNRBQ_V2_*	D-latch, neg-gate, lo-async-clear, q-only	0.5, 1, 2, 4
SAED14_LDOR2PQ_*	2-to-1 or data inputs latch, pos-gate, q-only	1, 2, 4
SAED14_LDPQ_*	D-latch, pos-gate, q-only	1, 2, 3, 4, 5, 6, 8
SAED14_LDPQ_ECO_*	D-latch, pos-gate, q-only	1
SAED14_LDPQ_U_*	D-latch, pos-gate, q-only	0.5
SAED14_LDPQ_V1_*	D-latch, pos-gate, q-only	1, 2, 4
SAED14_LDPRSQB_*	D-latch, pos-gate, hi-async-clear, \square	1

Cell name	Cell Description	Driver option
	hi-async-set, qn-only	
SAED14_LDPSBQ_V2_*	D-latch, pos-gate, lo-async-set, q-only	0.5, 1, 2, 4
Clocked Gates		
SAED14_CKGTNLT_V5_*	Clock Gater, negative clock, synchronous enable, pre control	1, 12, 2, 3, 4, 5, 6, 8
SAED14_CKGTPLT_V5_*	Clock Gater, positive clock, synchronous enable, pre control	1, 12, 16, 2, 20, 24, 3, 4, 5, 6, 8
SAED14_CKGTPL_V5_*	Positive edge triggered, Clock Gater	0.5, 1, 2, 4
SAED14_CKINVGTPLT_V7_*	Clock Gater with inverted output, positiveclock, synchronous enable, pre control	1, 2, 3, 4, 5, 6, 8
Miscellaneous Cells		
SAED14_TIE0_*	Tie low	4
SAED14_TIE1_V1ECO_*	Tie high	1
Tap Cells		
SAED14_CAPTTAPP6	Tap cell	
SAED14_TAPPP10	Tap cell, Always On	
Isolation Cells		
SAED14_AN2_ISO_*	ISOLATION CELL, High-Enable, 2-Input-AND	1, 4
SAED14_AN2_ISO4_*	ISOLATION CELL, High-Enable, 2-Input-AND, 4bit	1, 4
SAED14_ISOFSDPQ_PECO_*	ISOLATION D-Flip Flop w/scan, pos-edge triggered, syn-active low reset, q-only, Always On	8, 4
SAED14_ISOS0CL1_PECO_*	ISOLATION CELL-Enable0 Input OR, Always On	1, 2, 4, 8
SAED14_ISOS0CL1_P_*	ISOLATION CELL-Enable0 Input OR, Always On	2, 8
SAED14_ISOS1CL0_PECO_*	ISOLATION CELL-Enable1 Input AND, Always On	1, 2, 4, 8
SAED14_ISOS1CL0_P_*	ISOLATION CELL-Enable1 Input AND, Always On	2, 8
SAED14_OR2_ISO_*	ISOLATION CELL, Low-Enable, 2-Input-OR	1, 4
SAED14_NR2_ISO_*	ISOLATION CELL, Low-Enable, 2-Input-NOR	1, 4
Level Shifters		
SAED14_LVLDUFE0_IY2V1_*	VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
SAED14_LVLDUFE0_IY2_*	VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
SAED14_LVLDUFE1_IY2V1_*	VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
SAED14_LVLDUFE1_IY2_*	VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
SAED14_LVLDUF_IY2V1_*	VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
SAED14_LVLDUF_IY2_*	VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8

Cell name	Cell Description	Driver option
SAED14_ELVLDNOR_V2_*	Nor Style High to Low Enable Level Shifter	1, 2, 4, 8
SAED14_ELVLDNOR_IY2_*	Nor Style High to Low Enable Level Shifter	1, 2, 4, 8
SAED14_LVLBUF4_E0_IY2V1_*	4 bit VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
SAED14_LVLBUF4_E0_IY2_*	4 bit VDD Up-Down-Level Translator - Buffer	1, 10, 12, 2, 3, 4, 6, 8
Always on Cells		
SAED14_AN2B_PMM_*	2-Input AND (A inverted input), symmetric rise/fall, always-on	2, 8
SAED14_AN2B_PSECO_*	2-Input AND (A inverted input), symmetric rise/fall, always-on	1, 2, 4, 8
SAED14_AOLVLDNOR_E0_IY2V1_*	Nor Style Low to High Enable Level Shifter, Always On	1, 2, 4, 8
SAED14_AOLVLDNOR_E0_IY2_*	Nor Style Low to High Enable Level Shifter, Always On	1, 2, 4, 8
SAED14_AOLVLDNOR_E1_IY2V1_*	Nor Style Low to High Enable Level Shifter, Always On	1, 2, 4, 8
SAED14_AOLVLDNOR_E1_IY2_*	Nor Style Low to High Enable Level Shifter, Always On	1, 2, 4, 8
SAED14_AOLVLDNOR_IY2V1_*	Nor Style Low to High Enable Level Shifter, Always On	1, 2, 4, 8
SAED14_AOLVLDNOR_IY2_*	Nor Style Low to High Enable Level Shifter, Always On	1, 2, 4, 8
SAED14_AOLVLDBUF_E0_IY2V1_*	VDD Up-Down-Level Translator -Buffer, Always On	1, 10, 12, 2, 3, 4, 6, 8
SAED14_AOLVLDBUF_E1_IY2V1_*	VDD Up-Down-Level Translator -Buffer, Always On	1, 10, 12, 2, 3, 4, 6, 8
SAED14_AOLVLDBUF_IY2V1_*	VDD Up-Down-Level Translator -Buffer, Always On	1, 10, 12, 2, 3, 4, 6, 8
SAED14_AOBUF_IW_*	Always on Non-inverting Buffer Insulated Well	0.75, 3, 6
SAED14_BUF_PECO_*	Buffer, Always On	4, 8, 12, 1, 2
SAED14_BUF_PS_*	Symmetric rise/fall delay buffer, Always On	0.75, 1.5, 3, 6
SAED14_AOINV_IW_*	Always on inverter Insulated Well	0.5, 1, 1.5, 2, 3, 4, 6
SAED14_INV_PECO_*	Inverter, Always-on	4, 8, 12, 1, 2
SAED14_INV_PS_*	Symmetric rise/fall time inverter, State Retention	1, 2, 3, 6
SAED14_OR2B_PMM_*	2-Input OR (A inverted input), symmetric rise/fall, always-on, State Retention	2, 8
SAED14_OR2B_PSECO_*	2-Input OR (A inverted input), symmetric rise/fall, always-on, State Retention	1, 2, 4, 8
SAED14_TIE0_PV1ECO_*	Tie low, Always-on	1
SAED14_TIE1_PV1ECO_*	Tie high, Always-on	1
SAED14_TIEDIN_PV1ECO_*	Diode made of MOS usable for ECO version, □Always-on	6
De-coupling Filler Cells		
SAED14_DCAP_PV1ECO_*	Filler cell; both NMOS and PMOS; butterfly □architecture; decoupling;	12, 15, 18, 6, 9

Cell name	Cell Description	Driver option
	Always On; State Retention	
SAED14_DCAP_PV3_*	Filler cell; both NMOS and PMOS; butterfly architecture; decoupling; Always On; State Retention	3

2.10. Digital Standard Cell Library Deliverables

Table 2.12. Digital Standard Cell Library deliverables

N	Type	Description
1	.pdf	Databook / User guide, Layer usage file
2	.db, .lib	Synthesis
3	.v	Verilog simulation models
4	.ndm	NDM models (frame-only NDM)
5	.cdl, .sp	LVS, HSPICE netlists
6	.spf	Extracted C and RC netlists for different corners
7	.gds	GDSII layout views
8	.clf	Cell antenna information
9	.lef	LEF files
10	.FRAM, .CEL	FRAM views, layout views

2.11. Digital Standard Cell Library Deliverables

Table 2.13. Digital Standard Cell Library deliverables

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1	.pdf	Databook / User guide, Layer usage file
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4	.cdl, .sp	LVS, HSPICE netlists
5	.spf	Extracted C and RC netlists for different corners
6	.gds	GDSII layout views
7	.clf	Cell antenna information
8	.lef	LEF files
9	.FRAM, .CEL, ndm	FRAM views, layout views

2.12. Physical structure of digital cell

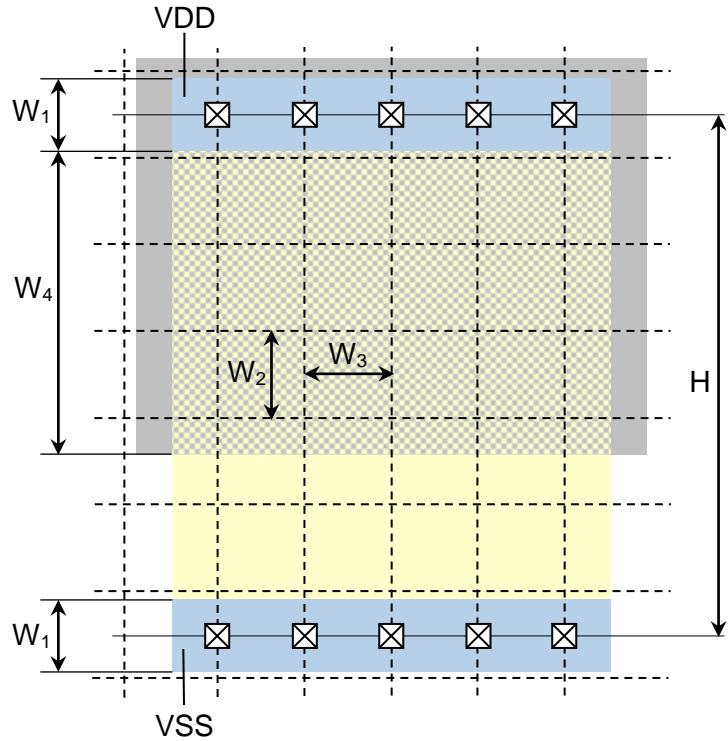


Figure 2.1. Physical structure of digital standard cells

The selection of physical structure of digital cell should be aimed at providing maximum cell density in digital designs. It is more important to provide minimal area for the most frequently used cells. In general, these are usually NAND cells with two inputs, and D flip-flops. The width of the power rails will be selected on the basis of acceptable current density given by the design rules, and electromigration.

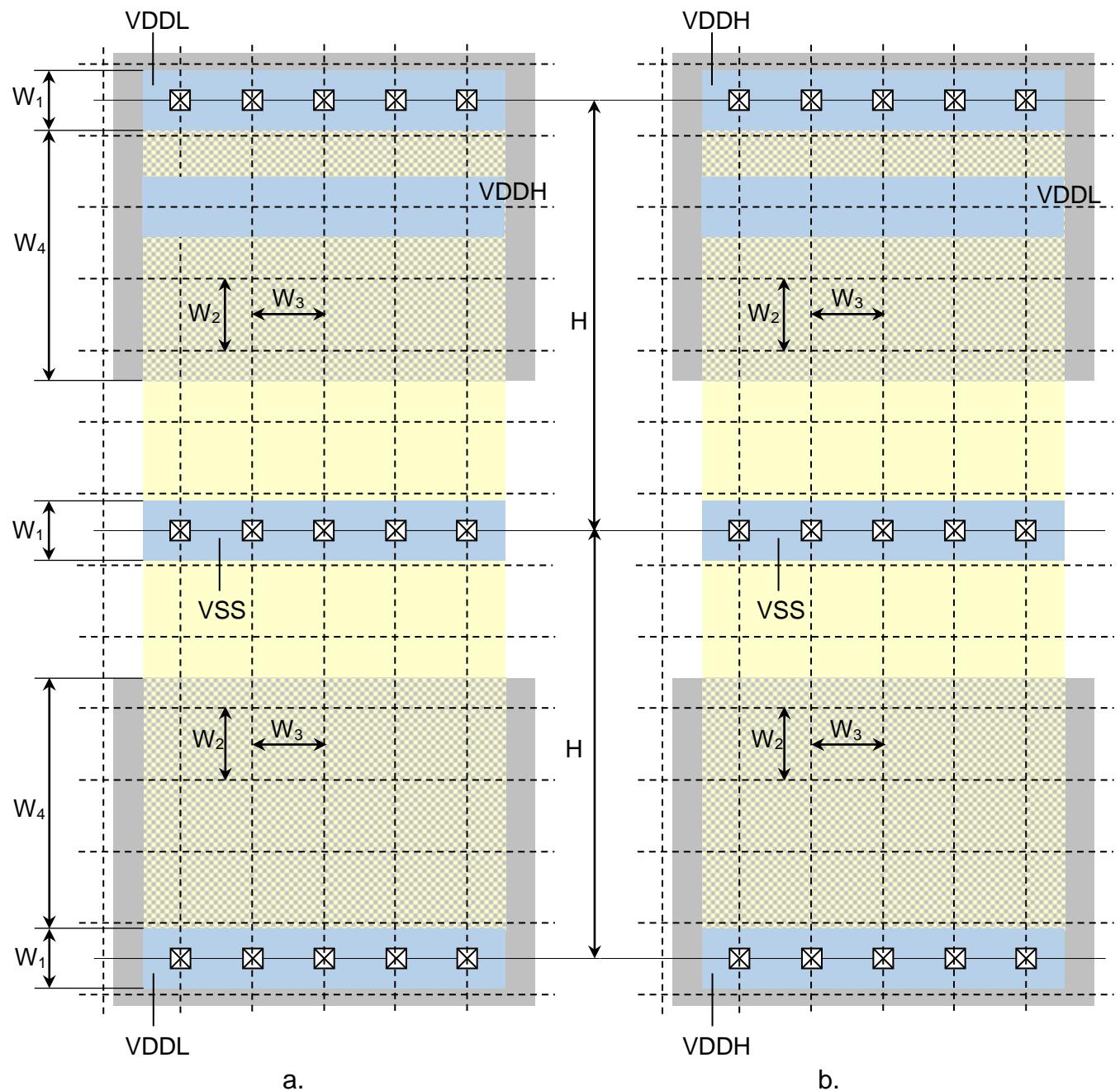


Figure 2.2. Physical structure of Level-shifter cells:
a. High-to-Low, b. Low-to-High

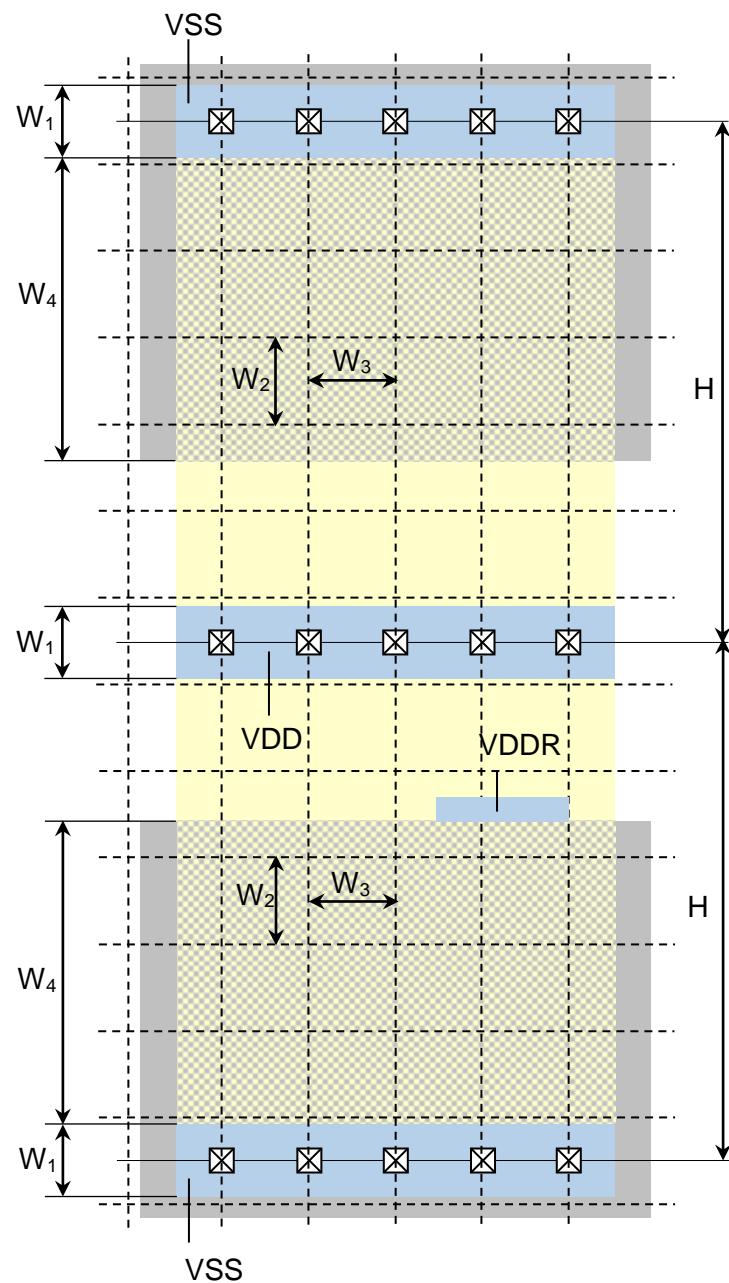


Figure 2.3. Physical structure of Always on and Power Gating Cells

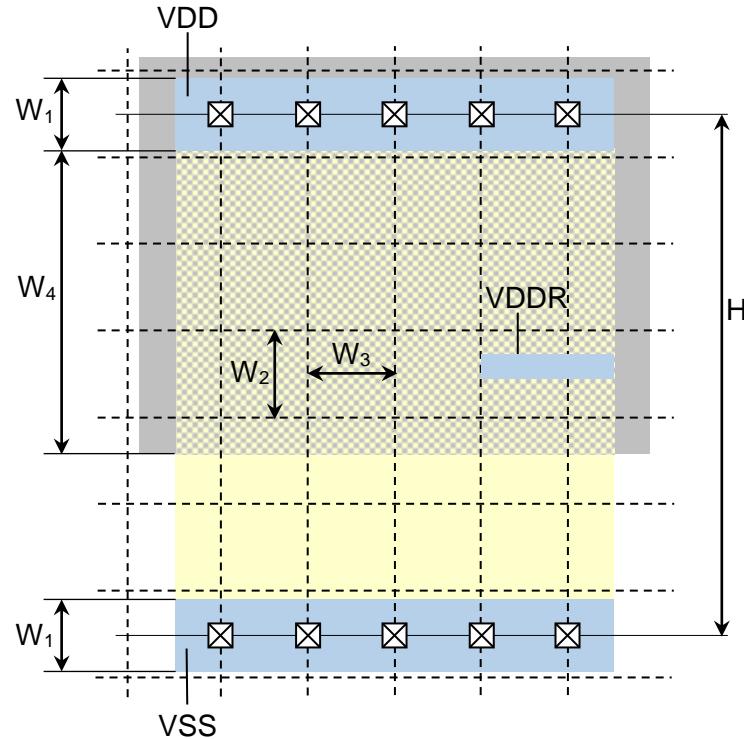


Figure 2.4. Physical structure of digital standard cells: Retention Flip-Flops

Table 2.14. Physical structure specification

Parameter	Symbol	Value
Cell height	H	0.6 um
Power rail width	W ₁	0.094 um
Vertical grid	W ₂	0.06 um (d_{track})
Horizontal grid	W ₃	0.074 um (d_{track})
Horizontal grid offset	-	0.037 um
NWell height	W ₄	0.253 um

d_{track} is the minimum center-to-center distance for metal2 layers (with VIA12). It will be used as a grid for cell architecture.

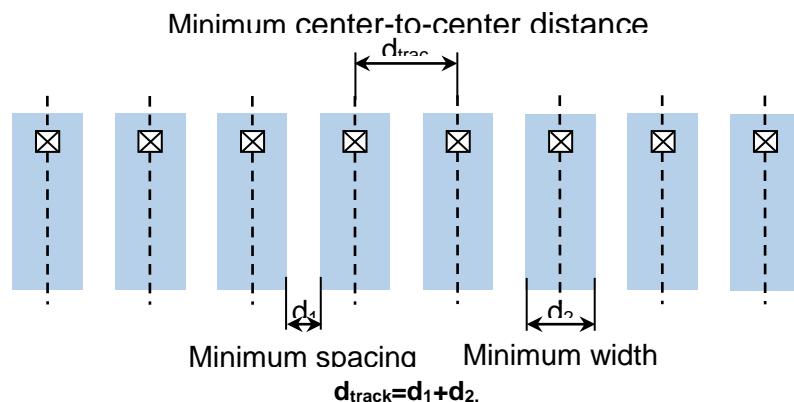


Figure 2.5. Definition of d_{track}

2.13. Digital Standard Cells' descriptions

BUF_*

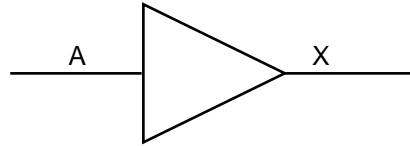


Figure 2.6. Logic Symbol of BUF

Table 2.15. BUF Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8 V DC, Temp=25 Deg.C, Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area (um ²)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz		
BUF_1	1 x Csl	29	0.17	8.4	0.2664	
BUF_10	10 x Csl	34	1.2	78	0.7104	
BUF_12	12 x Csl	33	1.46	94	0.8436	
BUF_16	16 x Csl	34	1.93	136	1.0656	
BUF_1P5	1.5 x Csl	32	0.2	12	0.3108	
BUF_2	2 x Csl	31	0.27	15	0.3108	
BUF_20	20 x Csl	68	2.4	158	1.2876	
BUF_3	3 x Csl	34	0.37	24	0.3552	
BUF_4	4 x Csl	25	0.5	31	0.3996	
BUF_6	6 x Csl	33	0.73	47	0.4884	
BUF_8	8 x Csl	32	0.98	62	0.6216	

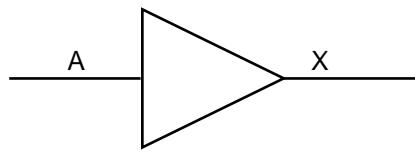


Figure 2.6. Logic Symbol of BUF_CDC

Table 2.16. BUF_CDC Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8V, Temperature=25Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area (um ²)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
BUF_CDC_2	2 x Csl	31	0.27	15.8	0.3108	
BUF_CDC_4	4 x Csl	31	0.5	31.3	0.3996	

BUF_ECO_*

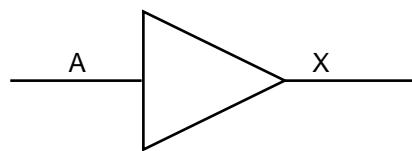


Figure 2.7. Logic Symbol of BUF_ECO

Table 2.17. BUF_ECO Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8V, Temperature=25Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
BUF_ECO_1	1 x Csl	25	0.17	8.4	0.2664	
BUF_ECO_2	2 x Csl	32	0.27	16.6	0.489	
BUF_ECO_3	3 x Csl	34	0.37	24.8	0.6216	
BUF_ECO_4	4 x Csl	33	0.5	33.1	0.88	
BUF_ECO_6	6 x Csl	35	0.73	49.2	1.1544	
BUF_ECO_7	7 x Csl	37	0.84	57.2	1.2876	
BUF_ECO_8	8 x Csl	38	0.94	65.2	1.4208	

BUF_S *

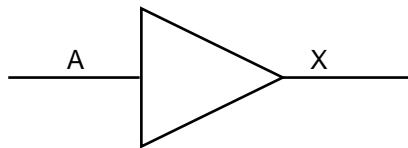


Figure 2.8. Logic Symbol of BUF_S

Table 2.18. BUF_S Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8V, Temperature=25Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
BUF_S_0P5	0.5 x Csl	31	0.08	4.4	0.2664	
BUF_S_0P75	0.75 x Csl	30	0.13	6.4	0.2664	
BUF_S_1	1 x Csl	30	0.17	8.4	0.2664	

BUF_S_10	10 x Csl	34	1.2	78.4	0.756058
BUF_S_12	12 x Csl	34	1.46	93.3	0.8436
BUF_S_16	16 x Csl	34	1.93	57.2	1.11
BUF_S_1P5	1.5 x Csl	30	0.13	6.4	0.3108
BUF_S_2	2 x Csl	32	0.27	15.8	0.3108
BUF_S_20	20 x Csl	35	2.4	15.8	1.2876
BUF_S_3	3 x Csl	34	0.37	23.9	0.3996
BUF_S_4	4 x Csl	31	0.5	31.3	0.3996
BUF_S_6	6 x Csl	34	0.73	46.8	0.4884
BUF_S_8	8 x Csl	33	0.99	62.5	0.666

BUF_UCDC_*

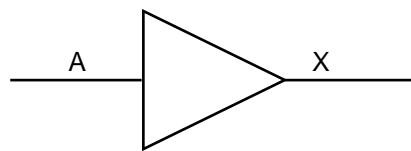


Figure 2.9. Logic Symbol of BUF_UCDC

Table 2.19. BUF_UCDC Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8 V DC, Temp=25 Deg.C, Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Deg.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
BUF_UCDC_0P5	0.5 x Csl	31	0.08	4.4	0.2664	
BUF_UCDC_1	1 x Csl	30	0.17	8.4	0.2664	

BUF_U_*

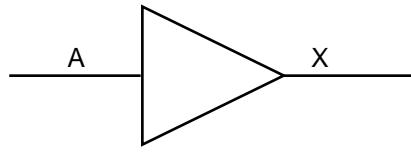


Figure 2.10. Logic Symbol of BUF_U

Table 2.20. BUF_U Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8 V DC, Temp=25 Deg.C, Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Deg.C)	Dynamic		
BUF_U_0P5	0.5 x Csl	31	0.084	4.4	0.2664	
BUF_U_0P75	0.75 x Csl	30	0.13	6.4	0.2664	

DELPROGS4_*

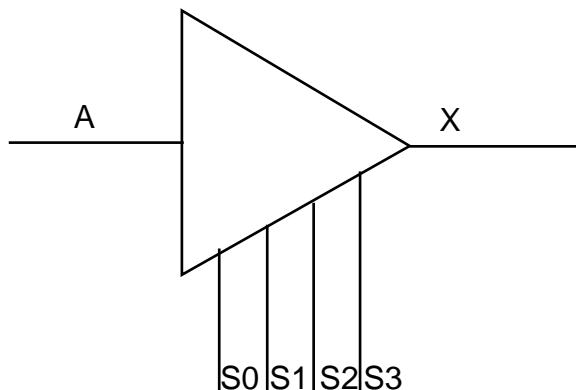


Figure 2.11. Logic Symbol of DELPROGS4

Table 2.21. DELPROGS4 Truth Table

A	X
0	0
1	1

General Information

Cell Name	Operating Conditions: VDD=0.8V, Temperature=25Operating Frequency: Freq=1 GHz, Capacitive Standard Load: Csl=2.6 fF				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
DELPROGS4_12	12 x Csl	53	1.98	48.9	2.5308	
DELPROGS4_16	14 x Csl	56	2.4	65.5	2.7972	
DELPROGS4_4	4 x Csl	47	1.07	15.8	1.776	
DELPROGS4_6	6 x Csl	49	1.31	24	1.9536	
DELPROGS4_8	8 x Csl	50	1.58	33.3	2.1756	

DELPROGS4_Y2 *

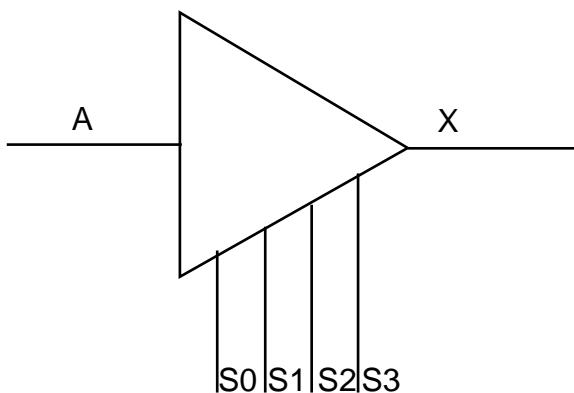


Figure 2.12. Logic Symbol of DELPROGS4_Y2

Table 2.22. DELPROGS4_Y2 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
DELPROGS4_Y2_24	24 x Csl	62	3.62	0.21	5.0616	

DELPROGS9_V1_*

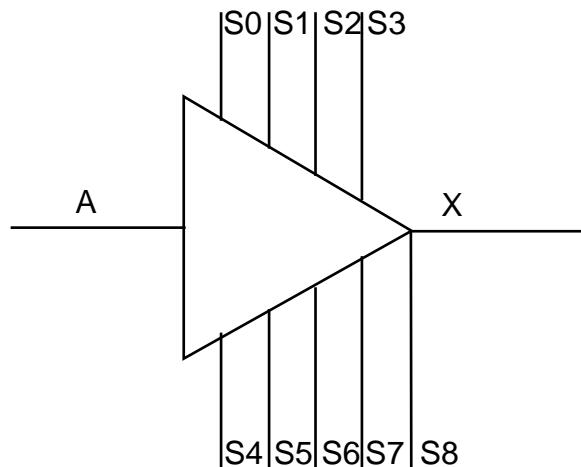


Figure 2.13. Logic Symbol of DELPROGS9_V1

Table 2.23. DELPROGS9_V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
DELPROGS9_V1_4	4 x Csl	80	2.44	26.58	4.5288	

DELPROGS9_V2_*

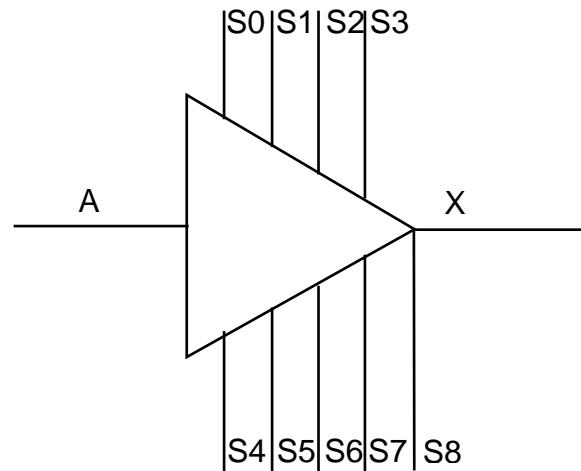


Figure 2.14. Logic Symbol of DELPROGS9_V2

Table 2.24. DELPROGS9_V2 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
DELPROGS9_V2_4	4 x Csl	105	3.66	26.58	6.0828	

DEL_R2V1_*

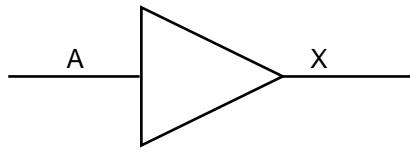


Figure 2.15. Logic Symbol of DEL_R2V1

Table 2.25. DEL_R2V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	pW/MHz	
DEL_R2V1_1	1 x Csl	41	0.12	0.28	0.3108	
DEL_R2V1_2	2 x Csl	47	0.36	0.36	0.3552	

DEL_R2V2_*

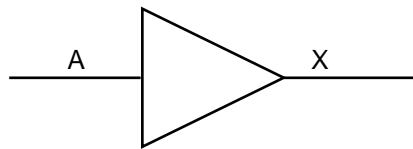


Figure 2.16. Logic Symbol of DEL_R2V2

Table 2.26. DEL_R2V2 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
DEL_R2V2_1	1 x Csl	49	0.06	0.45	0.3552	
DEL_R2V2_2	2 x Csl	47	0.12	0.67	0.4884	

DEL_R2V3_*

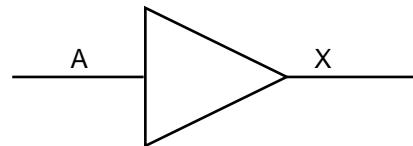


Figure 2.17. Logic Symbol of DEL_R2V3

Table 2.27. DEL_R2V2 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
DEL_R2V3_1	1 x Csl	55	0.09	0.65	0.3996	
DEL_R2V3_2	2 x Csl	58	0.15	0.8	0.4884	

DEL_L4D100_*

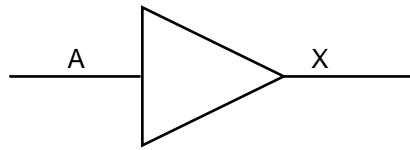


Figure 2.18. Logic Symbol of DEL_L4D100

Table 2.28. DEL_L4D100 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz				
DEL_L4D100_1	1 x Csl	45	0.19	0.56	0.4884	
DEL_L4D100_2	2 x Csl	46	0.29	0.63	0.5328	

CLKSPLT_*

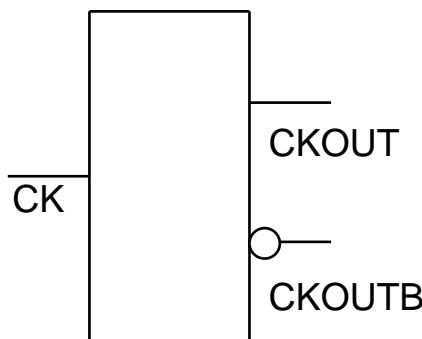


Figure 2.19. Logic Symbol of CLKSPLT
Table 2.29. CLKSPLT Truth Table

CK	CKOUT	CKOUTB
1	1	0
0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
CLKSPLT_1	1 x Csl	34	1.02	0.56	1.1544	
CLKSPLT_8	8 x Csl	39	2.19	0.63	1.6428	

INV_*

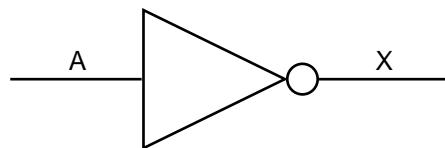


Figure 2.20. Logic Symbol of INV_*

Table 2.30. INV_*Truth Table

A	X
0	1
1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
INV_0P5	0.5 x Csl	33	0.05	0.04	0.1776	
INV_0P75	0.75 x Csl	33	0.08	0.05	0.1776	
INV_1	1 x Csl	32	0.1	0.07	0.1776	
INV_10	10 x Csl	32	1.01	0.73	0.5772	
INV_12	12 x Csl	32	1.21	0.88	0.666	
INV_16	16 x Csl	32	1.62	1.2	0.8436	
INV_1P5	1.5 x Csl	32	0.1	0.07	0.1776	
INV_2	2 x Csl	31	0.2	0.14	0.222	
INV_20	20 x Csl	22	2.02	1.48	1.0212	
INV_3	3 x Csl	32	0.23	0.16	0.2664	
INV_4	4 x Csl	32	0.4	0.29	0.3108	
INV_6	6 x Csl	32	0.6	0.43	0.3996	
INV_8	8 x Csl	32	0.81	0.59	0.4884	

INV_ECO_*

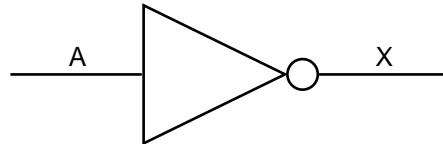


Figure 2.21. Logic Symbol of INV_ECO

Table 2.31. INV_ECO Truth Table

A	X
0	1
1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz		
INV_ECO_1	1 x Csl	32	0.1	0.07	0.222	
INV_ECO_2	2 x Csl	32	0.2	0.14	0.3552	
INV_ECO_3	3 x Csl	32	0.3	0.21	0.4884	
INV_ECO_4	4 x Csl	32	0.4	0.33	0.6216	
INV_ECO_6	6 x Csl	32	0.6	0.59	0.888	
INV_ECO_8	8 x Csl	33	0.8	0.67	1.1544	

INV_S_*

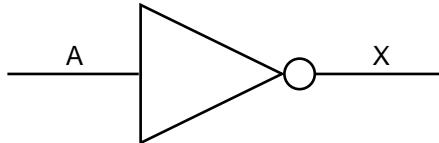


Figure 2.22. Logic Symbol of INV_S

Table 2.32. INV_S Truth Table

A	X
0	1
1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
INV_S_0P5	0.5 x Csl	33	0.05	0.04	0.1776	
INV_S_0P75	0.75 x Csl	32	0.08	0.05	0.1776	
INV_S_1	1 x Csl	32	1.01	0.07	0.1776	
INV_S_10	10 x Csl	32	1.01	0.81	0.4884	
INV_S_12	12 x Csl	32	1.2	0.98	0.666	
INV_S_16	16 x Csl	32	1.62	1.31	0.8436	
INV_S_1P5	1.5 x Csl	32	0.15	0.12	0.222	
INV_S_2	2 x Csl	31	0.2	0.15	0.222	
INV_S_20	20 x Csl	22	2.02	1.65	1.0212	
INV_S_3	3 x Csl	32	0.3	0.21	0.3108	
INV_S_4	4 x Csl	32	0.4	0.29	0.3108	
INV_S_5	5 x Csl	32	0.5	0.36	0.3996	
INV_S_6	6 x Csl	32	0.6	0.5	0.3996	
INV_S_7	7 x Csl	32	0.7	0.57	0.4884	
INV_S_8	8 x Csl	32	0.8	0.65	0.4884	
INV_S_9	9 x Csl	32	0.9	0.73	0.5772	

AN2B_MM_*

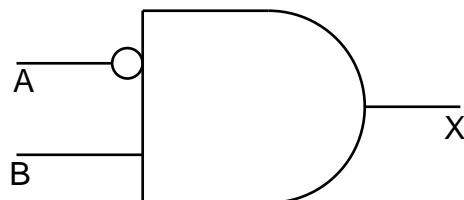


Figure 2.23. Logic Symbol of AN2B_MM

Table 2.33. AN2B_MM Truth Table

A	B	X
0	0	0
0	1	1
1	0	0
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AN2B_MM_1	1 x Csl	34	0.31	0.23	0.3996	
AN2B_MM_12	12 x Csl	41	1.71	0.53	1.1544	
AN2B_MM_16	16 x Csl	42	2.21	0.62	1.4208	
AN2B_MM_2	2 x Csl	38	0.54	0.24	0.624	
AN2B_MM_20	20 x Csl	32	2.7	0.59	1.6872	
AN2B_MM_4	4 x Csl	40	0.49	0.24	0.5364	
AN2B_MM_6	6 x Csl	41	0.85	0.27	0.714	
AN2B_MM_8	8 x Csl	39	1.21	0.46	0.888	

AN2_*

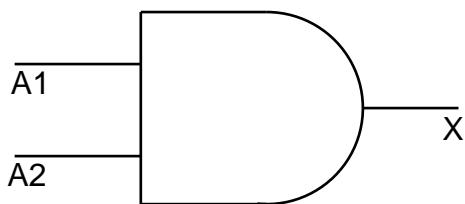


Figure 2.24. Logic Symbol of AN2

Table 2.34. AN2 Truth Table

A1	A2	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AN2_0P5	0.5 x Csl	36	0.16	0.06	0.3552	
AN2_0P75	0.75 x Csl	34	0.19	0.09	0.3558	
AN2_1	1 x Csl	33	0.17	0.09	0.3108	
AN2_2	2 x Csl	33	0.28	0.12	0.3552	
AN2_4	4 x Csl	33	0.56	0.24	0.5328	
AN2_8	8 x Csl	33	1.12	0.48	0.8904	

AN2_ECO_*

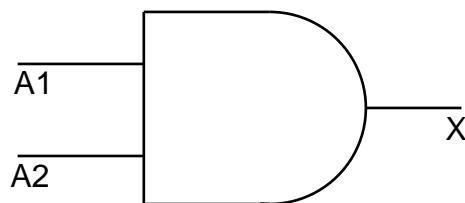


Figure 2.25. Logic Symbol of AN2_ECO

Table 2.35. AN2_ECO Truth Table

A1	A2	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AN2_ECO_2	2 x Csl	38	0.33	0.12	0.7548	

AN2_MM_*

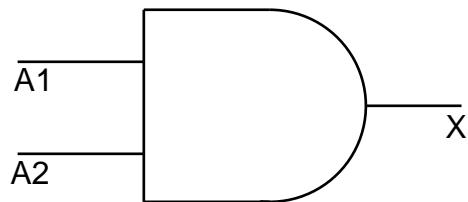


Figure 2.26. Logic Symbol of AN2_MM

Table 2.36. AN2_MM Truth Table

A1	A2	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz				
AN2_MM_0P5	0.5 x Csl	31	0.11	0.06	0.3108	
AN2_MM_1	1 x Csl	33	0.16	0.06	0.3108	
AN2_MM_12	12 x Csl	37	1.59	0.37	1.0656	
AN2_MM_16	16 x Csl	35	1.99	0.37	1.2432	
AN2_MM_2	2 x Csl	36	0.26	0.06	0.3552	
AN2_MM_20	20 x Csl	35	2.49	0.46	1.5096	
AN2_MM_3	3 x Csl	36	0.4	0.09	0.3996	
AN2_MM_4	4 x Csl	36	0.53	0.13	0.5328	
AN2_MM_6	6 x Csl	36	0.79	0.19	0.6216	
AN2_MM_8	8 x Csl	35	1.09	0.28	0.7992	

AN3_*

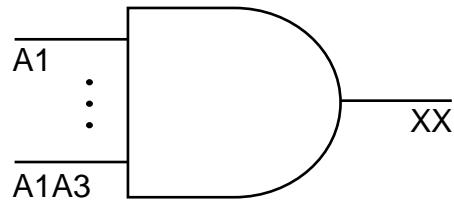


Figure 2.27. Logic Symbol of AN3

Table 2.37. AN3Truth Table

A1	A2	A3	X
0	-	-	0
-	0	-	0
-	-	0	0
1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz				
AN3_0P5	0.5 x Csl	37	0.14	0.08	0.3552	
AN3_0P75	0.75 x Csl	36	0.22	0.1	0.3552	
AN3_1	1 x Csl	36	0.22	0.1	0.3552	
AN3_2	2 x Csl	39	0.26	0.08	0.3996	
AN3_4	4 x Csl	38	0.56	0.16	0.6216	
AN3_8	8 x Csl	37	1.11	0.24	1.0656	

AN3_ECO_*

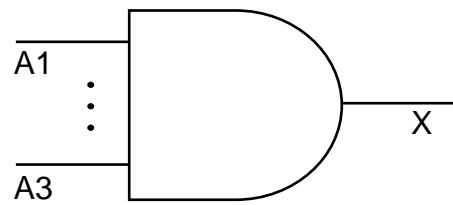


Figure 2.28. Logic Symbol of AN3_ECO

Table 2.38. AN3_ECO Truth Table

A1	A2	A3	X
0	-	-	0
-	0	-	0
-	-	0	0
1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
AN3_ECO_1	1 x Csl	42	0.2	0.1	0.6216	

AN4_*

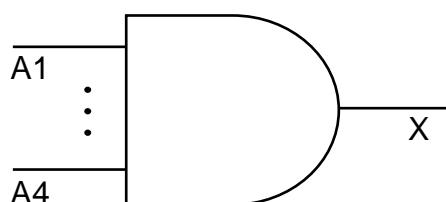


Figure 2.29. Logic Symbol of AN4

Table 2.39. AN4 Truth Table

A1	A2	A3	A4	X
0	-	-	-	0
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
AN4_0P5	0.5 x Csl	39	0.75	0.08	0.4002	
AN4_0P75	0.75 x Csl	39	0.19	0.09	0.4002	
AN4_1	1 x Csl	39	0.22	0.08	0.3996	
AN4_2	2 x Csl	41	0.28	0.07	0.4446	
AN4_4	4 x Csl	44	0.53	0.13	0.7648	
AN4_8	8 x Csl	41	1.32	0.26	1.2894	

AN4_ECO_*

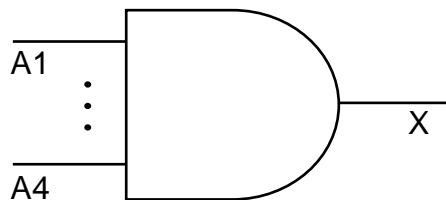


Figure 2.30. Logic Symbol of AN4_ECO

Table 2.40. AN4_ECO Truth Table

A1	A2	A3	A4	X
0	-	-	-	0
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AN4_ECO_2	2 x Csl	48 ps	0.23 nW	0.14 pW/MHz	0.888	

ND2B_*

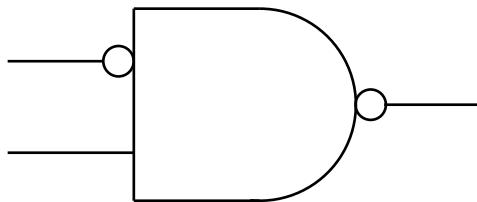


Figure 2.31. Logic Symbol of ND2B

Table 2.41. ND2B Truth Table

A	B	X
0	0	1
0	1	0
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
ND2B_0P75	0.75 x Csl	42	0.24	0.26	0.6216	
ND2B_1	1 x Csl	42	0.24	0.41	0.6216	
ND2B_1P5	1.5 x Csl	40	0.49	0.41	0.888	
ND2B_2	2 x Csl	40	0.49	0.41	0.888	
ND2B_4	4 x Csl	39	0.97	0.77	1.4208	

ND2B_U_*

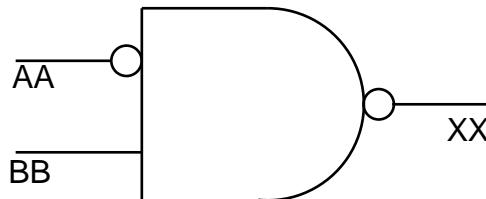


Figure 2.32. Logic Symbol of ND2B_U

Table 2.42. ND2B_U Truth Table

A	B	X
0	0	1
0	1	0
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
ND2B_U_0P5	0.5 x Csl	30	0.12	0.19	0.3108	

ND2_*

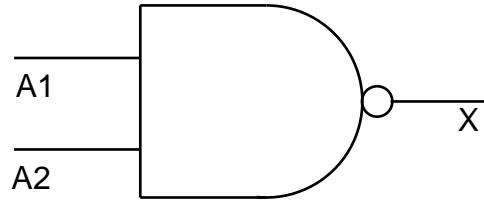


Figure 2.33. Logic Symbol of ND2

Table 2.43. ND2 Truth Table

A1	A2	X
0	0	1
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz		
ND2_0P5	0.5 x Csl	31	0.18	0.11	0.3108	
ND2_1	1 x Csl	31	0.2	0.35	0.3108	
ND2_16	16 x Csl	36	1.45	0.35	1.554	
ND2_1P5	1.5 x Csl	32	0.28	0.26	0.3996	
ND2_2	2 x Csl	32	0.03	0.26	0.3996	
ND2_3	3 x Csl	32	0.4	0.36	0.4884	
ND2_4	4 x Csl	31	0.5	0.45	0.5772	
ND2_5	5 x Csl	33	0.6	0.45	0.666	
ND2_6	6 x Csl	64	0.7	0.51	0.7548	
ND2_8	8 x Csl	32	0.9	0.67	0.9324	

ND2_CDC_*

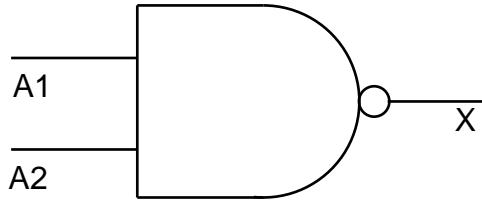


Figure 2.34. Logic Symbol of ND2_CDC

Table 2.44. ND2_CDC Truth Table

A1	A2	X
0	0	1
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ND2_CDC_0P5	0.5 x Csl	32	0.1	0.09	0.222	
ND2_CDC_1	1 x Csl	32	0.1	0.09	0.222	
ND2_CDC_2	2 x Csl	29	0.22	0.24	0.3108	
ND2_CDC_4	4 x Csl	30	0.44	0.49	0.4884	

ND2_ECO_*

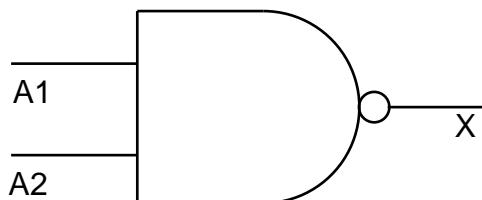


Figure 2.35. Logic Symbol of ND2_ECO

Table 2.45. ND2_ECO Truth Table

A1	A2	X
0	0	1
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
ND2_ECO_1	1 x Csl	31	0.1	0.06	0.3552	
ND2_ECO_2	2 x Csl	31	0.18	0.12	0.6216	

ND2_MM_*

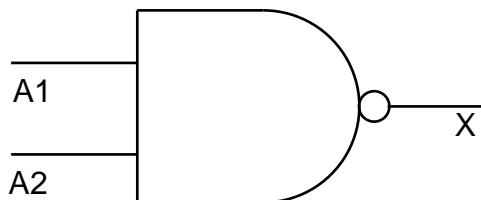


Figure 2.36. Logic Symbol of ND2_MM

Table 2.46. ND2_MM Truth Table

A1	A2	X
0	0	1
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
ND2_MM_0P5	0.5 x Csl	31	0.1	0.06	0.3108	
ND2_MM_1	1 x Csl	31	0.2	0.24	0.3108	
ND2_MM_2	2 x Csl	31	0.4	0.24	0.4884	
ND2_MM_3	3 x Csl	31	0.4	0.26	0.4884	
ND2_MM_4	4 x Csl	31	0.6	0.36	0.666	
ND2_MM_6	6 x Csl	32	0.8	0.55	0.8436	
ND2_MM_8	8 x Csl	33	1	0.74	1.0212	
ND2_MM_10	10 x Csl	33	1.2	0.92	1.1988	
ND2_MM_12	12 x Csl	32	1.41	1.11	1.4652	
ND2_MM_16	16 x Csl	33	1.91	1.49	1.8648	

ND3B_*

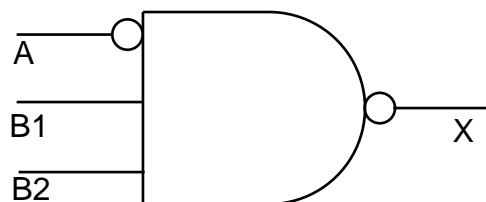


Figure 2.37. Logic Symbol of ND3B

Table 2.47. ND3B Truth Table

A	B1	B2	X
1	-	-	1
-	0	-	1
-	-	0	1
0	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
ND3B_0P5	0.5 x Csl	41	0.26	0.24	0.3108	
ND3B_0P75	0.75 x Csl	42	0.29	0.24	0.222	
ND3B_1	1 x Csl	42	0.29	0.24	0.222	
ND3B_2	2 x Csl	36	0.83	0.55	0.7992	
ND3B_4	4 x Csl	36	1.66	0.99	1.2876	

ND3_*

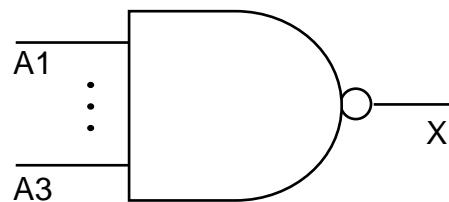


Figure 2.38. Logic Symbol of ND3

Table 2.48. ND3 Truth Table

A1	A2	A3	X
0	-	-	1
-	0	-	1
-	-	0	1
1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
ND3_0P5	0.5 x Csl	36	0.29	0.90	0.444	
ND3_0P75	0.75 x Csl	36	0.29	0.09	0.444	
ND3_1	1 x Csl	36	0.29	0.09	0.444	
ND3_2	2 x Csl	35	0.52	0.12	0.7104	

ND3_ECO_*

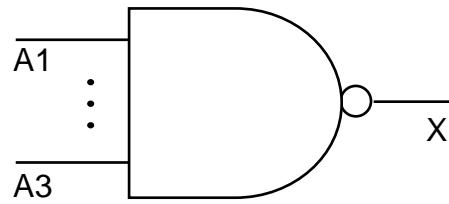


Figure 2.39. Logic Symbol of ND3_ECO

Table 2.49. ND3_ECO Truth Table

A1	A2	A3	X
0	-	-	1
-	0	-	1
-	-	0	1
1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ND3_ECO_1	1 x Csl	39	0.3	0.09	0.7548	

ND4_*

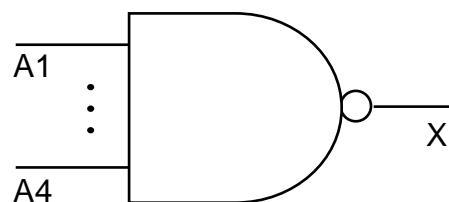


Figure 2.40. Logic Symbol of ND4

Table 2.50. ND4Truth Table

A1	A2	A3	A4	X
0	-	-	-	1
-	0	-	-	1
-	-	0	-	1
-	-	-	0	1
1	1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
ND4_0P5	0.5 x Csl	46	0.31	0.09	0.8436	
ND4_0P75	0.75 x Csl	46	0.31	0.09	0.8436	
ND4_1	1 x Csl	47	0.34	0.09	0.9324	
ND4_2	2 x Csl	47	0.59	0.13	1.4208	
ND4_3	3 x Csl	47	0.93	0.28	2.0868	
ND4_4	4 x Csl	47	1.24	0.37	2.3532	
ND4_8	8 x Csl	52	2.48	0.74	4.1292	

NR2B_*

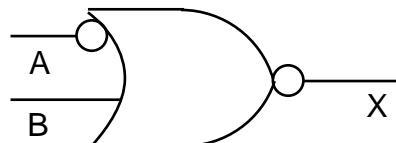


Figure 2.41. Logic Symbol of NR2B

Table 2.51. NR2B Truth Table

A	B	X
0	0	0
0	1	0
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
NR2B_0P75	0.75 x Csl	42	0.24	0.26	0.4884	
NR2B_1	1 x Csl	42	0.24	0.24	0.5772	
NR2B_1P5	1.5 x Csl	40	0.49	0.41	0.5772	
NR2B_2	2 x Csl	40	0.49	0.41	0.5772	
NR2B_4	4 x Csl	39	0.97	0.77	0.7104	

NR2B_U_*

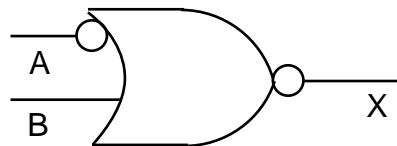


Figure 2.42. Logic Symbol of NR2B_U

Table 2.52. NR2B_U Truth Table

A	B	X
0	0	0
0	1	0
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
NR2B_U_0P5	0.5 x Csl	30	0.22	0.19	0.4884	

NR2_*

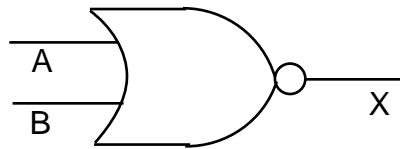


Figure 2.43. Logic Symbol of NR2

Table 2.53. NR2 Truth Table

A1	A2	X
0	0	1
0	1	0
1	0	0
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
NR2_0P5	0.5 x Csl	31	0.15	0.4	0.2664	
NR2_1	1 x Csl	31	1	0.05	0.222	
NR2_16	16 x Csl	1.35	1.64	0.35	1.554	
NR2_1P5	1.5 x Csl	40	0.2	0.26	0.3108	
NR2_2	2 x Csl	40	0.3	0.26	0.3108	
NR2_3	3 x Csl	32	0.66	0.36	0.6666	
NR2_4	4 x Csl	39	0.41	0.45	0.489	
NR2_5	5 x Csl	32	0.86	0.45	0.7548	
NR2_6	6 x Csl	32	0.61	0.51	0.7104	
NR2_8	8 x Csl	32	0.82	0.67	0.8436	

NR2_ECO_*

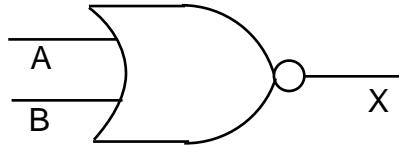


Figure 2.44. Logic Symbol of NR2_ECO

Table 2.54. NR2_ECO Truth Table

A1	A2	X
0	0	1
0	1	0
1	0	0
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
NR2_ECO_1	1 x Csl	35	0.24	0.06	0.6216	
NR2_ECO_2	2 x Csl	38	0.31	0.12	0.7548	

NR2_MM_*

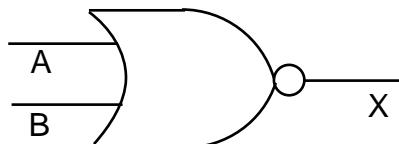


Figure 2.45. Logic Symbol of NR2_MM

Table 2.55. NR2_MM Truth Table

A1	A2	X
0	0	1
0	1	0
1	0	0
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
NR2_MM_0P5	0.5 x Csl	31	0.1	0.05	0.222	
NR2_MM_1	1 x Csl	30	0.15	0.07	0.222	
NR2_MM_10	10 x Csl	29	1.52	0.72	1.0212	
NR2_MM_12	12 x Csl	29	1.83	0.87	1.1988	
NR2_MM_16	16 x Csl	29	2.44	1.16	1.554	
NR2_2	2 x Csl	29	0.3	0.12	0.311318	
NR2_3	3 x Csl	37	0.31	0.19	0.3996	
NR2_4	4 x Csl	31	0.61	0.26	0.4884	
NR2_6	6 x Csl	31	0.91	0.31	0.666	
NR2_8	8 x Csl	31	1.22	0.52	0.8436	

NR3B_*

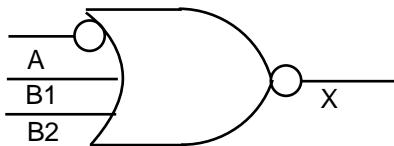


Figure 2.46. Logic Symbol of NR3B

Table 2.56. NR3B Truth Table

A	B1	B2	X
0	-	-	0
-	1	-	0
-	-	1	0
1	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
NR3B_0P75	0.75 x Csl	39	0.27	0.25	0.5772	
NR3B_1	1 x Csl	41	0.27	0.24	0.666	
NR3B_1P5	1.5 x Csl	37	0.45	0.29	0.7554	
NR3B_2	2 x Csl	37	0.45	0.29	0.7548	
NR3B_4	4 x Csl	38	0.84	0.41	1.0656	

NR3B_U_*

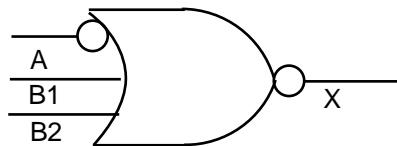


Figure 2.47. Logic Symbol of NR3B_U

Table 2.57. NR3B_U Truth Table

A	B1	B2	X
0	-	-	0
-	1	-	0
-	-	1	0
1	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
NR3B_U_0P5	0.5 x Csl	39	0.27	0.23	0.5328	

NR3_*

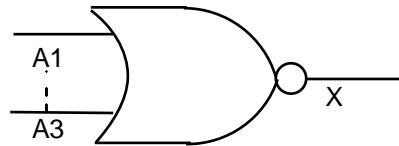


Figure 2.48. Logic Symbol of NR3

Table 2.58. NR3 Truth Table

A1	A2	A3	X
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
NR3_0P5	0.5 x Csl	37	0.29	0.09	0.444	
NR3_0P75	0.75 x Csl	36	0.4	0.12	0.444	
NR3_1	1. x Csl	36	0.4	0.12	0.444	
NR3_2	2 x Csl	38	0.52	0.12	0.4884	
NR3_3	3 x Csl	39	0.65	0.12	0.5328	
NR3_4	4 x Csl	41	0.77	0.12	0.666	
NR3_8	8 x Csl	48	1.41	0.12	1.0212	

NR3_ECO_*

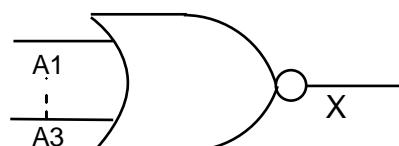


Figure 2.49. Logic Symbol of NR3_ECO

Table 2.59. NR3_ECO Truth Table

A1	A2	A3	X
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
NR3_ECO_1	1 x Csl	39	0.39	0.21	0.7548	

NR4_*

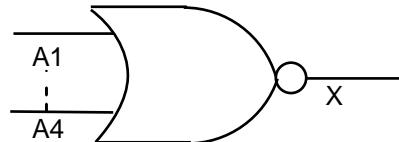


Figure 2.50. Logic Symbol of NR4

Table 2.60. NR4 Truth Table

A1	A2	A3	A4	X
0	0	0	0	1
1	-	-	-	0
-	1	-	-	0
-	-	1	-	0
-	-	-	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
NR4_0P75	1 x Csl	41	0.34	0.12	0.4884	
NR4_2	2 x Csl	38	0.75	0.38	0.7104	

OR2_*

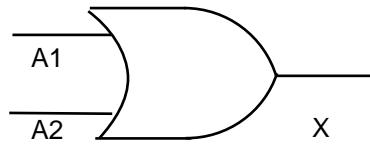


Figure 2.51. Logic Symbol of OR2

Table 2.61. OR2 Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OR2_0P5	0.5 x Csl	41	0.14	0.12	0.3108	
OR2_0P75	0.75 x Csl	38	0.18	0.38	0.3108	
OR2_1	1 x Csl	33	0.19	0.06	0.3108	
OR2_2	2 x Csl	35	0.31	0.07	0.3552	
OR2_4	4 x Csl	34	0.63	0.15	0.5328	

R2_ECO_*

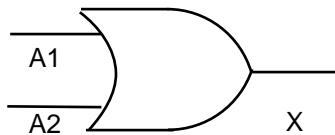


Figure 2.52. Logic Symbol of OR2_ECO

Table 2.62. OR2_ECO Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OR2_ECO_2	2 x Csl	37 ps	0.31 nW	0.12 pW/MHz	0.6216 μm^2	

OR2_MM_*

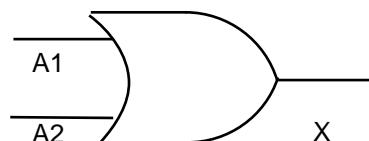


Figure 2.53. Logic Symbol of OR2_MM

Table 2.63. OR2_MM Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz		
OR2_MM_0P5	0.5 x Csl	33	0.14	0.06	0.222	
OR2_MM_0P75	0.75 x Csl	34	0.15	0.05	0.3108	
OR2_MM_1	1 x Csl	35	0.17	0.29	0.3108	
OR2_MM_12	12 x Csl	37	1.47	0.29	0.9768	
OR2_MM_16	16 x Csl	39	1.86	0.29	1.2432	
OR2_MM_1P5	1.5 x Csl	37	0.2	0.05	0.3552	
OR2_MM_2	2 x Csl	38	0.25	0.36	0.3552	
OR2_MM_20	20 x Csl	40	2.35	0.36	1.5096	
OR2_MM_3	3 x Csl	38	0.37	0.07	0.3996	
OR2_MM_4	4 x Csl	37	0.37	0.11	0.5328	
OR2_MM_6	6 x Csl	38	0.74	0.15	0.5328	
OR2_MM_8	8 x Csl	37	1	0.22	0.7992	

OR3_*

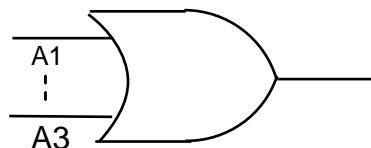


Figure 2.54. Logic Symbol of OR3

Table 2.64. OR3 Truth Table

A1	A2	A3	X
0	0	0	0
1	-	-	1
-	1	-	1
-	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
OR3_0P5	0.5 x Csl	37	0.19	0.1	0.3552	
OR3_0P75	0.75 x Csl	36	0.23	0.1	0.3552	
OR3_1	1 x Csl	37	0.22	0.09	0.3552	
OR3_2	2 x Csl	40	0.29	0.12	0.3996	
OR3_4	4 x Csl	39	0.63	0.3	0.6216	

OR4_*

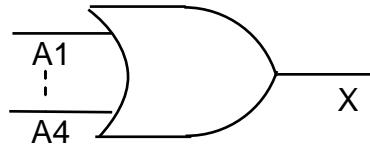


Figure 2.55. Logic Symbol of OR4

Table 2.65. OR4 Truth Table

A1	A2	A3	X
0	0	0	0
1	-	-	1
-	1	-	1
-	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
OR4_1	1 x Csl	40	0.27	0.15	0.3996	
OR4_2	2 x Csl	42	0.34	0.17	0.444	

EN2_*

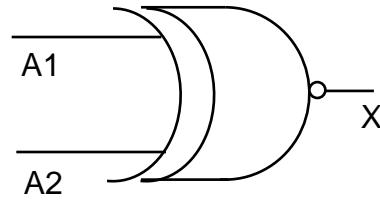


Figure 2.56. Logic Symbol of EN2

Table 2.66. EN2 Truth Table

A1	A2	X
0	0	1
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
EN2_0P5	0.5 x Csl	36	0.37	0.17	0.5772	
EN2_1	1 x Csl	36	042	0.23	0.5328	
EN2_1P5	1.5 x Csl	40	0.53	0.23	0.666	
EN2_2	2 x Csl	38	0.48	0.24	0.6216	
EN2_3	3 x Csl	43	0.69	0.26	0.7104	
EN2_4	4 x Csl	43	0.99	0.29	0.888	

EN2_ECO_*

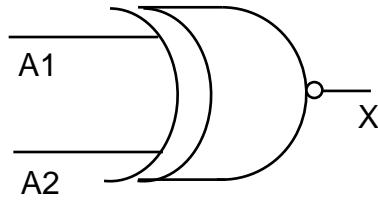


Figure 2.57. Logic Symbol of EN2_ECO

Table 2.67. EN2_ECO Truth Table

A1	A2	X
0	0	1
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EN2_ECO_1	1 x Csl	43	0.53	0.16	0.888	

EN2_V1_*

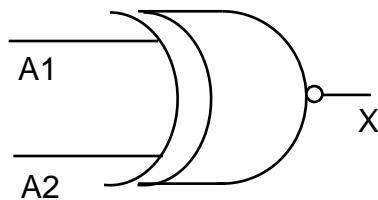


Figure 2.58. Logic Symbol of EN2_V1

Table 2.68. EN2_V1 Truth Table

A1	A2	X
0	0	1
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
EN2_V1_0P75	0.75 x Csl	39	0.3	0.11	0.666	
EN2_V1_1P5	1.5 x Csl	40	0.35	0.13	0.666	

EN3_*

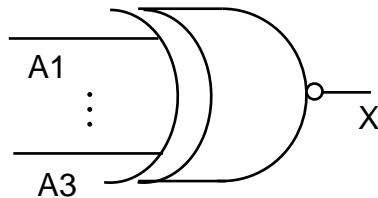


Figure 2.59. Logic Symbol of EN3

Table 2.69. EN3 Truth Table

A1	A2	A3	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
EN3_1	1 x Csl	45	0.68	0.3	0.8436	
EN3_2	2 x Csl	48	0.9	0.4	0.9768	
EN3_3	3 x Csl	51	1.38	0.72	1.2432	

EN3_U_*

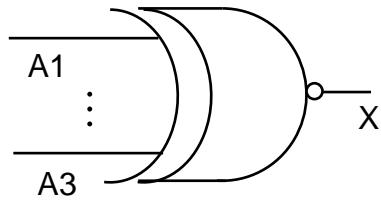


Figure 2.60. Logic Symbol of EN3_U

Table 2.70. EN3_UTruth Table

A1	A2	A3	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EN3_U_0P5	0.5 x Csl	44	0.63	0.3	0.8436	

EN4_M_*

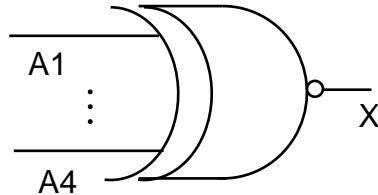


Figure 2.61. Logic Symbol of EN4_M

Table 2.71. EN4_M Truth Table

A1	A2	A3	A4	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EN4_M_1	1 x Csl	50 ps	0.79 nW	0.36 pW/MHz	1.2432	

EN4_*

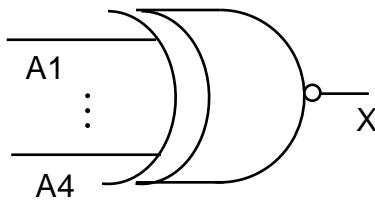


Figure 2.62. Logic Symbol of EN4

Table 2.72. EN4 Truth Table

A1	A2	A3	A4	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
EN4_2	2 x Csl	51	1.287	0.42	1.332	
EN4_4	4 x Csl	50	1.97	0.92	1.554	

EN4_U_*

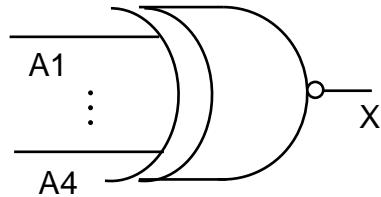


Figure 2.63. Logic Symbol of EN4_U

A1	A2	A3	A4	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Table 2.73. EN4_U Truth Table

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EN4_U_0P5	0.5 x Csl	48	0.77	0.32	1.2432	

EO2_*

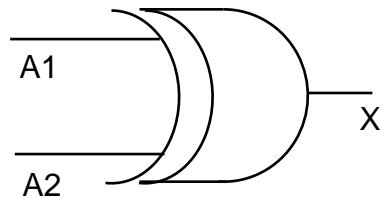


Figure 2.64. Logic Symbol of EO2

Table 2.74. EO2 Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EO2_0P5	0.5 x Csl	37	0.24	0.23	0.4884	
EO2_1	1 x Csl	38	0.29	0.25	0.4884	
EO2_1P5	1.5 x Csl	38	0.51	0.39	0.666	
EO2_2	2 x Csl	40	0.56	0.41	0.666	
EO2_3	3 x Csl	26	0.66	0.44	0.7104	
EO2_4	4 x Csl	46	0.76	0.64	0.8436	

EO2_ECO_*

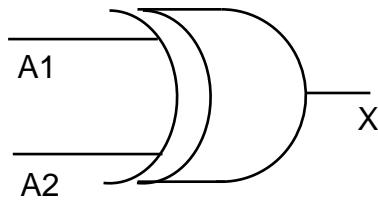


Figure 2.65. Logic Symbol of EO2_ECO

Table 2.75. EO2_ECO Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EO2_ECO_1	1 x Csl	49	0.44	0.71	1.2876	

EO2_MM_*

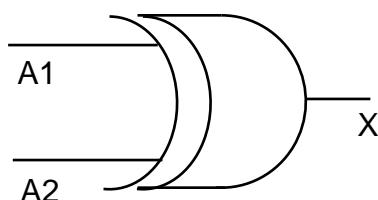


Figure 2.66. Logic Symbol of EO2_MM

Table 2.76. EO2_MM Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
EO2_MM_0P5	0.5 x Csl	48	0.45	0.70	0.888	
EO2_MM_1	1 x Csl	49	0.44	0.70	0.888	
EO2_MM_2	2 x Csl	46	0.88	1.28	1.2876	
EO2_MM_4	4 x Csl	46	1.77	2.44	2.0868	

EO2_V1_*

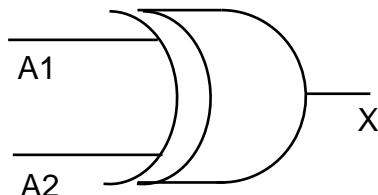


Figure 2.67. Logic Symbol of EO2_V1

Table 2.77. EO2_V1 Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
EO2_V1_0P75	0.75 x Csl	39	0.19	0.30	0.444	
EO2_V1_1P5	1.5 x Csl	39	0.29	0.57	0.5328	

EO3_*

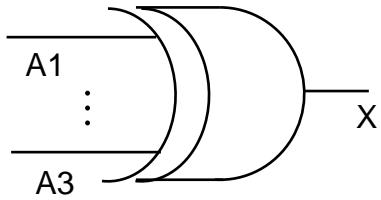


Figure 2.68. Logic Symbol of EO2_MM

Table 2.78. EO2_MM Truth Table

A1	A2	A3	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(μm^2)			
EO3_0P5	0.5 x Csl	51	0.6	0.64	1.0212	
EO3_1	1 x Csl	51	0.61	0.66	1.0212	
EO3_2	2 x Csl	52	0.66	0.68	1.0656	
EO3_4	4 x Csl	54	0.81	0.73	1.11	

EO4_*

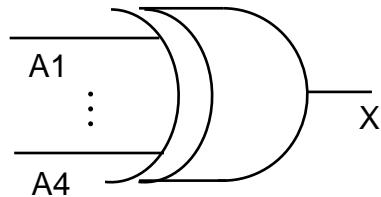


Figure 2.69. Logic Symbol of EO4

Table 2.79. EO4 Truth Table

A1	A2	A3	A4	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EO4_1	1 x Csl	48	0.82	0.81	1.2432	
EO4_2	2 x Csl	49	1.04	0.90	1.2876	
EO4_4	4 x Csl	54	1.29	1.06	1.3764	

EO4_U_*

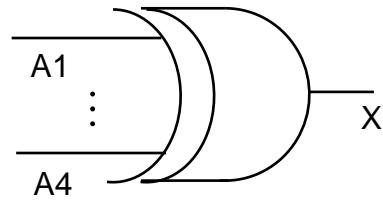


Figure 2.70. Logic Symbol of EO4_U

Table 2.80. EO4_U Truth Table

A1	A2	A3	A4	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
EO4_U_0P5	0.5 x Csl	58 ps	nW	pW/MHz	(um ²)	
			1.22	1.53	1.998	

AO21B_*

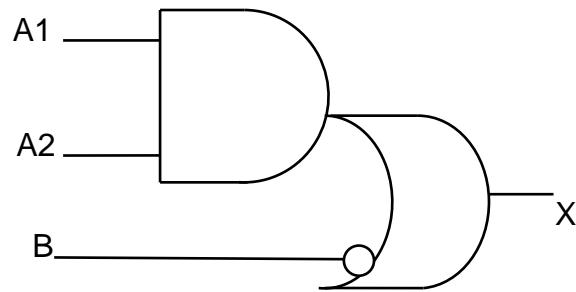


Figure 2.71. Logic Symbol of AO21B

Table 2.81. AO21B Truth Table

A1	A2	B	X
1	1	-	1
-	-	0	1
0	-	1	0
-	0	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO21B_0P5	0.5 x Csl	36	0.15	0.06	0.3552	
AO21B_1	1 x Csl	36	0.26	0.09	0.5328	
AO21B_2	2 x Csl	36	0.45	0.12	0.6216	
AO21B_4	4 x Csl	38	0.73	0.12	0.7992	

AO21_*

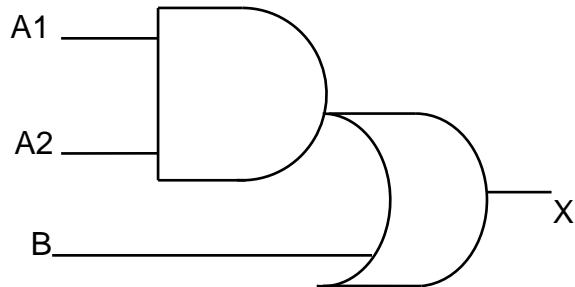


Figure 2.72. Logic Symbol of AO21

Table 2.82. AO21 Truth Table

A1	A2	B	X
1	1	-	1
-	-	0	1
0	-	1	0
-	0	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO21_1	1 x Csl	33	0.22	0.10	0.3552	
AO21_2	2 x Csl	36	0.29	0.09	0.3996	
AO21_4	4 x Csl	37	0.57	0.19	0.6216	

AO21_ECO_*

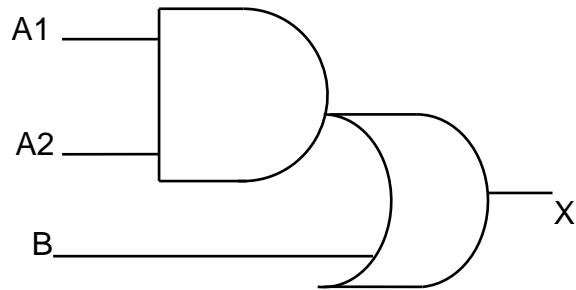


Figure 2.73. Logic Symbol of AO21_ECO

Table 2.83. AO21_ECO Truth Table

A1	A2	B	X
1	1	-	1
-	-	0	1
0	-	1	0
-	0	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO21_ECO_1	1 x Csl	39 ps	0.27 nW	0.11 pW/MHz	0.6216 μm^2	

AO21_U_*

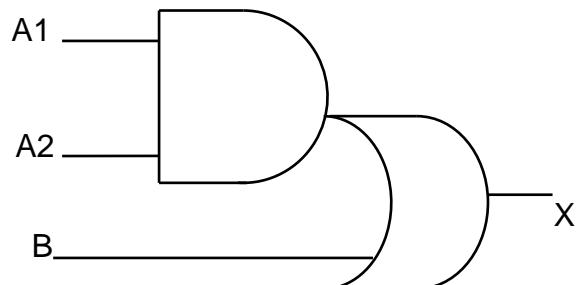


Figure 2.74. Logic Symbol of AO21_U

Table 2.84. AO21_U Truth Table

A1	A2	B	X
1	1	-	1
-	-	0	1
0	-	1	0
-	0	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO21_U_0P5	0.5 x Csl	34	0.13	0.07	0.3564	

AO221_*

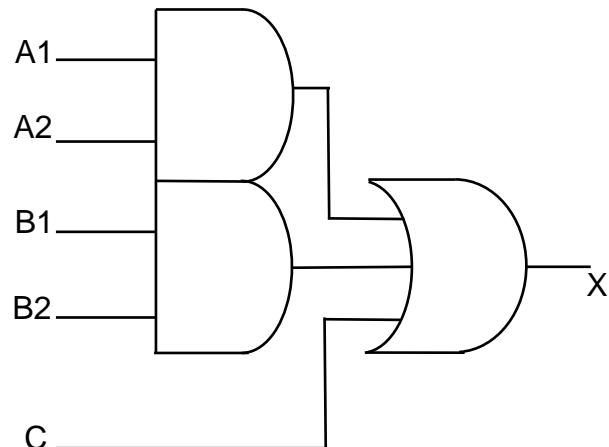


Figure 2.75. Logic Symbol of AO221

Table 2.85. AO221 Truth Table

A1	A2	B1	B2	C	X
1	1	-	-	-	1
-	-	1	1	-	1
-	-	-	-	1	1
0	-	0	-	0	0
-	0	0	-	0	0
0	-	-	0	0	0
-	0	-	0	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AO221_0P5	0.5 x Csl	40	0.19	0.09	0.4884	
AO221_1	1 x Csl	39	0.25	0.10	0.4884	
AO221_2	2 x Csl	40	0.28	0.09	0.5772	
AO221_4	4 x Csl	37	0.8	0.24	0.933	

AO222_*

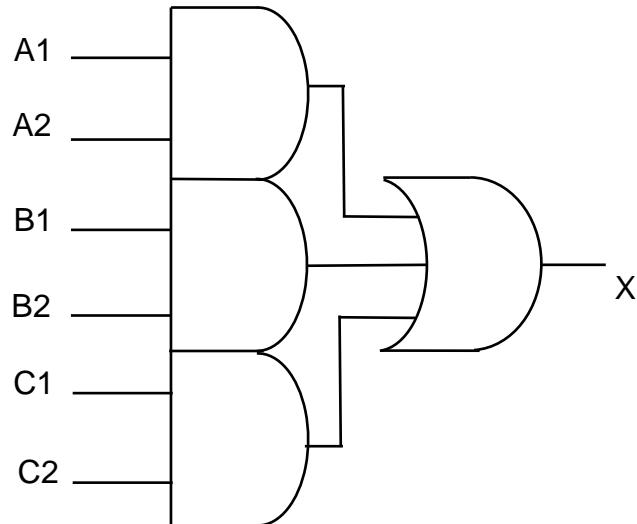


Figure 2.76. Logic Symbol of AO222

Table 2.86. AO222 Truth Table

A1	A2	B1	B2	C1	C2	X
1	1	-	-	-	-	1
-	-	1	1	-	-	1
-	-	-	-	1	1	1
0	-	0	-	0	-	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	0	-	-	0	0
-	0	-	0	0	-	0
-	0	-	0	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AO222_1	1 x Csl	46	0.32	0.08	0.7548	
AO222_2	2 x Csl	44	0.64	0.15	1.0212	
AO222_4	4 x Csl	45	1.4	0.32	1.6872	

AO222_U_*

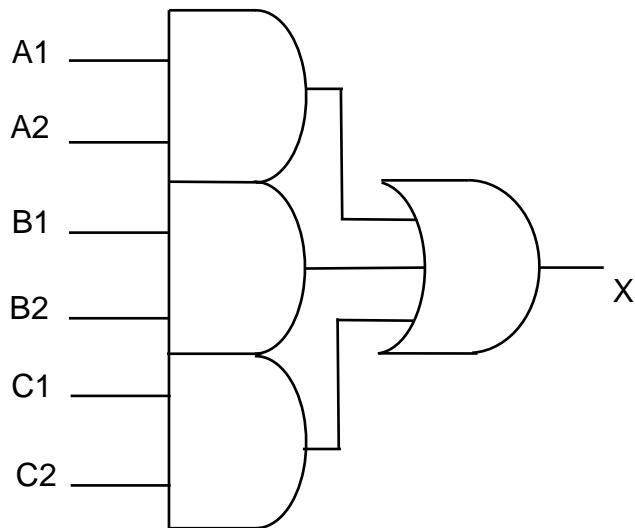


Figure 2.77. Logic Symbol of AO222_U

Table 2.87. AO222_U Truth Table

A1	A2	B1	B2	C1	C2	X
1	1	-	-	-	-	1
-	-	1	1	-	-	1
-	-	-	-	1	1	1
0	-	0	-	0	-	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	0	-	-	0	0
-	0	-	0	0	-	0
-	0	-	0	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO22_U_0P5	0.5 x Csl	45 ps	0.22 nW	0.08 pW/MHz	0.7992	

AO22_*

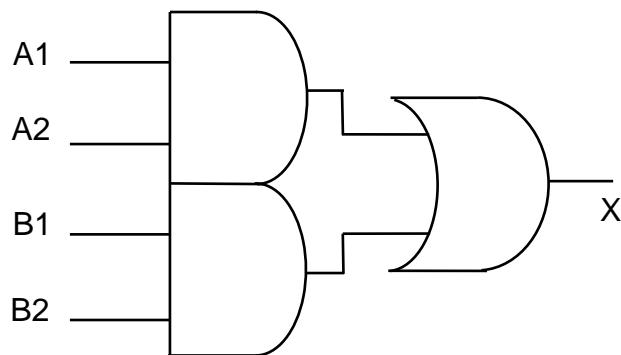


Figure 2.78. Logic Symbol of AO22

Table 2.88. AO22 Truth Table

A1	A2	B1	B2	X
-	-	1	1	1
1	1	-	-	1
0	-	0	-	0
-	0	0	-	0
0	-	-	0	0
-	0	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AO22_0P5	0.5 x Csl	38	0.18	0.06	0.5328	
AO22_0P75	0.75 x Csl	38	0.18	0.06	0.5328	
AO22_1	1 x Csl	38	0.21	0.06	0.444	

AO2BB2_*

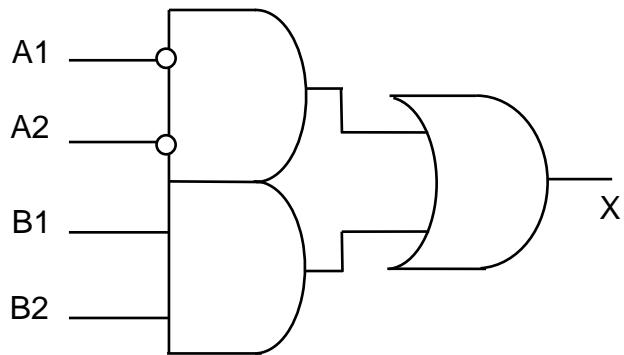


Figure 2.79. Logic Symbol of AO2BB2

Table 2.89. AO2BB2 Truth Table

A1	A2	B1	B2	X
-	-	1	1	1
0	0	-	-	1
1	-	0	-	0
-	1	0	-	0
1	-	-	0	0
-	1	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AO2BB2_0P5	0.5 x Csl	39	0.28	0.08	0.6216	
AO2BB2_1	1 x Csl	39	0.31	0.08	0.6216	
AO2BB2_2	2 x Csl	40	0.38	0.08	0.666	
AO2BB2_4	4 x Csl	42	0.53	0.08	0.7104	

AO2BB2_V1_*

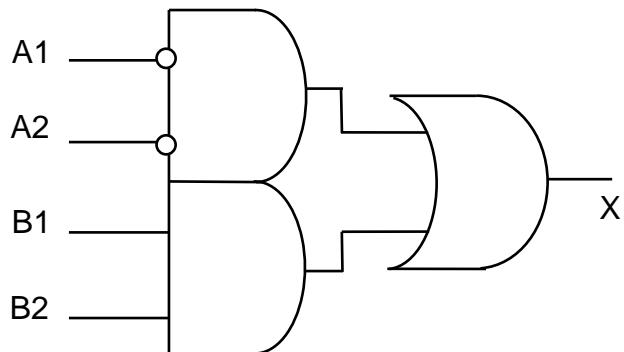


Figure 2.80. Logic Symbol of AO2BB2_V1

Table 2.90. AO2BB2_V1 Truth Table

A1	A2	B1	B2	X
-	-	1	1	1
0	0	-	-	1
1	-	0	-	0
-	1	0	-	0
1	-	-	0	0
-	1	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
AO2BB2_V1_0P5	0.5 x Csl	42	0.25	0.11	0.6216	
AO2BB2_V1_0P75	0.75 x Csl	42	0.25	0.11	0.6216	
AO2BB2_V1_1	1 x Csl	42	0.27	0.11	0.6216	
AO2BB2_V1_2	2 x Csl	44	0.35	0.11	0.666	
AO2BB2_V1_4	4 x Csl	48	0.5	0.11	0.7104	

AO31_*

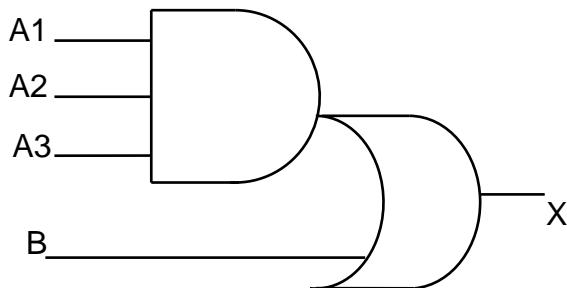


Figure 2.81. Logic Symbol of AO31

Table 2.91. AO31 Truth Table

A1	A2	A3	B	X
1	1	1	-	1
-	-	-	1	1
0	-	-	0	0
-	0	-	0	0
-	-	0	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
AO31_1	1 x Csl	36	0.25	0.09	0.6216	
AO31_2	2 x Csl	43	0.63	0.18	1.11	
AO31_4	4 x Csl	39	1.27	0.38	1.7316	

AO31_U_*

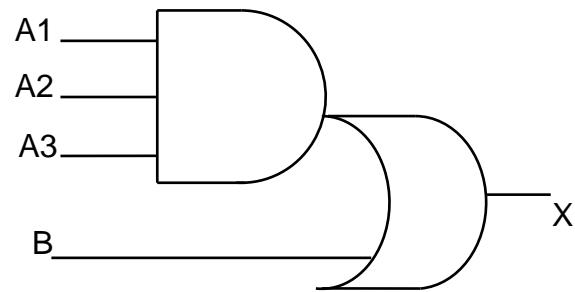


Figure 2.82. Logic Symbol of AO31_U

Table 2.92. AO31_U Truth Table

A1	A2	A3	B	X
1	1	1	-	1
-	-	-	1	1
0	-	-	0	0
-	0	-	0	0
-	-	0	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO31_U_0P5	0.5 x Csl	35	0.29	0.12	0.7104	

AO32_*

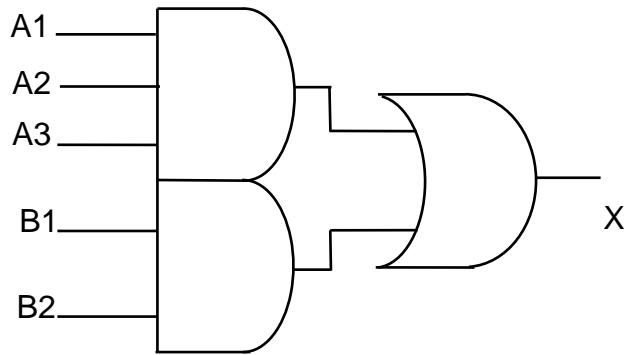


Figure 2.83. Logic Symbol of AO32

Table 2.93. AO32 Truth Table

A1	A2	A3	B1	B2	X
-	-	-	1	1	1
1	1	1	-	-	1
0	-	-	0	-	0
-	0	-	0	-	0
-	-	0	0	-	0
0	-	-	-	0	0
-	0	-	-	0	0
-	-	0	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
AO32_1	1 x Csl	39	0.23	0.06	0.444	
AO32_2	2 x Csl	42	0.3	0.06	0.4884	
AO32_4	4 x Csl	48	0.46	0.06	0.7104	

AO32_U_*

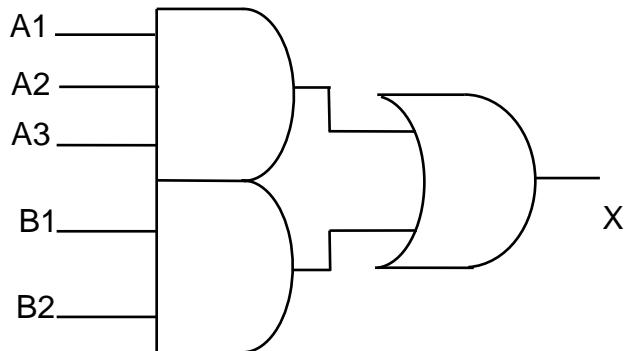


Figure 2.84. Logic Symbol of AO32_U

Table 2.94. AO32_U Truth Table

A1	A2	A3	B1	B2	X
-	-	-	1	1	1
1	1	1	-	-	1
0	-	-	0	-	0
-	0	-	0	-	0
-	-	0	0	-	0
0	-	-	-	0	0
-	0	-	-	0	0
-	-	0	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO32_U_0P5	0.5 x Csl	38 ps	0.21 nW	0.06 pW/MHz	0.444 μm^2	

AO33_*

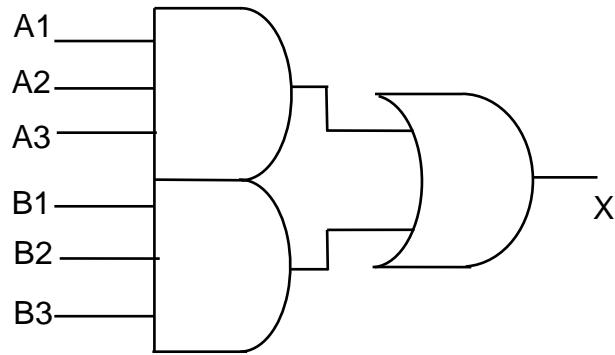


Figure 2.85. Logic Symbol of AO33

Table 2.95. AO33 Truth Table

A1	A2	A3	B1	B2	B3	X
-	-	-	1	1	1	1
1	1	1	-	-	-	1
0	-	-	0	-	-	0
-	0	-	0	-	-	0
-	-	0	0	-	-	0
0	-	-	-	0	-	0
-	0	-	-	0	-	0
-	-	0	-	0	-	0
0	-	-	-	-	0	0
-	0	-	-	-	0	0
-	-	0	-	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(um ²)			
AO33_1	1 x Csl	44	0.2	0.08	0.5328	
AO33_2	2 x Csl	47	0.3	0.08	0.5772	
AO33_4	4 x Csl	49	0.5	0.08	0.666	

AO33_U_*

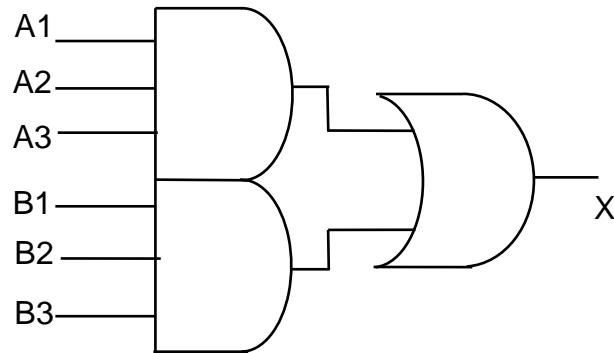


Figure 2.86. Logic Symbol of AO33_U

Table 2.96. AO33_U Truth Table

A1	A2	A3	B1	B2	B3	X
-	-	-	1	1	1	1
1	1	1	-	-	-	1
0	-	-	0	-	-	0
-	0	-	0	-	-	0
-	-	0	0	-	-	0
0	-	-	-	0	-	0
-	0	-	-	0	-	0
-	-	0	-	0	-	0
0	-	-	-	-	0	0
-	0	-	-	-	0	0
-	-	0	-	-	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AO33_U_0P5	0.5 x Csl	43 ps	0.16 nW	0.08 pW/MHz	0.5328 μm^2	

AOI211_*

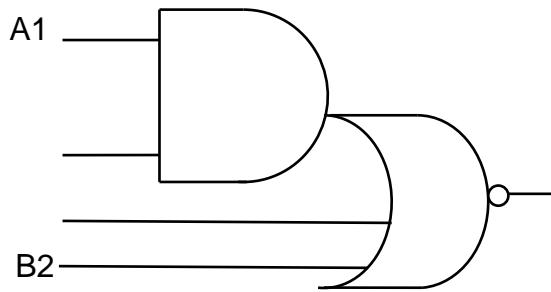


Figure 2.87. Logic Symbol of AOI211

Table 2.97. AOI211 Truth Table

A1	A2	B1	B2	X
-	-	-	1	0
-	-	1	-	0
1	1	-	-	0
0	-	0	0	1
-	0	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
AOI211_0P5	0.5 x Csl	44	0.44	0.09	0.9324	
AOI211_1	1 x Csl	44	0.69	0.15	0.9324	
AOI211_2	2 x Csl	46	0.8	0.15	1.0656	
AOI211_4	4 x Csl	42	1.8	0.56	1.9536	

AOI21_*

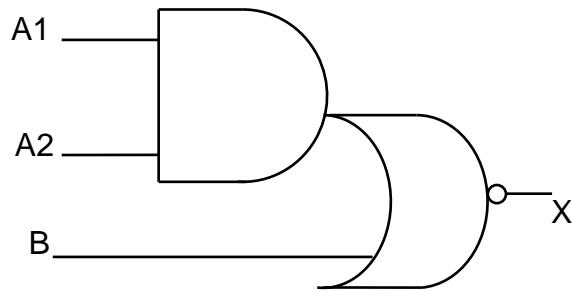


Figure 2.88. Logic Symbol of AOI21

Table 2.98. AOI21 Truth Table

A1	A2	B	X
1	1	-	0
-	-	1	0
0	-	0	1
-	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
AOI21_0P5	0.5 x Csl	32	0.15	0.08	0.2664	
AOI21_0P75	0.75 x Csl	32	0.15	0.08	0.2664	
AOI21_1	1 x Csl	32	0.15	0.11	0.3108	
AOI21_1P5	1.5 x Csl	32	0.3	0.23	0.444	
AOI21_2	2 x Csl	32	0.3	0.23	0.444	
AOI21_3	3 x Csl	30	0.46	0.35	0.6216	
AOI211_4	4 x Csl	30	0.61	0.48	0.7548	
AOI211_6	6 x Csl	30	0.91	0.70	1.0212	
AOI211_8	8 x Csl	30	1.22	0.94	1.2876	

AOI21_ECO_*

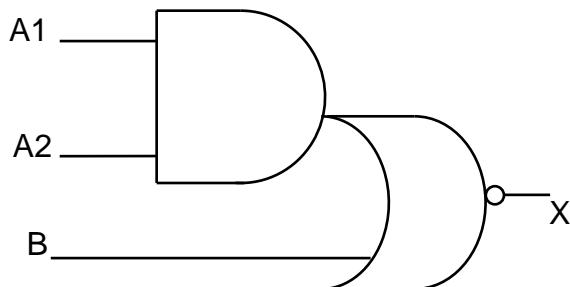


Figure 2.89. Logic Symbol of AOI21_ECO

Table 2.99. AOI21_ECO Truth Table

A1	A2	B	X
1	1	-	0
-	-	1	0
0	-	0	1
-	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
AOI21_ECO_1	1 x Csl	32	0.15	0.12	0.4884	

AOI21_V1_*

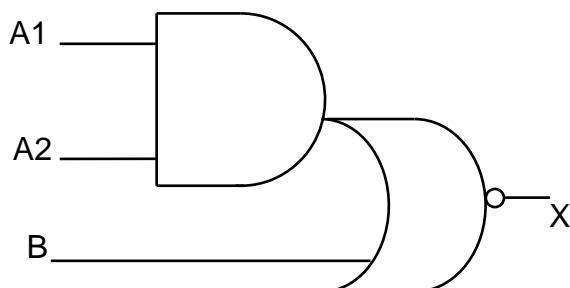


Figure 2.90. Logic Symbol of AOI21_V1

Table 2.100. AOI21_V1 Truth Table

A1	A2	B	X
1	1	-	0
-	-	1	0
0	-	0	1
-	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AOI21_V1_4	4 x Csl	30	0.51	0.43	0.7104	
AOI21_V1_6	6 x Csl	30	0.77	0.71	0.9768	
AOI21_V1_8	8 x Csl	30	1.03	0.97	1.2432	

AOI221_*

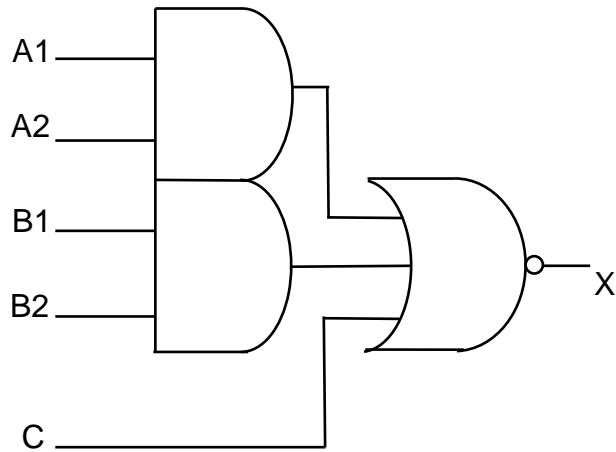


Figure 2.91. Logic Symbol of AOI221

Table 2.101. AOI221 Truth Table

A1	A2	B1	B2	C	X
1	1	-	-	-	0
-	-	1	1	-	0
-	-	-	-	1	0
0	-	0	-	0	1
-	0	0	-	0	1
0	-	-	0	0	1
-	0	-	0	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AOI221_0P5	0.5 x Csl	49	0.39	0.08	0.9768	
AOI221_1	1 x Csl	45	0.5	0.24	1.0212	
AOI221_2	2 x Csl	42	0.7	0.26	1.2876	
AOI221_4	4 x Csl	44	1.2	0.48	1.6428	

AOI222_*

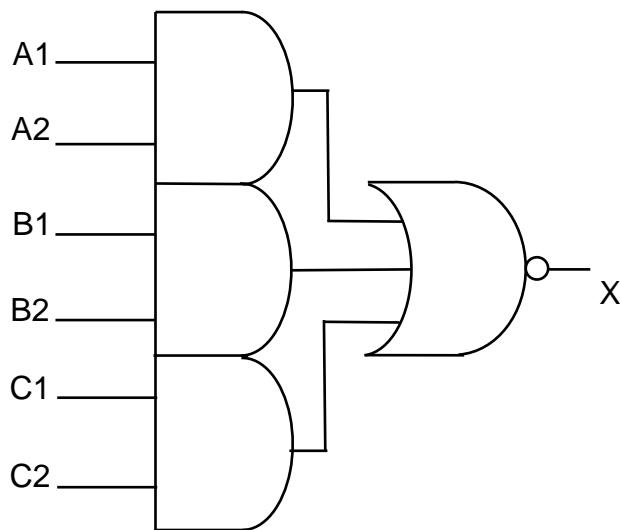


Figure 2.92. Logic Symbol of AOI222

Table 2.102. AOI222 Truth Table

A1	A2	B1	B2	C1	C2	X
1	1	-	-	-	-	0
-	-	1	1	-	-	0
-	-	-	-	1	1	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	0	-	-	0	1
-	0	-	0	0	-	1
-	0	-	0	-	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AOI22_0P5	0.5 x Csl	47	0.26	0.1	0.7104	
AOI22_1	1 x Csl	48	0.39	0.12	0.7104	
AOI22_2	2 x Csl	48	0.48	0.12	0.8436	
AOI22_4	4 x Csl	52	0.63	0.12	0.888	

AOI22_*

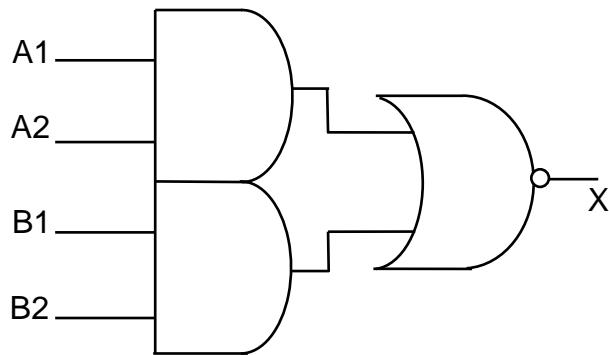


Figure 2.93. Logic Symbol of AOI22

Table 2.103. AOI22 Truth Table

A1	A2	B1	B2	X
-	-	1	1	0
1	1	-	-	0
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1
-	0	-	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(μm^2)	
AOI22_0P5	0.5 x Csl	42	0.21	0.06	0.4884	
AOI22_0P75	0.75 x Csl	41	0.26	0.09	0.4884	
AOI22_1	1 x Csl	40	0.31	0.11	0.444	
AOI22_1P5	1.5 x Csl	41	0.34	0.12	0.444	
AOI22_2	2 x Csl	41	0.39	0.12	0.5772	
AOI22_3	3 x Csl	43	0.46	0.12	0.6216	
AOI22_4	4 x Csl	45	0.54	0.12	0.6216	
AOI22_6	6 x Csl	49	0.74	0.12	0.7104	

AOI22_ECO_*

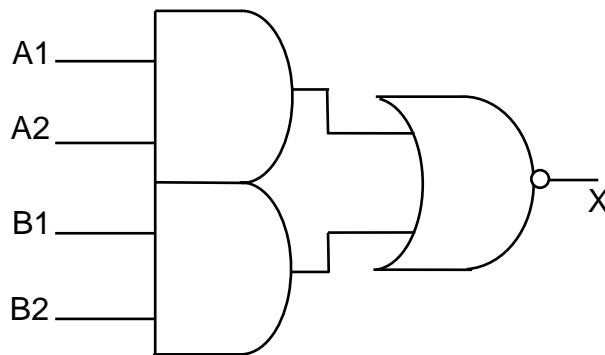


Figure 2.94. Logic Symbol of AOI22_ECO

Table 2.104. AOI22_ECO Truth Table

A1	A2	B1	B2	X
-	-	1	1	0
1	1	-	-	0
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1
-	0	-	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AOI22_ECO_1	1 x Csl	42	0.32	0.12	0.888	

AOI31_*

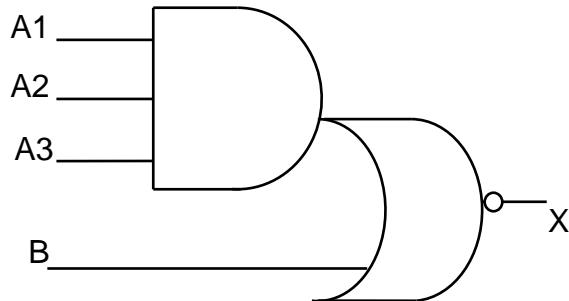


Figure 2.95. Logic Symbol of AOI31

Table 2.105. AOI31 Truth Table

A1	A2	A3	B	X
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AOI31_0P5	0.5 x Csl	41	0.24	0.07	0.4884	
AOI31_0P75	0.75 x Csl	40	0.24	0.06	0.4884	
AOI31_1	1 x Csl	40	0.24	0.06	0.4884	
AOI31_2	2 x Csl	41	0.31	0.06	0.5328	
AOI31_4	4 x Csl	45	0.46	0.06	0.5772	

AOI31_ECO_*

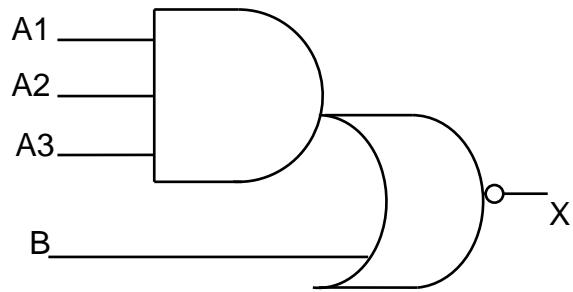


Figure 2.96. Logic Symbol of AOI31_ECO

Table 2.106. AOI31_ECO Truth Table

A1	A2	A3	B	X
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
AOI31_ECO_1	1 x Csl	40	0.26	0.11	0.9324	

AOI32_*

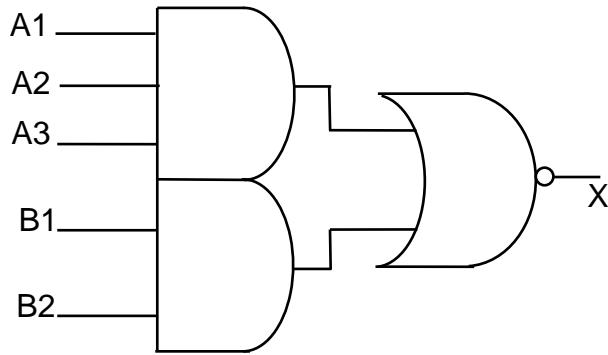


Figure 2.97. Logic Symbol of AOI32

Table 2.107. AOI32 Truth Table

A1	A2	A3	B1	B2	X
-	-	-	1	1	0
1	1	1	-	-	0
0	-	-	0	-	1
-	0	-	0	-	1
-	-	0	0	-	1
0	-	-	-	0	1
-	0	-	-	0	1
-	-	0	-	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz				
AOI32_0P5	0.5 x Csl	39	0.6	0.12	1.0656	
AOI32_0P75	0.75 x Csl	42	0.75	0.16	1.2876	
AOI32_1	1 x Csl	41	0.99	0.19	1.2876	
AOI32_2	2 x Csl	40	0.86	0.17	1.3764	
AOI32_4	4 x Csl	39	1.15	0.24	1.554	

AOI33_*

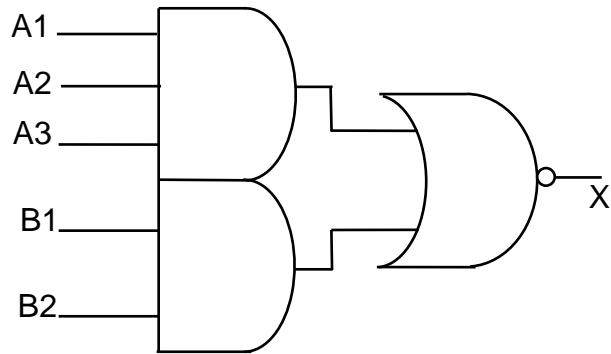


Figure 2.98. Logic Symbol of AOI33

Table 2.108. AOI33 Truth Table

A1	A2	A3	B1	B2	B3	X
-	-	-	1	1	1	0
1	1	1	-	-	-	0
0	-	-	0	-	-	1
-	0	-	0	-	-	1
-	-	0	0	-	-	1
0	-	-	-	0	-	1
-	0	-	-	0	-	1
-	-	0	-	0	-	1
0	-	-	-	-	0	1
-	0	-	-	-	0	1
-	-	0	-	-	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(um ²)			
AOI33_0P5	0.5 x Csl	48	0.84	0.1	1.776	
AOI33_0P75	0.75 x Csl	46	0.9	0.12	1.9092	
AOI33_1	1 x Csl	45	1.2	0.15	1.9092	
AOI33_2	2 x Csl	45	1.2	0.16	1.776	
AOI33_4	4 x Csl	46	1.7	0.17	2.5764	

AOI311_*

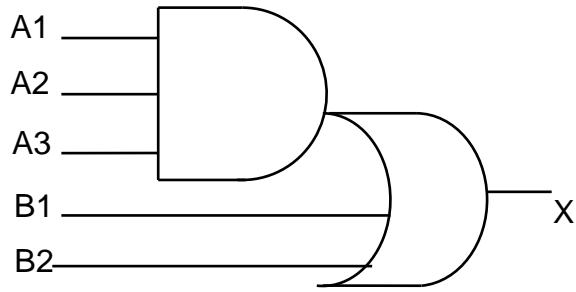


Figure 2.99. Logic Symbol of AOI311

Table 2.109. AOI311 Truth Table

A1	A2	A3	B1	B2	X
1	1	1	-	-	1
-	-	-	1	-	1
-	-	-	-	1	1
0	-	-	0	0	0
-	0	-	0	0	0
-	-	0	0	0	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(um ²)			
AOI311_0P5	0.5 x Csl	41	0.28	0.07	0.5772	
AOI311_0P75	0.75 x Csl	41	0.28	0.07	0.5772	
AOI311_1	1 x Csl	42	0.3	0.07	0.5772	
AOI311_2	2 x Csl	43	0.38	0.07	0.6216	
AOI311_4	4 x Csl	46	0.53	0.07	0.7104	

OA21B_*

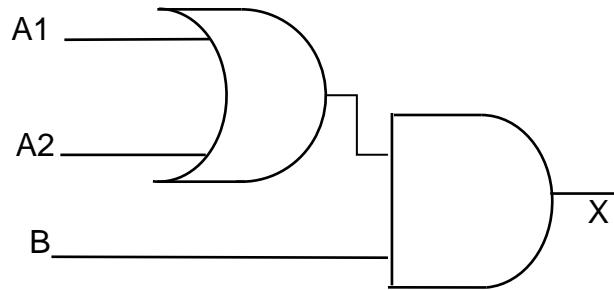


Figure 2.100. Logic Symbol of OA21B

Table 2.110. OA21B Truth Table

A1	A2	B	X
0	0	-	0
-	-	1	0
1	-	0	1
-	1	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(μm^2)			
OA21B_1	1 x Csl	37	0.17	0.25	0.3552	
OA21B_2	2 x Csl	36	0.62	0.51	0.6216	
OA21B_4	4 x Csl	39	1.13	0.78	0.8436	

OA21_MM_*

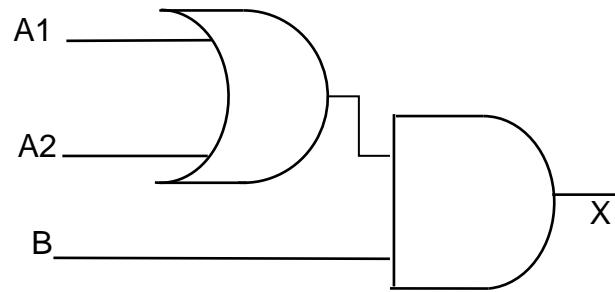


Figure 2.101. Logic Symbol of OA21_MM

Table 2.111. OA21_MM Truth Table

A1	A2	B	X
0	0	-	0
-	-	1	0
1	-	0	1
-	1	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA21_MM_1	1 x Csl	37	0.24	0.09	0.3996	
OA21_MM_2	2 x Csl	39	0.31	0.09	0.444	
OA21_MM_6	6 x Csl	37	1.01	0.36	0.9312	

OA21_U_*

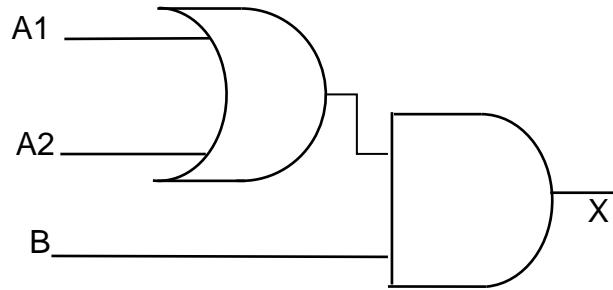


Figure 2.102. Logic Symbol of OA21_U

Table 2.112. OA21_U Truth Table

A1	A2	B	X
0	0	-	0
-	-	1	0
1	-	0	1
-	1	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA21_U_0P5	0.5 x Csl	36	0.26	0.14	0.5328	

OA211_*

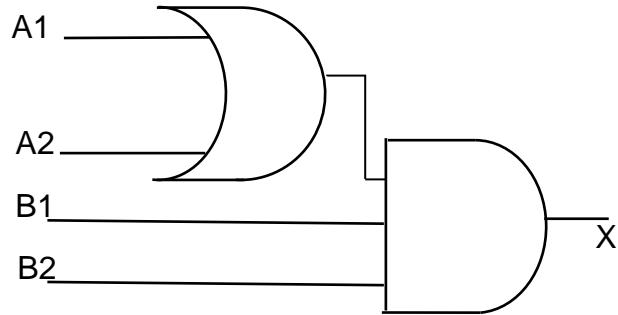


Figure 2.103. Logic Symbol of OA211

Table 2.113. OA211 Truth Table

A1	A2	B1	B2	X
0	0	-	-	0
-	-	0	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(um ²)			
OA211_1	1 x Csl	38	0.47	0.11	0.666	
OA211_2	2 x Csl	37	0.67	0.11	0.9324	
OA211_4	4 x Csl	38	1.24	0.14	1.3764	

OA211_U_*

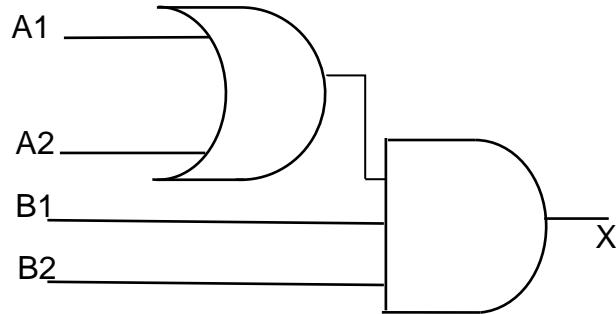


Figure 2.104. Logic Symbol of OA211_U

Table 2.114. OA211_U Truth Table

A1	A2	B1	B2	X
0	0	-	-	0
-	-	0	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA211_U_0P5	0.5 x Csl	38	0.39	0.10	0.7548	

OA22_*

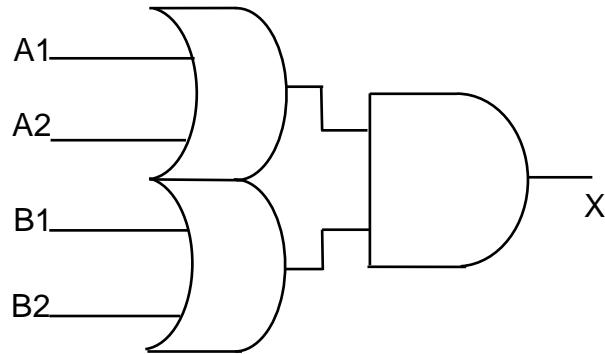


Figure 2.105. Logic Symbol of OA22

Table 2.115. OA22 Truth Table

A1	A2	B1	B2	X
0	0	-	-	0
-	-	0	0	0
1	-	1	-	1
-	1	1	-	1
1	-	-	1	1
-	1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
OA22_0P75	0.75 x Csl	36	0.2	0.07	0.3996	
OA22_1	1 x Csl	36	0.2	0.07	0.3996	
OA22_2	2 x Csl	39	0.25	0.07	0.444	
OA22_4	4 x Csl	45	0.4	0.07	0.5328	

OA22_U_*

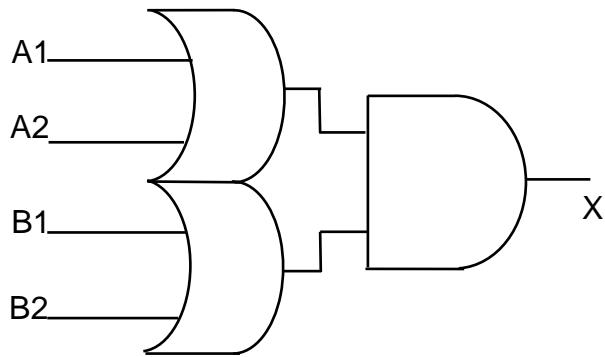


Figure 2.106. Logic Symbol of OA22_U

Table 2.116. OA22_U Truth Table

A1	A2	B1	B2	X
0	0	-	-	0
-	-	0	0	0
1	-	1	-	1
-	1	1	-	1
1	-	-	1	1
-	1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA22_U_0P5	0.5 x Csl	37	0.14	0.07	0.3996	

OA2BB2_*

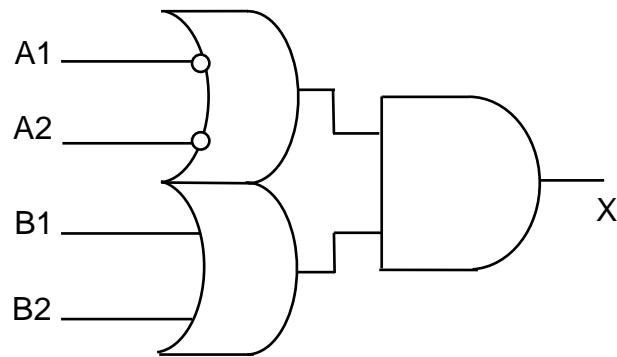


Figure 2.107. Logic Symbol of OA2BB2

Table 2.117. OA2BB2 Truth Table

A1	A2	B1	B2	X
1	1	-	-	0
-	-	0	0	0
0	-	1	-	1
-	0	1	-	1
0	-	-	1	1
-	0	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA2BB2_0P5	0.5 x Csl	39	0.36	0.08	0.8436	
OA2BB2_1	1 x Csl	39	0.31	0.08	0.7992	
OA2BB2_2	2 x Csl	40	0.62	0.08	1.1544	
OA2BB2_4	4 x Csl	43	1.24	0.08	1.8648	

OA2BB2_V1_*

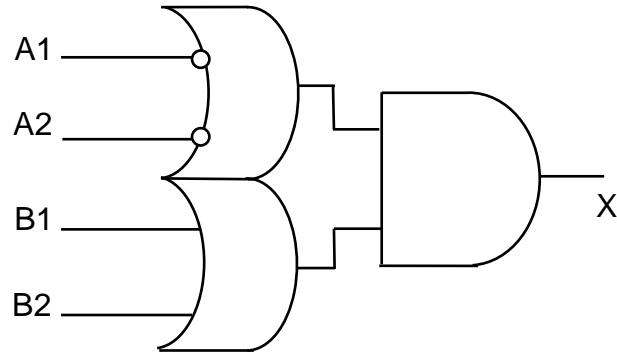


Figure 2.108. Logic Symbol of OA2BB2_V1

Table 2.118. OA2BB2_V1 Truth Table

A1	A2	B1	B2	X
1	1	-	-	0
-	-	0	0	0
0	-	1	-	1
-	0	1	-	1
0	-	-	1	1
-	0	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA2BB2_V1_0P5	0.5 x Csl	42	0.14	0.11	0.489	
OA2BB2_V1_0P75	0.75 x Csl	42	0.36	0.11	0.5772	
OA2BB2_V1_1	1 x Csl	42	0.23	0.11	0.444	
OA2BB2_V1_2	2 x Csl	44	0.7	0.11	0.9768	
OA2BB2_V1_4	4 x Csl	48	0.95	0.11	1.1988	

OA221_*

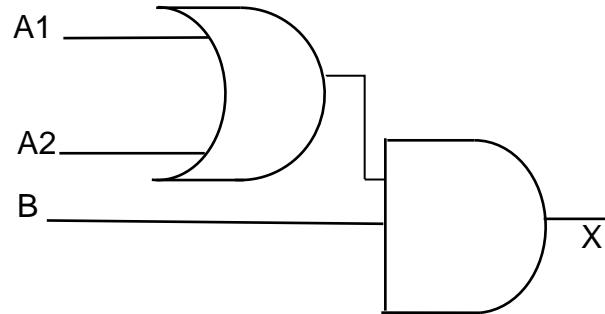


Figure 2.109. Logic Symbol of OA222

Table 2.119. OA222 Truth Table

A1	A2	B1	X
0	0	-	0
-	-	0	0
-	-	-	0
1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	pW/MHz	
OA221_1	1 x Csl	39	0.3	0.10	0.7104	
OA221_2	2 x Csl	40	0.4	0.09	0.8436	
OA221_4	4 x Csl	37	0.86	0.24	1.0656	

OA221_U_*

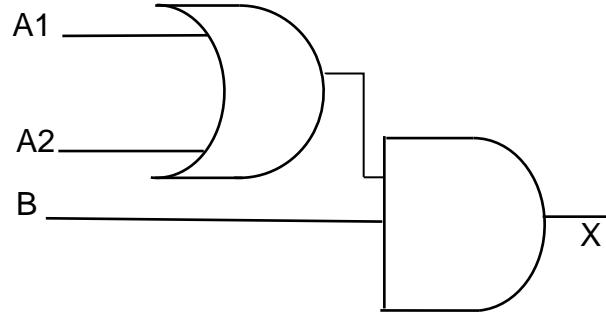


Figure 2.110. Logic Symbol of OA222

Table 2.120. OA222 Truth Table

A1	A2	B1	X
0	0	-	0
-	-	0	0
-	-	-	0
1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA221_U_OP5	0.5 x Csl	39	0.16	0.06	0.4884	

OA222_*

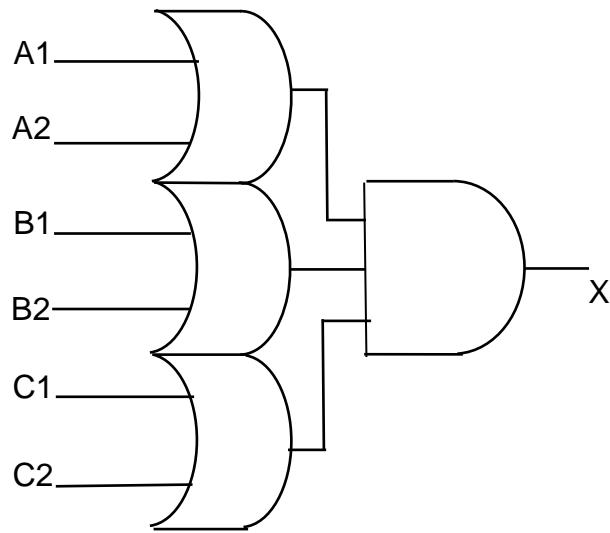


Figure 2.111. Logic Symbol of OA222

Table 2.121. OA222 Truth Table

A1	A2	B1	B2	C1	C2	X
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	1	-	1	-	1
1	-	1	-	-	1	1
1	-	-	1	1	-	1
1	-	-	1	-	1	1
-	1	1	-	1	-	1
-	1	1	-	-	1	1
-	1	-	1	1	-	1
-	1	-	1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA222_1	1 x Csl	46	0.33	0.08	0.7992	
OA222_2	2 x Csl	44	0.57	0.15	1.2432	
OA222_4	4 x Csl	45	1.27	0.32	1.9092	

OA222_U_*

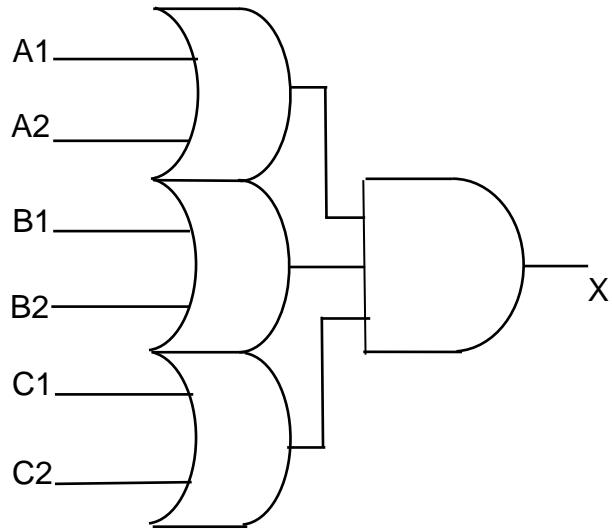


Figure 2.112. Logic Symbol of OA222_U

Table 2.122. OA222_U Truth Table

A1	A2	B1	B2	C1	C2	X
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	1	-	1	-	1
1	-	1	-	-	1	1
1	-	-	1	1	-	1
1	-	-	1	-	1	1
-	1	1	-	1	-	1
-	1	1	-	-	1	1
-	1	-	1	1	-	1
-	1	-	1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA222_U_0P5	0.5 x Csl	45 ps	0.33 nW	0.08 pW/MHz	0.7992	

OA31_*

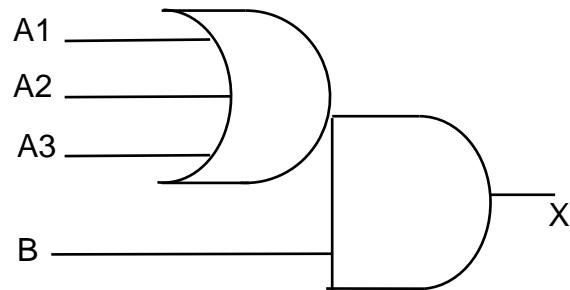


Figure 2.113. Logic Symbol of OA31

Table 2.123. OA31 Truth Table

A1	A2	A3	B	X
0	0	0	-	0
-	-	-	0	0
1	-	-	1	1
-	1	-	1	1
-	-	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz				
OA31_1	1 x Csl	36	0.26	0.09	0.3996	
OA31_1P5	1.5 x Csl	36	0.29	0.09	0.444	
OA31_2	2 x Csl	38	0.33	0.18	0.444	
OA31_4	4 x Csl	39	0.59	0.38	0.7548	

OA31_U_*

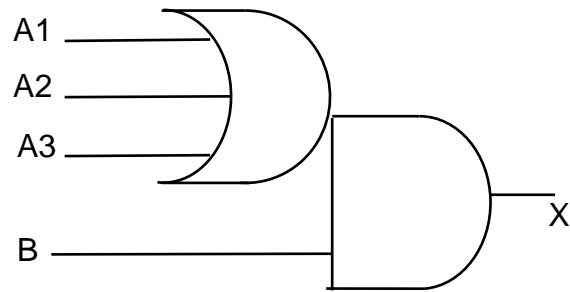


Figure 2.114. Logic Symbol of OA31_U

Table 2.124. OA31_U Truth Table

A1	A2	A3	B	X
0	0	0	-	0
-	-	-	0	0
1	-	-	1	1
-	1	-	1	1
-	-	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA31_U_0P5	0.5 x Csl	35	0.25	0.12	0.6216	

OA32_*

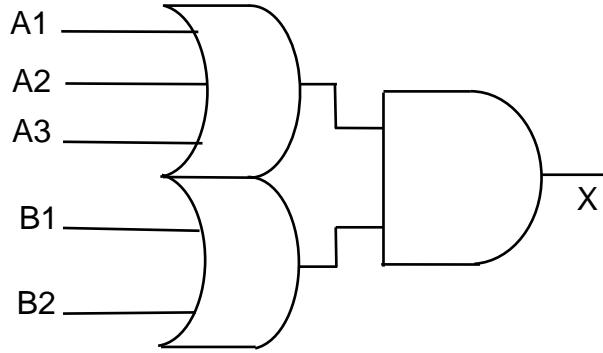


Figure 2.115. Logic Symbol of OA32

Table 2.125. OA32 Truth Table

A1	A2	A3	B1	B2	X
-	-	-	0	0	0
0	0	0	-	-	0
1	-	-	1	-	1
-	1	-	1	-	1
-	-	1	1	-	1
1	-	-	-	1	1
-	1	-	-	1	1
-	-	1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA32_1	1 x Csl	38	0.2	0.06	0.6216	
OA32_2	2 x Csl	42	0.45	0.06	0.888	
OA32_4	4 x Csl	47	0.9	0.06	1.4652	

OA32_U_*

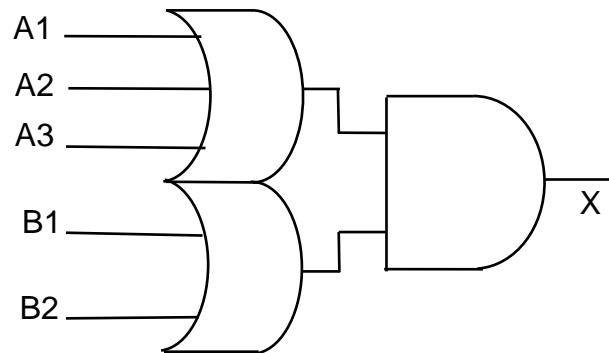


Figure 2.116. Logic Symbol of OA32_U

Table 2.126. OA32_U Truth Table

A1	A2	A3	B1	B2	X
-	-	-	0	0	0
0	0	0	-	-	0
1	-	-	1	-	1
-	1	-	1	-	1
-	-	1	1	-	1
1	-	-	-	1	1
-	1	-	-	1	1
-	-	1	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA32_U_0P5	0.5 x Csl	38	0.16	0.07	0.5328	

OA33_*

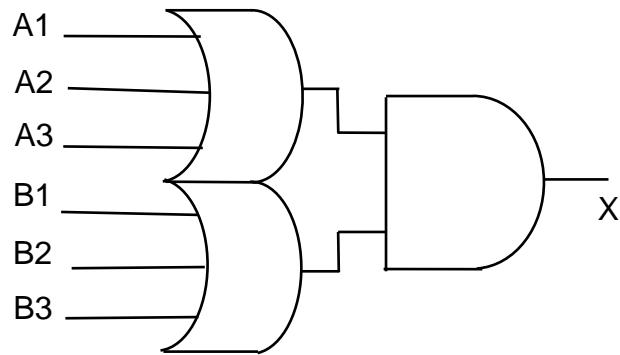


Figure 2.117. Logic Symbol of OA33

Table 2.127. OA33 Truth Table

A1	A2	A3	B1	B2	B3	X
-	-	-	0	0	0	0
0	0	0	-	-	-	0
1	-	-	1	-	-	1
-	1	-	1	-	-	1
-	-	1	1	-	-	1
1	-	-	-	1	-	1
-	1	-	-	1	-	1
-	-	1	-	1	-	1
1	-	-	1	-	-	1
-	1	-	-	1	-	1
-	-	1	-	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA33_1	1 x Csl	45	0.26	0.12	0.5328	
OA33_2	2 x Csl	49	0.31	0.13	0.5772	
OA33_4	4 x Csl	58	0.52	0.13	0.7548	

OA33_U_*

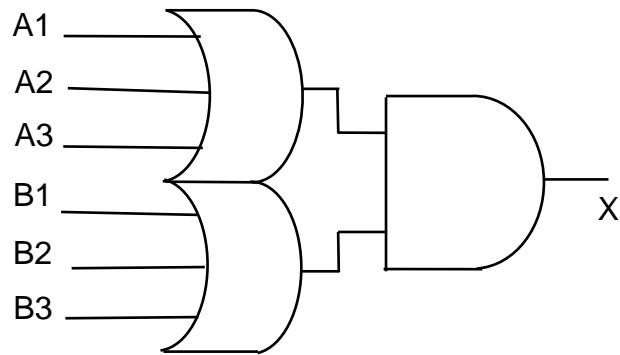


Figure 2.118. Logic Symbol of OA33_U

Table 2.128. OA33_U Truth Table

A1	A2	A3	B1	B2	B3	X
-	-	-	0	0	0	0
0	0	0	-	-	-	0
1	-	-	1	-	-	1
-	1	-	1	-	-	1
-	-	1	1	-	-	1
1	-	-	-	1	-	1
-	1	-	-	1	-	1
-	-	1	-	1	-	1
1	-	-	1	-	-	1
-	1	-	-	1	-	1
-	-	1	-	-	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	pW/MHz	
OA33_U_0P5	0.5 x Csl	43	0.21	0.1	0.5352	

OAI211_*

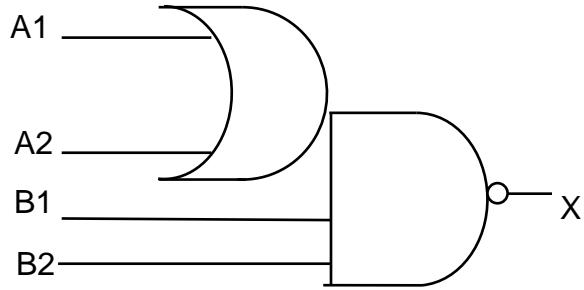


Figure 2.119. Logic Symbol of OAI211

Table 2.129. OAI211 Truth Table

A1	A2	B1	B2	X
-	1	-	-	0
1	-	-	-	0
-	-	1	1	0
0	0	0	-	1
0	0	-	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
OAI211_0P5	0.5 x Csl	39	0.23	0.09	0.6216	
OAI211_1	1 x Csl	38	0.37	0.18	0.7992	
OAI211_2	2 x Csl	37	0.66	0.34	1.1544	
OAI211_4	4 x Csl	37	1.27	0.68	1.9098	

OA121_*

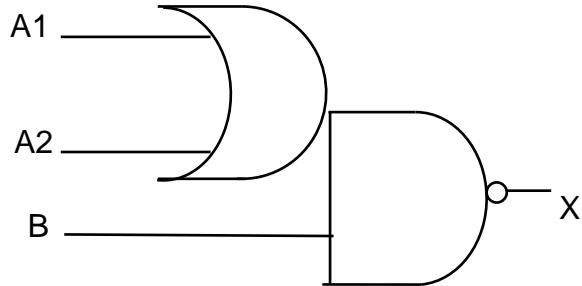


Figure 2.120. Logic Symbol of OA121

Table 2.130. OA121 Truth Table

A1	A2	B	X
-	1	-	0
1	-	-	0
-	-	1	0
0	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(μm^2)			
OA121_0P5	0.5 x Csl	33	0.15	0.11	0.2664	
OA121_0P75	0.75x Csl	33	0.15	0.11	0.2664	
OA121_1	1 x Csl	34	0.21	0.11	0.3552	
OA121_1P5	1.5 x Csl	32	0.3	0.24	0.444	
OA121_2	2 x Csl	31	0.3	0.18	0.444	
OA121_3	3 x Csl	31	0.45	0.24	0.6216	
OA121_4	4 x Csl	31	0.6	0.32	0.7548	

OA121_V1_*

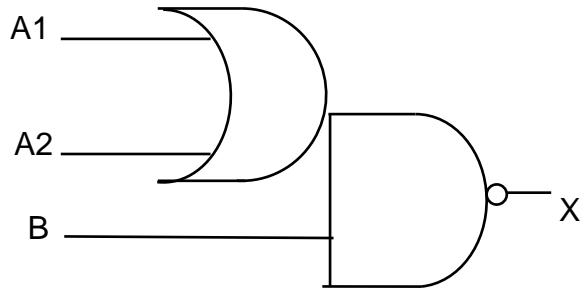


Figure 2.121. Logic Symbol of OA121_V1

Table 2.131. OA121_V1 Truth Table

A1	A2	B	X
-	1	-	0
1	-	-	0
-	-	1	0
0	0	0	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OA121_V1_4	4 x Csl	29	0.81	0.45	0.7104	
OA121_V1_6	6 x Csl	29	1.2	0.71	0.9768	
OA121_V1_8	8 x Csl	29	1.62	0.97	1.2432	

OAII21_*

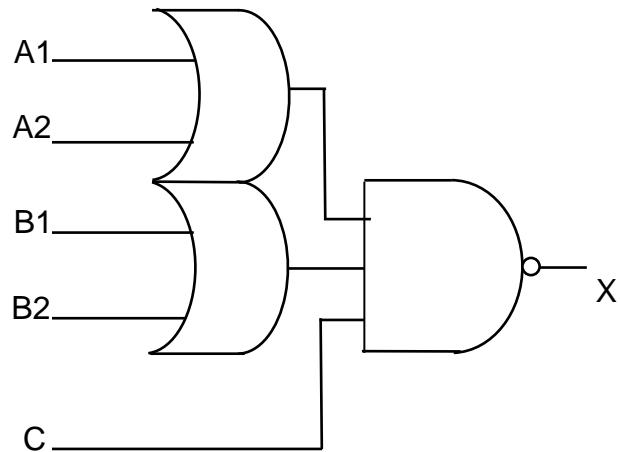


Figure 2.122. Logic Symbol of OAII21

Table 2.132. OAII21 Truth Table

A1	A2	B1	B2	C	X
0	0	-	-	-	1
-	-	0	0	-	1
-	-	-	-	0	1
1	-	1	-	1	0
-	1	1	-	1	0
1	-	-	1	1	0
-	1	-	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz				
OAII21_0P5	0.5 x Csl	48	0.49	0.09	1.0212	
OAII21_1	1 x Csl	46	0.69	0.16	1.0212	
OAII21_2	2 x Csl	45	0.72	0.29	1.1544	
OAII21_4	4 x Csl	44	0.99	0.6	1.5984	

OAI222_*

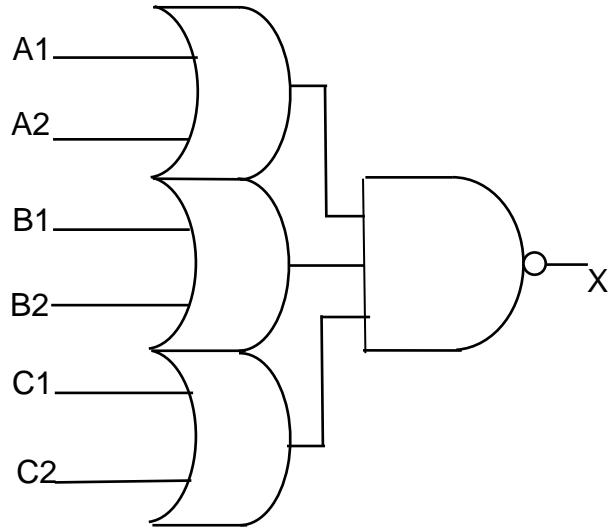


Figure 2.123. Logic Symbol of OAI222

Table 2.133. OAI222 Truth Table

A1	A2	B1	B2	C1	C2	X
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1
1	-	1	-	1	-	0
1	-	1	-	-	1	0
1	-	-	1	1	-	0
1	-	-	1	-	1	0
-	1	1	-	1	-	0
-	1	1	-	-	1	0
-	1	-	1	1	-	0
-	1	-	1	-	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OAI222_0P5	0.5 x Csl	44	0.28	0.09	0.7104	
OAI222_1	1 x Csl	45	0.3	0.09	0.7104	
OAI222_2	2 x Csl	46	0.38	0.09	0.7584	
OAI222_4	4 x Csl	50	0.53	0.09	0.7584	

OA122_*

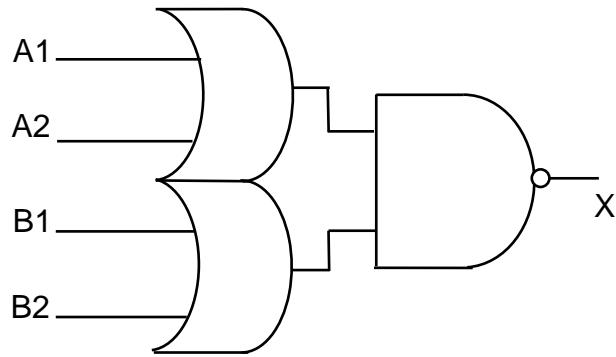


Figure 2.124. Logic Symbol of OA122

Table 2.134. OA122 Truth Table

A1	A2	B1	B2	X
0	0	-	-	1
-	-	0	0	1
1	-	1	-	0
-	1	1	-	0
1	-	-	1	0
-	1	-	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(μm^2)			
OA122_0P5	0.5 x Csl	31	0.1	0.07	0.3108	
OA122_0P75	0.75 x Csl	31	0.15	0.1	0.3108	
OA122_1	1 x Csl	31	0.2	0.17	0.3108	
OA122_1P5	1.5 x Csl	31	0.31	0.17	0.5328	
OA122_2	2 x Csl	30	0.31	0.17	0.5772	
OA122_3	3 x Csl	31	0.61	0.33	0.7548	
OA122_4	4 x Csl	30	0.81	0.44	0.8874	

OA1311_*

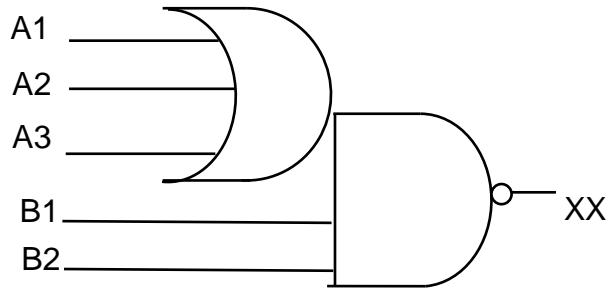


Figure 2.125. Logic Symbol of OA1311

Table 2.135. OA1311 Truth Table

A1	A2	A3	B1	B2	X
-	-	-	-	0	1
-	-	-	0	-	1
0	0	0	-	-	1
1	-	-	1	1	0
-	1	-	1	1	0
-	-	1	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA1311_0P5	0.5 x Csl	41	0.21	0.11	0.5772	
OA1311_0P75	0.75 x Csl	42	0.21	0.11	0.5772	
OA1311_1	1 x Csl	43	0.24	0.11	0.5772	
OA1311_2	2 x Csl	42	0.31	0.11	0.6216	
OA1311_4	4 x Csl	48	0.46	0.11	0.7104	

OA131_*

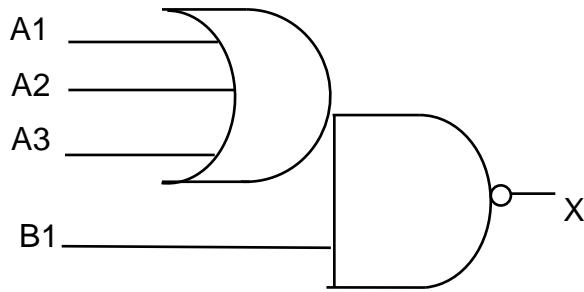


Figure 2.126. Logic Symbol of OA131

Table 2.136. OA131 Truth Table

A1	A2	A3	B	X
0	0	0	-	1
-	-	-	0	1
1	-	-	1	0
-	1	-	1	0
-	-	1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
OA131_0P5	0.5 x Csl	39	0.24	0.11	0.4884	
OA131_0P75	0.75 x Csl	39	0.26	0.11	0.4884	
OA131_1	1 x Csl	40	0.26	0.11	0.4884	
OA131_2	2 x Csl	39	0.36	0.09	0.5328	
OA131_4	4 x Csl	43	0.51	0.09	0.4884	

OA132_*

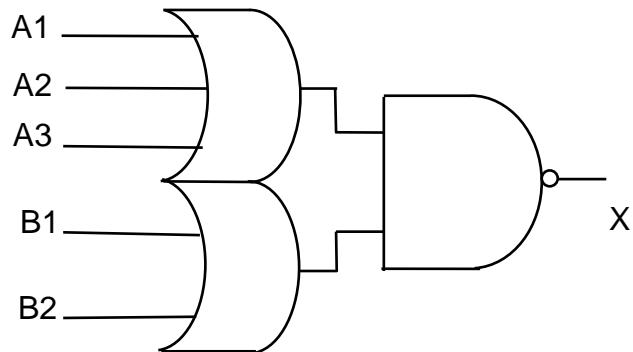


Figure 2.127. Logic Symbol of OA132

Table 2.137. OA132 Truth Table

A1	A2	A3	B1	B2	X
-	-	-	0	0	1
0	0	0	-	-	1
1	-	-	1	-	0
-	1	-	1	-	0
-	-	1	1	-	0
1	-	-	-	1	0
-	1	-	-	1	0
-	-	1	-	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	pW/MHz	
OA132_0P5	0.5 x Csl	41	0.3	0.11	0.5772	
OA132_0P75	0.75 x Csl	42	0.32	0.11	0.5772	
OA132_1	1 x Csl	41	0.32	0.11	0.5772	
OA132_2	2 x Csl	42	0.4	0.11	0.6216	
OA132_4	4 x Csl	46	0.55	0.11	0.666	

MUX2_*

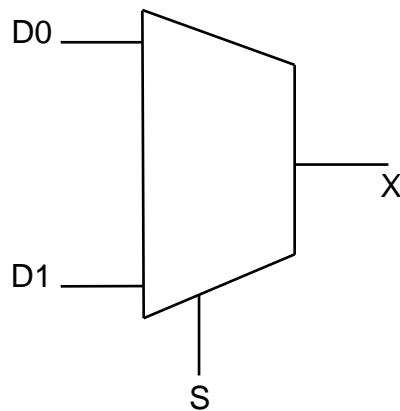


Figure 2.128. Logic Symbol of MUX2

Table 2.138. MUX2 Truth Table

S	X
0	D0
1	D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
MUX2_1	0.5 x Csl	38	0.21	0.07	0.4908	
MUX2_1P5	1.5 x Csl	37	0.39	0.14	0.6216	
MUX2_2	2 x Csl	40	0.38	0.14	0.6216	
MUX2_4	4 x Csl	40	0.76	0.24	0.9768	

MUX2_ECO_*

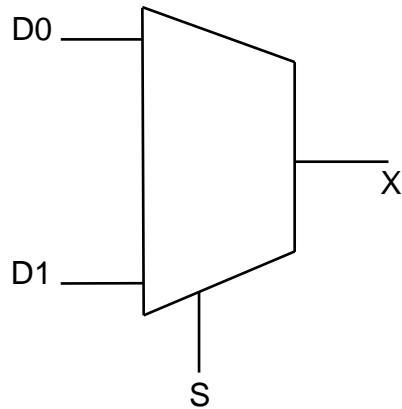


Figure 2.129. Logic Symbol of MUX2_ECO

Table 2.139. MUX2_ECO Truth Table

S	X
0	D0
1	D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUX2_ECO_1	1 x Csl	40	0.36	0.14	0.888	
MUX2_ECO_2	2 x Csl	43	0.43	0.14	1.0212	

MUX2_MM_*

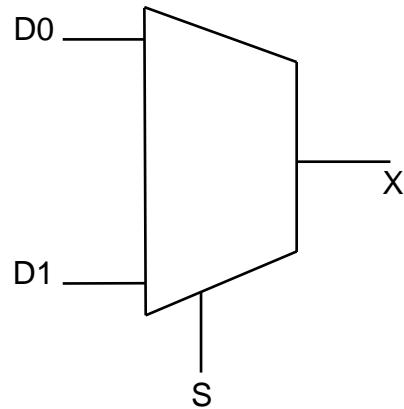


Figure 2.130. Logic Symbol of MUX2_MM

Table 2.140. MUX2_MM Truth Table

S	X
0	D0
1	D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUX2_MM_0P5	0.5 x Csl	36	0.18	0.07	0.402	
MUX2_MM_1	1 x Csl	38	0.21	0.07	0.4908	
MUX2_MM_2	2 x Csl	38	0.43	0.14	0.6216	
MUX2_MM_4	4 x Csl	40	0.76	0.24	0.9768	

MUX2_U_*

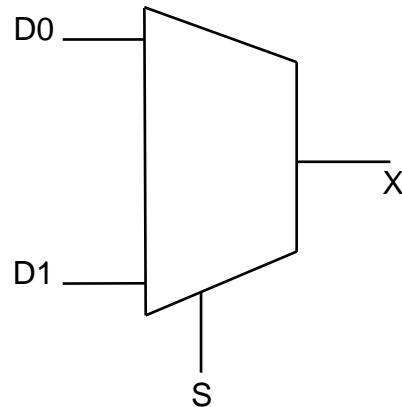


Figure 2.131. Logic Symbol of MUX2_U

Table 2.141. MUX2_U Truth Table

S	X
0	D0
1	D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUX2_U_0P5	0.5 x Csl	36 ps	0.18 nW	0.07 pW/MHz	0.4464	

MUXI2_*

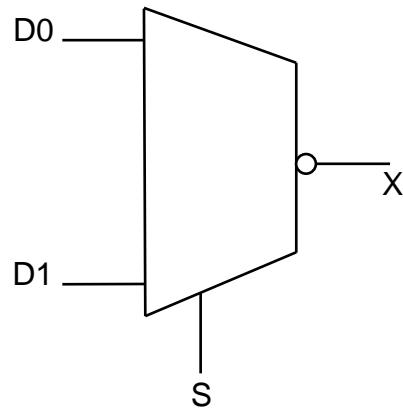


Figure 2.132. Logic Symbol of MUXI2

Table 2.142. MUXI2 Truth Table

S	X
0	!D0
1	!D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUXI2_0P5	0.5 x Csl	40	0.23	0.07	0.5352	
MUXI2_1	1 x Csl	40	0.28	0.07	0.5352	
MUXI2_2	2 x Csl	40	0.41	0.07	0.624	
MUXI2_4	4 x Csl	45	0.68	0.07	0.7128	

MUXI2_B_*

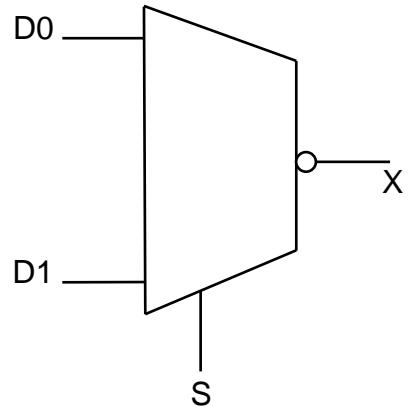


Figure 2.133. Logic Symbol of MUXI2

Table 2.143. MUXI2 Truth Table

S	X
0	!D0
1	!D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUXI2_B_1	1 x Csl	33	0.29	0.12	0.5328	

MUXI2_ECO_*

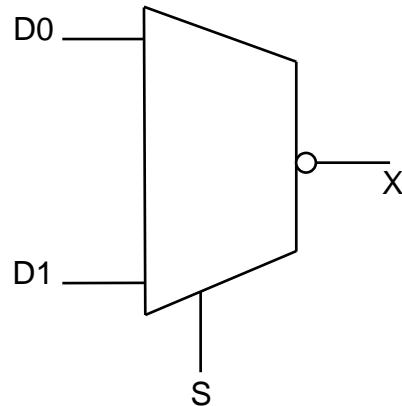


Figure 2.134. Logic Symbol of MUXI2_ECO

Table 2.144. MUXI2_ECO Truth Table

S	X
0	!D0
1	!D1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUXI2_ECO_1	1 x Csl	41	0.46	0.13	1.0212	
MUXI2_ECO_2	2 x Csl	42	0.56	0.14	1.1544	

MUXI2_U_*

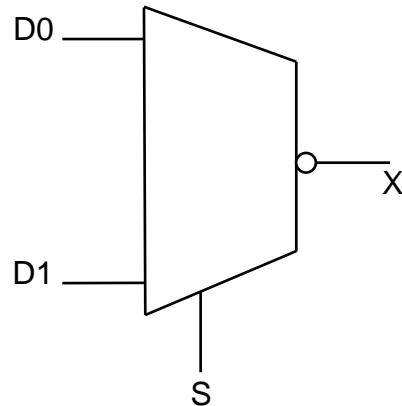


Figure 2.135. Logic Symbol of MUXI2_U

Table 2.145. MUXI2_U Truth Table

S	X
0	$\neg D_0$
1	$\neg D_1$

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUXI2_U_0P5	0.5 x Csl	32	0.14	0.07	0.402	

MUX3_V1M_*

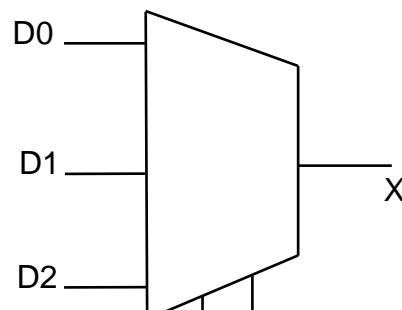


Figure 2.136. Logic Symbol of MUX3_V1M

Table 2.146. MUX3_V1M Truth Table

S0	S1	X
0	0	D0
0	1	D1
1	0	D2

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz		
MUX3_V1M_0P5	0.5 x Csl	45	0.37	0.27	0.888	
MUX3_V1M_1	1 x Csl	45	0.37	0.27	0.888	
MUX3_V1M_2	2 x Csl	42	0.75	0.56	1.0656	
MUX3_V1M_4	4 x Csl	45	1.07	1.04	1.4214	

MUXI3_*

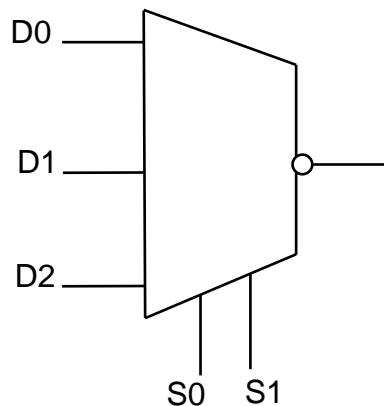


Figure 2.137. Logic Symbol of MUXI3

Table 2.147. MUXI3 Truth Table

S0	S1	X
0	0	!D0
0	1	!D1
1	0	!D2

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
MUXI3 _0P5	0.5 x Csl	47	0.39	0.29	0.9762	
MUXI3 _1	1 x Csl	47	0.44	0.29	0.9768	
MUXI3 _2	2 x Csl	46	0.88	0.52	1.0656	
MUXI3 _4	4 x Csl	48	1.15	0.53	1.2432	

MUX4_V1M_*

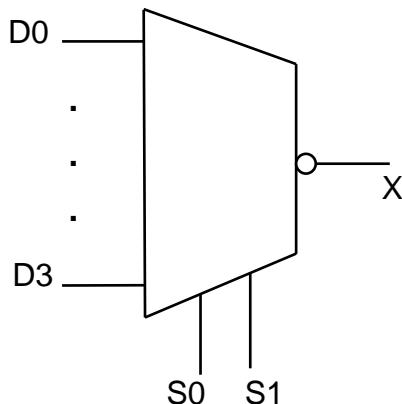


Figure 2.138. Logic Symbol of MUX4_V1M

Table 2.148. MUX4_V1M Truth Table

S0	S1	X
0	0	D0
0	1	D1
1	0	D2
1	1	D3

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
MUX4_V1M_1	1 x Csl	51	0.5	0.36	1.0656	
MUX4_V1M_2	2 x Csl	47	0.84	0.58	1.3764	
MUX4_V1M_4	4 x Csl	49	1.31	1.06	1.9986	

MUX4_V1U_*

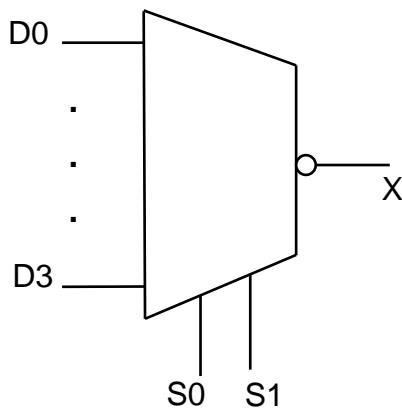


Figure 2.139. Logic Symbol of MUX4_V1U

Table 2.149. MUX4_V1U Truth Table

S0	S1	X
0	0	D0
0	1	D1
1	0	D2
1	1	D3

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	pW/MHz	(um ²)	
MUX4_V1U_0P5	0.5 x Csl	51	0.5	0.36	1.0656	

MUXI4_*

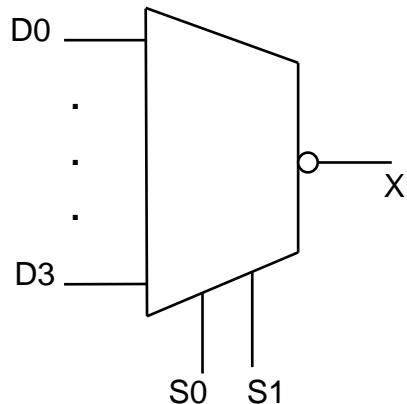


Figure 2.140. Logic Symbol of MUXI4

Table 2.150. MUXI4 Truth Table

S0	S1	X
0	0	!D0
0	1	!D1
1	0	!D2
1	1	!D3

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUXI4_2	2 x Csl	ps	nW	pW/MHz	(um ²)	
		45	0.64	0.44	1.1544	
MUXI4_4	4 x Csl	46	1.19	0.90	1.1544	

MUXI4_U_*

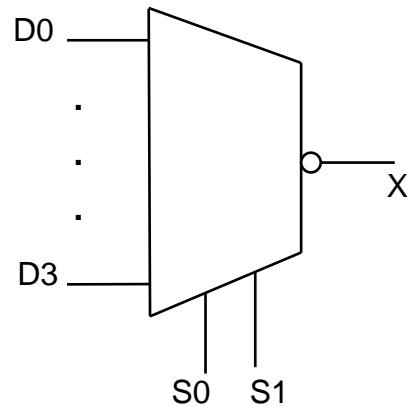


Figure 2.141. Logic Symbol of MUXI4_U

Table 2.151. MUXI4_U Truth Table

S0	S1	X
0	0	!D0
0	1	!D1
1	0	!D2
1	1	!D3

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
MUXI4_U_0P5	0.5 x Csl	43 ps	0.39 nW	0.32 pW/MHz	0.9784 μm^2	

ADDF_V1_*

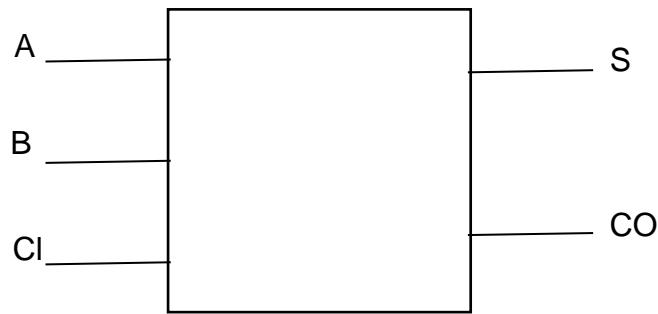


Figure 2.142. Logic Symbol of ADDF_V1

Table 2.152. ADDF_V1 Truth Table

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(μm^2)			
ADDF_V1_0P5	0.5 x Csl	52	0.35	0.25	1.0212	
ADDF_V1_1	1 x Csl	50	0.57	0.58	1.0212	
ADDF_V1_2	2 x Csl	50	0.74	0.75	1.0656	

ADDF_V2_*

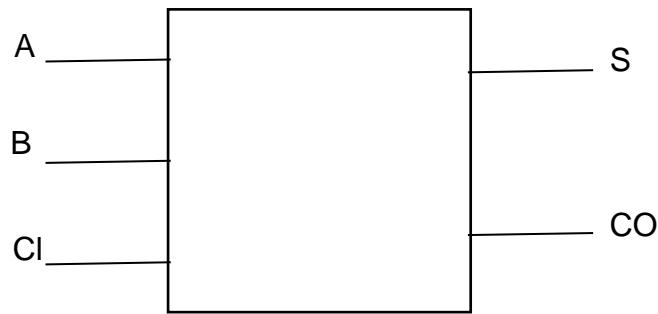


Figure 2.143. Logic Symbol of ADDF_V2

Table 2.153. ADDF_V2 Truth Table

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
ADDF_V2_0P5	0.5 x Csl	45	0.69	0.41	1.2426	
ADDF_V2_1	1 x Csl	42	0.98	0.57	1.2432	
ADDF_V2_2	2 x Csl	45	1.15	0.52	1.332	

ADDH_*

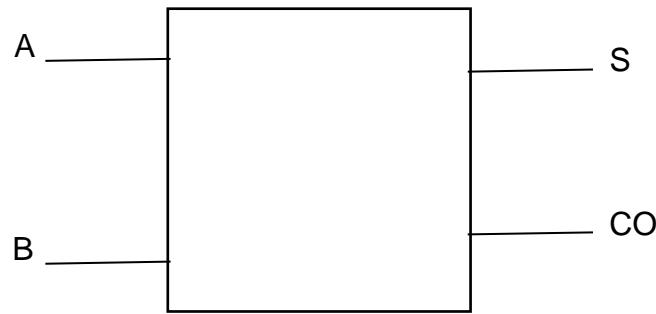


Figure 2.144. Logic Symbol of ADDH

Table 2.154. ADDH Truth Table

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ADDH_0P5	0.5 x Csl	34	0.4	0.22	0.666	
ADDH_1	1 x Csl	37	0.48	0.33	0.7548	
ADDH_2	2 x Csl	36	0.81	0.51	0.9324	
ADDH_4	4 x Csl	38	1.45	1.05	1.2432	

FDPQB_V2LP_*

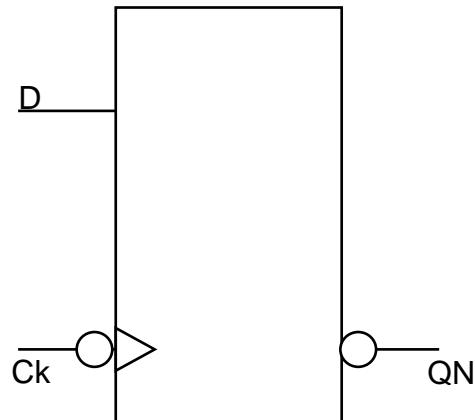


Figure 2.145. Logic Symbol of FDPQB_V2LP

Table 2.155. FDPQB_V2LP Truth Table

Ck	D	QN	QN+
R	0	-	1
R	1	-	0
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW		
FDPQB_V2LP_0P5	0.5 x Csl	43	0.4	0.92	0.8436	
FDPQB_V2LP_1	1 x Csl	41	0.45	0.90	0.8436	
FDPQB_V2LP_2	2 x Csl	40	0.63	1.13	0.888	

FDPQB_V2_*

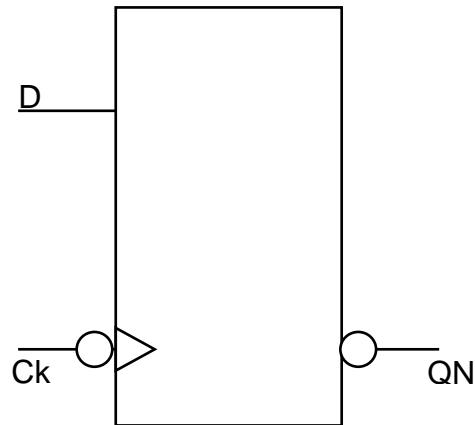


Figure 2.146. Logic Symbol of FDPQB_V2

Table 2.156. FDPQB_V2 Truth Table

Ck	D	QN	QN+
R	0	-	1
R	1	-	0
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPQB_V2_1	1 x Csl	38	0.57	1.22	0.8436	
FDPQB_V2_2	2 x Csl	37	0.68	1.22	0.888	
FDPQB_V2_4	4 x Csl	47	0.88	1.15	1.0656	
FDPQB_V2_8	8 x Csl	50	1.47	1.50	1.332	

FDPQB_V3_*

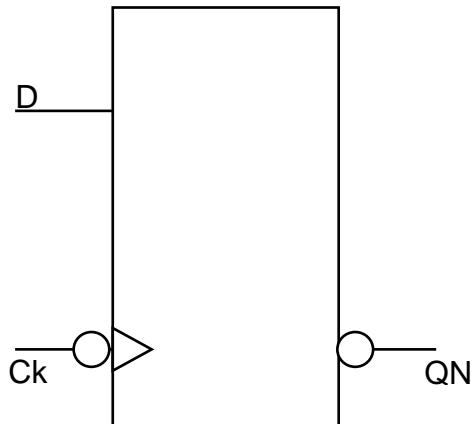


Figure 2.147. Logic Symbol of FDPQB_V3

Table 2.157. FDPQB_V3 Truth Table

Ck	D	QN	QN+
R	0	-	1
R	1	-	0
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ps	nW	pW/MHz	(μm^2)			
FDPQB_V3_1	1 x Csl	40	0.62	1.22	0.9768	
FDPQB_V3_2	2 x Csl	41	0.84	1.50	1.2882	
FDPQB_V3_4	4 x Csl	50	1.12	1.97	1.4652	
FDPQB_V3_8	8 x Csl	58	1.52	1.97	1.6428	

FDPQ_V2ECO_*

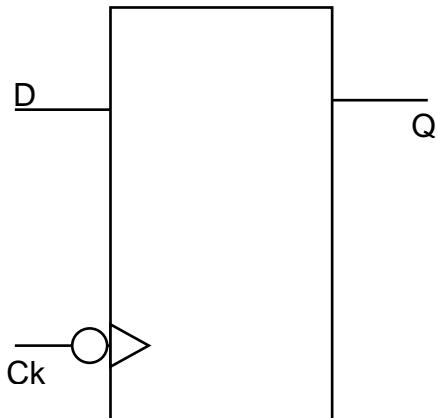


Figure 2.148. Logic Symbol of FDPQ_V2ECO

Table 2.158. FDPQ_V2ECO Truth Table

Ck	D	Q	Q+
R	0	-	0
R	1	-	1
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPQ_V2ECO_1	1 x Csl	40 ps	0.81 nW	0.94 pW/MHz	1.6872 μm^2	

FDPQ_V2_*

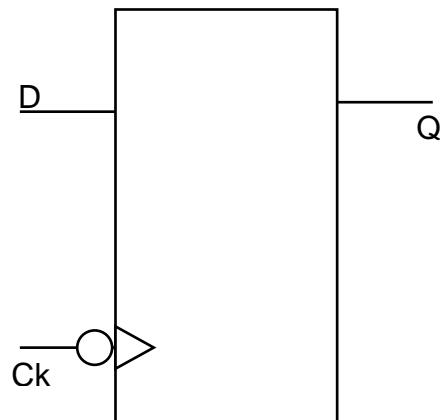


Figure 2.149. Logic Symbol of FDPQ_V2

Table 2.159. FDPQ_V2 Truth Table

Ck	D	Q	Q+
R	0	-	0
R	1	-	1
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPQ_V2_1	1 x Csl	41	0.9	1.28	1.1544	
FDPQ_V2_6	6 x Csl	44	1.53	1.05	1.4652	
FDPQ_V2_8	8 x Csl	46	1.89	1.86	1.7316	

FDPQ_V3_*

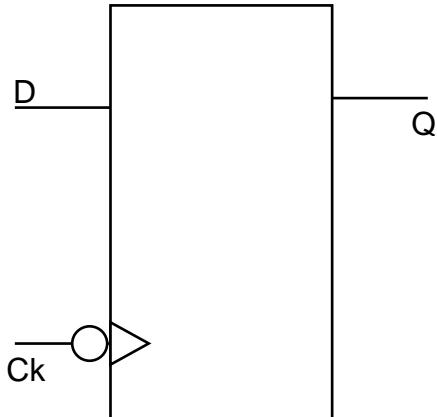


Figure 2.150. Logic Symbol of FDPQ_V3

Table 2.160. FDPQ_V3 Truth Table

Ck	D	Q	Q+
R	0	-	0
R	1	-	1
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPQ_V3_1	1 x Csl	41	0.65	0.65	1.0656	
FDPQ_V3_2	2 x Csl	41	0.76	0.67	0.9768	
FDPQ_V3_4	4 x Csl	43	1.01	0.67	1.332	

FDPRBQ_V2LP_*

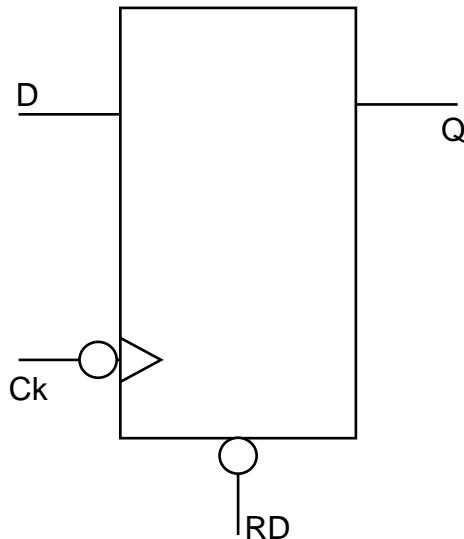


Figure 2.151. Logic Symbol of FDPRBQ_V2LP

Table 2.161. FDPRBQ_V2LP Truth Table

RD	Ck	D	Q	Q+
0	-	-	-	0
1	R	1	-	1
1	$\sim R$	-	-	NC
-	R	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPRBQ_V2LP_0P5	0.5 x Csl	43	0.43	0.62	1.0656	
FDPRBQ_V2LP_1	1 x Csl	44	0.48	0.62	1.0656	
FDPRBQ_V2LP_2	2 x Csl	47	0.58	0.62	1.111	

FDPRBQ_V2_*

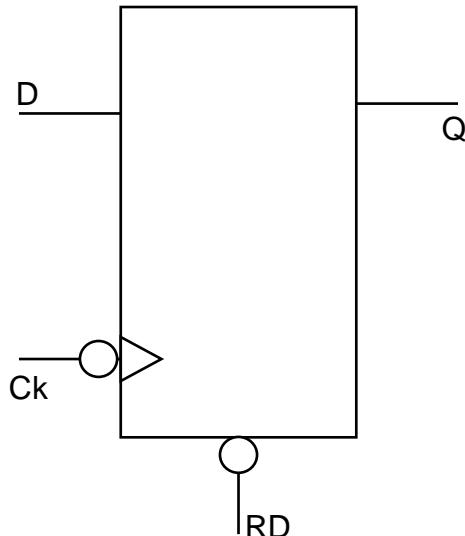


Figure 2.152. Logic Symbol of FDPRBQ_V2

Table 2.162. FDPRBQ_V2 Truth Table

RD	Ck	D	Q	Q+
0	-	-	-	0
1	R	1	-	1
1	$\sim R$	-	-	NC
-	R	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPRBQ_V2_0P5	0.5 x Csl	42	0.51	0.68	1.0656	
FDPRBQ_V2_1	1 x Csl	42	0.56	0.68	1.0656	
FDPRBQ_V2_2	2 x Csl	44	0.67	0.68	1.11	
FDPRBQ_V2_4	4 x Csl	48	0.86	0.68	1.1988	

FDPRBSBQ_V2_*

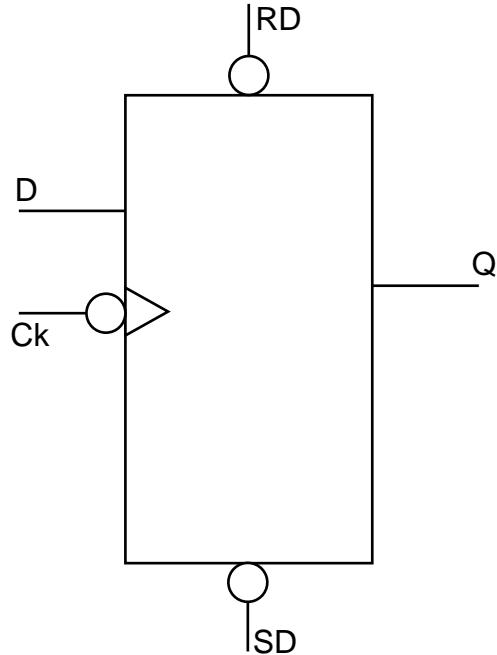


Figure 2.153. Logic Symbol of FDNRBSBQ_V2

Table 2.163. FDNRBSBQ_V2 Truth Table

RD	CK	D	SD	Q	Q+
0	-	-	-	-	0
1	R	1	-	-	1
1	$\sim R$	-	1	-	NC
1	-	-	0	-	1
-	R	0	1	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
FDPRBSBQ_V2_0P5	0.5 x Csl	42	0.58	0.72	1.1994		
FDPRBSBQ_V2_1	1 x Csl	42	0.63	0.72	1.1988		
FDPRBSBQ_V2_2	2 x Csl	44	0.9	0.72	1.332		
FDPRBSBQ_V2_4	4 x Csl	48	1.1	0.72	1.4208		

FDPRB_V3_*

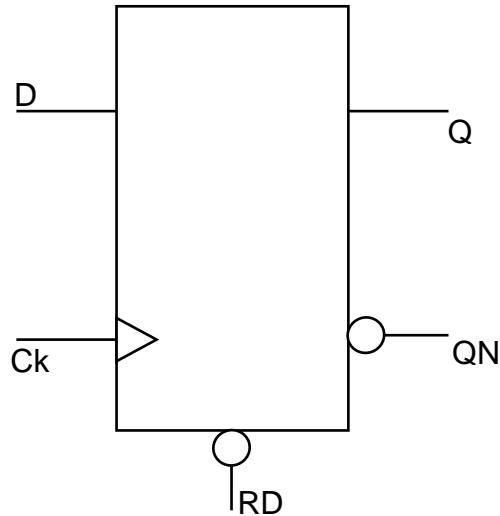


Figure 2.154. Logic Symbol of FDPRB_V3

Table 2.164. FDPRB_V3 Truth Table

RD	CK	D	Q	Q+
0	-	-	-	0
1	R	1	-	1
1	$\sim R$	-	-	NC
-	R	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FDPRB_V3_2	2 x Csl	47	1.23	0.83	1.5984	

FDPSBQ_*

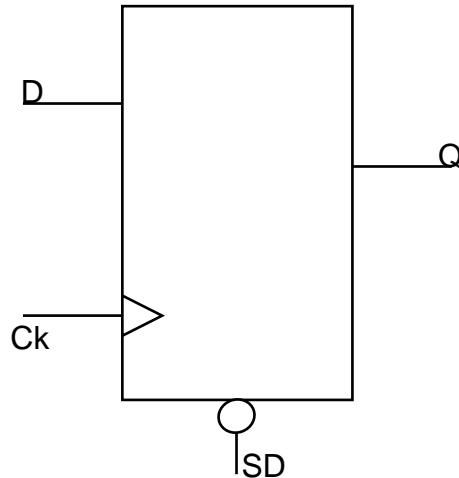


Figure 2.155. Logic Symbol of FDPSBQ

Table 2.165. FDPSBQ Truth Table

CK	D	SD	Q	Q+
R	0	1	-	0
R	1	-	-	1
$\sim R$	-	1	-	NC
R	-	0	-	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPSBQ_0P5	0.5 x Csl	46	0.55	0.64	1.11	
FDPSBQ_1	1 x Csl	46	0.59	0.64	1.11	
FDPSBQ_2	2 x Csl	47	0.75	0.64	1.1544	
FDPSBQ_4	4 x Csl	49	0.95	0.64	1.2432	

FDPSQB_*

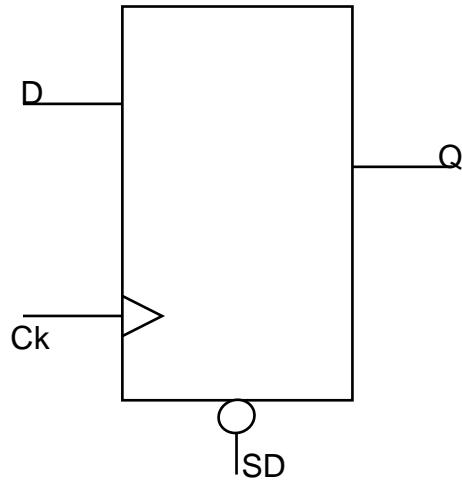


Figure 2.156. Logic Symbol of FDPSQB

Table 2.166. FDPSQB Truth Table

CK	D	SD	Q	Q+
R	0	0	-	1
R	1	-	-	0
$\sim R$	-	0	-	NC
-	-	1	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPSQB_2	2 x Csl	47	0.83	1.31	1.2876	

FDPSYNSBQ_V2_*

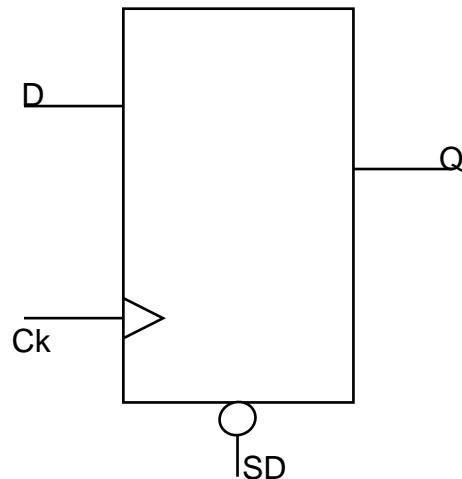


Figure 2.157. Logic Symbol of FDPSYNSBQ_V2

Table 2.167. FDPSYNSBQ_V2 Truth Table

CK	D	SD	Q	Q+
R	0	1	-	0
R	1	-	-	1
R	-	0	-	1
$\sim R$	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area (μm^2)	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
FDPSYNSBQ_V2_0P5	0.5 x Csl	44	0.57	1.01	1.0656		
FDPSYNSBQ_V2_1	1 x Csl	44	0.62	1.01	1.0656		
FDPSYNSBQ_V2_2	2 x Csl	45	0.77	1.16	1.1544		
FDPSYNSBQ_V2_4	4 x Csl	46	0.9	0.85	1.2432		

FDPS_V3_*

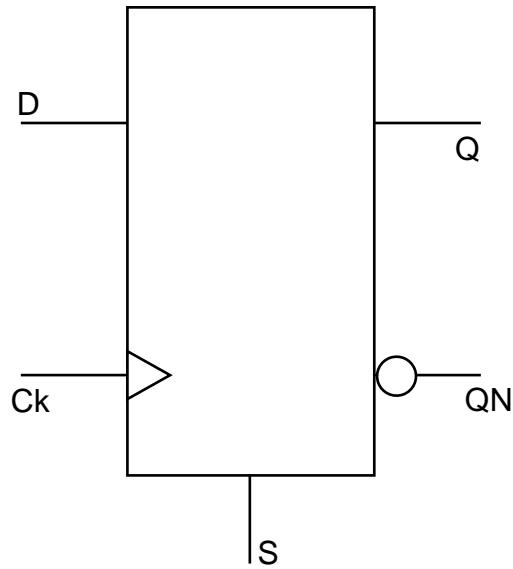


Figure 2.158. Logic Symbol of FDPS_V3

Table 2.168. FDPS_V3 Truth Table

CK	D	S	Q	Q+
R	0	0	-	0
R	1	-	-	1
$\sim R$	-	0	-	NC
-	-	1	-	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDPS_V3_2	2 x Csl	48	1.23	0.92	1.5984	

FDP_V2LP_*

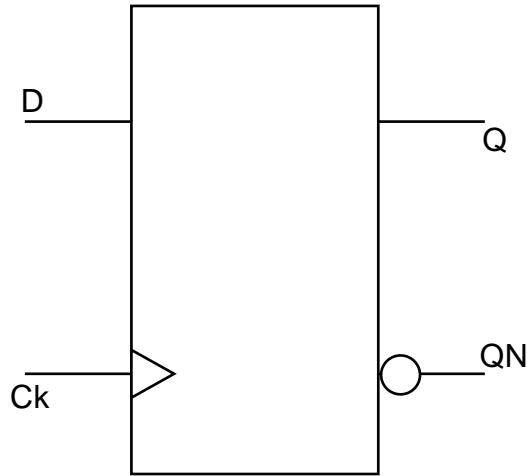


Figure 2.159. Logic Symbol of FDP_V2LP

Table 2.169. FDP_V2LP Truth Table

CK	D	Q	Q+
R	0	-	0
R	1	-	1
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FDP_V2LP_0P5	0.5 x Csl	45	0.44	0.45	0.9324	
FDP_V2LP_1	1 x Csl	46	0.52	0.43	0.9324	
FDP_V2LP_2	2 x Csl	50	0.69	0.44	1.0212	

FDP_V2_*

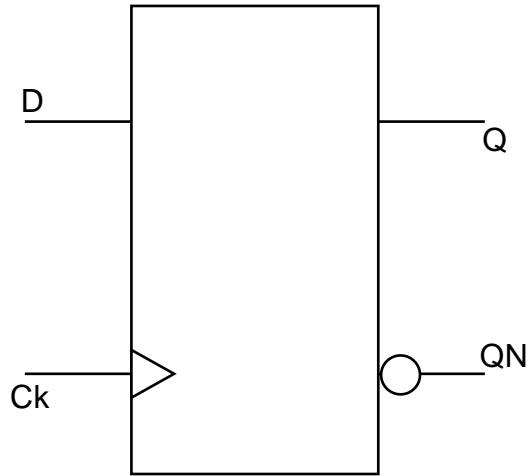


Figure 2.160. Logic Symbol of FDP_V2

Table 2.170. FDP_V2 Truth Table

CK	D	Q	Q+
R	0	-	0
R	1	-	1
$\sim R$	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
FDP_V2_0P5	0.5 x Csl	43	0.56	0.59	0.9324	
FDP_V2_1	1 x Csl	44	0.64	0.59	0.9324	
FDP_V2_2	2 x Csl	46	0.89	0.58	1.1544	
FDP_V2_4	4 x Csl	50	1.31	0.60	1.3764	

FSDNQ_V3_*

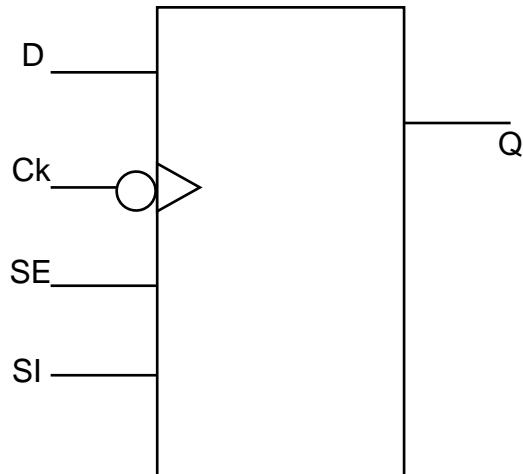


Figure 2.161. Logic Symbol of FSDNQ_V3

Table 2.171. FSDNQ_V3 Truth Table

CK	SI	D	SE	Q	Q+
F	0	0	-	-	0
F	0	-	1	-	0
F	1	1	-	-	1
F	1	-	1	-	1
F	-	0	0	-	0
F	-	1	0	-	1
$\sim F$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
FSDNQ_V3_1	1 x Csl	41	0.83	0.67	1.332	
FSDNQ_V3_2	2 x Csl	42	1.05	0.69	1.6872	
FSDNQ_V3_4	4 x Csl	46	1.25	0.69	1.776	

FSDN_V2_*

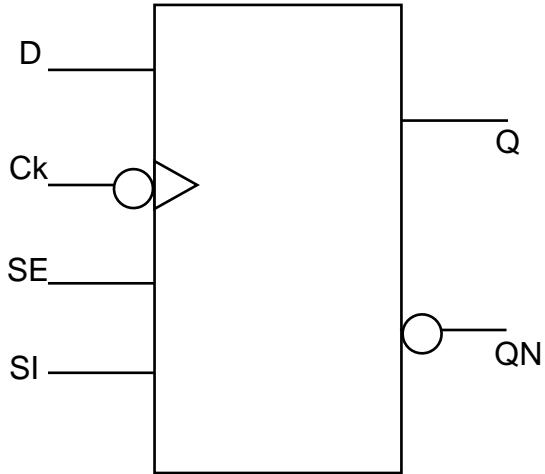


Figure 2.162. Logic Symbol of FSDN_V2

Table 2.172. FSDN_V2 Truth Table

CK	SI	D	SE	Q	Q+
F	0	0	-	-	0
F	0	-	1	-	0
F	1	1	-	-	1
F	1	-	1	-	1
F	-	0	0	-	0
F	-	1	0	-	1
$\sim F$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FSDN_V2_0P5	0.5 x Csl	47	0.58	0.61	1.1988	
FSDN_V2_1	1 x Csl	47	0.77	0.61	1.1988	
FSDN_V2_2	2 x Csl	48	1.01	0.61	1.332	
FSDN_V2_4	4 x Csl	54	1.39	0.67	1.5096	

FSDPMQ_*

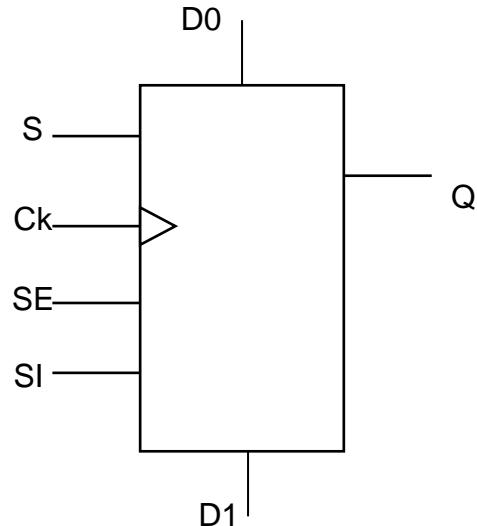


Figure 2.163. Logic Symbol of FSDPMQ

Table 2.173. FSDPMQ Truth Table

CK	SI	D1	D0	SE	S	Q	Q+
R	0	0	0	-	-	-	0
R	0	0	-	-	1	-	0
R	0	-	0	-	0	-	0
R	0	-	-	1	-	-	0
R	1	1	1	-	-	-	1
R	1	1	-	-	1	-	1
R	1	-	1	-	0	-	1
R	1	-	-	1	-	-	1
R	-	0	0	0	-	-	0
R	-	0	-	0	1	-	0
R	-	1	1	0	-	-	1
R	-	1	-	0	1	-	1
R	-	-	0	0	0	-	0
R	-	-	1	0	0	-	1
$\sim R$	-	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
FSDPMQ_0P5	0.5 x Csl	43	0.77	0.71	1.5096	
FSDPMQ_1	1 x Csl	44	0.82	0.71	1.5096	
FSDPMQ_2	2 x Csl	43	0.95	0.70	1.554	
FSDPMQ_4	4 x Csl	48	1.15	0.69	1.6428	

FSDPMQ_LP *

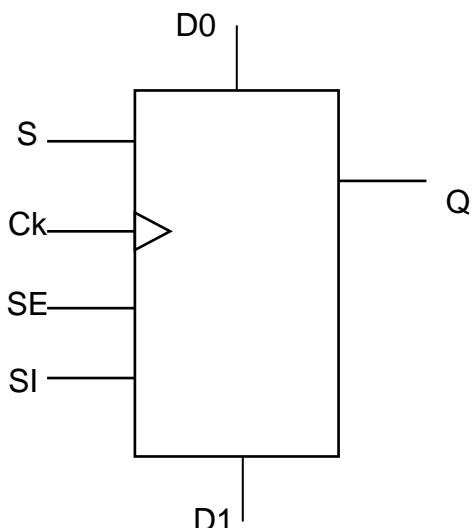


Figure 2.164. Logic Symbol of FSDPMQ_LP

Table 2.174. FSDPMQ_LP Truth Table

CK	SI	D1	D0	SE	S	Q	Q+
R	0	0	0	-	-	-	0
R	0	0	-	-	1	-	0
R	0	-	0	-	0	-	0
R	0	-	-	1	-	-	0
R	1	1	1	-	-	-	1
R	1	1	-	-	1	-	1
R	1	-	1	-	0	-	1
R	1	-	-	1	-	-	1
R	-	0	0	0	-	-	0
R	-	0	-	0	1	-	0
R	-	1	1	0	-	-	1
R	-	1	-	0	1	-	1
R	-	-	0	0	0	-	0
R	-	-	1	0	0	-	1
~R	-	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
Ps	nW	pW/MHz	(μm^2)			
FSDPMQ_LP_0P5	0.5 x Csl	44	0.65	0.47	1.5096	
FSDPMQ_LP_1	1 x Csl	45	0.7	0.47	1.5096	
FSDPMQ_LP_2	2 x Csl	47	0.88	0.52	1.554	

FSDPQB_V2LP_*

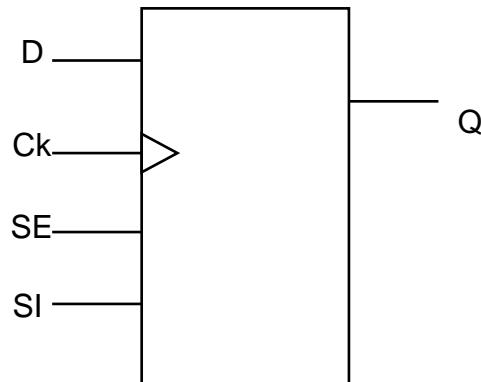


Figure 2.165. Logic Symbol of FSDPQB_V2LP

Table 2.175. FSDPQB_V2LP Truth Table

CK	SE	SI	D	Q	Q+
R	0	-	0	-	1
R	0	-	1	-	0
R	1	0	-	-	1
R	1	1	-	-	0
R	-	0	0	-	1
R	-	1	1	-	0
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FSDPQB_V2LP_0P5	0.5 x Csl	44	0.48	1.03	1.1094	
FSDPQB_V2LP_1	1 x Csl	46	0.53	1.02	1.1544	
FSDPQB_V2LP_2	2 x Csl	48	0.64	1.02	1.3764	

FSDPQB_V2_*

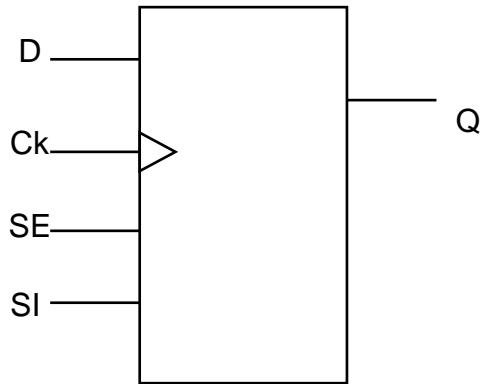


Figure 2.166. Logic Symbol of FSDPQB_V2

Table 2.176. FSDPQB_V2 Truth Table

CK	SE	SI	D	Q	Q+
R	0	-	0	-	1
R	0	-	1	-	0
R	1	0	-	-	1
R	1	1	-	-	0
R	-	0	0	-	1
R	-	1	1	-	0
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FSDPQB_V2_0P5	0.5 x Csl	42	0.65	1.32	1.11	
FSDPQB_V2_1	1 x Csl	43	0.7	1.32	1.11	
FSDPQB_V2_2	2 x Csl	43	0.87	1.47	1.1988	
FSDPQB_V2_4	4 x Csl	46	1.08	1.34	1.322	
FSDPQB_V2_8	8 x Csl	51	1.64	1.57	1.6428	

FSDPQB_V3_*

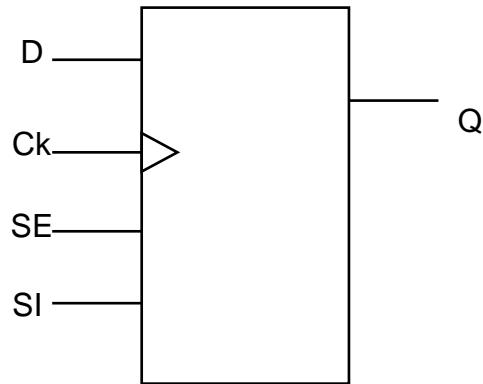


Figure 2.167. Logic Symbol of FSDPQB_V3

Table 2.177. FSDPQB_V3 Truth Table

CK	SE	SI	D	Q	Q+
R	0	-	0	-	1
R	0	-	1	-	0
R	1	0	-	-	1
R	1	1	-	-	0
R	-	0	0	-	1
R	-	1	1	-	0
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
FSDPQB_V3_1	1 x Csl	42	0.86	1.34	1.3764	
FSDPQB_V3_2	2 x Csl	43	093	1.34	1.3764	
FSDPQB_V3_4	4 x Csl	45	1.17	1.40	1.7316	
FSDPQB_V3_8	8 x Csl	48	1.57	1.40	1.9092	

FSDPQ_V2LP_*

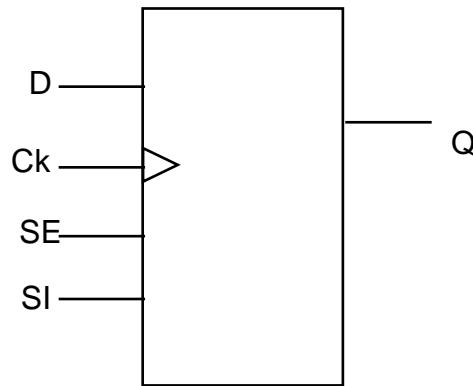


Figure 2.168. Logic Symbol of FSDPQ_V2LP

Table 2.178. FSDPQ_V2LP Truth Table

CK	SI	D	SE	Q	Q+
R	0	0	-	-	0
R	0	-	1	-	0
R	1	1	-	-	1
R	1	-	1	-	1
R	-	0	0	-	0
R	-	1	0	-	1
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FSDPQ_V2LP_0P5	0.5 x Csl	45	0.55	0.51	1.11	
FSDPQ_V2LP_1	1 x Csl	45	0.6	0.50	1.1094	
FSDPQ_V2LP_2	2 x Csl	47	0.7	0.50	1.1544	

FSDPQ_V2_*

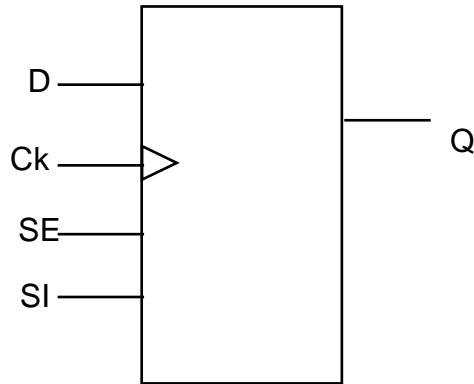


Figure 2.169. Logic Symbol of FSDPQ_V2

Table 2.179. FSDPQ_V2 Truth Table

CK	SI	D	SE	Q	Q+
R	0	0	-	-	0
R	0	-	1	-	0
R	1	1	-	-	1
R	1	-	1	-	1
R	-	0	0	-	0
R	-	1	0	-	1
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz		
FSDPQ_V2_0P5	0.5 x Csl	41	0.72	0.62	1.11	
FSDPQ_V2_1	1 x Csl	42	0.77	0.62	1.11	
FSDPQ_V2_2	2 x Csl	44	0.87	0.62	1.1544	
FSDPQ_V2_4	4 x Csl	47	1.11	0.61	1.2432	

FSDPQ_V3_*

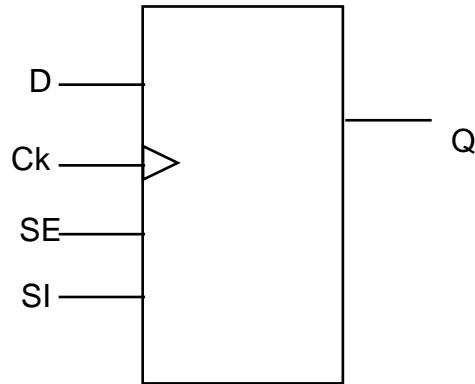


Figure 2.170. Logic Symbol of FSDPQ_V3

Table 2.180. FSDPQ_V3 Truth Table

CK	SI	D	SE	Q	Q+
R	0	0	-	-	0
R	0	-	1	-	0
R	1	1	-	-	1
R	1	-	1	-	1
R	-	0	0	-	0
R	-	1	0	-	1
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FSDPQ_V3_1	1 x Csl	42	0.83	0.74	1.3764	
FSDPQ_V3_2	2 x Csl	43	1.06	0.87	1.6872	
FSDPQ_V3_4	4 x Csl	45	1.26	0.87	1.776	

FSDPRBQ_V2LP_*

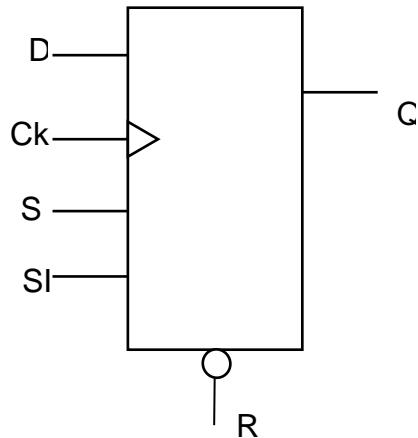


Figure 2.171. Logic Symbol of FSDPRBQ_V2LP

Table 2.181. FSDPRBQ_V2LP Truth Table

RD	CK	SI	D	SE	Q	Q+
0	-	-	-	-	-	0
1	R	1	1	-	-	1
1	R	1	-	1	-	1
1	R	-	1	0	-	1
1	~R	-	-	-	-	NC
-	R	0	0	-	-	0
-	R	0	-	1	-	0
-	R	-	0	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FSDPRBQ_V2LP_0P5	0.5 x Csl	43	0.52	0.59	1.2876	
FSDPRBQ_V2LP_1	1 x Csl	44	0.57	0.59	1.2876	
FSDPRBQ_V2LP_2	2 x Csl	47	0.67	0.59	1.332	

FSDPRBQ_V2_*

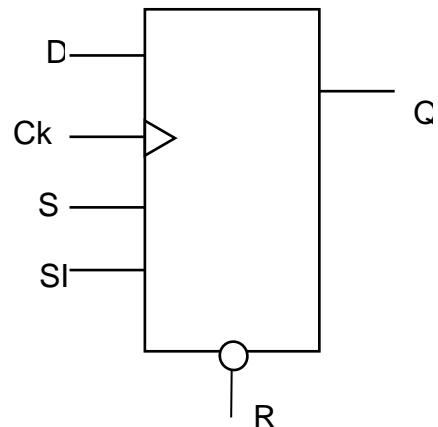


Figure 2.172. Logic Symbol of FSDPRBQ_V2

Table 2.182. FSDPRBQ_V2 Truth Table

RD	CK	SI	D	SE	Q	Q+
0	-	-	-	-	-	0
1	R	1	1	-	-	1
1	R	1	-	1	-	1
1	R	-	1	0	-	1
1	~R	-	-	-	-	NC
-	R	0	0	-	-	0
-	R	0	-	1	-	0
-	R	-	0	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FSDPRBQ_V2_0P5	0.5 x Csl	42	0.67	0.69	1.2876	
FSDPRBQ_V2_1	1 x Csl	43	0.72	0.69	1.2876	
FSDPRBQ_V2_2	2 x Csl	45	0.82	0.69	1.332	

FSDPRBQ_V3_*

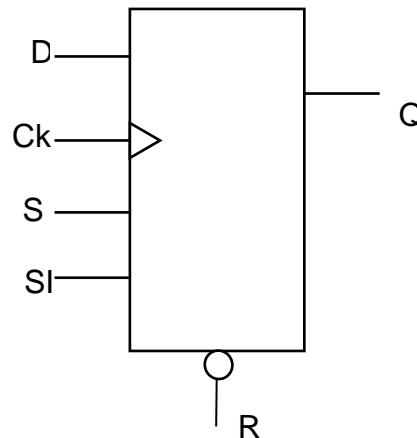


Figure 2.173. Logic Symbol of FSDPRBQ_V3

Table 2.183. FSDPRBQ_V3 Truth Table

RD	CK	SI	D	SE	Q	Q+
0	-	-	-	-	-	0
1	R	1	1	-	-	1
1	R	1	-	1	-	1
1	R	-	1	0	-	1
1	~R	-	-	-	-	NC
-	R	0	0	-	-	0
-	R	0	-	1	-	0
-	R	-	0	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FSDPRBQ_V3_1	1 x Csl	44	0.81	0.73	1.5096	
FSDPRBQ_V3_2	2 x Csl	47	0.97	0.91	1.6428	
FSDPRBQ_V3_4	4 x Csl	52	1.24	0.92	1.8648	

FSDPRBSBQ_V2LP_*

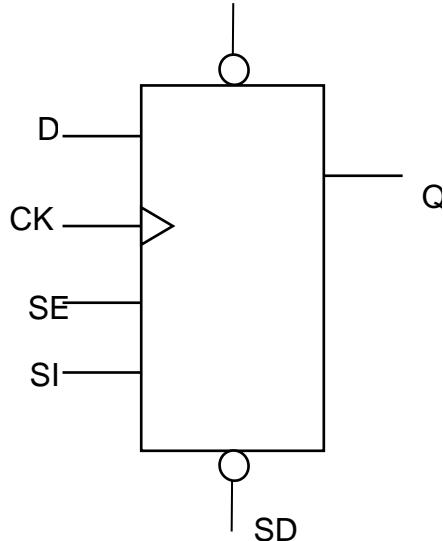


Figure 2.174. Logic Symbol of FSDPRBSBQ_V2LP

Table 2.184. FSDPRBSBQ_V2LP Truth Table

RD	CK	SI	D	SE	SD	Q	Q+
0	-	-	-	-	-	-	0
1	R	1	1	-	-	-	1
1	R	1	-	1	-	-	1
1	R	-	1	0	-	-	1
1	~R	-	-	-	1	-	NC
1	-	-	-	-	0	-	1
-	R	0	0	-	1	-	0
-	R	0	-	1	1	-	0
-	R	-	0	0	1	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
FSDPRBSBQ_V2LP_0P5	0.5 x Csl	43	0.55	0.61	1.3764	
FSDPRBSBQ_V2LP_1	1 x Csl	45	0.6	0.61	1.4208	
FSDPRBSBQ_V2LP_2	2 x Csl	47	0.7	0.61	1.4652	

FSDPRBSBQ_V2_*

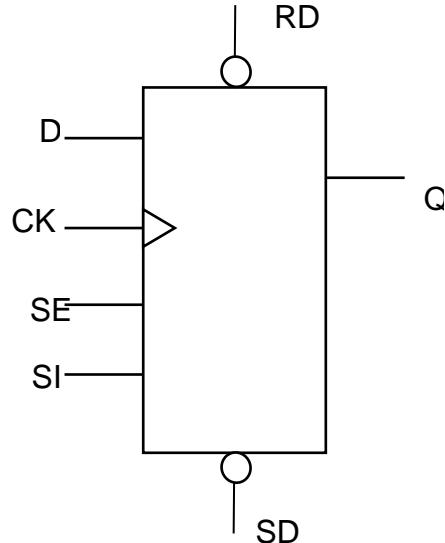


Figure 2.175. Logic Symbol of FSDPRBSBQ_V2

Table 2.185. FSDPRBSBQ_V2 Truth Table

RD	CK	SI	D	SE	SD	Q	Q+
0	-	-	-	-	-	-	0
1	R	1	1	-	-	-	1
1	R	1	-	1	-	-	1
1	R	-	1	0	-	-	1
1	~R	-	-	-	1	-	NC
1	-	-	-	-	0	-	1
-	R	0	0	-	1	-	0
-	R	0	-	1	1	-	0
-	R	-	0	0	1	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz		
FSDPRBSBQ_V2_0P5	0.5 x Csl	42	0.71	0.73	1.3764	
FSDPRBSBQ_V2_1	1 x Csl	42	0.8	0.73	1.4208	
FSDPRBSBQ_V2_2	2 x Csl	41	1.06	0.73	1.554	
FSDPRBSBQ_V2_4	4 x Csl	44	1.26	0.73	1.6428	

FSDPSBQ_V2LP_*

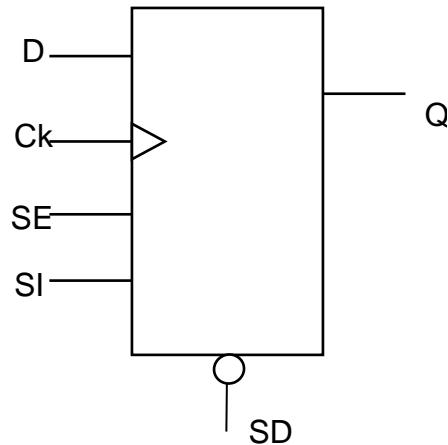


Figure 2.176. Logic Symbol of FSDPSBQ_V2LP

Table 2.186. FSDPSBQ_V2LP Truth Table

CK	SI	D	SE	SD	Q	Q+
R	0	0	-	1	-	0
R	0	-	1	1	-	0
R	1	1	-	-	-	1
R	1	-	1	-	-	1
R	-	0	0	1	-	0
R	-	1	0	-	-	1
$\sim R$	-	-	-	1	-	NC
-	-	-	-	0	-	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FSDPSBQ_V2LP_0P5	0.5 x Csl	43	0.52	0.52	1.2876	
FSDPSBQ_V2LP_1	1 x Csl	45	0.57	0.52	1.332	
FSDPSBQ_V2LP_2	2 x Csl	48	0.67	0.52	1.3764	

FSDPSBQ_V2_*

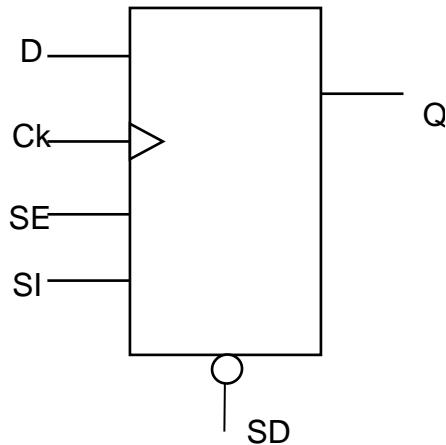


Figure 2.177. Logic Symbol of FSDPSBQ_V2

Table 2.187. FSDPSBQ_V2 Truth Table

CK	SI	D	SE	SD	Q	Q+
R	0	0	-	1	-	0
R	0	-	1	1	-	0
R	1	1	-	-	-	1
R	1	-	1	-	-	1
R	-	0	0	1	-	0
R	-	1	0	-	-	1
$\sim R$	-	-	-	1	-	NC
-	-	-	-	0	-	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area (μm^2)	
	Cload	Power					
		Prop Delay (Avg)	Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
			Ps	nW	pW/MHz		
FSDPSBQ_V2_0P5	0.5 x Csl	46	0.7	0.60	1.332		
FSDPSBQ_V2_1	1 x Csl	46	0.75	0.60	1.332		
FSDPSBQ_V2_2	2 x Csl	47	0.91	0.61	1.3764		
FSDPSBQ_V2_4	4 x Csl	50	1.11	0.61	1.4652		

FSDPSYNRBQ_V2LP_*

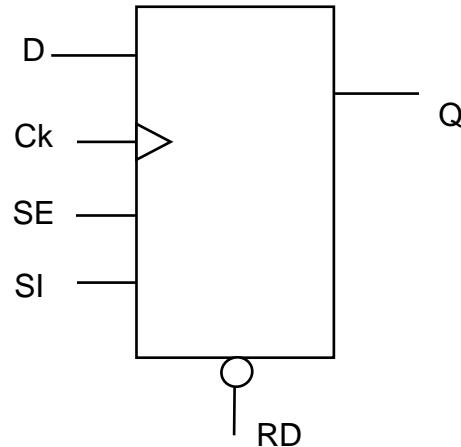


Figure 2.178. Logic Symbol of FSDPSYNRBQ_V2LP

Table 2.188. FSDPSYNRBQ_V2LP Truth Table

CK	SI	SE	RD	D	Q	Q+
R	0	1	-	-	-	0
R	0	-	0	-	-	0
R	0	-	-	0	-	0
R	1	1	-	-	-	1
R	1	-	1	1	-	1
R	-	0	0	-	-	0
R	-	0	1	1	-	1
R	-	0	-	0	-	0
$\sim R$	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FSDPSYNRBQ_V2LP_0P5	0.5 x Csl	43	0.62	0.51	1.2432	
FSDPSYNRBQ_V2LP_1	1 x Csl	45	0.67	0.51	1.2432	
FSDPSYNRBQ_V2LP_2	2 x Csl	47	0.78	0.51	1.2876	

FSDPSYNRBQ_V2_*

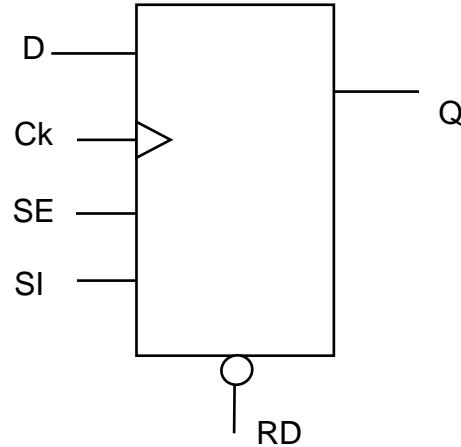


Figure 2.179. Logic Symbol of FSDPSYNRBQ_V2

Table 2.189. FSDPSYNRBQ_V2 Truth Table

CK	SI	SE	RD	D	Q	Q+
R	0	1	-	-	-	0
R	0	-	0	-	-	0
R	0	-	-	0	-	0
R	1	1	-	-	-	1
R	1	-	1	1	-	1
R	-	0	0	-	-	0
R	-	0	1	1	-	1
R	-	0	-	0	-	0
$\sim R$	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
			Ps	nW	pW/MHz		
FSDPSYNRBQ_V2_0P5	0.5 x Csl	41	0.74	0.66	1.2432		
FSDPSYNRBQ_V2_1	1 x Csl	42	0.8	0.66	1.2438		
FSDPSYNRBQ_V2_2	2 x Csl	43	0.87	0.63	1.3758		
FSDPSYNRBQ_V2_4	4 x Csl	48	1.13	0.63	1.4652		

FSDPSYNRBQ_V3_*

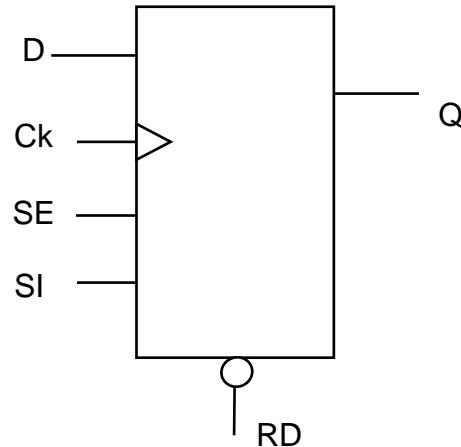


Figure 2.180. Logic Symbol of FSDPSYNRBQ_V3

Table 2.190. FSDPSYNRBQ_V3 Truth Table

CK	SI	SE	RD	D	Q	Q+
R	0	1	-	-	-	0
R	0	-	0	-	-	0
R	0	-	-	0	-	0
R	1	1	-	-	-	1
R	1	-	1	1	-	1
R	-	0	0	-	-	0
R	-	0	1	1	-	1
R	-	0	-	0	-	0
$\sim R$	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
FSDPSYNRBQ_V3_1	1 x Csl	42	0.84	0.86	1.3764	
FSDPSYNRBQ_V3_2	2 x Csl	42	1.07	0.85	1.6878	
FSDPSYNRBQ_V3_4	4 x Csl	47	1.34	0.99	1.8654	

FSDPSYNSBQ_V2LP_*

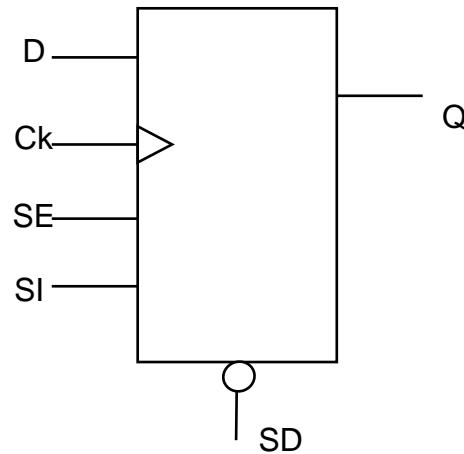


Figure 2.181. Logic Symbol of FSDPSYNSBQ_V2LP

Table 2.191. FSDPSYNSBQ_V2LP Truth Table

CK	SI	D	SE	SD	Q	Q+
R	0	0	-	1	-	0
R	0	-	1	-	-	0
R	1	1	-	-	-	1
R	1	-	1	-	-	1
R	1	-	-	0	-	1
R	-	0	0	1	-	0
R	-	1	0	-	-	1
R	-	-	0	0	-	1
$\sim R$	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
FSDPSYNSBQ_V2LP_0P5	0.5 x Csl	43	0.66	0.83	1.332		
FSDPSYNRBQ_V2LP_1	1 x Csl	44	0.69	0.82	1.3326		
FSDPSYNRBQ_V2LP_2	2 x Csl	47	0.79	0.51	1.3764		

FSDPSYNBQ_V2_*

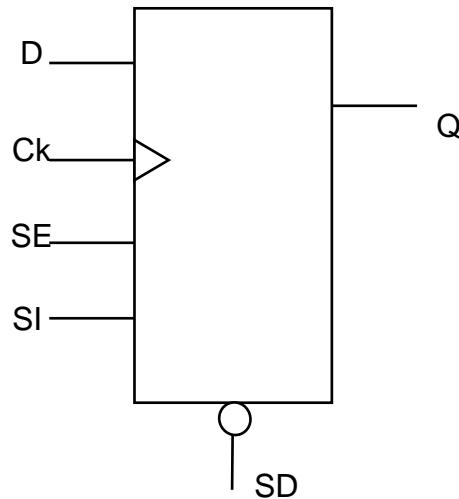


Figure 2.182. Logic Symbol of FSDPSYNBQ_V2

Table 2.192. FSDPSYNBQ_V2 Truth Table

CK	SI	D	SE	SD	Q	Q+
R	0	0	-	1	-	0
R	0	-	1	-	-	0
R	1	1	-	-	-	1
R	1	-	1	-	-	1
R	1	-	-	0	-	1
R	-	0	0	1	-	0
R	-	1	0	-	-	1
R	-	-	0	0	-	1
$\sim R$	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic	Area	
FSDPSYNBQ_V2_0P5	0.5 x Csl	41	0.78	1.11	1.332	
FSDPSYNRBQ_V2_1	1 x Csl	42	0.81	0.66	1.332	
FSDPSYNRBQ_V2_2	2 x Csl	43	0.89	0.63	1.5096	
FSDPSYNRBQ_V2_4	4 x Csl	47	1.15	0.63	1.467	

FSDP_V2LP_*

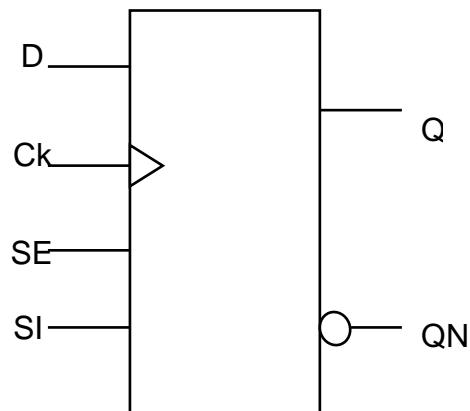


Figure 2.183. Logic Symbol of FSDP_V2LP

Table 2.193. FSDP_V2LP Truth Table

CK	SI	D	SE	Q	Q+
R	0	0	-	-	0
R	0	-	1	-	0
R	1	1	-	-	1
R	1	-	1	-	1
R	-	0	0	-	0
R	-	1	0	-	1
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
FSDP_V2LP_1	1 x Csl	47	0.61	0.43	1.5096	
FSDP_V2LP_2	2 x Csl	51	0.84	0.49	1.467	

FSDP_V2_*

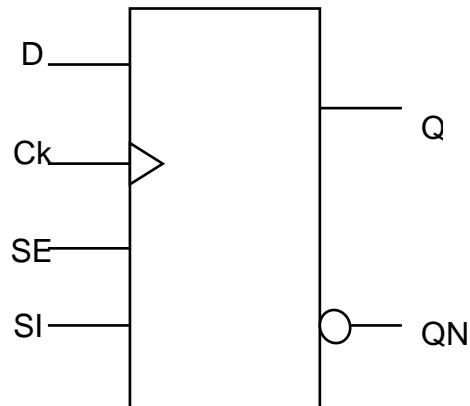


Figure 2.184. Logic Symbol of FSDP_V2

Table 2.194. FSDP_V2 Truth Table

CK	SI	D	SE	Q	Q+
R	0	0	-	-	0
R	0	-	1	-	0
R	1	1	-	-	1
R	1	-	1	-	1
R	-	0	0	-	0
R	-	1	0	-	1
$\sim R$	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
Ps	nW	pW/MHz	(μm^2)			
FSDP_V2_0P5	0.5 x Csl	44	0.69	0.60	1.11	
FSDP_V2_1	1 x Csl	44	0.78	0.59	1.1988	
FSDP_V2_2	2 x Csl	47	1.01	0.59	1.332	
FSDP_V2_4	4 x Csl	52	1.4	0.60	1.5546	

LDCKNR2PQ_*

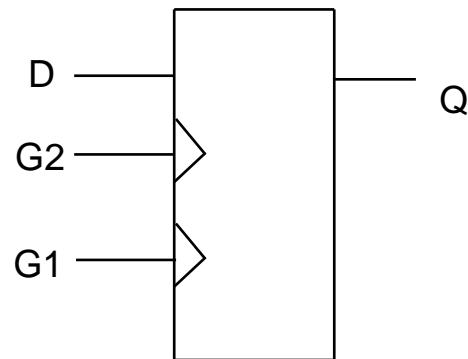


Figure 2.185. Logic Symbol of LDCKNR2PQ

Table 2.195. LDCKNR2PQ Truth Table

D	G2	G1	Q	Q+
0	1	-	-	0
0	-	1	-	0
1	1	-	-	1
1	-	1	-	1
-	0	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDCKNR2PQ_5	5 x Csl	41	1.08	0.34	1.1544	

LDND2NQ_*

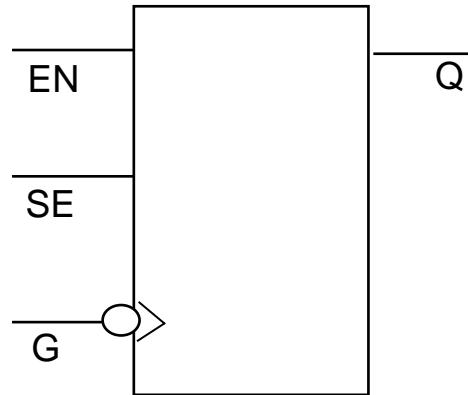


Figure 2.186. Logic Symbol of LDND2NQ

Table 2.196. LDND2NQ Truth Table

G	SE	EN	Q	Q+
0	0	-	-	0
0	1	1	-	1
0	-	0	-	0
1	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDND2NQ_1	1 x Csl	44	0.33	0.09	0.7104	
LDND2NQ_2	2 x Csl	47	0.43	0.09	0.7548	
LDND2NQ_4	4 x Csl	55	0.7	0.10	0.9768	

LDNQ_*

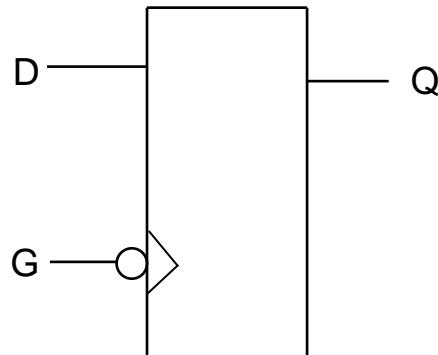


Figure 2.187. Logic Symbol of LDNQ

Table 2.197. LDNQ Truth Table

G	D	Q	Q+
0	0	-	0
0	1	-	1
1	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDNQ_1	1 x Csl	41	0.34	0.10	0.6216	
LDNQ_2	2 x Csl	43	0.44	0.10	0.666	
LDNQ_3	3 x Csl	46	0.63	0.15	0.7998	
LDNQ_4	4 x Csl	45	0.86	0.24	0.8886	
LDNQ_5	5 x Csl	45	0.86	0.24	0.933	
LDNQ_6	6 x Csl	47	0.96	0.24	0.9774	
LDNQ_8	8 x Csl	50	1.32	0.35	1.155	

LDNQ_U_*

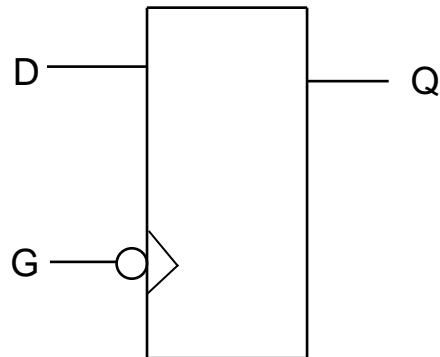


Figure 2.188. Logic Symbol of LDNQ_U

Table 2.198. LDNQ_U Truth Table

G	D	Q	Q+
0	0	-	0
0	1	-	1
1	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
LDNQ_U_0P5	0.5 x Csl	39	0.31	0.10	0.6216	

LDNQ_V1_*

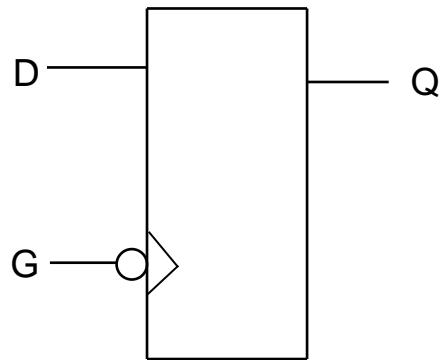


Figure 2.189. Logic Symbol of LDNQ_V1

Table 2.199. LDNQ_V1 Truth Table

G	D	Q	Q+
0	0	-	0
0	1	-	1
1	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDNQ_V1_1	0.5 x Csl	41	0.31	0.12	0.666	
LDNQ_V1_2	2 x Csl	44	0.41	0.12	0.7104	
LDNQ_V1_4	4 x Csl	48	0.68	0.13	0.7992	

LDNR2PQ_*

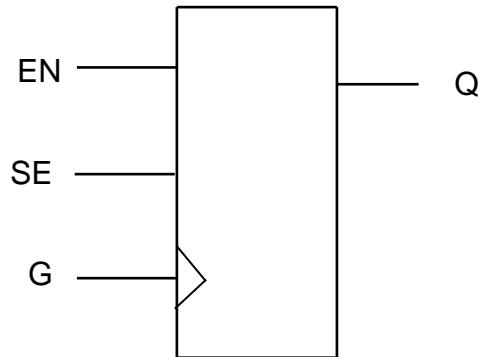


Figure 2.190. Logic Symbol of LDNR2PQ

Table 2.200. LDNR2PQ Truth Table

G	SE	EN	Q	Q+
0	0	0	-	0
0	1	-	-	1
0	-	1	-	1
1	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDNR2PQ_1	1 x Csl	45	0.3	0.07	0.666	
LDNR2PQ_2	2 x Csl	49	0.4	0.07	0.7104	
LDNR2PQ_4	4 x Csl	53	0.69	0.13	0.9324	

LDNRBQ_V2_*

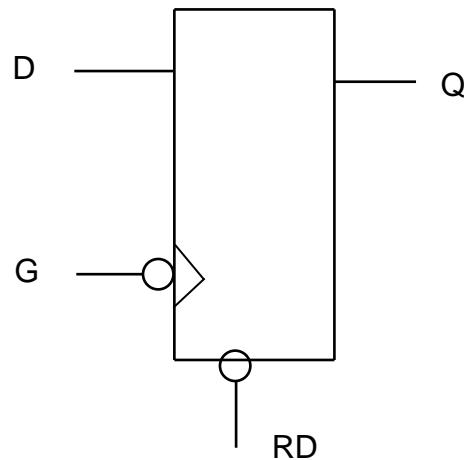


Figure 2.191. Logic Symbol of LDNRBQ

Table 2.201. LDNRBQ Truth Table

RD	G	D	Q	Q+
0	-	-	-	0
1	0	1	-	1
1	1	-	-	NC
-	0	0	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDNRBQ_V2_0P5	0.5 x Csl	47	0.37	0.09	0.7992	
LDNRBQ_V2_1	1 x Csl	48	0.42	0.09	0.7992	
LDNRBQ_V2_2	2 x Csl	48	0.55	0.17	0.888	
LDNRBQ_V2_4	4 x Csl	52	0.8	0.26	1.0212	

LDOR2PQ_*

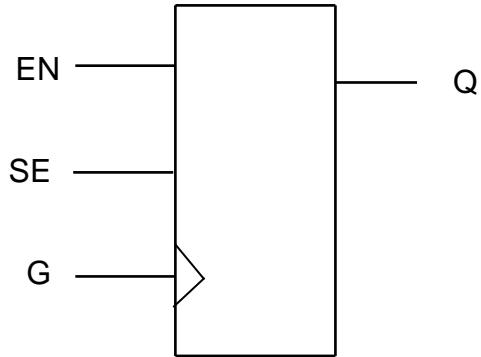


Figure 2.192. Logic Symbol of LDOR2PQ

Table 2.202. LDOR2PQ Truth Table

SE	EN	G	Q	Q+
0	0	1	-	0
1	-	1	-	1
-	1	1	-	1
-	-	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDOR2PQ_1	1 x Csl	47	0.3	0.07	0.666	
LDOR2PQ_2	2 x Csl	50	0.4	0.07	0.7104	
LDOR2PQ_4	4 x Csl	52	0.69	0.13	0.9324	

LDPQ_*

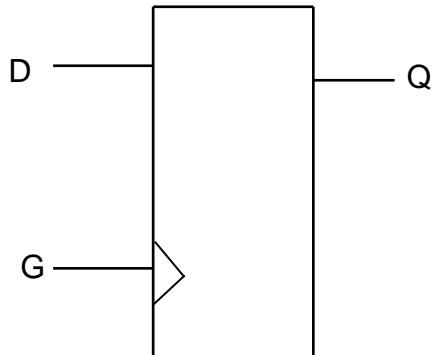


Figure 2.193. Logic Symbol of LDPQ

Table 2.203. LDPQ Truth Table

D	G	Q	Q+
0	1	-	0
1	1	-	1
-	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
Ps	nW	pW/MHz	(μm^2)			
LDPQ_1	1 x Csl	41	0.35	0.10	0.6216	
LDPQ_2	2 x Csl	42	0.45	0.10	0.666	
LDPQ_3	3 x Csl	47	0.63	0.15	0.7998	
LDPQ_4	4 x Csl	50	0.69	0.13	0.886	
LDPQ_5	5 x Csl	45	0.86	0.24	0.933	
LDPQ_6	6 x Csl	47	0.96	0.24	0.9774	

LDPQ_ECO_*

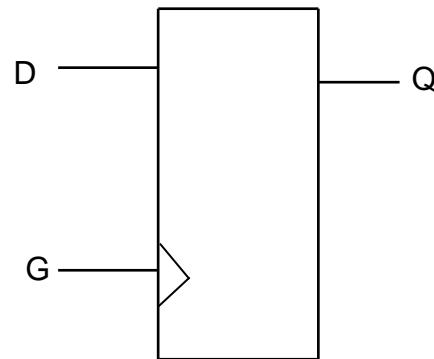


Figure 2.194. Logic Symbol of LDPQ_ECO

Table 2.204. LDPQ_ECO Truth Table

D	G	Q	Q+
0	1	-	0
1	1	-	1
-	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
LDPQ_ECO_1	1 x Csl	46	0.51	0.16	1.1544	

LDPQ_U_*

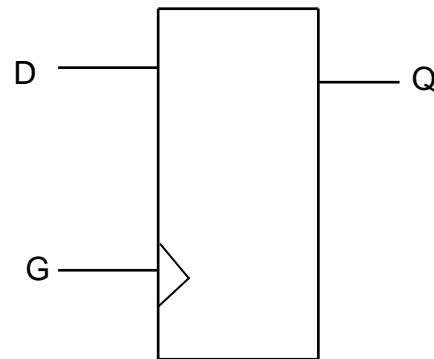


Figure 2.195. Logic Symbol of LDPQ_U

Table 2.205. LDPQ_U Truth Table

D	G	Q	Q+
0	1	-	0
1	1	-	1
-	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDPQ_U_0P5	0.5 x Csl	39	0.31	0.10	0.6216	

LDPQ_V1_*

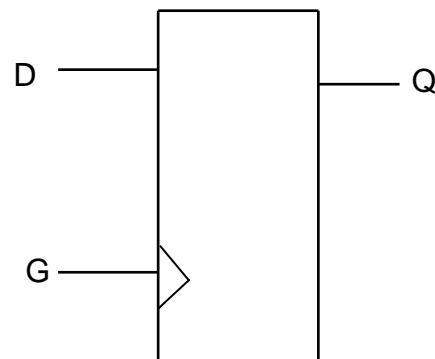


Figure 2.196. Logic Symbol of LDPQ_V1

Table 2.206. LDPQ_V1 Truth Table

D	G	Q	Q+
0	1	-	0
1	1	-	1
-	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
LDPQ_V1_1	1 x Csl	41	0.31	0.12	0.666	
LDPQ_V1_2	2 x Csl	44	0.41	0.12	0.7104	
LDPQ_V1_4	4 x Csl	50	0.69	0.13	0.888	

LDPRSQB_*

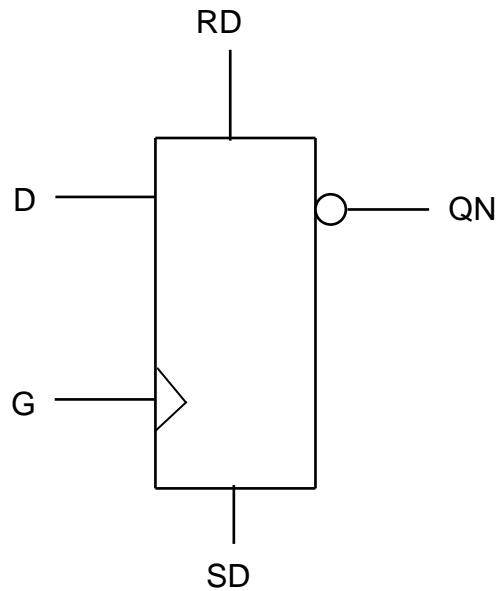


Figure 2.197. Logic Symbol of LDPRSQB

Table 2.207. LDPRSQB Truth Table

RD	D	G	SD	QN	QN+
0	1	1	-	-	0
0	-	0	0	-	NC
1	-	-	0	-	1
-	0	1	0	-	1
-	-	-	1	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
LDPRSQB_1	1 x Csl	42	0.45	0.07	0.7992	

LDPSBQ_V2_*

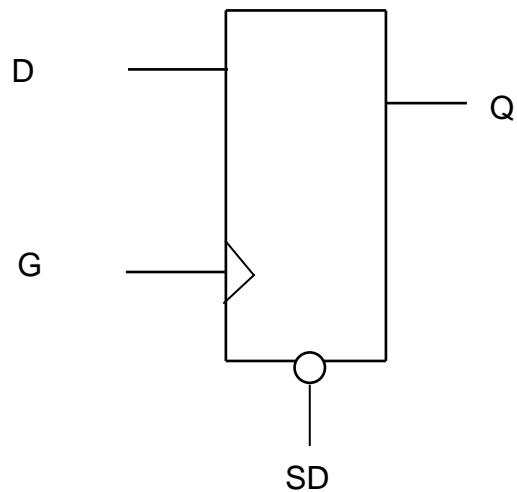


Figure 2.198. Logic Symbol of LDPSBQ_V2

Table 2.208. LDPSBQ_V2 Truth Table

D	SD	G	Q	Q+
0	1	1	-	0
1	-	1	-	1
-	0	-	-	1
-	1	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LDPSBQ_V2_0P5	0.5 x Csl	45	0.28	0.07	0.7104	
LDPSBQ_V2_1	1 x Csl	46	0.31	0.07	0.7104	
LDPSBQ_V2_2	2 x Csl	53	0.46	0.14	0.9768	
LDPSBQ_V2_4	4 x Csl	55	0.75	0.26	1.11	

CKGTNLT_V5

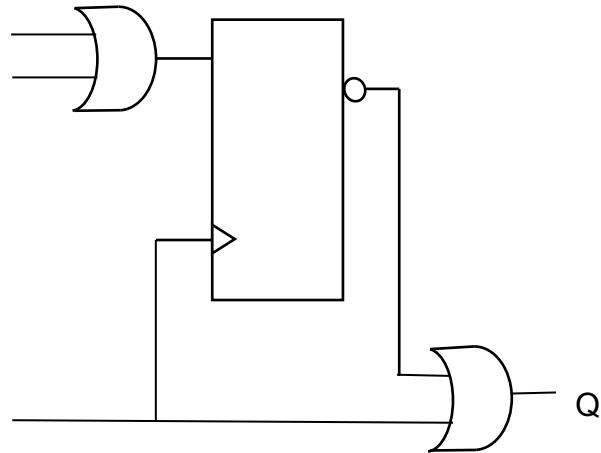


Figure 2.199. Logic Symbol of CKGTNLT_V5

Table 2.209. CKLGTNLT_V5 Truth Table

SE	EN	CK	IQ	IQ+
0	0	1	-	0
1	-	1	-	1
-	1	1	-	1
-	-	0	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
CKGTNLT_V5_1	1 x Csl	31	0.45	0.50	0.888		
CKGTNLT_V5_12	12 x Csl	40	1.85	0.74	1.776		
CKGTNLT_V5_2	2 x Csl	35	0.54	0.54	0.9324		
CKGTNLT_V5_3	3 x Csl	34	0.68	0.64	1.0656		
CKGTNLT_V5_4	4 x Csl	36	0.78	0.65	1.11		
CKGTNLT_V5_5	5 x Csl	37	1.012	0.66	1.332		
CKGTNLT_V5_6	6 x Csl	39	1.12	0.65	1.3764		
CKGTNLT_V5_8	8 x Csl	38	1.38	0.69	1.554		

CKGTPLT_V5_*

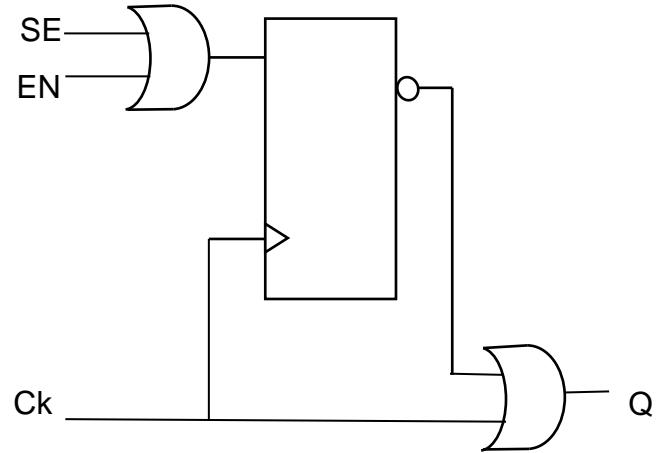


Figure 2.200. Logic Symbol of CKGTPLT_V5

Table 2.210. CKGTPLT_V5 Truth Table

SE	EN	CK	IQ	IQ+
0	0	0	-	0
1	-	0	-	1
-	1	0	-	1
-	-	1	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
CKGTPLT_V5_1	1 x Csl	32	0.37	0.41	0.7992	
CKGTPLT_V5_12	12 x Csl	36	1.89	0.82	1.6884	
CKGTPLT_V5_16	16 x Csl	39	2.39	0.80	1.9092	
CKGTPLT_V5_2	2 x Csl	36	0.47	0.43	0.7992	
CKGTPLT_V5_20	20 x Csl	39	2.9	0.91	2.1312	
CKGTPLT_V5_24	24 x Csl	40	3.42	0.01	2.4420	
CKGTONLT_V5_3	3 x Csl	36	0.64	0.53	0.9324	
CKGTONLT_V5_4	4 x Csl	35	0.73	0.48	1.0212	
CKGTONLT_V5_5	5 x Csl	37	0.96	0.65	1.2432	
CKGTONLT_V5_6	6 x Csl	36	1.13	0.70	1.1544	
CKGTONLT_V5_8	8 x Csl	35	1.43	0.80	1.4208	

CKGTPL_V5_*

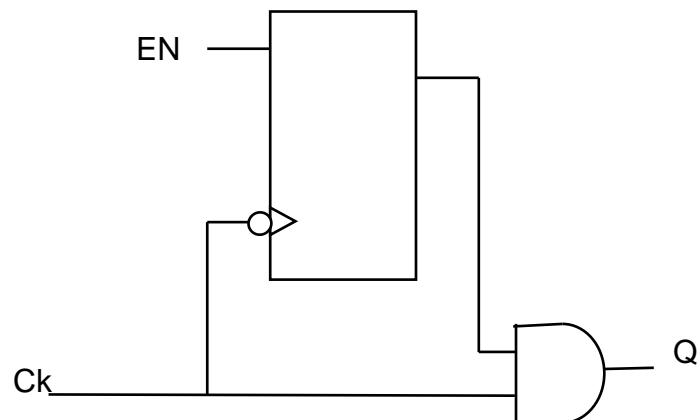


Figure 2.201. Logic Symbol of CKGTPL_V5

Table 2.211. CKGTPL_V5 Truth Table

EN	CK	IQ	IQ+
0	0	-	0
1	0	-	1
-	1	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
CKGTPL_V5_0P5	0.5 x Csl	33	0.36	0.46	0.8436	
CKGTPL_V5_1	1 x Csl	33	0.44	0.46	0.843	
CKGTPL_V5_2	2 x Csl	37	0.54	0.46	0.888	
CKGTPL_V5_4	4 x Csl	43	0.74	0.46	0.9768	

CKINVGTPLT_V7_*

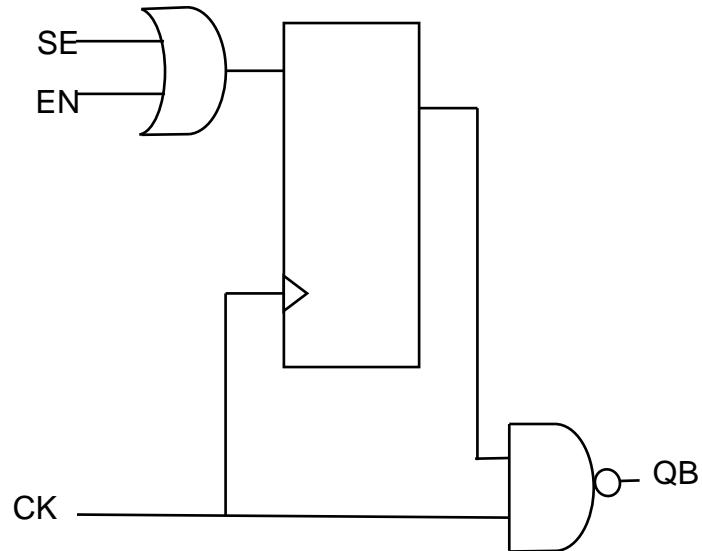


Figure 2.202. Logic Symbol of CKINVGTPLT_V7

Table 2.212. CKINVGTPLT_V7 Truth Table

SE	EN	CK	IQ	IQ+
0	0	0	-	0
1	-	0	-	1
-	1	0	-	1
-	-	1	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area (μm^2)	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
			Ps	nW	pW/MHz		
CKINVGTPLT_V7_1	1 x Csl	33	0.28	0.45	0.7104		
CKINVGTPLT_V7_2	2 x Csl	33	0.34	0.50	0.7992		
CKINVGTPLT_V7_3	3 x Csl	32	0.42	0.57	0.888		
CKINVGTPLT_V7_4	4 x Csl	33	0.5	0.62	0.9774		
CKINVGTPLT_V7_5	5 x Csl	33	0.57	0.69	0.9768		
CKINVGTPLT_V7_6	6 x Csl	33	0.65	0.76	1.1544		
CKINVGTPLT_V7_8	8 x Csl	33	0.81	0.89	1.332		

TIE0_*

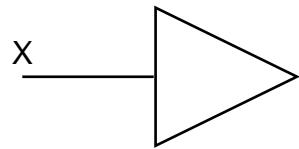
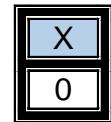


Figure 2.203. Logic Symbol of TIE0

Table 2.213. TIE0 Truth Table



General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25			Area (μm^2)	
	Cload	Power			
		Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
TIE0_4	4 x Csl	0	1.04	0.4884	

AN2_ISO4_*

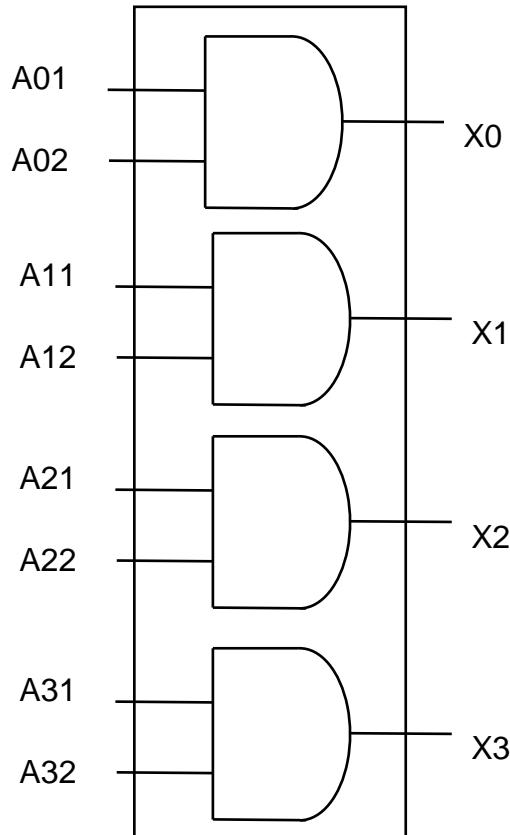


Figure 2.204. Logic Symbol of AN2_ISO4

Table 2.214. AN2_ISO4 Truth Table

A01	A02	X0
0	0	0
0	1	0
1	0	0
1	1	1

A11	A12	X1
0	0	0
0	1	0
1	0	0
1	1	1

A21	A22	X2
0	0	0
0	1	0
1	0	0
1	1	1

A31	A32	X3
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(um ²)	
AN2_ISO4_1	1 x Csl	33	0.6	0.09	0.9768	
AN2_ISO4_4	4 x Csl	34	1.97	0.23	1.8648	

ISOFSDPQ_PECO *

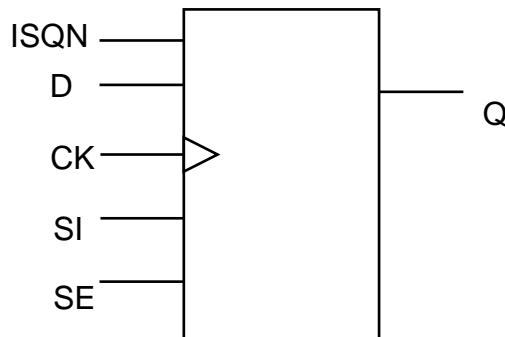


Figure 2.205. Logic Symbol of ISOFSDPQ_PECO

Table 2.215. ISOFSDPQ_PECO Truth Table

CK	D	SI	SE	ISON	Q	Q+
R	0	0	-	-	-	0
R	0	-	0	-	-	0
R	0	-	-	0	-	0
R	1	1	-	-	-	1
R	1	-	0	-	-	1
R	1	-	-	0	-	1
R	-	0	1	1	-	0
R	-	1	1	1	-	1
~R	-	-	-	-	-	NC

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ISOFSDPQ_PECO_4	4 x Csl	54	2.14	0	4.5012	
ISOFSDPQ_PECO_8	8 x Csl	56	2.64	0	5.1504	

ISOS0CL1_PECO_*

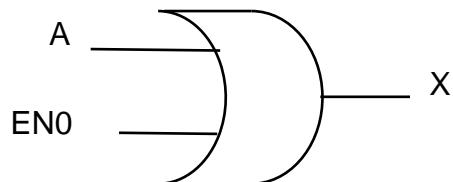


Figure 2.206. Logic Symbol of ISOS0CL1_PECO

Table 2.216. ISOS0CL1_PECO Truth Table

A	EN0	X
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ISOS0CL1_PECO_1	1 x Csl	35	0.21	0.10	0.6216	
ISOS0CL1_PECO_2	2 x Csl	35	0.24	0.10	0.6216	
ISOS0CL1_PECO_4	4 x Csl	35	0.28	0.10	0.621	
ISOS0CL1_PECO_8	8 x Csl	37	0.31	0.10	0.6216	

ISOS0CL1_P_*

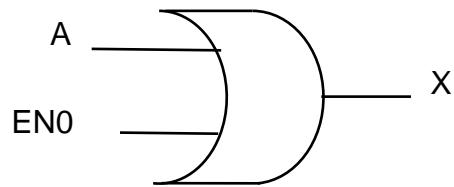


Figure 2.207. Logic Symbol of ISOS0CL1_P

Table 2.217. ISOS0CL1_P Truth Table

A	EN0	X
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ISOS0CL1_P_2	2 x Csl	35	0.17	0.07	0.3996	
ISOS0CL1_P_8	8 x Csl	39	0.47	0.11	0.4884	

ISOS0CL1_PECO4_*

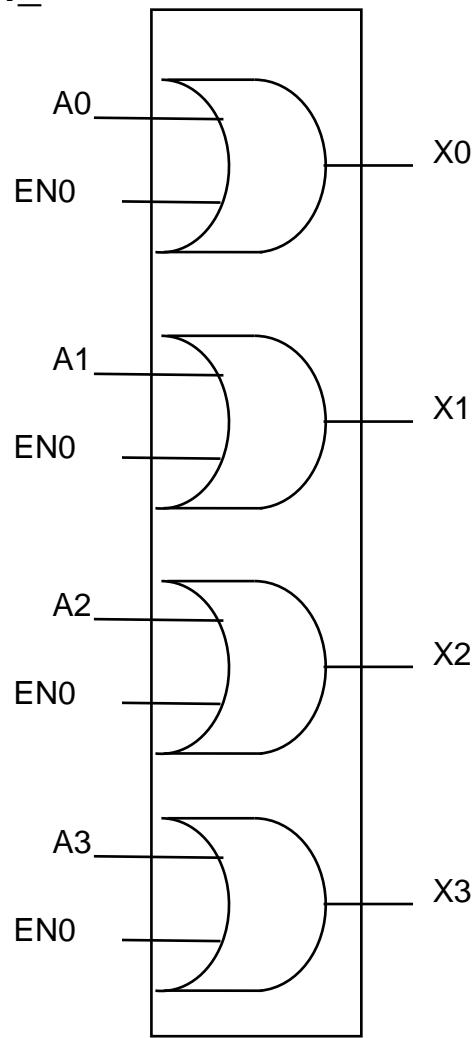


Figure 2.208. Logic Symbol of ISOS0CL1_PECO4

Table 2.218. ISOS0CL1_PECO4 Truth Table

A0	EN0	X0
0	0	0
0	1	1
1	0	1
1	1	1

A1	EN0	X1
0	0	0
0	1	1
1	0	1
1	1	1

A2	EN0	X2
0	0	0
0	1	1
1	0	1
1	1	1

A3	EN0	X3
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ISOS0CL1_PECO4_1	1 x Csl	42	1.43	3.42	3.108	
ISOS0CL1_PECO4_2	2 x Csl	40	1.69	4.78	3.108	

ISOS1CL0_PECO_*

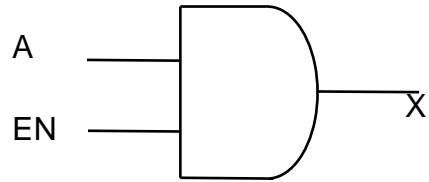


Figure 2.209. Logic Symbol of ISOS1CL0_PECO

Table 2.219. ISOS1CL0_PECO Truth Table

A	EN	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
ISOS1CL0_PECO_1	1 x Csl	38	0.16	0.01	0.6216	
ISOS1CL0_PECO_2	2 x Csl	34	0.18	0.01	0.6216	
ISOS1CL0_PECO_4	4 x Csl	36	0.23	0.01	0.6216	
ISOS1CL0_PECO_8	8 x Csl	38	0.26	0.01	0.6216	

ISOS1CL0_P_*

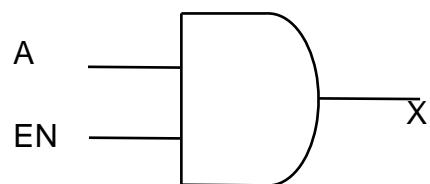


Figure 2.210. Logic Symbol of ISOS1CL0_P

Table 2.220. ISOS1CL0_P Truth Table

A	EN	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
ISOS1CL0_P_2	2 x Csl	35	0.23	0.01	0.3996	
ISOS1CL0_P_8	8 x Csl	40	0.48	0.01	0.4842	

OR2_ISO_*

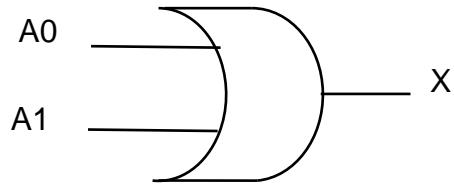


Figure 2.211. Logic Symbol of OR2_ISO

Table 2.221. OR2_ISO Truth Table

A1	A2	X
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OR2_ISO_1	1 x Csl	33	0.19	0.10	0.3558	
OR2_ISO_4	4 x Csl	34	0.22	0.10	0.3552	

NOR2_ISO4_*

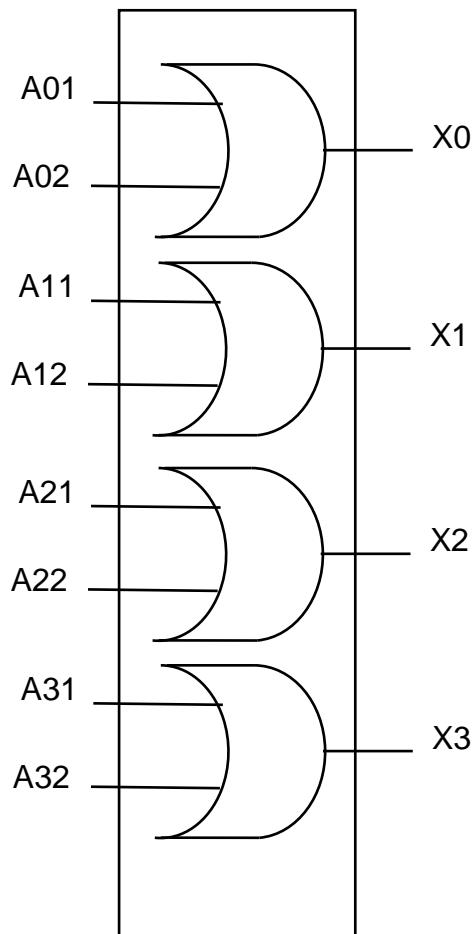


Figure 2.212. Logic Symbol of OR2_ISO4

Table 2.222. OR2_ISO4 Truth Table

A01	A02	X0
0	0	0
0	1	1
1	0	1
1	1	1

A11	A12	X1
0	0	0
0	1	1
1	0	1
1	1	1

A21	A22	X2
0	0	0
0	1	1
1	0	1
1	1	1

A31	A32	X3
0	0	0
0	1	1
1	0	1
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
NR2_ISO_1	1 x Csl	31	0.1	0.05	0.1776	
NR2_ISO_4	4 x Csl	32	0.41	0.26	0.4884	

LVLDBUFE0_IY2V1_*

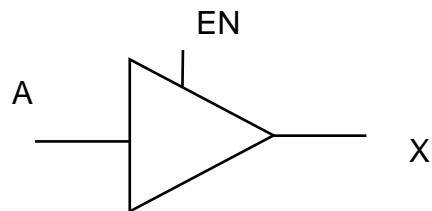


Figure 2.213. Logic Symbol of LVLDBUFE0_IY2V1

Table 2.223. LVLDBUFE0_IY2V1 Truth Table

A	EN	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
LVLDBUFE0_IY2V1_1	1 x Csl	7	1.76	0.95	4.3512	
LVLDBUFE0_IY2V1_10	10 x Csl	58	1.76	0.95	5.2392	
LVLDBUFE0_IY2V1_12	12 x Csl	60	1.94	0.95	5.4168	
LVLDBUFE0_IY2V1_2	2 x Csl	13	0.93	0.95	4.3512	
LVLDBUFE0_IY2V1_3	3 x Csl	18	1.03	0.95	4.44	
LVLDBUFE0_IY2V1_4	4 x Csl	25	1.14	0.95	4.5288	
LVLDBUFE0_IY2V1_6	6 x Csl	54	1.29	0.95	4.7952	
LVLDBUFE0_IY2V1_8	8 x Csl	56	1.47	0.95	4.9728	

LVLDBUFE0_IY2_*

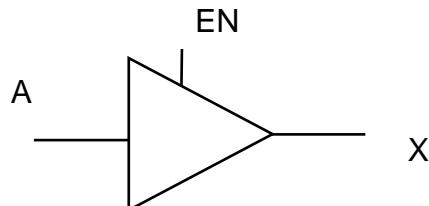


Figure 2.214. Logic Symbol of LVLDBUFE0_IY2

Table 2.224. LVLDBUFE0_IY2 Truth Table

A	EN	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(um ²)	
LVLDBUFE0_IY2_1	1 x Csl	49	0.83	0.95	4.3512	
LVLDBUFE0_IY2_10	10 x Csl	57	1.91	0.95	5.2392	
LVLDBUFE0_IY2_12	12 x Csl	60	2.11	0.95	5.4168	
LVLDBUFE0_IY2_2	2 x Csl	51	0.93	0.95	4.3512	
LVLDBUFE0_IY2_3	3 x Csl	52	1.03	0.95	4.44	
LVLDBUFE0_IY2_4	4 x Csl	52	1.15	0.95	4.5288	
LVLDBUFE0_IY2_6	6 x Csl	56	1.34	0.95	4.7952	

LVLDBUFE1_IY2V1_*

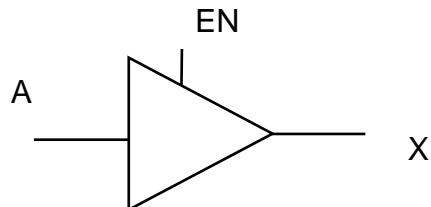


Figure 2.215. Logic Symbol of LVLDBUFE1_IY2V1

Table 2.225. LVLDBUFE1_IY2V1 Truth Table

A	EN	X
0	0	0
0	1	0
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
LVLDBUFE1_IY2V1_1	1 x Csl	52	1.31	1.30	4.5288	
LVLDBUFE1_IY2V1_10	10 x Csl	63	2.3	1.30	5.772	
LVLDBUFE1_IY2V1_12	12 x Csl	65	2.43	1.30	6.1272	
LVLDBUFE1_IY2V1_2	2 x Csl	52	1.38	1.30	4.5288	
LVLDBUFE1_IY2V1_3	3 x Csl	53	1.45	1.30	4.5288	
LVLDBUFE1_IY2V1_4	4 x Csl	53	1.52	1.30	4.5276	
LVLDBUFE1_IY2V1_6	6 x Csl	56	1.86	1.30	4.9728	
LVLDBUFE1_IY2V1_8	8 x Csl	59	1.98	1.30	5.328	

LVLDBUFE1_IY2_*

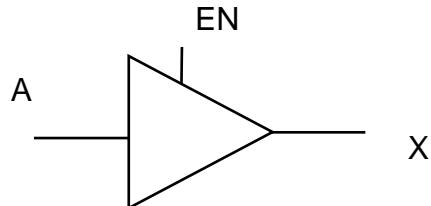


Figure 2.216. Logic Symbol of LVLDBUFE1_IY2

Table 2.226. LVLDBUFE1_IY2 Truth Table

A	EN	X
0	0	0
0	1	0
1	0	1
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
LVLDBUFE1_IY2_1	1 x Csl	52	1.31	1.36	4.5288	
LVLDBUFE1_IY2_10	10 x Csl	62	2.3	1.36	5.772	
LVLDBUFE1_IY2_12	12 x Csl	65	2.43	1.36	6.1272	
LVLDBUFE1_IY2_2	2 x Csl	51	2.43	1.36	4.5288	
LVLDBUFE1_IY2_4	4 x Csl	52	1.52	1.36	4.5288	
LVLDBUFE1_IY2_6	6 x Csl	55	1.86	1.36	4.9728	
LVLDBUFE1_IY2_8	8 x Csl	58	1.98	1.36	5.328	

LVLDBUF_IY2V1_*

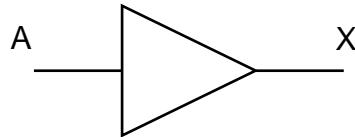


Figure 2.217. Logic Symbol of LVLDBUF_IY2V1

Table 2.227. LVLDBUF_IY2V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(μm^2)	
LVLDBUF_IY2V1_1	1 x Csl	43	1.49	1.36	4.5288	
LVLDBUF_IY2V1_10	10 x Csl	52	2.5	1.39	5.772	
LVLDBUF_IY2V1_12	12 x Csl	54	2.64	1.41	6.1272	
LVLDBUF_IY2V1_2	2 x Csl	45	1.56	1.22	4.5288	
LVLDBUF_IY2V1_3	3 x Csl	46	1.63	1.25	4.5288	
LVLDBUF_IY2V1_4	4 x Csl	48	1.69	1.28	4.5276	
LVLDBUF_IY2V1_6	6 x Csl	49	2.13	1.34	4.9728	
LVLDBUF_IY2V1_8	8 x Csl	51	2.3	1.38	5.328	

ELVLDNOR_V2_*

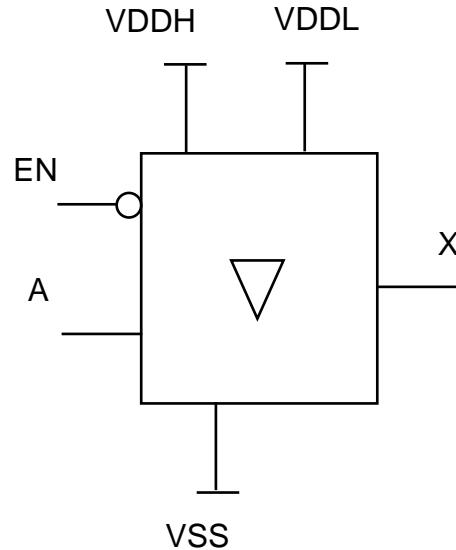


Figure 2.218. Logic Symbol of ELVLDNOR_V2_IY2V1

Table 2.228. ELVLDNOR_V2_IY2V1 Truth Table

A	EN	X
-	1	0
0	0	1
1	-	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
ELVLDNOR_V2_1	1 x Csl	46	0.25	0.003	3.2868	
ELVLDNOR_V2_2	2 x Csl	41	0.33	0.08	3.7308	
ELVLDNOR_V2_3	4 x Csl	39	0.38	0.08	3.3756	
ELVLDNOR_V2_4	8 x Csl	41	0.41	0.08	3.4644	

AN2B_PMM_*

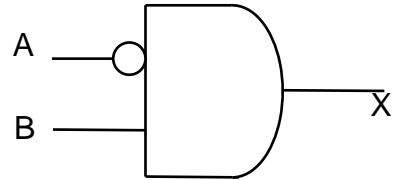


Figure 2.219. Logic Symbol of AN2B_PMM

Table 2.229. AN2B_PMM Truth Table

A	B	X
0	0	0
0	1	1
1	0	0
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AN2B_PMM_2	2 x Csl	33	0.34	0.30	0.4464	
AN2B_PMM_8	8 x Csl	42	0.79	0.30	0.624	

AN2B_PSECO_*

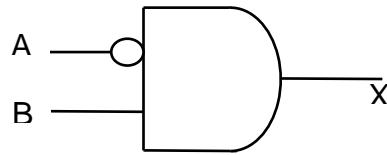


Figure 2.220. Logic Symbol of AN2B_PSECO

Table 2.230. AN2B_PSECO Truth Table

A	B	X
0	0	0
0	1	1
1	0	0
1	1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AN2B_PSECO_1	1 x Csl	40	0.23	0.29	0.7548	
AN2B_PSECO_2	2 x Csl	38	0.3	0.29	0.7548	
AN2B_PSECO_4	4 x Csl	42	0.56	0.49	1.2876	
AN2B_PSECO_8	8 x Csl	46	0.96	0.64	2.0868	

AOLVLUBUF_E0_IY2V1_*

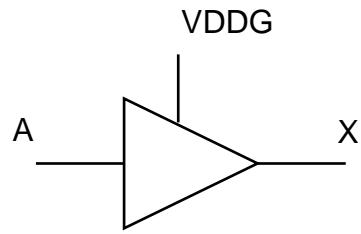


Figure 2.221. Logic Symbol of AOLVLUBUF_E0_IY2V1

Table 2.231. AOLVLUBUF_E0_IY2V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(um ²)	
AOLVLUBUF_E0_IY2V1_1	1 x Csl	52	0.87	0.95	4.3512	
AOLVLUBUF_E0_IY2V1_10	10 x Csl	60	1.98	0.92	5.2395	
AOLVLUBUF_E0_IY2V1_12	12 x Csl	62	2.18	0.92	5.4168	
AOLVLUBUF_E0_IY2V1_2	2 x Csl	54	0.93	0.92	4.3512	
AOLVLUBUF_E0_IY2V1_3	3 x Csl	55	1.04	0.92	4.44	
AOLVLUBUF_E0_IY2V1_4	4 x Csl	56	1.14	0.92	4.5288	
AOLVLUBUF_E0_IY2V1_6	6 x Csl	56	1.41	0.92	4.7952	
AOLVLUBUF_E0_IY2V1_8	8 x Csl	58	1.61	0.92	4.9728	

AOLVLUBUF_E1_IY2V1_*

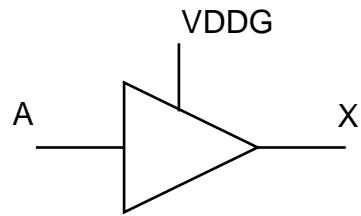


Figure 2.222. Logic Symbol of AOLVLUBUF_E1_IY2V1

Table 2.232. AOLVLUBUF_E1_IY2V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(um ²)	
AOLVLUBUF_E1_IY2V1_1	1 x Csl	51	1.31	1.32	4.3512	
AOLVLUBUF_E1_IY2V1_10	10 x Csl	63	2.3	1.32	5.772	
AOLVLUBUF_E1_IY2V1_12	12 x Csl	66	2.43	1.32	6.1272	
AOLVLUBUF_E1_IY2V1_2	2 x Csl	52	1.38	1.32	4.5288	
AOLVLUBUF_E1_IY2V1_3	3 x Csl	54	1.45	1.32	4.5288	
AOLVLUBUF_E1_IY2V1_4	4 x Csl	54	1.52	1.32	4.5288	
AOLVLUBUF_E1_IY2V1_6	6 x Csl	57	1.86	1.32	4.7952	
AOLVLUBUF_E1_IY2V1_8	8 x Csl	60	1.98	1.32	5.328	

AOLVLUBUF_IY2V1_*

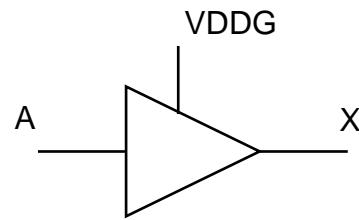


Figure 2.223. Logic Symbol of AOLVLUBUF_IY2V1

Table 2.233. AOLVLUBUF_IY2V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(um ²)	
AOLVLUBUF_IY2V1_1	1 x Csl	40	1.69	1.23	3.9072	
AOLVLUBUF_IY2V1_10	10 x Csl	53	2.7	1.46	5.6832	
AOLVLUBUF_IY2V1_12	12 x Csl	55	2.84	1.48	6.0384	
AOLVLUBUF_IY2V1_2	2 x Csl	46	1.76	1.36	4.0848	
AOLVLUBUF_IY2V1_3	3 x Csl	47	1.83	1.42	4.2624	
AOLVLUBUF_IY2V1_4	4 x Csl	49	1.99	1.44	4.44	
AOLVLUBUF_IY2V1_6	6 x Csl	49	2.33	1.49	4.9728	
AOLVLUBUF_IY2V1_8	8 x Csl	51	2.47	1.53	5.328	

ELVLUNOR_V2_*

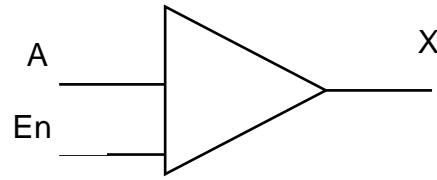


Figure 2.224. Logic Symbol of ELVLUNOR_V2

Table 2.234. ELVLUNOR_V2 Truth Table

A	En	X
0	0	0
0	1	0
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
			Ps	nW		
ELVLUNOR_V2_1	1 x Csl	37	0.5	2.57	3.8196	
ELVLUNOR_V2_2	2 x Csl	40	0.52	1.77	3.8196	
ELVLUNOR_V2_3	3 x Csl	40	0.58	2.25	3.9084	
ELVLUNOR_V2_4	4 x Csl	41	0.59	3.86	3.9972	
ELVLUNOR_V2_6	6 x Csl	40	0.67	2.25	3.9972	
ELVLUNOR_V2_8	8 x Csl	41	0.77	2.17	4.086	
ELVLUNOR_V2_10	10 x Csl	42	0.87	2.21	4.1748	
ELVLUNOR_V2_12	12 x Csl	43	0.97	2.44	4.2636	

AOBUF_IW_*

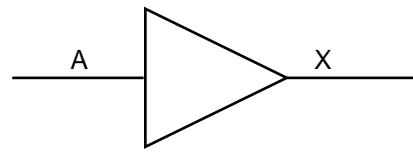


Figure 2.225. Logic Symbol of BUF_IW

Table 2.235. BUF_IW Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
AOBUF_IW_0P75	0.75 x Csl	30	0.13	0.02	0.5286	
AOBUF_IW_3	3 x Csl	32	0.14	0.03	0.5328	
AOBUF_IW_6	6 x Csl	33	0.14	0.03	0.5328	

BUF_PECO_*

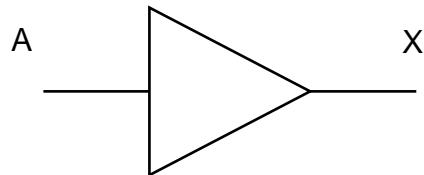


Figure 2.226. Logic Symbol of BUF_PECO

Table 2.236. BUF_PECO Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
BUF_PECO_1	1 x Csl	31	0.143	0.03	0.4884	
BUF_PECO_12	12 x Csl	34	0.43	0.09	0.888	
BUF_PECO_2	2 x Csl	35	0.22	0.04	0.4884	
BUF_PECO_4	4 x Csl	34	0.43	0.09	0.888	
BUF_PECO_8	8 x Csl	34	0.43	0.09	0.888	

BUF_PS_*

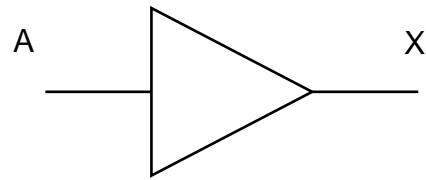


Figure 2.227. Logic Symbol of BUF_PS

Table 2.237. BUF_PS Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
BUF_PS_0P75	0.75 x Csl	30	0.13	0.23	0.3108	
BUF_PS_1P5	1.5 x Csl	31	0.2	0.24	0.3558	
BUF_PS_3	3 x Csl	30	0.4	0.38	0.4434	
BUF_PS_6	6 x Csl	31	0.75	0.61	0.711	

AOINV_IW_*

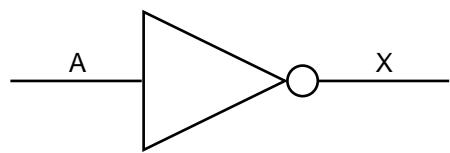


Figure 2.228. Logic Symbol of INV_CW

Table 2.238. INV_CW Truth Table

A	X
0	1
1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		Ps	nW	pW/MHz	(um ²)	
AOINV_IW_0P5	0.5 x Csl	32	0.008	0.004	0.3996	
AOINV_IW_1	1 x Csl	33	0.016	0.0094	0.3996	
AOINV_IW_2	2 x Csl	32	0.03	0.02	0.444	
AOINV_IW_4	4 x Csl	32	0.06	0.04	0.5328	
AOINV_IW_6	6 x Csl	32	0.1	0.062	0.5772	

INV_PECO_*

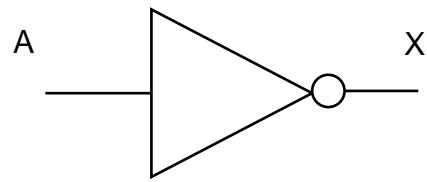


Figure 2.229. Logic Symbol of INV_PECO

Table 2.239. INV_PECO Truth Table

A	X
0	1
1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
INV_PECO_1	1 x Csl	31	0.1	0.02	0.3552	
INV_PECO_12	12 x Csl	31	1.21	0.16	1.6872	
INV_PECO_2	2 x Csl	31	0.2	0.02	0.3552	
INV_PECO_4	4 x Csl	31	0.4	0.05	0.6216	
INV_PECO_8	8 x Csl	31	0.81	0.10	1.1544	

INV_PS_*

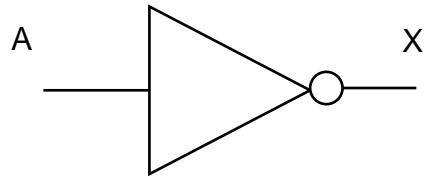


Figure 2.230. Logic Symbol of INV_PS

Table 2.240. INV_PS Truth Table

A	X
0	1
1	0

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area (μm^2)	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
INV_PS_1	1 x Csl	31	0.1	0.07	0.1776	
INV_PS_2	2 x Csl	30	0.2	0.15	0.222	
INV_PS_3	3 x Csl	30	0.3	0.23	0.2664	
INV_PS_6	6 x Csl	30	0.61	0.47	0.3996	

OR2B_PMM_*

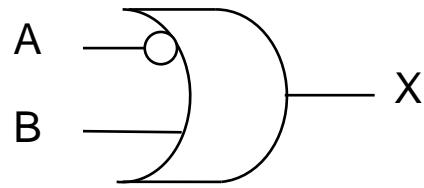


Figure 2.231. Logic Symbol of OR2B_PMM

Table 2.241. OR2B_PMM Truth Table

A	B	X
0	0	1
0	1	1
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OR2B_PMM_2	2 x Csl	37	0.29	0.05	0.4884	
OR2B_PMM_8	8 x Csl	38	1.32	0.14	1.0212	

OR2B_PSECO_*

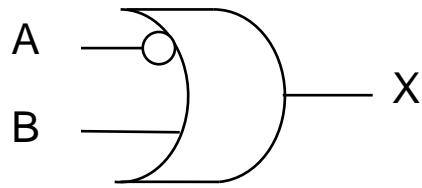


Figure 2.232. Logic Symbol of OR2B_PSECO

Table 2.242. OR2B_PSECO Truth Table

A	B	X
0	0	1
0	1	1
1	0	0
1	1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
OR2B_PSECO_1	1 x Csl	38	0.3	0.29	0.7548	
OR2B_PSECO_2	2 x Csl	38	0.37	0.28	0.7548	
OR2B_PSECO_4	4 x Csl	39	0.66	0.46	1.2876	
OR2B_PSECO_8	8 x Csl	42	1.09	0.60	2.055	

TIE0_PV1ECO

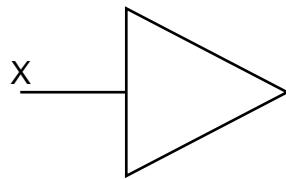
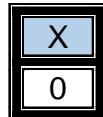


Figure 2.233. Logic Symbol of TIE0_PV1ECO

Table 2.243. TIE0_PV1ECO Truth Table



General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25			Area (μm^2)	
	Cload	Power			
		Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		nW	pW/MHz		
TIE0_PV1ECO_1	1 x Csl	0	1.04	0.222	

TIE1_PV1ECO_*

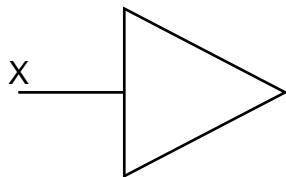
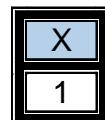


Figure 2.234. Logic Symbol of TIE1_PV1ECO

Table 2.244. TIE1_PV1ECO Truth Table



General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25			Area (μm^2)	
	Cload	Power			
		Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		nW	pW/MHz		
TIE1_PV1ECO_1	1 x Csl	0	1.04	0.222	

TIEDIN_PV1ECO_*

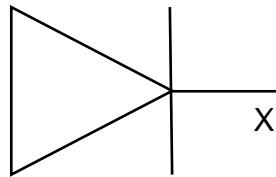


Figure 2.235. Logic Symbol of TIE1_PV1ECO

Table 2.245. TIE1_PV1ECO Truth Table

No Truth Table for the cell(s)

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25			Area (μm^2)	
	Cload	Power			
		Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		nW	pW/MHz		
TIEDIN_PV1ECO_6	6 x Csl	0	1.04	0.3552	

DCAP_PV1ECO_*

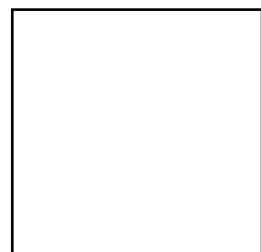


Figure 2.236. Logic Symbol of DCAP_PV1ECO

Table 2.246. DCAP_PV1ECO Truth Table

No Truth Table for the cell(s)

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25			Area (um ²)	
	Cload	Power			
		Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		nW	pW/MHz		
DCAP_PV1ECO_12	12 x Csl	0.13	1.04	0.6216	
DCAP_PV1ECO_15	15 x Csl	0.17	1.04	0.7548	
DCAP_PV1ECO_18	18 x Csl	0.2	1.04	0.9324	
DCAP_PV1ECO_6	6 x Csl	0.07	1.04	0.3996	
DCAP_PV1ECO_9	9 x Csl	0.11	1.04	0.4884	

DCAP_PV3_*

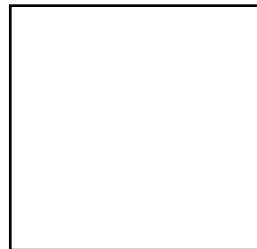


Figure 2.237. Logic Symbol of DCAP_PV1ECO

Table 2.247. DCAP_PV3 Truth Table

No Truth Table for the cell(s)

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25			Area (um ²)	
	Cload	Power			
		Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
		nW	pW/MHz		
DCAP_PV3_3	3 x Csl	0	1.04	0.3552	

LVLUBUFE0_IY2

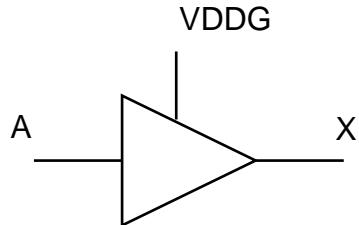


Figure 2.238. Logic Symbol of LVLUBUFE0_IY2

Table 2.248. LVLUBUFE0_IY2 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25					Area	
	Cload	Prop Delay (Avg)	Power				
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic			
		Ps	nW	pW/MHz	(um ²)		
LVLUBUFE0_IY2_1	1 x Csl	49	0.83	0.95	4.3512		
LVLUBUFE0_IY2_2	2 x Csl	45	0.93	0.95	4.2624		
LVLUBUFE0_IY2_3	3 x Csl	51	1.03	0.95	4.44		
LVLUBUFE0_IY2_4	4 x Csl	54	1.15	0.95	4.44		
LVLUBUFE0_IY2_6	6 x Csl	55	1.15	0.95	4.7952		
LVLUBUFE0_IY2_8	8 x Csl	57	1.61	0.95	4.9728		
LVLUBUFE0_IY2_10	10 x Csl	58	1.91	0.95	5.2392		
LVLUBUFE0_IY2_12	12x Csl	61	2.11	0.95	5.4168		

LVLUBUF4E0_IY2_2

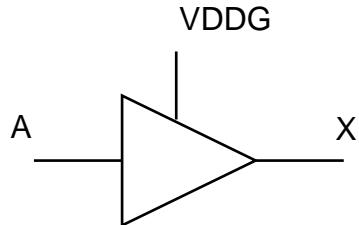


Figure 2.239. Logic Symbol of LVLUBUF4E0_IY2_2

Table 2.249. LVLUBUF4E0_IY2_2 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
LVLUBUF4E0_IY2_2	2 x Csl	50	1.78	0.89		
LVLUBUF4E0_IY2_4	4 x Csl	45	2.02	0.89		
LVLUBUF4E0_IY2_8	8 x Csl	58	2.82	0.89		

LVLDBUFE0_IY2_V1_*

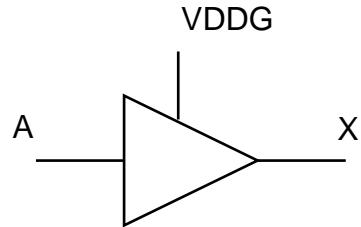


Figure 2.240. Logic Symbol of LVLDBUFE0_IY2_V1

Table 2.250. LVLDBUFE0_IY2_V1 Truth Table

A	X
0	0
1	1

General Information

Cell Name	TT SPICE model, VDD=0.8V, Temperature=25				Area	
	Cload	Prop Delay (Avg)	Power			
			Leakage (VDD=0.8 V DC, Temp=25 Dec.C)	Dynamic		
	Ps	nW	pW/MHz	(um ²)		
LVLDBUFE0_IY2_V1_1	1 x Csl	52	0.42	0.95	4.3512	
LVLDBUFE0_IY2_V1_2	2 x Csl	52	0.46	0.95	4.3512	
LVLDBUFE0_IY2_V1_3	3 x Csl	53	0.51	0.95	4.44	
LVLDBUFE0_IY2_V1_4	4 x Csl	54	0.56	0.95	4.5288	
LVLDBUFE0_IY2_V1_6	6 x Csl	54	0.64	0.95	4.7952	
LVLDBUFE0_IY2_V1_8	8 x Csl	56	0.73	0.95	4.9728	
LVLDBUFE0_IY2_V1_10	10 x Csl	58	0.88	0.95	5.2392	
LVLDBUFE0_IY2_V1_12	12x Csl	60	0.96	0.95	5.4168	

3. I/O Standard Cell Library SAED_EDK14_FINFET_IO_STD

3.1. General Information

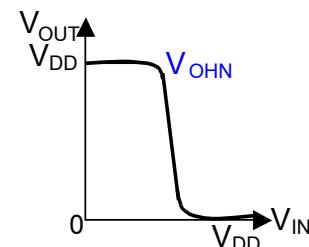
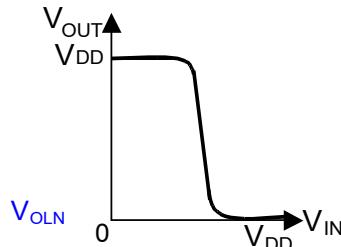
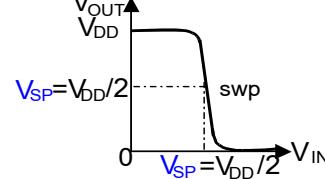
The used symbols of logic elements' states in the specification of SAED_EDK14_FINFET_IO_STD Standard I/O Library are shown in Table 3.1.

Table 3.1. Symbols of logic elements' states

Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIGH Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

DC parameters and measurement conditions of the elements included in SAED_EDK14_FINFET_IO_STD standard I/O library are shown in Table 3.2.

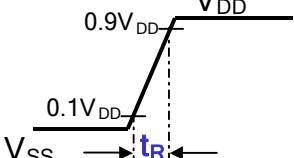
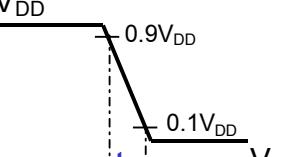
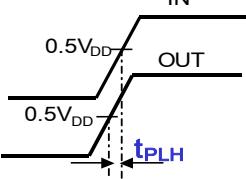
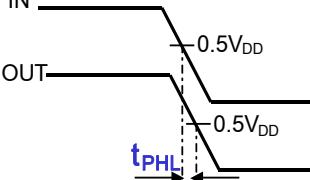
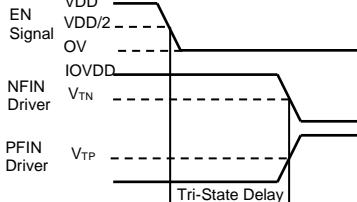
Table 3.2. DC Parameters and measurement conditions of I/O cells

No	Parameter	Unit	Symbol	Figure	Definition
1	Output high level voltage (nominal)	V	V_{OHN}		Output high voltage at nominal condition, usually equals to V_{DD} for input buffer and $(0.8 \div 1.0) \cdot IOVDD$ for output buffer (current equal to drive strength sink/sourced from output buffer)
2	Output low level voltage (nominal)	V	V_{OLN}		Output low voltage at nominal condition, usually $V_{OLN}=0$ for input buffer and $(VSSIO \div 0.2 \cdot IOVDD)$ for output buffer (current equal to drive strength sink/sourced from output buffer)
3	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT} = IOVDD/2$ ($VDD/2$)
4	Static leakage current	uA	I_{LEAKH}	None	The current consumed when the output is high

No	Parameter	Unit	Symbol	Figure	Definition
	consumption at output on high state	uA	I_{LEAKL}	None	The current consumed when the output is low
5	Leakage power consumption (dissipation) at output	pW	$P_{LEAKH} = V_{DD} \times I_{LEAKH}$	None	The power consumed when the output is high
		pW	$P_{LEAKL} = V_{DD} \times I_{LEAKL}$	None	The power consumed when the output is low

AC parameters and measurement conditions of the elements included in SAED_EDK14_FINFET_IO_STD standard I/O library are shown in Table 3.3.

Table 3.3. AC Parameters and measurement conditions of I/O cells

No	Parameter	Unit	Symbol	Figure	Definition
1.	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from kV_{DD} to $(1-k)V_{DD}$ value. Usually $k=0.1$ (also possible $k=0.2, 0.3, \text{etc}$)
2.	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to kV_{DD} value. Usually $k=0.1$ (also possible $k=0.2, 0.3, \text{etc}$)
3.	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4.	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low
5.	Average supply current	uA	$I_{V_{DD}AVG} = \frac{1}{T} \int_0^T I_{V_{DD}}(t) dt$	None	The power supply current average value for a period (T)
6.	Z-state entry time, (only for tri-state output cells) delay	ns	t_{HZ}		The amount of time that takes the output to change from high to Z-state after control signal is applied

No	Parameter	Unit	Symbol	Figure	Definition
7.	Enable time, (only for tri-state output cells) delay	ns	TZH		The amount of time that takes the output to change from Z-state to active after control signal is applied

3.1.1. ESD Protection

Special structures should be included in the I/O cells to protect against electrostatic discharge (ESD) for guaranteed minimum 2KV human-body model (HBM), 300V machine model (MM), and 400V and latch-up of up to 100mA (Figure 4.1).

3.1.2. Latch-Up Protection

Provision of rules of Latch-Up protection is anticipated.

3.1.3. CLAMP circuit

NFIN Clamp circuit will be utilized on all power supply buses and will be included in the Power and Ground pads to minimize the voltage spike present at the gates of internal circuits and to alleviate some of the current stress on the ESD/latch-up structures (figure 4.1).

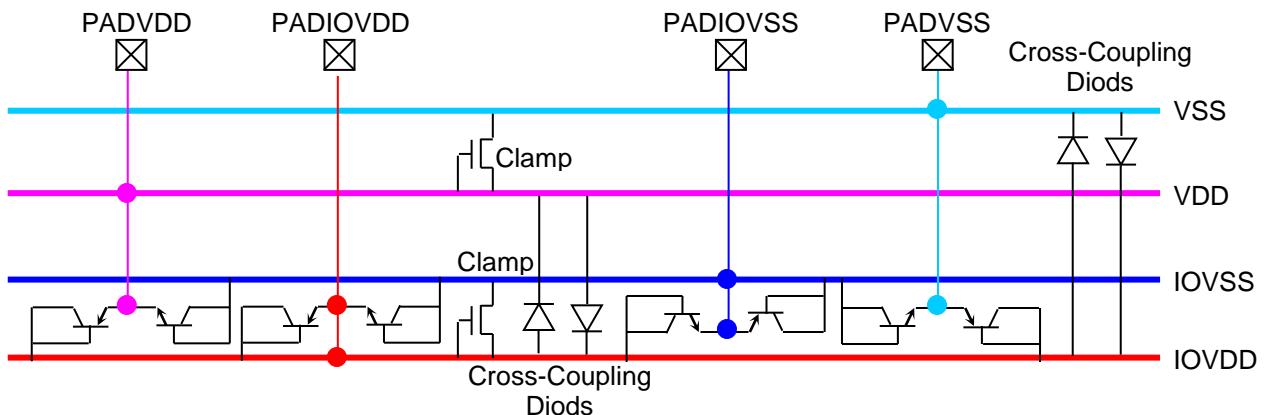


Figure 3.1. Implementation of ESD current paths

3.1.4. Decoupling capacitors

Decoupling capacitors should be built wherever possible, thus assuring a minimum decoupling capacitance on the die.

3.2. Operating conditions

SAED_EDK14_FINFET_IO_STD Standard I/O Library specification is given for 0.8V/1.5V/1.8V operation. The process technology will be SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V.

The operating conditions of SAED_EDK14_FINFET_IO_STD Standard I/O Library are shown in Table 3.4.

Table 3.4. Operating conditions

Parameter	Min	Typ	Max	Unit
Core Supply (VDD) voltage	0.72	0.8	0.88	V
I/O Supply (IOVDD) voltage	1.62	1.8	1.98	V
Operating temperature	-40	25	125	°C
Operating Frequency (F)	-	-	1	1GHz

3.3. AC Characteristics

3.3.1. Characterization corners

Composite Current Source (CCS) modeling technology will be applied for characterization to meet the contemporary methods of low power design. The application of that technology will support timing, noise, and power analyses simultaneously with consideration of the relevant nanometer dependencies. It will allow meeting the requirements of variation-aware analysis. The characterization results will be given for process/voltage/temperature (PVT) conditions shown in Table 3.5.

Table 3.5. Characterization corners

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Core Power Supply VDD (V)	I/O Power Supply IOVDD (V)	Library Name Suffix
FF	Fast – Fast	125	0.88	1.98	ff0p88v125c_1p98v
FF	Fast – Fast	25	0.88	1.98	ff0p88v25c_1p98v
FF	Fast – Fast	-40	0.88	1.98	ff0p88vm40c_1p98v
SS	Slow-Slow	125	0.72	1.62	ss0p72v125c_1p62v
SS	Slow-Slow	25	0.72	1.62	ss0p72v25c_1p62v
SS	Slow-Slow	-40	0.72	1.62	ss0p72vm40c_1p62v
TT	Typical – Typical	125	0.8	1.8	ss0p8v125c_1p8v
TT	Typical – Typical	25	0.8	1.8	ss0p8v25c_1p8v
TT	Typical – Typical	-40	0.8	1.8	ss0p8vm40c_1p8v

3.3.2. The values of Output Load and Input slope

Characterization should be realized for 8 different values of Output Load and 6 different values of Input slope shown in Table 3.6.

Table 3.6. The values to be used for characterization

Parameter	Value							
Core loading capacitance (pF)	0.0	0.2	0.4	0.6	0.8	1.0	1.2	1.4
PAD loading capacitance (pF)	0	5	10	15	20	25	30	35
Input signal slope (ns)	0.4	1.2	2.0	2.4	2.8	3.0	-	-

3.4. I/O Standard Cells List

To have the mentioned reliabilities and to have the complete set of standard functionality the presented cell list is required. SAED_EDK14_FINFETIO library will contain 42 cells in total, the list of which is shown in Table 3.7.. All the cells will be available in both wire-bond and flip-chip version, all cells will have EW (East-West) and NS(North-South) types, and 4 additional cells (numbers 43-46) will be present in the library for specific purposes.

Table 3.7. I/O Standard Cells List

Item#	Description	Cell name
	Digital pads	
1.	FINFET non-inverting input buffer (on chip load -0.5pf)	I1025EW
2.	FINFET non-inverting Schmitt trigger input buffer (on chip load -0.5pf)	ISH1025EW
3.	FINFET non-inverting Bi-directional cell, 4 mA Tri-State driver with pull-up and pull-down (off chip load-5pf, on chip load -0.5pF)	B4I1025EW
4.	FINFET non-inverting Bi-directional cell, 8 mA Tri-State driver with pull-up and pull-down (off chip load-5pf, on chip load -0.5pF)	B8I1025EW
5.	FINFET non-inverting Bi-directional cell, 12 mA Tri-State driver with pull-up and pull-down (off chip load-10pf, on chip load -0.5pF)	B12I1025EW
6.	FINFET non-inverting Bi-directional cell, 16 mA Tri-State driver with pull-up and pull-down (off chip load-10pf, on chip load -0.5pF)	B16I1025EW
7.	FINFET non-inverting Bi-directional cell, 4 mA Tri-State driver with pull-up and pull-down , and Schmitt triggered input buffer (off chip load-5pf, on chip load – 0.5pF)	B4ISH1025EW
8.	FINFET non-inverting Bi-directional cell, 8 mA Tri-State driver with pull-up and pull-down, and Schmitt triggered input buffer (off chip load-5pf, on chip load – 0.5pF)	B8ISH1025EW
9.	FINFET non-inverting Bi-directional cell, 12 mA Tri-State driver with pull-up and pull-down, and Schmitt triggered input buffer (off chip load-10pf, on chip load – 0.5pF)	B12ISH1025EW
10.	FINFET non-inverting Bi-directional cell, 16 mA Tri-State driver with pull-up and pull-down, and Schmitt triggered input buffer (off chip load-10pf, on chip load – 0.5pF)	B16ISH1025EW
11.	FINFET non-inverting Driver, 4 mA Tri-State, without pull-up and pull-down (off chip load-5pf, on chip load – 0.5pF)	D4I1025EW
12.	FINFET non-inverting Driver, 8 mA Tri-State, without pull-up and pull-down (off chip load-5pf, on chip load – 0.5pF)	D8I1025EW
13.	FINFET non-inverting Driver, 12 mA Tri-State, without pull-up and pull-down (off chip load-10pf, on chip load – 0.5pF)	D12I1025EW
14.	FINFET non-inverting Driver, 16 mA Tri-State , without pull-up and pull-down (off chip load-10pf, on chip load – 0.5pF)	D16I1025EW
15.	FINFET non-inverting input buffer (on chip load -0.5pf)	I1025NS
16.	FINFET non-inverting Schmitt trigger input buffer (on chip load -0.5pf)	ISH1025NS
17.	FINFET non-inverting Bi-directional cell, 4 mA Tri-State driver with pull-up and pull-down (off chip load-5pf, on chip load -0.5pF)	B4I1025NS
18.	FINFET non-inverting Bi-directional cell, 8 mA Tri-State driver with pull-up and pull-down (off chip load-5pf, on chip load -0.5pF)	B8I1025NS
19.	FINFET non-inverting Bi-directional cell, 12 mA Tri-State driver with pull-up and pull-down (off chip load-10pf, on chip load -0.5pF)	B12I1025NS

20.	FINFET non-inverting Bi-directional cell, 16 mA Tri-State driver with pull-up and pull-down (off chip load-10pf, on chip load -0.5pF)	B16I1025NS
21.	FINFET non-inverting Bi-directional cell, 4 mA Tri-State driver with pull-up and pull-down , and Schmitt triggered input buffer (off chip load-5pf,	B4ISH1025NS
22.	FINFET non-inverting Bi-directional cell, 8 mA Tri-State driver with pull-up and pull-down, and Schmitt triggered input buffer (off chip load-5pf, on	B8ISH1025NS
23.	FINFET non-inverting Bi-directional cell, 12 mA Tri-State driver with pull-up and pull-down, and Schmitt triggered input buffer (off chip load-10pf,	B12ISH1025NS
24.	FINFET non-inverting Bi-directional cell, 16 mA Tri-State driver with pull-up and pull-down, and Schmitt triggered input buffer (off chip load-10pf,	B16ISH1025NS
25.	FINFET non-inverting Driver, 4 mA Tri-State, without pull-up and pull-down (off chip load-5pf, on chip load – 0.5pF)	D4I1025NS
26.	FINFET non-inverting Driver, 8 mA Tri-State, without pull-up and pull-down (off chip load-5pf, on chip load – 0.5pF)	D8I1025NS
27.	FINFET non-inverting Driver, 12 mA Tri-State, without pull-up and pull-down (off chip load-10pf, on chip load – 0.5pF)	D12I1025NS
28.	FINFET non-inverting Driver, 16 mA Tri-State , without pull-up and pull-down (off chip load-10pf, on chip load – 0.5pF)	D16I1025NS
Analog pads		
29.	Analog, non-inverting Bi-directional without resistor pad (R=0.3Ohm) with ESD protection (0.8V,1.8V, 60mA)	A1825EW
30.	Analog, non-inverting Bi-directional with R=200Ohm resistor, ESD protection(0.8V,1.8V, 60mA)	AR1825EW
31.	Analog, non-inverting Bi-directional without resistor pad (R=0.3Ohm) with ESD protection (0.8V,1.8V, 60mA)	A1825NS
32.	Analog, non-inverting Bi-directional with R=200Ohm resistor, ESD protection(0.8V,1.8V, 60mA)	AR1825NS
Power/Ground pads		
33.	Core power pad (VDD=0.8V, 40mA)	VDD
34.	I/O power pad (VDDIO=1.8V, 40mA)	IOVDD
35.	Analog power pad(AVDD=1.8V,40mA)	AVDD
36.	Core ground pad (VSS=0V, 40mA)	VSS
37.	I/O ground pad (VSSIO=0V, 40mA)	IOVSS
38.	Analog ground pad(AVSS=0V)	AVSS
39.	Core power pad (VDD=0.8V, 40mA)	VDD
40.	I/O power pad (VDDIO=1.8V, 40mA)	IOVDD
41.	Analog power pad(AVDD=1.8V,40mA)	AVDD
42.	Core ground pad (VSS=0V, 40mA)	VSS
43.	I/O ground pad (VSSIO=0V, 40mA)	IOVSS
44.	Analog ground pad(AVSS=0V)	AVSS
Miscellaneous Cells		
45.	Cross-coupling diode, VSSIO to VSS	DIOVSSVSS
46.	Break cell (Only VDDIO and VSSIO buses are present)	BREAKCORE
47.	Break cell (Only VDD and VSS buses are present)	BREAKIO
48.	Corner pad	CORNER
49.	Filler cell (Width/Height – 39um/180um)	FILLER
50.	Filler cell (Width/Height- 0.01um/180um)	FILLER01
51.	Filler cell (Width/Height – 1um/180um)	FILLER1
52.	Filler cell (Width/Height – 3um/180um)	FILLER5
Pad cells		
53.	Bonding Pad (Wire-Bond only)	BONDPAD

NOTE: Wherever possible, decoupling capacitors should be added.

3.5. Standard I/O Library Deliverables

Table 3.8. Standard I/O Library deliverables

N	Type	Description
1	.pdf	Databook / User guide
2	.db, .lib	Synthesis models
3	.v	Verilog simulation models
4	.cdl, .sp	LVS, HSPICE netlists
5	.spf	Extracted C and RC netlists for different corners
6	.gds	GDSII layout views
7	.clf	Cell antenna information
8	.lef	LEF files
9	.FRAM, .CEL	FRAM views, layout views

3.6. Introduction

The SAED_EDK14_FINFET_IO_STD Standard Cell Library will be built using SAED14nm_FinFET 1P9M 0.8V/1.5V/1.8V design rules. The library will include typical I/O cells which are necessary for integrated circuits design for educational purposes. Compiling the cell list has been based on the analysis of different educational designs. Both wire-bond and flip-chip versions of cells in SAED_EDK14_FINFET_IO_STD Standard Cell Library will be designed.

3.7. Physical Structure of I/O Cell

3.7.1. Physical Structure of Flip-Chip I/O Cell

All cells should fit into 32umx240um size and the buses should be implemented as presented in figure 4.2. The power rails should be selected on the basis of acceptable current density given by the design rules and acceptable current density given by the design rules and electromigration. Pad is placed over cell so buses contain metals up to M9 and BUMP is implemented by redistribution layer.

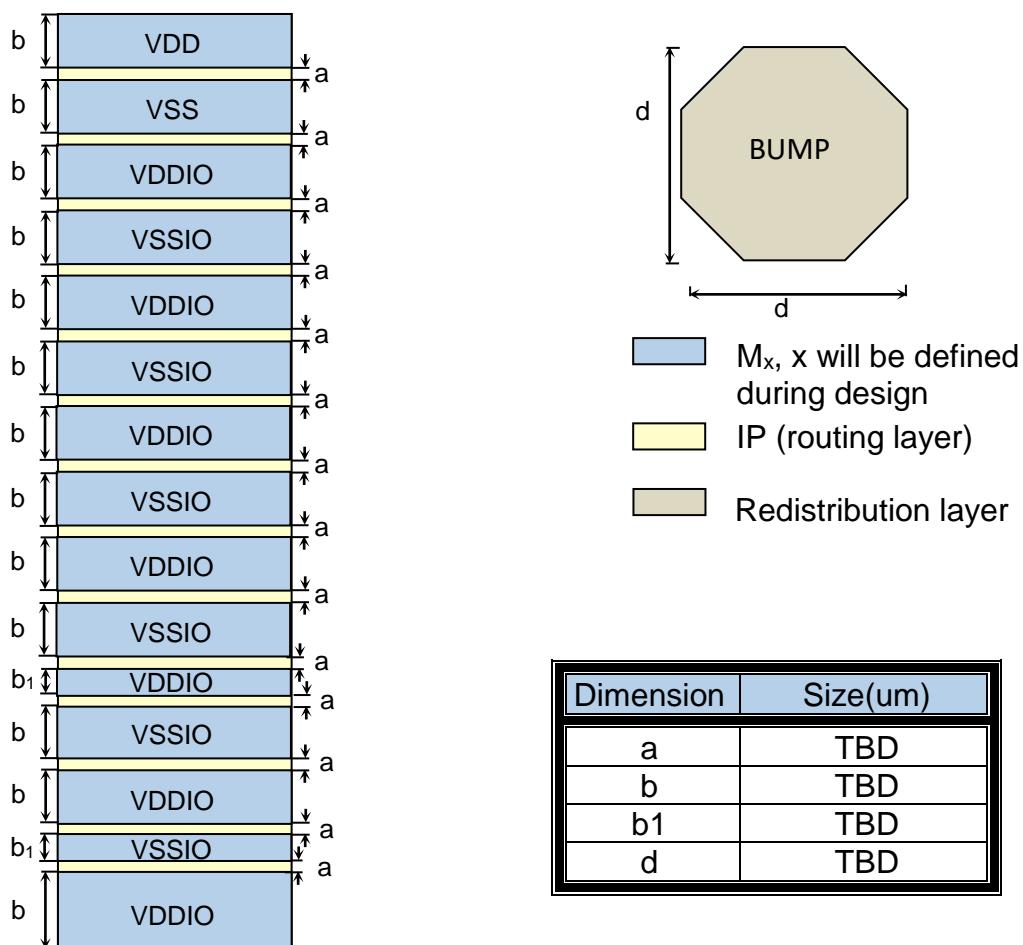


Figure 3.2. Physical structure of flip-chip I/O cell

3.7.2. Physical Structure of Wire-Bond I/O Cell

All cells should fit into 32umx240um size and the buses should be implemented as presented in figure 5.3. The power rails will be selected on the basis of acceptable current density given by the design rules and acceptable current density given by the design rules and electromigration.

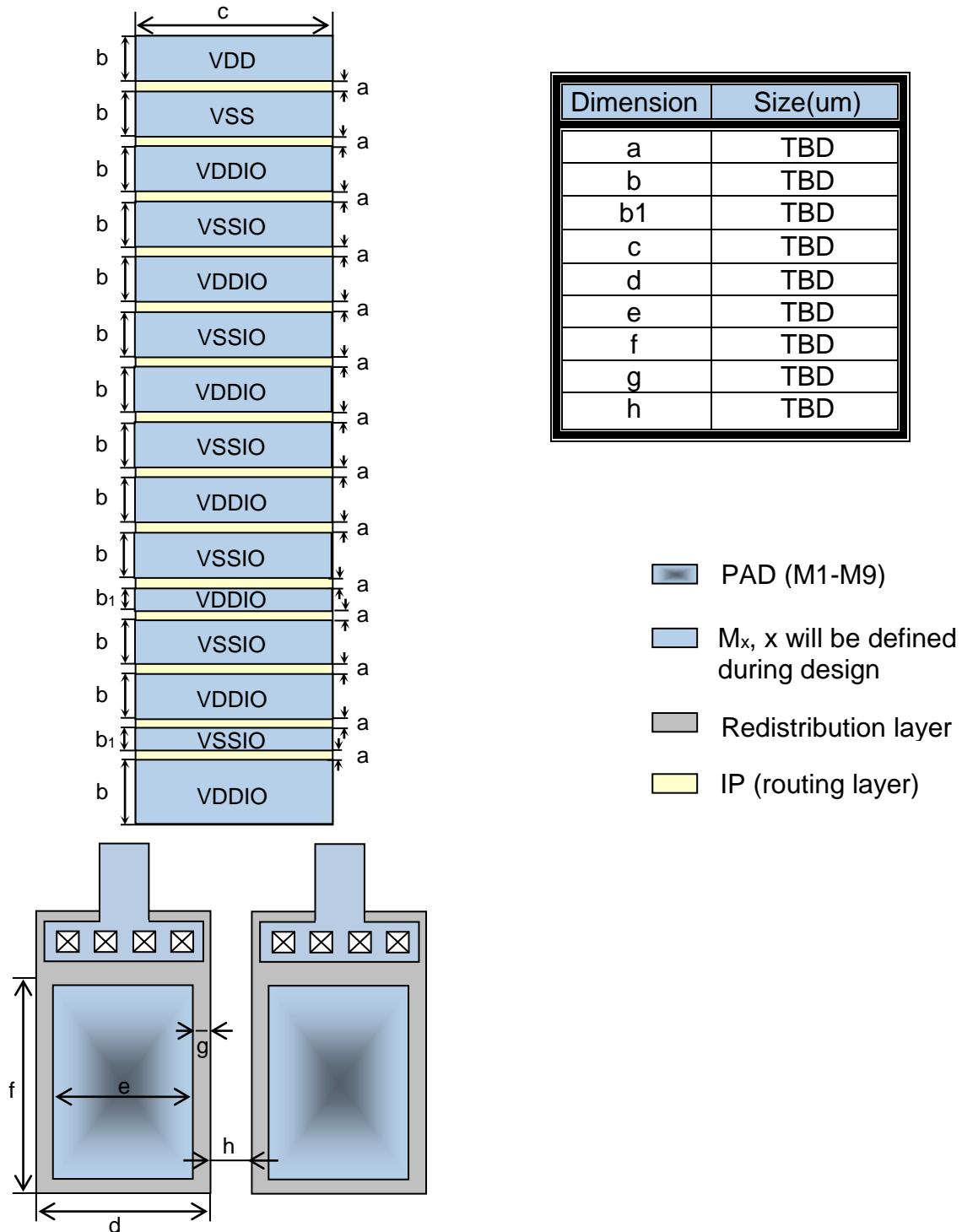


Figure 3.3. Physical structure of wire-bond I/O cell

3.7.3. Standard I/O Cell's Description

FinFet non-inverting input buffer (on chip load -0.5pf): I1025EW,I1025NS

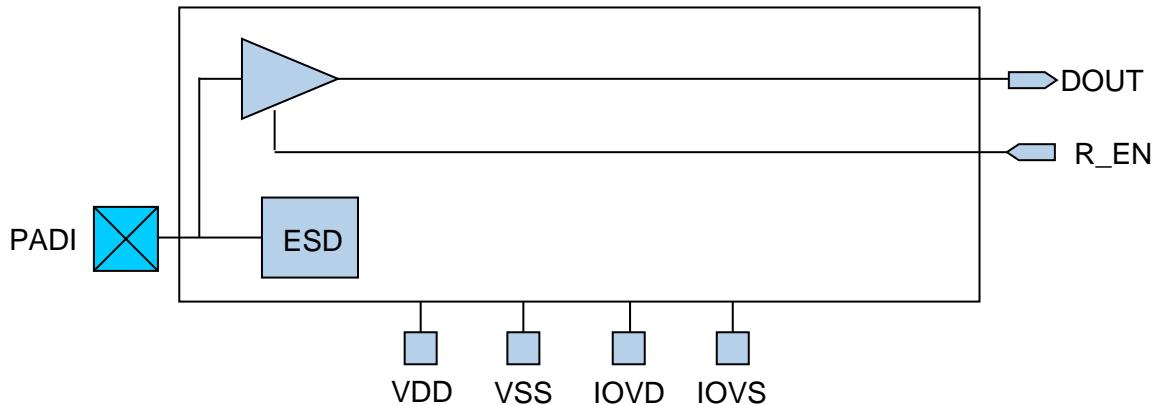


Figure 3.4. I1025x cell block diagram

Table 3.9. I1025x Truth Table

Input		Output
PADIO	R_E	DOUT
1	1	1
0	1	0
Z	0	0
0	0	0
1	0	0

Table 3.10. I1025x Timing and Dynamic Current consumption Data

IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 0.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			0.64	ns
High to Low prop Delay	T _{PUL}			0.64	ns
Output Rise time	T _{RISE}			0.12	ns
Output Fall time	T _{FALL}			0.12	ns
Current consumption on IOVDD	I _{DIOVDD}			75	uA
Current consumption on VDD	I _{DVDD}			115	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

FinFet non-inverting Schmitt trigger input buffer (on chip load -0.5pf):
ISH1025EW,ISH1025NS

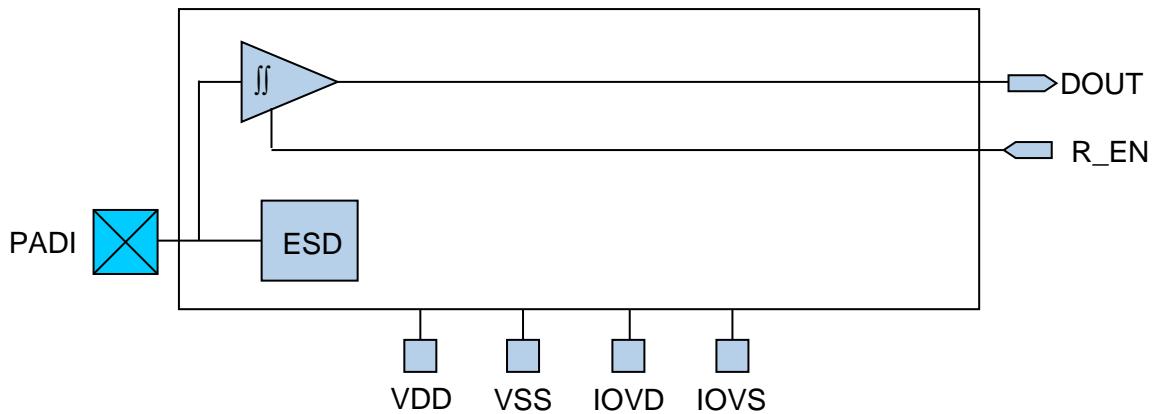


Figure 3.5. ISH1025x cell block diagram

Table 3.11. ISH1025x Truth Table

Input		Output
PADIO	R_E	DOUT
1	1	1
0	1	0
Z	0	0
0	0	0
1	0	0

Table 3.12. ISH1025x Timing and Dynamic Current consumption Data
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 0.5pF

	Symbol	TT	FF	Max	Units
Low to High prop Delay	T _{PLH}	0.27	0.17	0.64	Ns
High to Low prop Delay	T _{PUL}	0.24	0.17	0.64	Ns
Output Rise time	T _{RISE}			0.12	Ns
Output Fall time	T _{FALL}			0.12	Ns
Current consumption on IOVDD	I _{DIOVDD}			75	uA
Current consumption on VDD	I _{DVDD}			115	uA
High switch threshold voltage	V _{SWIH}			0.6	V
Low switch threshold voltage	V _{SWIL}	0.6			V
Hysteresis value	V _{HYST}	150		150	mV
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

FinFet non-inverting Bi-directional cell: B4I1025EW, B4I1025NS, B8I1025EW, B8I1025NS, B12I1025EW, B12I1025NS, B16I1025EW, B16I1025NS

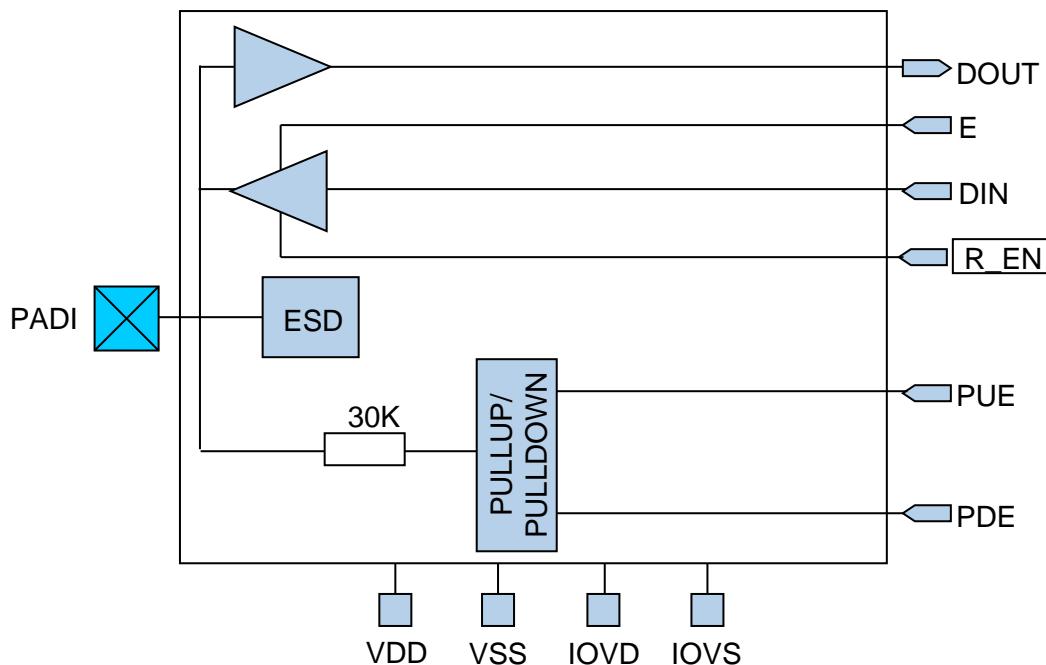


Figure 3.6. Bi-directional cells block diagram

Table 3.13. BxI1025x Truth Table – Tx Mode

Input		Output
E	DIN	PADIO
1	1	1
1	0	0
0	X	z
X	X	z

Table 3.14. BxI1025x Truth Table – Rx Mode

Input		Output
PADIO	R_EN	DOUT
1	1	1
0	1	0
z	0	0
0	0	0
1	0	0

Table 3.15. BxI1025x Truth Table – Pullup/Pulldown

Input		Output
PDE	PUE	PADIO
0	0	Pull up/down resistors are not connected
1	0	Connected to IOVSS via the resistor
0	1	Connected to IOVDD via the resistor
1	1	Pull up/down resistors are not connected

Table 3.16. B2I1025x Timing and Dynamic Current consumption Data (TX – 2mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 2.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PUL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on IOVDD	IDIOVDD			1.0	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.17. B4I1025x Timing and Dynamic Current consumption Data (TX – 4mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PUL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on IOVDD	IDIOVDD			2	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.18. B8I1025x Timing and Dynamic Current consumption Data (TX – 8mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 7.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PUL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on IOVDD	IDIOVDD			3.5	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.19. B12I1025x Timing and Dynamic Current consumption Data (TX – 12mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 10pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PUL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on IOVDD	IDIOVDD			5	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.20. B16I1025x Timing and Dynamic Current consumption Data (TX – 16mA)
 IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 10pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PUL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on IOVDD	ID_{IOVDD}			6.5	mA
Current consumption on VDD	ID_{VDD}			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.21. BxI1025x Timing and Dynamic Current consumption Data (RX)
 IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 0.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			0.64	ns
High to Low prop Delay	T_{PUL}			0.64	ns
Output Rise time	T_{RISE}			0.12	ns
Output Fall time	T_{FALL}			0.12	ns
Current consumption on IOVDD	ID_{IOVDD}			75	uA
Current consumption on VDD	ID_{VDD}			115	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

FINFET non-inverting Bi-directional cell: B4ISH1025EW, B4ISH1025NS, B8ISH1025EW, B8ISH1025NS, B12ISH1025EW, B12ISH1025NS, B16ISH1025EW, B16ISH1025NS

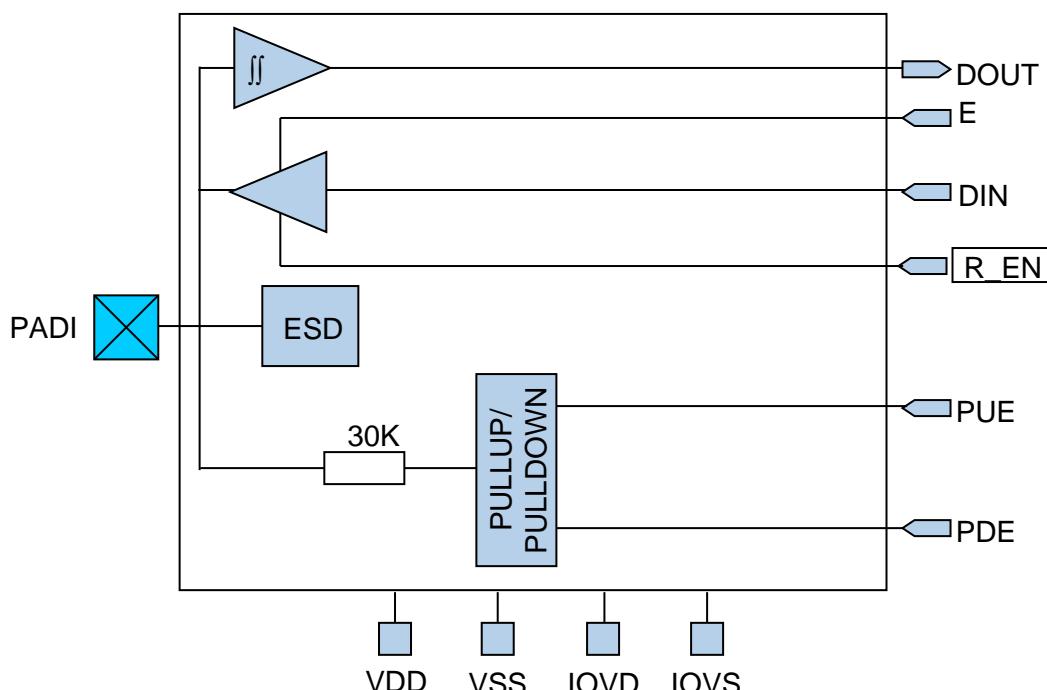


Figure 3.7. Bi-directional cells block diagram

Table 3.22. BxISH1025x Logic Truth Table – Tx Mode

Input		Output
E	DIN	PADIO
1	1	1
1	0	0
0	X	Z
X	X	Z

Table 3.23. BxISH1025x Logic Truth Table – Rx Mode

Input		Output
PADIO	R_EN	DOUT
1	1	1
0	1	0
Z	0	0
0	0	0
1	0	0

Table 3.24. BxISH1025x Pullup/Pulldown Truth Table

Input		Output
PDE	PUE	PADIO
0	0	Pull up/down resistors are not connected
1	0	Connected to IOVSS via the resistor
0	1	Connected to IOVDD via the resistor
1	1	Pull up/down resistors are not connected

Table 3.25. B2ISH1025x Timing and Dynamic Current consumption Data (TX – 2mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 2.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			2.25	ns
High to Low prop Delay	T _{PUL}			2.25	ns
Output Rise time	T _{RISE}			1	ns
Output Fall time	T _{FALL}			1	ns
Minimal Sink/Source current	ISS			0.7	mA
Current consumption on IOVDD	IDIOVDD			1.0	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.26. B4ISH1025x Timing and Dynamic Current consumption Data (TX – 4mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns;cload – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			1.7	ns
High to Low prop Delay	T _{PUL}			1.7	ns
Output Rise time	T _{RISE}			0.8	ns
Output Fall time	T _{FALL}			0.8	ns
Minimal Sink/Source current	ISS			1.5	mA
Current consumption on IOVDD	IDIOVDD			2	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.27. B8ISH1025x Timing and Dynamic Current consumption Data (TX – 8mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			1.7	ns
High to Low prop Delay	T _{PUL}			1.7	ns
Output Rise time	T _{RISE}			0.8	ns
Output Fall time	T _{FALL}			0.8	ns
Minimal Sink/Source current	ISS			3	mA
Current consumption on IOVDD	IDIOVDD			3.5	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.28. B12ISH1025x Timing and Dynamic Current consumption Data (TX – 12mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns;cload – 10pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			1.7	ns
High to Low prop Delay	T _{PUL}			1.7	ns
Output Rise time	T _{RISE}			0.8	ns
Output Fall time	T _{FALL}			0.8	ns
Minimal Sink/Source current	ISS			4	mA
Current consumption on IOVDD	IDIOVDD			5	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.29. B16ISH1025x Timing and Dynamic Current consumption Data (TX – 16mA)
 IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 10pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PUL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Minimal Sink/Source current	ISS			6	mA
Current consumption on IOVDD	$IDIOVDD$			7	mA
Current consumption on VDD	$IDVDD$			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.30. BxISH1025x Timing and Dynamic Current consumption Data (RX)
 IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 0.5pF

	Symbol	TT	FF	Max	Units
Low to High prop Delay	T_{PLH}	0.27	0.17	0.64	ns
High to Low prop Delay	T_{PUL}	0.24	0.17	0.64	ns
Output Rise time	T_{RISE}			0.12	ns
Output Fall time	T_{FALL}			0.12	ns
Current consumption on IOVDD	$IDIOVDD$			75	uA
Current consumption on VDD	$IDVDD$			115	uA
High switch threshold voltage	V_{SWIH}			0.6	V
Low switch threshold voltage	V_{SWIL}	0.6			V
Hysteresis value	V_{HYST}	150		150	mV
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

FINFET non-inverting Driver cell: D4I1025EW, D4I1025NS, D8I1025EW,
 D8I1025NS,D12I1025EW, D12I1025NS, D16I1025EW, D16I1025NS

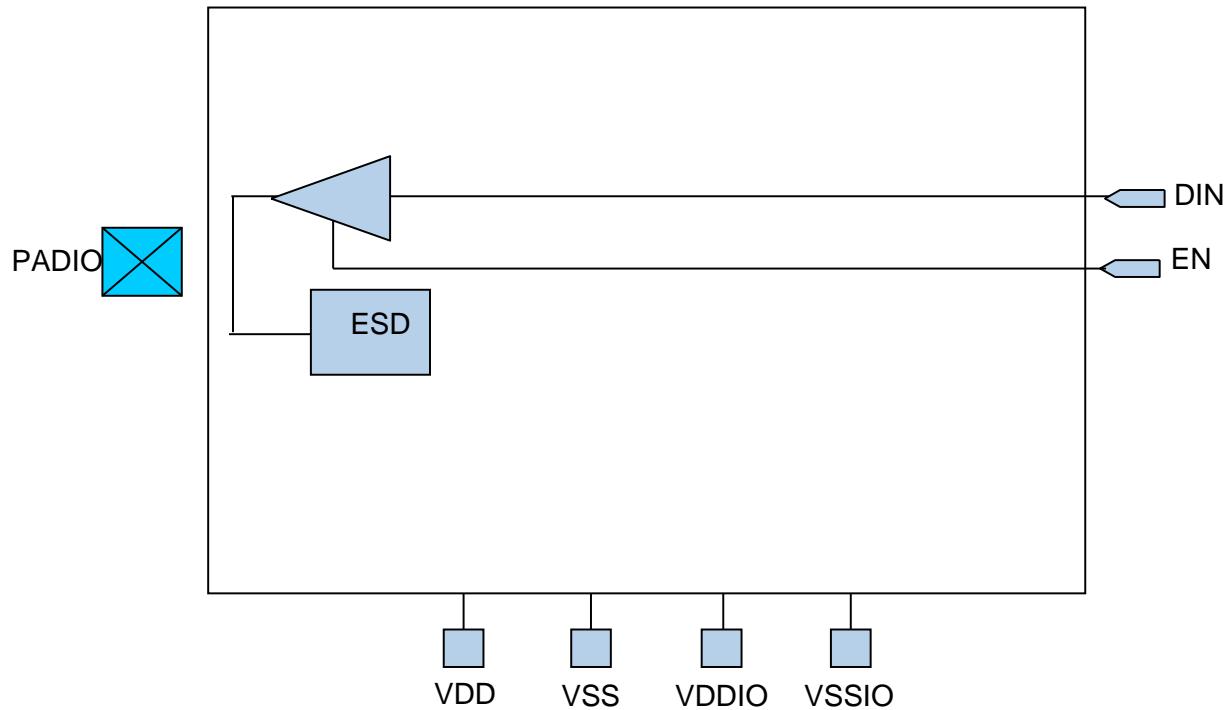


Figure 3.8. Driver cells block diagram

Table 3.31. DxI1025x Truth Table – Tx Mode

Input		Output
EN	DIN	PADIO
1	1	1
1	0	0
0	X	z
X	X	z

Table 3.32. D2I1025x Timing and Dynamic Current consumption Data (TX – 2mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 2.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PHL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on VDDIO	ID_{VDDIO}			1.0	mA
Current consumption on VDD	ID_{VDD}			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 3.33. D4I1025x Timing and Dynamic Current consumption Data (TX – 4mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			1.7	ns
High to Low prop Delay	T _{PHL}			1.7	ns
Output Rise time	T _{RISE}			0.8	ns
Output Fall time	T _{FALL}			0.8	ns
Current consumption on VDDIO	IDVDDIO			2	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.34. D8I1025x Timing and Dynamic Current consumption Data (TX – 8mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.2ns; CLOAD – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			1.7	ns
High to Low prop Delay	T _{PHL}			1.7	ns
Output Rise time	T _{RISE}			0.8	ns
Output Fall time	T _{FALL}			0.8	ns
Current consumption on VDDIO	IDVDDIO			3.5	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.35. D12I1025x Timing and Dynamic Current consumption Data (TX – 12mA)
IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 10pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			1.7	ns
High to Low prop Delay	T _{PHL}			1.7	ns
Output Rise time	T _{RISE}			0.8	ns
Output Fall time	T _{FALL}			0.8	ns
Current consumption on VDDIO	IDVDDIO			5	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 3.36. D16I1025x Timing and Dynamic Current consumption Data (TX – 16mA)
 IOVDD = 1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; CLOAD – 10pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			1.7	ns
High to Low prop Delay	T_{PHL}			1.7	ns
Output Rise time	T_{RISE}			0.8	ns
Output Fall time	T_{FALL}			0.8	ns
Current consumption on VDDIO	IDVDDIO			6	mA
Current consumption on VDD	IDVDD			200	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Analog, non-inverting bi-directional without resistor pad (R=0.3Ohm) with ESD protection (1.2V,2.5V, 60mA): A1825EW, A1825NS

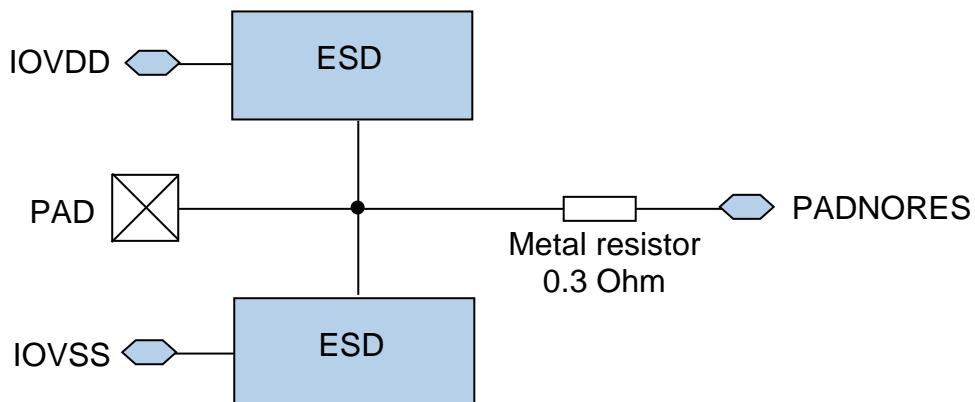


Figure 3.9. Analog (A1825x) cell block diagrams

Breaker cells break the cells: Breakcore, Breakio

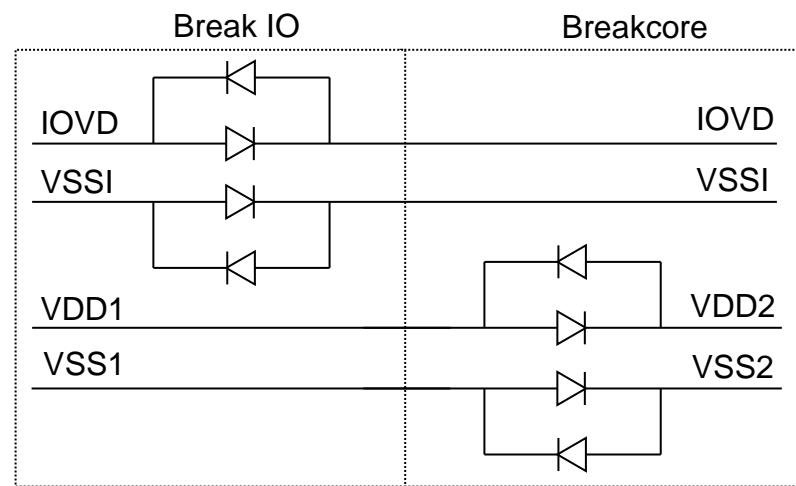


Figure 3.10. Breakcore & Breakio block diagram

Power/ground cells, cross coupling diodes and decoupling capacitors connection diagram:
VDD, IOVDD, VSS, IOVSS, CIOIOVDDIOVSS

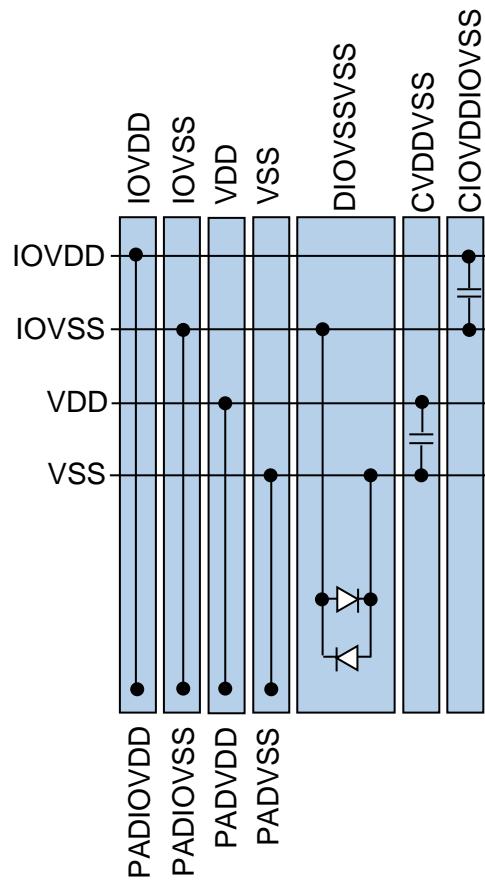


Figure 3.11. Power/ground cells, cross coupling diodes and decoupling capacitors connection diagram

Corner Pad cells: CORNER

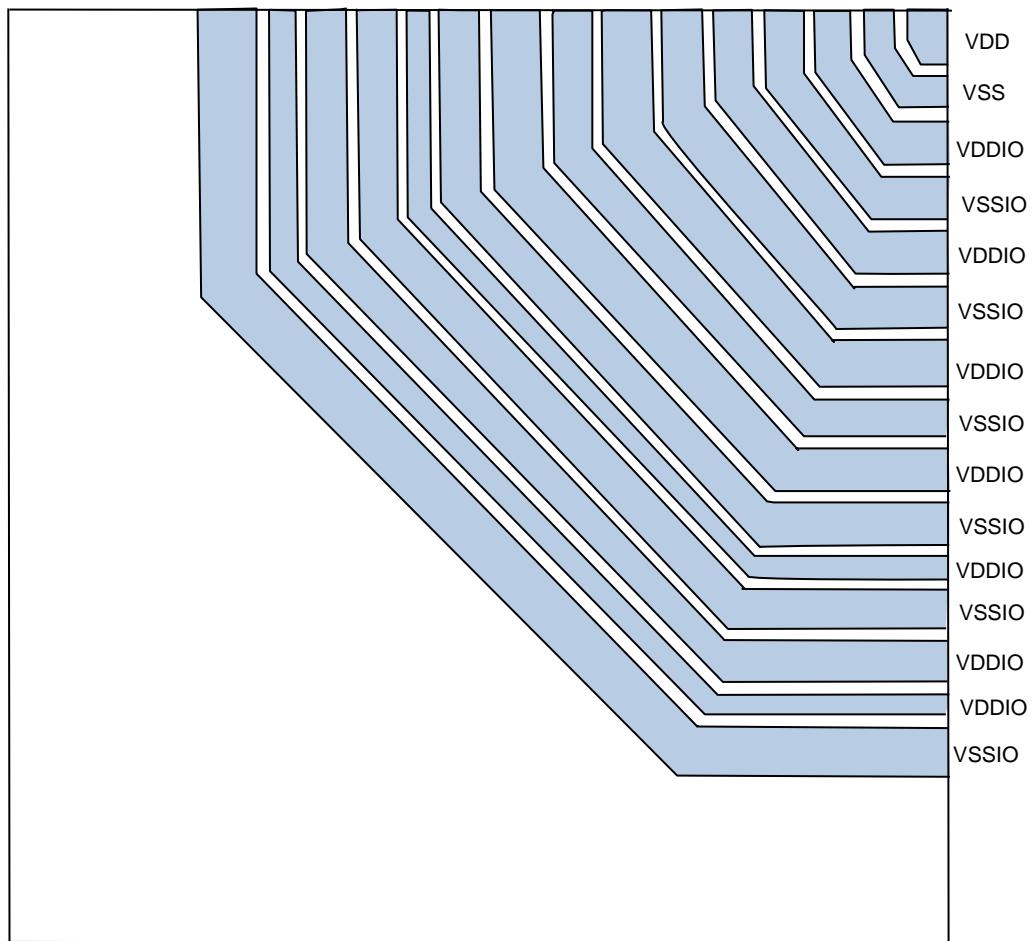


Figure 3.12. Physical structure of Corner Pad cell

Filler cells: FILLER, FILLER01, FILLER1, FILLER5.

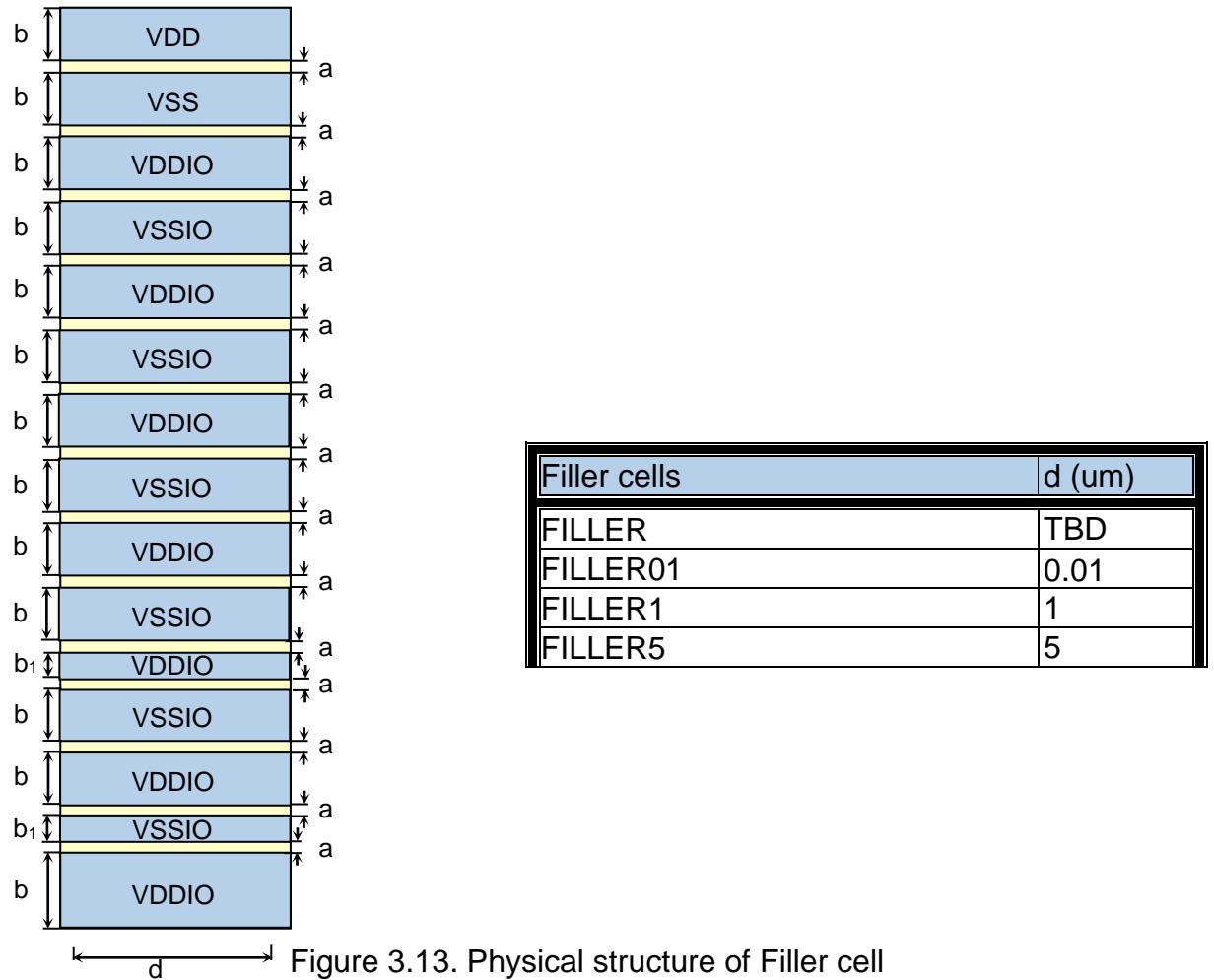


Figure 3.13. Physical structure of Filler cell

4. I/O Special Cell Library SAED_EDK14_FINFET_IO_SP

4.1. Introduction

The SAED_EDK14_FINFET_IO_SP I/O Special Cell Library will be built using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V design rules. The library will include widely used special I/O cells which are necessary for integrated circuits design for educational purposes. Both wire-bond and flip-chip versions of cells in SAED_EDK14_FINFET_IO_SP I/O Special Cell Library will be designed. All special I/Os will have EW and NS types. This designs will be implemented according to specifications of corresponding special I/Os.

4.2. General Information

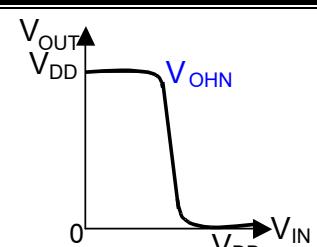
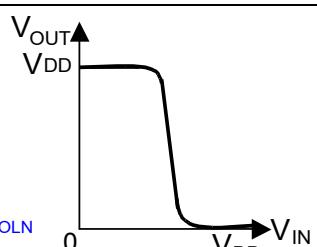
The used symbols of logic elements' states in the specification of SAED_EDK14_FINFET_IO_SP Special I/O Library are shown in Table 4.1.

Table 4.1. Symbols of logic elements' states

Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIGH Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

DC parameters and measurement conditions of the elements included in SAED_EDK14_FINFET_IO_SP special I/O library are shown in Table 4.2 / 4.3 / 4.4 / 4.5 / 4.6 / 4.7.

Table 4.2. DC Parameters and measurement conditions of HSTLX cells

No	Parameter	Unit	Symbol	Figure	Definition
6	Output high level voltage (nominal)	V	V_{OHN}		Output high voltage at nominal condition, usually equals to V_{DD} for input buffer and $(VDDIO - 0.4 \div VDDIO)$ for output buffer (current equal to drive strength sink/sourced from output buffer)
7	Output low level voltage (nominal)	V	V_{OLN}		Output low voltage at nominal condition, usually $V_{OLN}=0$ for input buffer and $(VSSIO \div VSSIO + 0.4)$ for output buffer (current equal to drive strength sink/sourced from output buffer)

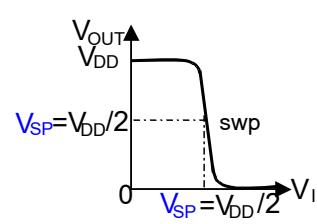
No	Parameter	Unit	Symbol	Figure	Definition
8	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT} = V_{DD}/2$ ($V_{DD}/2$)
9	Static leakage current consumption at output on high state	uA	I_{LEAKH}	None	The current consumed when the output is high
		uA	I_{LEAKL}	None	The current consumed when the output is low
10	Leakage power consumption (dissipation) at output	pW	$P_{LEAKH} = V_{DD} \times I_{LEAKH}$	None	The power consumed when the output is high
		pW	$P_{LEAKL} = V_{DD} \times I_{LEAKL}$	None	The power consumed when the output is low

Table 4.3. DC Parameters and measurement conditions of SSTLX cells

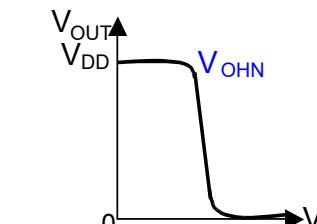
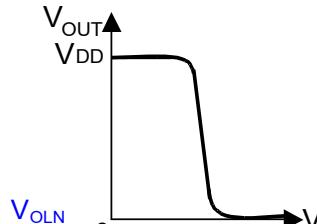
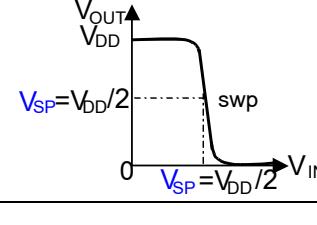
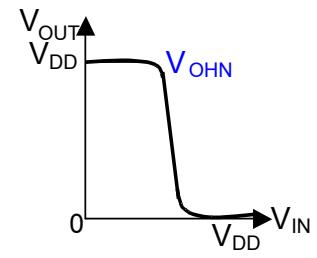
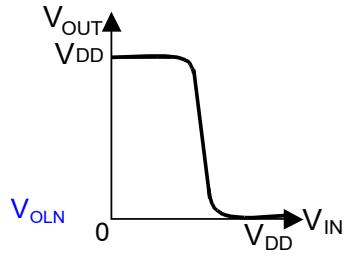
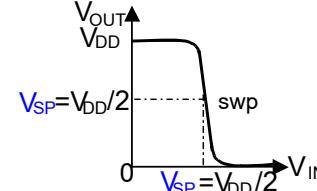
No	Parameter	Unit	Symbol	Figure	Definition
1	Output high level voltage (nominal)	V	V_{OHN}		Output high voltage at nominal condition, usually equals to V_{DD} for input buffer and $(0.8 \div V_{DD})$ for output buffer (current equal to drive strength sink/sourced from output buffer)
2	Output low level voltage (nominal)	V	V_{OLN}		Output low voltage at nominal condition, usually $V_{OLN}=0$ for input buffer and $(V_{SSIO} \div V_{DD} \times 0.2)$ for output buffer (current equal to drive strength sink/sourced from output buffer)
3	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT} = V_{DD}/2$ ($V_{DD}/2$)
4	Static leakage current consumption at output on high state	uA	I_{LEAKH}	None	The current consumed when the output is high
		uA	I_{LEAKL}	None	The current consumed when the output is low
5	Leakage power consumption (dissipation) at output	pW	$P_{LEAKH} = V_{DD} \times I_{LEAKH}$	None	The power consumed when the output is high
		pW	$P_{LEAKL} = V_{DD} \times I_{LEAKL}$	None	The power consumed when the output is low

Table 4.4. DC Parameters and measurement conditions of LPDDRX cells

No	Parameter	Unit	Symbol	Figure	Definition
1	Output high level voltage (nominal)	V	V_{OHN}		Output high voltage at nominal condition, usually equals to V_{DD} for input buffer and $(0.9 \cdot VDDIO \div VDDIO)$ for output buffer (current equal to drive strength sink/sourced from output buffer)
2	Output low level voltage (nominal)	V	V_{OLN}		Output low voltage at nominal condition, usually $V_{OLN}=0$ for input buffer and $(VSSIO \div VDDIO \cdot 0.1)$ for output buffer (current equal to drive strength sink/sourced from output buffer)
3	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT} = VDDIO/2$ ($VDD/2$)
4	Static leakage current consumption at output on high state	uA	I_{LEAKH}	None	The current consumed when the output is high
		uA	I_{LEAKL}	None	The current consumed when the output is low
5	Leakage power consumption (dissipation) at output	pW	$P_{LEAKH} = V_{DD} \times I_{LEAKH}$	None	The power consumed when the output is high
		pW	$P_{LEAKL} = V_{DD} \times I_{LEAKL}$	None	The power consumed when the output is low

AC parameters and measurement conditions of the elements included in SAED_EDK14_FINFET_IO_SP special I/O library are shown in Table 4.5 / 4.6 / 4.7

Table 4.5. AC Parameters and measurement conditions of HSTLX cells

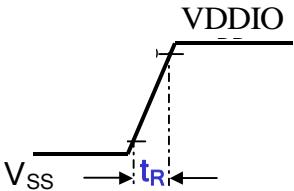
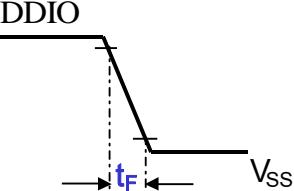
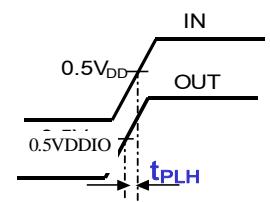
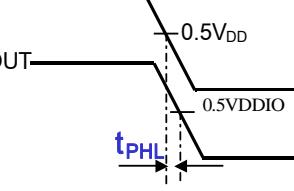
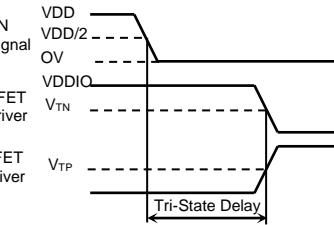
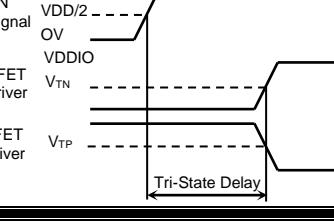
No	Parameter	Unit	Symbol	Figure	Definition
1.	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from k to (1-k)V _{DDIO} value. K=0.5
2.	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from (1-k)V _{DDIO} to k value. K=0.5
3.	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a 0.5V _{DD} and the output signal crossing its 0.5V _{DDIO} when the output signal is changing from low to high
4.	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a 0.5V _{DD} and the output signal crossing its 0.5V _{DDIO} when the output signal is changing from high to low
5.	Average supply current	uA	$I_{V_{DD}AVG} = \frac{1}{T} \int_0^T I_{V_{DD}}(t)dt$	None	The power supply current average value for a period (T)
6.	Z-state entry time, (only for tri-state output cells) delay	ns	t_{HZ}		The amount of time that takes the output to change from high to Z-state after control signal is applied
7.	Enable time, (only for tri-state output cells) delay	ns	t_{ZH}		The amount of time that takes the output to change from Z-state to active after control signal is applied

Table 4.6. AC Parameters and measurement conditions of SSTLX cells

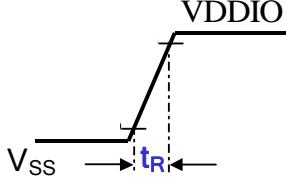
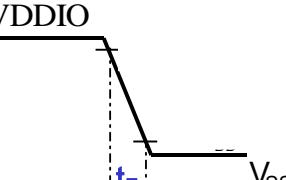
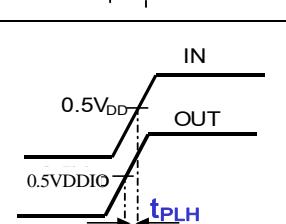
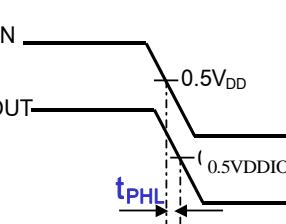
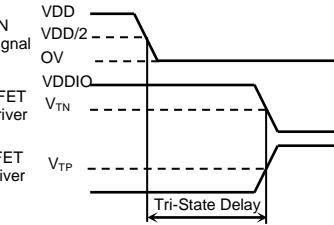
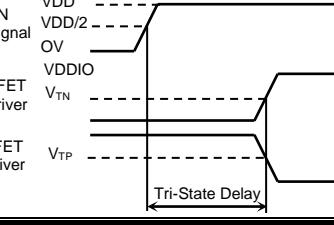
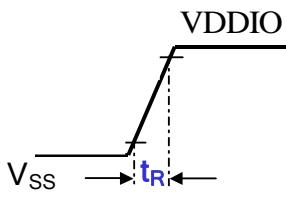
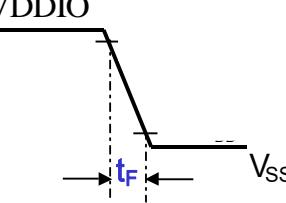
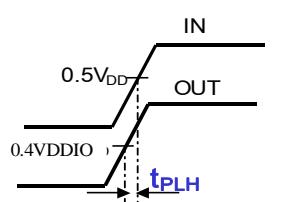
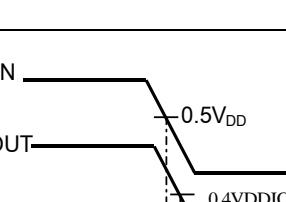
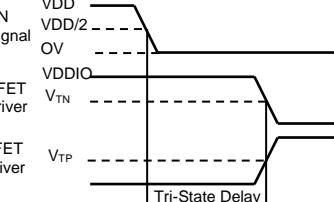
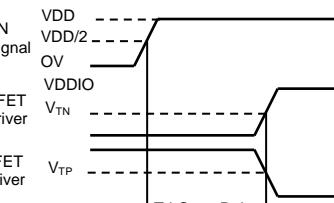
No	Parameter	Unit	Symbol	Figure	Definition
1	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from VTT-0.608 to VTT+0.608 value.
2	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from VTT+0.608 to VTT-0.608 value.
3	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DDIO}$ when the output signal is changing from low to high
4	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DDIO}$ when the output signal is changing from high to low
5	Average supply current	uA	$I_{V_{DD}AVG} = \frac{1}{T} \int_0^T I_{V_{DD}}(t) dt$	None	The power supply current average value for a period (T)
6	Z-state entry time, (only for tri-state output cells) delay	ns	t_{HZ}		The amount of time that takes the output to change from high to Z-state after control signal is applied
7	Enable time, (only for tri-state output cells) delay	ns	t_{ZH}		The amount of time that takes the output to change from Z-state to active after control signal is applied

Table 4.7. AC Parameters and measurement conditions of LPDDRX cells

No	Parameter	Unit	Symbol	Figure	Definition
1	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from $0.2 \cdot V_{DDIO}$ to $0.8 \cdot V_{DDIO}$ value.
2	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from $0.8 \cdot V_{DDIO}$ to $0.2 \cdot V_{DDIO}$ value.
3	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.4V_{DDIO}$ when the output signal is changing from low to high
4	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.4V_{DDIO}$ when the output signal is changing from high to low
5	Average supply current	uA	$I_{V_{DD}AVG} = \frac{1}{T} \int I_{V_{DD}}(t) dt$	None	The power supply current average value for a period (T)
6	Z-state entry time, (only for tri-state output cells) delay	ns	t_{HZ}		The amount of time that takes the output to change from high to Z-state after control signal is applied
7	Enable time, (only for tri-state output cells) delay	ns	t_{ZH}		The amount of time that takes the output to change from Z-state to active after control signal is applied

4.2.1. ESD Protection

Special structures should be included in the I/O cells to protect against electrostatic discharge (ESD) for guaranteed minimum 2KV human-body model (HBM), 300V machine model (MM), and 400V and latch-up of up to 100mA (figure 4.1).

4.2.2. Latch-Up Protection

Provision of rules of Latch-Up protection is anticipated.

4.2.3. CLAMP circuit

NFIN Clamp circuit will be utilized on all power supply buses and will be included in the Power and Ground pads to minimize the voltage spike present at the gates of internal circuits and to alleviate some of the current stress on the ESD/latch-up structures (figure 4.1).

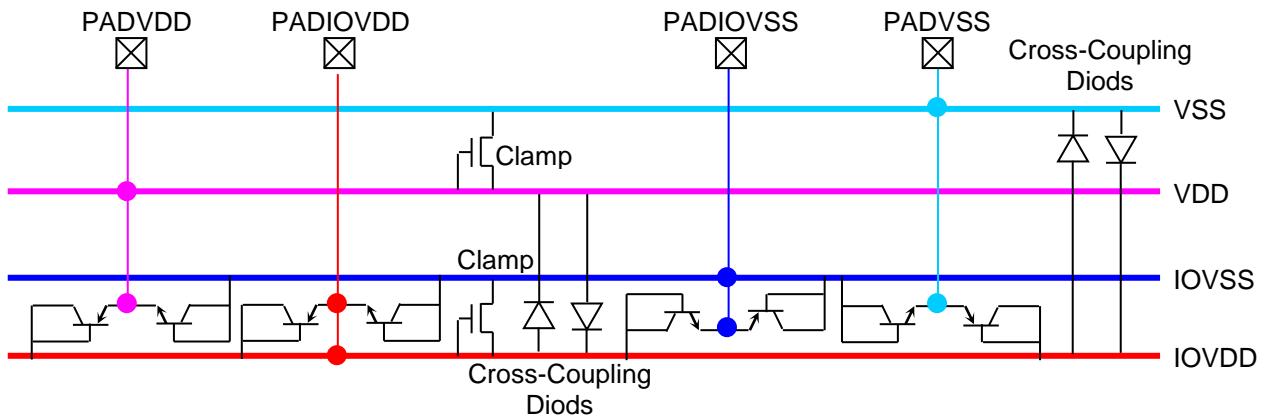


Figure 4.1. Implementation of ESD current paths

4.2.4. Decoupling capacitors

Decoupling capacitors should be built wherever possible, thus assuring a minimum decoupling capacitance on the die.

4.3. I/O Special Cells List

SAED_EDK14_FINFET_IO_SP library contains 3 cells in total, the list of which is shown in Table 4.8. I/O Special Cell Library will be designed in both wire-bond and flip-chip versions with both EW and NS types.

Table 4.8. I/O Special Cells List

Item#	Description	Cell name
1.	EIA/JEDEC STANDART No 8-6 compliant HSTL cell	HSTLEW
2.	EIA/JEDEC STANDART No 8-6 compliant HSTL cell	HSTLNS
3.	JEDEC Standard No 8-9B compliant SSTL cell	SSTLEW
4.	JEDEC Standard No 8-9B compliant SSTL cell	SSTLNS

4.4. Operating conditions

SAED_EDK14_FINFET_IO_SP Special I/O Library specification is given for operation specified in respective standards. The process technology is SAED14nm FinFET 1P9M 1.2V/2.5V/3.3V.

The operating conditions of **SAED_EDK14_FINFET_IO_SP** Special I/O Library are shown in Table 4.13 /4.14/ 4.15

Table 4.9 Operating conditions for HSTLX

Parameter	Min	Typ	Max	Unit
Core Supply (VDD) voltage	0.72	0.8	0.88	V
I/O Supply (VDDIO) voltage	1.4	1.5	1.6	V
Input reference voltage	0.68	0.75	0.90	V
Operating temperature	-40	25	125	°C
Operating Frequency (F)	-	-	1	GHz

Table 4.10. Operating conditions for SSTLX

Parameter	Min	Typ	Max	Unit
Core Supply (VDD) voltage	0.72	0.8	0.88	V
I/O Supply (VDDIO) voltage	2.3	2.5	2.7	V
Input reference voltage	1.13	1.25	1.38	V
Termination voltage	VREF-0.04	VREF	VREF+0.04	V
Operating temperature	-40	25	125	°C
Operating Frequency (F)	-	-	1	GHz

Table 4.11. Operating conditions for LPDDRX

Parameter	Min	Typ	Max	Unit
Core Supply (VDD) voltage	0.72	0.8	0.88	V
I/O Supply (VDDIO) voltage	1.7	1.8	1.9	V
Operating temperature	-40	25	125	°C
Operating Frequency (F)	-	-	1	GHz

4.5. AC Characteristics

4.5.1. Characterization corners

Composite Current Source (CCS) modeling technology will be applied for characterization. The application of that technology will support timing, noise, and power analyses simultaneously with consideration of the relevant nanometer dependencies. It allows meeting the requirements of variation-aware analysis.

The characterization results are given for process/voltage/temperature (PVT) conditions shown in Table 4.12 / 4.13 / 4.14.

Table 4.12. Characterization corners for HSTLX

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Core Power Supply VDD (V)	I/O Power Supply IOVDD (V)	Library Name Suffix
FF	Fast – Fast	-40	0.88	1.65	ff0p88vm40c_1p6v
TT	Typical – Typical	25	0.8	1.5	tt0p8v25c_1p5v
SS	Slow – Slow	125	0.72	1.35	ss0p72v125c_1p4v

Table 4.13. Characterization corners for SSTLX

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Core Power Supply VDD (V)	I/O Power Supply IOVDD (V)	Library Name Suffix
FF	Fast – Fast	-40	0.88	1.98	ff0p88vm40c_2p75v
TT	Typical – Typical	25	0.8	1.8	tt0p8v25c_2p5v
SS	Slow – Slow	125	0.72	1.62	ss0p72v125c_2p25v

Table 4.14. Characterization corners for LPDDRX

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Core Power Supply VDD (V)	I/O Power Supply IOVDD (V)	Library Name Suffix
FF	Fast – Fast	-40	0.88	1.9	ff0p88vm40c_1p9v
TT	Typical – Typical	25	0.8	1.8	tt0p8v25c_1p8v
SS	Slow – Slow	125	0.72	1.7	ss0p72v125c_1p7v

4.6. The values of Output Load and Input slope

Characterization will be realized for 8 different values of Output Load and 6 different values of Input slope shown in Table 4.15.

Table 4.15 The values used for characterization

Parameter	Value							
Core loading capacitance (pF)	0.0	0.2	0.4	0.6	0.8	1.0	1.2	1.4
PAD loading capacitance (pF)	0	5	10	15	20	25	30	35
Input signal slope (ns)	0.4	1.2	2.0	2.4	2.7	3.2	-	-

4.7. Special I/O Library Deliverables

Table 4.16. Special I/O Library deliverables

N	Type	Description
1	.pdf	Databook / User guide
2	.db, .lib	Synthesis models
3	.v	Verilog simulation models
4	.cdl, .sp	LVS, HSPICE netlists
5	.spf	Extracted C and RC netlists for different corners
6	.gds	GDSII layout views
7	.clf	Cell antenna information
8	.lef	LEF files
9	.FRAM, .CEL, NDM	FRAM views, layout views

4.8. Physical Structure of I/O Cell

4.8.1. Physical Structure of Flip-Chip I/O Cell

All cells should fit into 32umx160um size and the buses should be implemented as presented in figure 4.2. The power rails should be selected on the basis of acceptable current density given by the design rules and acceptable current density given by the design rules and electromigration. Pad is placed over cell so buses contain metals up to M9 and BUMP is implemented by redistribution layer.

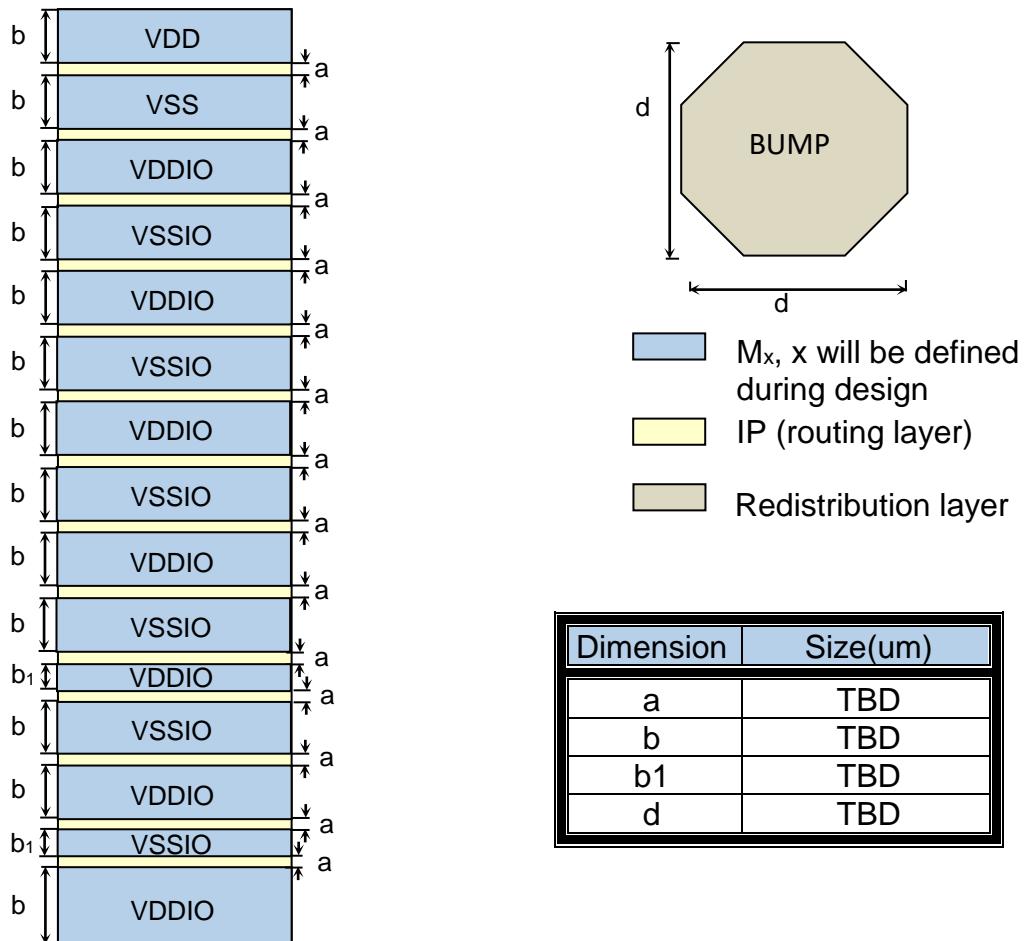


Figure 4.2. Physical structure of flip-chip I/O cell

4.8.2. Wire-Bond structure

All cells should fit into 32umx240um size and the buses should be implemented as presented in figure 4.3. The power rails will be selected on the basis of acceptable current density given by the design rules and acceptable current density given by the design rules and electromigration

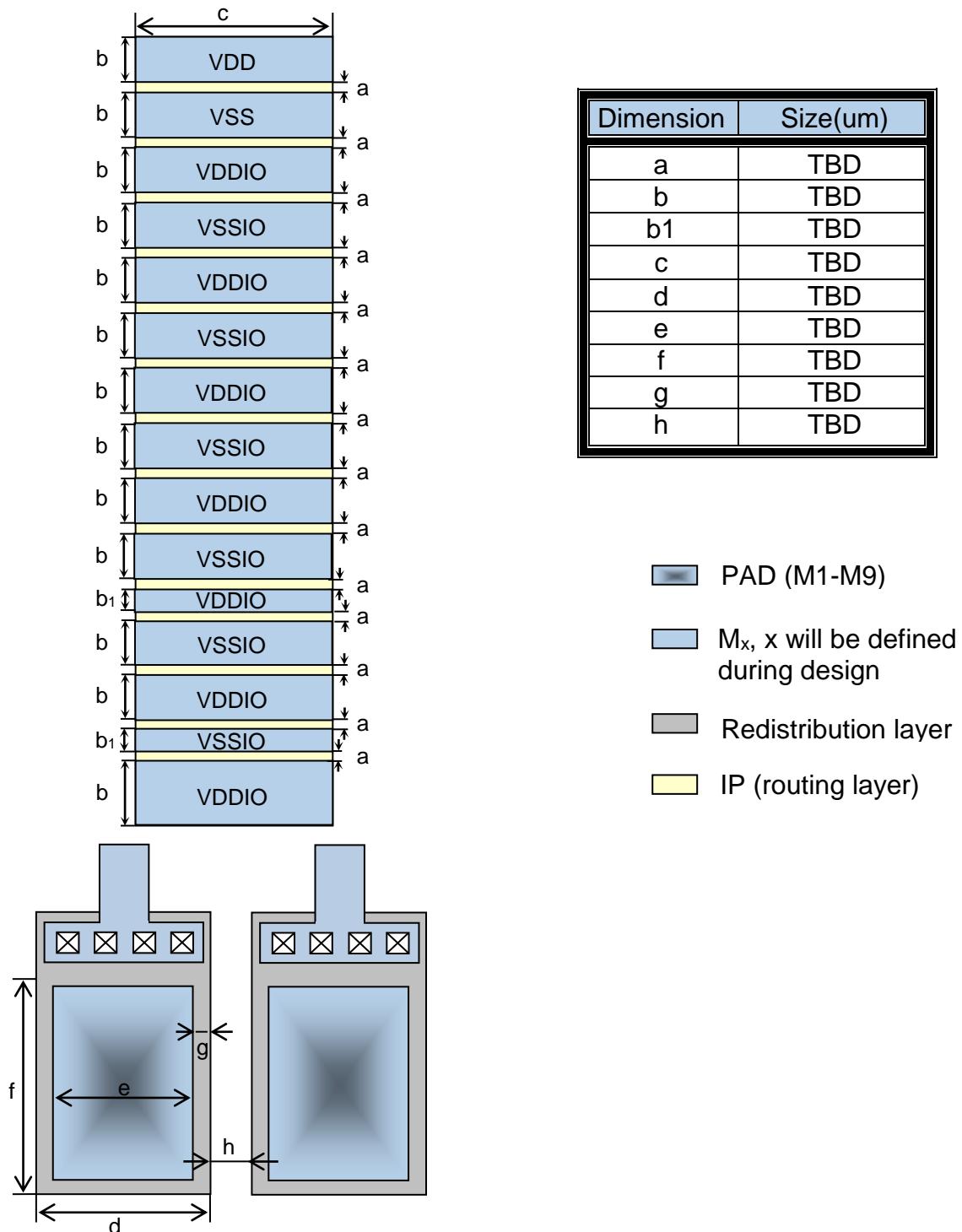


Figure 4.3. Physical structure of wire-bond I/O cell

4.9. Special I/O Cell's Description

HSTLEW, HSTLNS ,SSTLEW,SSTLNS,

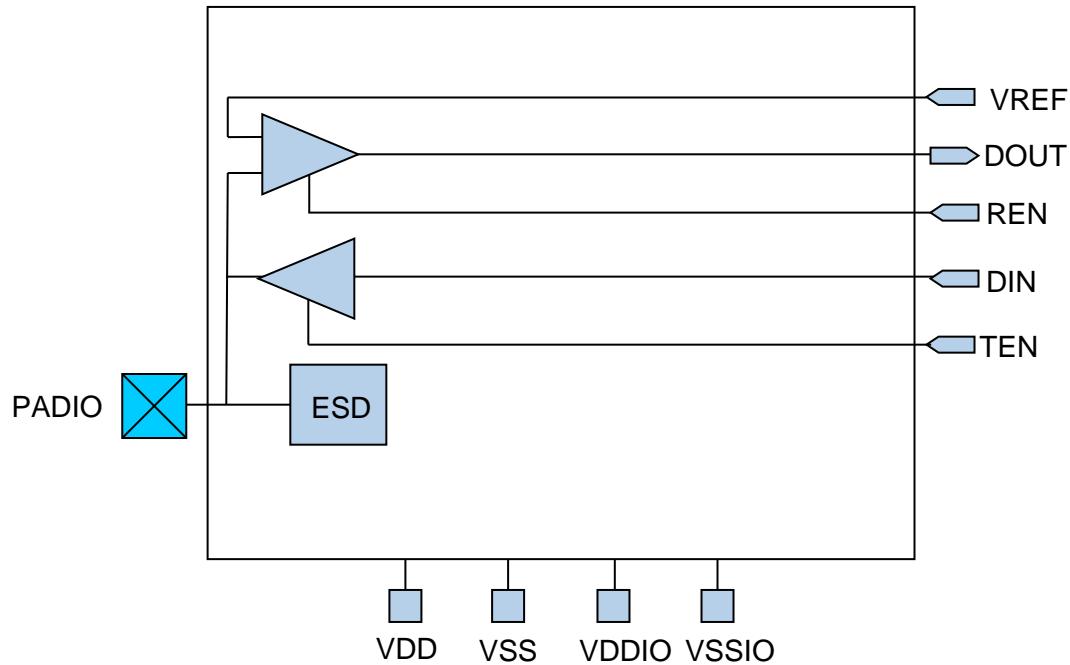


Figure 4.4. HSTLX,SSTLX cells block diagram

Table 4.17.HSTLX,SSTLX Logic Truth Table – Tx Mode

Input		Output
TEN	DIN	PADIO
1	1	1
1	0	0
0	X	z

Table 4.18 HSTLX,SSTLX Logic Truth Table – Rx Mode

Input		Output
PADIO	REN	DOUT
1	1	1
0	1	0
Z	0	0
X	0	0

Table 4.19. Input DC logic levels of HSTLX

Symbol	Parameter	Min	Max	Unit
$V_{IH(dc)}$	dc input logic high	$V_{REF}+0.10$	$V_{DDIO}+0.3$	V
$V_{IL(dc)}$	dc input logic low	-0.3	$V_{REF}-0.10$	V

Table 4.20. Input AC logic levels of HSTLX

Symbol	Parameter	Min	Max	Unit
$V_{IH(ac)}$	ac input logic high	$V_{REF}+0.20$		V
$V_{IL(ac)}$	ac input logic low		$V_{REF}-0.20$	V

Table 4.21. Input DC logic levels of SSTLX

Symbol	Parameter	Min	Max	Unit
$V_{IH(dc)}$	dc input logic high	$V_{REF}+0.15$	$V_{DDIO}+0.3$	V
$V_{IL(dc)}$	dc input logic low	1.4	$V_{REF}-0.15$	V

Table 4.22. Input AC logic levels of SSTLX

Symbol	Parameter	Min	Max	Unit
$V_{IH(ac)}$	ac input logic high	$V_{REF}+0.31$		V
$V_{IL(ac)}$	ac input logic low		$V_{REF}-0.31$	V

Table 4.23 HSTLX Timing and Dynamic Current consumption Data (TX)
 $V_{DDIO} = 1.5V$; $V_{DD} = 0.8V$, Frequency – 1GHz; Input Slope – 0.16ns; cload – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			0.9	ns
High to Low prop Delay	T_{PHL}			0.9	ns
Output Rise time	T_{RISE}			0.25	ns
Output Fall time	T_{FALL}			0.25	ns
Current consumption on vddio	IDIOVDD			6	mA
Current consumption on vdd	IDVDD			0.5	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 4.24 HSTLX Timing and Dynamic Current consumption Data (RX)
 $V_{DDIO} = 1.5V$; $V_{DD} = 0.8V$, Frequency – 1GHz; Input Slope – 0.16ns; cload – 0.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T_{PLH}			0.8	ns
High to Low prop Delay	T_{PHL}			0.8	ns
Output Rise time	T_{RISE}			0.08	ns
Output Fall time	T_{FALL}			0.08	ns
Current consumption on vddio	IDIOVDD			25	mA
Current consumption on vdd	IDVDD			50	uA
Duty Cycle Distortion	T_{DUTY}	45	50	55	%

Table 4.25 SSTLX Timing and Dynamic Current consumption Data (TX)
 $V_{DDIO} = 1.8V$; $V_{DD} = 0.8V$, Frequency – 1GHz; Input Slope – 0.16ns; cload – 5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			0.9	ns
High to Low prop Delay	T _{PHL}			0.9	ns
Output Rise time	T _{RISE}			0.25	ns
Output Fall time	T _{FALL}			0.25	ns
Current consumption on vddio	IDVDDIO			6	mA
Current consumption on vdd	IDVDD			0.5	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

Table 4.26 SSTLX Timing and Dynamic Current consumption Data (RX)
VDDIO =1.8V; VDD=0.8V, Frequency – 1GHz; Input Slope – 0.16ns; cload – 0.5pF

Parameter	Symbol	Min	Typ	Max	Units
Low to High prop Delay	T _{PLH}			0.8	ns
High to Low prop Delay	T _{PHL}			0.8	ns
Output Rise time	T _{RISE}			0.08	ns
Output Fall time	T _{FALL}			0.08	ns
Current consumption on vddio	IDVDDIO			25	mA
Current consumption on vdd	IDVDD			50	uA
Duty Cycle Distortion	T _{DUTY}	45	50	55	%

5. Set of Memories SAED_EDK14_FINFET_RAM

5.1. Introduction

The SAED_EDK14_FINFET_RAM set of memories will be designed using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V process. It will represent a set of several static SRAMs (SRAMs) with small number of words (word depth – m) and bits in word (data width – n). All SRAMs, included in SAED_EDK14_FINFET_RAM, will represent Synchronous Dual-Port or Single-port SRAM with Write Enable, Output Enable, Chip Select port(s). Each SRAM $m \times n$, included in the set, will have the same architecture and will differ from the rest with its $n \times m$ (width x depth) sizes. As SAED_EDK14_FINFET_RAM is anticipated for the use of educational purposes, only SRAMs of the sizes, shown in Table 5.1., will be included in it.

Table 5.1. SRAM $m \times n$ Cell List

No	Data width (n)	Word depth (m)	Address width (k= $\log_2 m$)	Cell Name
1	4	16	4	SRAM2RW16x4
2	4	32	5	SRAM2RW32x4
3	4	64	6	SRAM2RW64x4
4	4	128	7	SRAM2RW128x4
5	8	16	4	SRAM2RW16x8
6	8	32	5	SRAM2RW32x8
7	8	64	6	SRAM2RW64x8
8	8	128	7	SRAM2RW128x8
9	16	16	4	SRAM2RW16x16
10	16	32	5	SRAM2RW32x16
11	16	64	6	SRAM2RW64x16
12	16	128	7	SRAM2RW128x16
13	32	16	4	SRAM2RW16x32
14	32	32	5	SRAM2RW32x32
15	32	64	6	SRAM2RW64x32
16	32	128	7	SRAM2RW128x32
17	8	128	7	SRAM1RW128x8
18	32	64	6	SRAM1RW64x32
19	22	32	5	SRAM2RW32x22
20	39	32	5	SRAM2RW32x39
21	32	256	8	SRAM1RW256x32
22	8	1024	10	SRAM1RW102x84
23	8	512	9	SRAM1RW512x8
24	48	128	7	SRAM1RW128x48
25	50	32	5	SRAM1RW32x50
26	34	64	6	SRAM1RW64x34
27	46	256	8	SRAM1RW256x46
28	46	128	7	SRAM1RW128x46
29	8	64	6	SRAM1RW64x8
30	128	64	6	SRAM1RW64x128
31	128	256	8	SRAM1RW256x128
32	8	256	8	SRAM1RW256x8
33	48	256	8	SRAM1RW256x48
34	128	512	9	SRAM1RW512x128
35	32	512	9	SRAM1RW512x32

5.2. SRAM naming conventions

All memories in the set are named according to the following template (Fig. 3.1):



Figure 5.1. Memories naming template

The template contains symbols denoting specifics of the memory, the descriptions of the symbols are given in Table 5.2.

Table 5.2. Memories naming conventions

Symbol	Description	Values
p	Number of access ports	1,2
n	Number of words	Integer number, 2^n
w	Word size	Integer, various

5.3. General Information

The Synchronous Dual-Port SRAMmxn will have two ports (Primary and Dual) for the same memory location. Both ports can be independently accessed for read or write operations. Single-port cells have only one port.

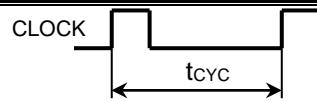
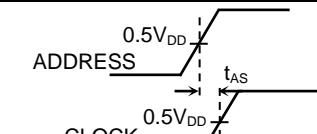
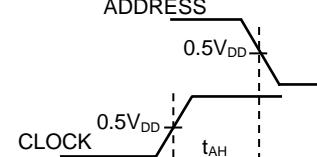
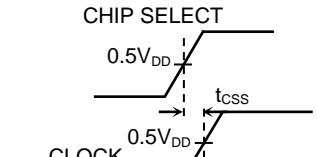
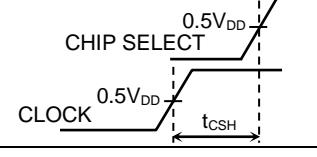
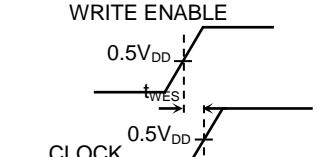
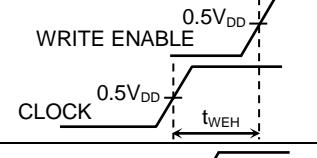
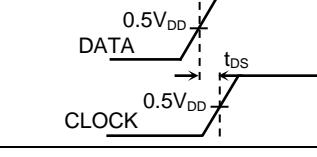
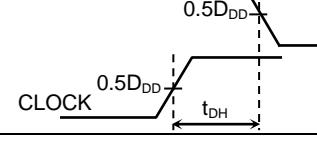
The used symbols of SRAMpRWnxm states are shown in Table 5.3.

Table 5.3. Symbols of SRAMmxn states

Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIG`H Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

Parameters and measurement conditions of SRAMmxn, included in SAED_EDK14_FINFET_RAM set of memories, are shown in Table 5.4.

Table 5.4. Parameters and measurement conditions of SRAMmxn

No	Parameter	Unit	Symbol	Figure	Definition
Timing parameters					
1	Cycle time	ns	t _{CYC}		The amount of time between two sequential active edges of clock signal
2	Access time	ns	t _A	None	The amount of time between applying Write/Read Enable signal and obtaining Access to Data in Memory
3	Address setup	ns	t _{AS}		The minimum amount of time in which the address to a SRAMmxn must be stable before the active edge of the clock occurs
4	Address hold	ns	t _{AH}		The minimum amount of time in which the address to a SRAMmxn must remain stable after the active edge of the clock has occurred
5	Chip select setup	ns	t _{CSS}		The minimum amount of time in which the Chip select signal to a SRAMmxn must be stable before the active edge of the clock occurs
6	Chip select hold	ns	t _{CSH}		The minimum amount of time in which the Chip select signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
7	Write enable setup	ns	t _{WES}		The minimum amount of time in which the Write enable signal to a SRAMmxn must be stable before the active edge of the clock occurs
8	Write enable hold	ns	t _{WEH}		The minimum amount of time in which the Write enable signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
9	Data setup	ns	t _{DS}		The minimum amount of time in which the input data to a SRAMmxn must be stable before the active edge of the clock occurs
10	Data hold	ns	t _{DH}		The minimum amount of time in which the input data to a SRAMmxn must remain stable after the active edge of the clock has occurred

No	Parameter	Unit	Symbol	Figure	Definition
11	Output Z state entry time	ns	t_{OZ}	None	The amount of time that takes the outputs to change to Z state after output enable signal is applied
12	Output Z state exit time	ns	t_{ZO}	None	The amount of time that takes the outputs to exit from Z state after output enable signal is applied
Power parameters					
13	AC current	mA	i_{AC}	None	Average value of dynamic current for read/write operations
14	Read AC current	mA	i_{ACR}	None	Dynamic current for read operation
15	Write AC current	mA	i_{ACW}	None	Dynamic current for write operation
16	Peak current	mA	i_{ACP}	None	Maximum value of dynamic current for read/write operations
17	Deselected current	mA	i_{ACD}	None	The value of current when SRAM _{mn} is disabled, all addresses switch and 50% of data input switch
18	Standby current	mA	i_{ACS}	None	The value of current in standby mode when all inputs and outputs are stable

5.4. Dual port SRAMs

5.4.1. Basic Pins

The Basic Pins of dual port SRAM2RWmxn are shown in Figure 5.2 and its descriptions are shown in Table 5.5.

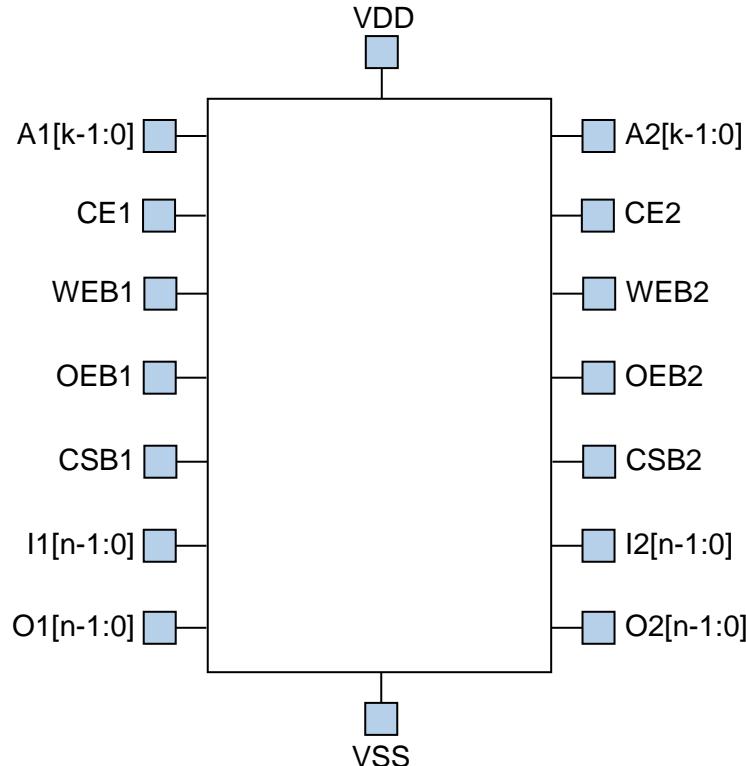


Figure 5.2. Dual port SRAMmmxn Basic Pins

Table 5.5. Dual port SRAM2RWmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A1	k	Input	Primary Read/Write Address
CE1	1	Input	Primary Positive-Edge Clock
WEB1	1	Input	Primary Write Enable, Active Low
OEB1	1	Input	Primary Output Enable, Active Low
CSB1	1	Input	Primary Chip Select, Active Low
I1	n	Input	Primary Input data bus
O1	n	Output	Primary Output data bus
A2	k	Input	Dual Read/Write Address
CE2	1	Input	Dual Positive-Edge Clock
WEB2	1	Input	Dual Write Enable, Active Low
OEB2	1	Input	Dual Output Enable, Active Low
CSB2	1	Input	Dual Chip Select, Active Low
I2	n	Input	Dual Input data bus
O2	n	Output	Dual Output data bus
VDD			Power supply
VSS			Power ground

5.4.2. Dual port SRAMmxn Description

The general block-diagram of SRAMmxn is shown in Figure 5.2.

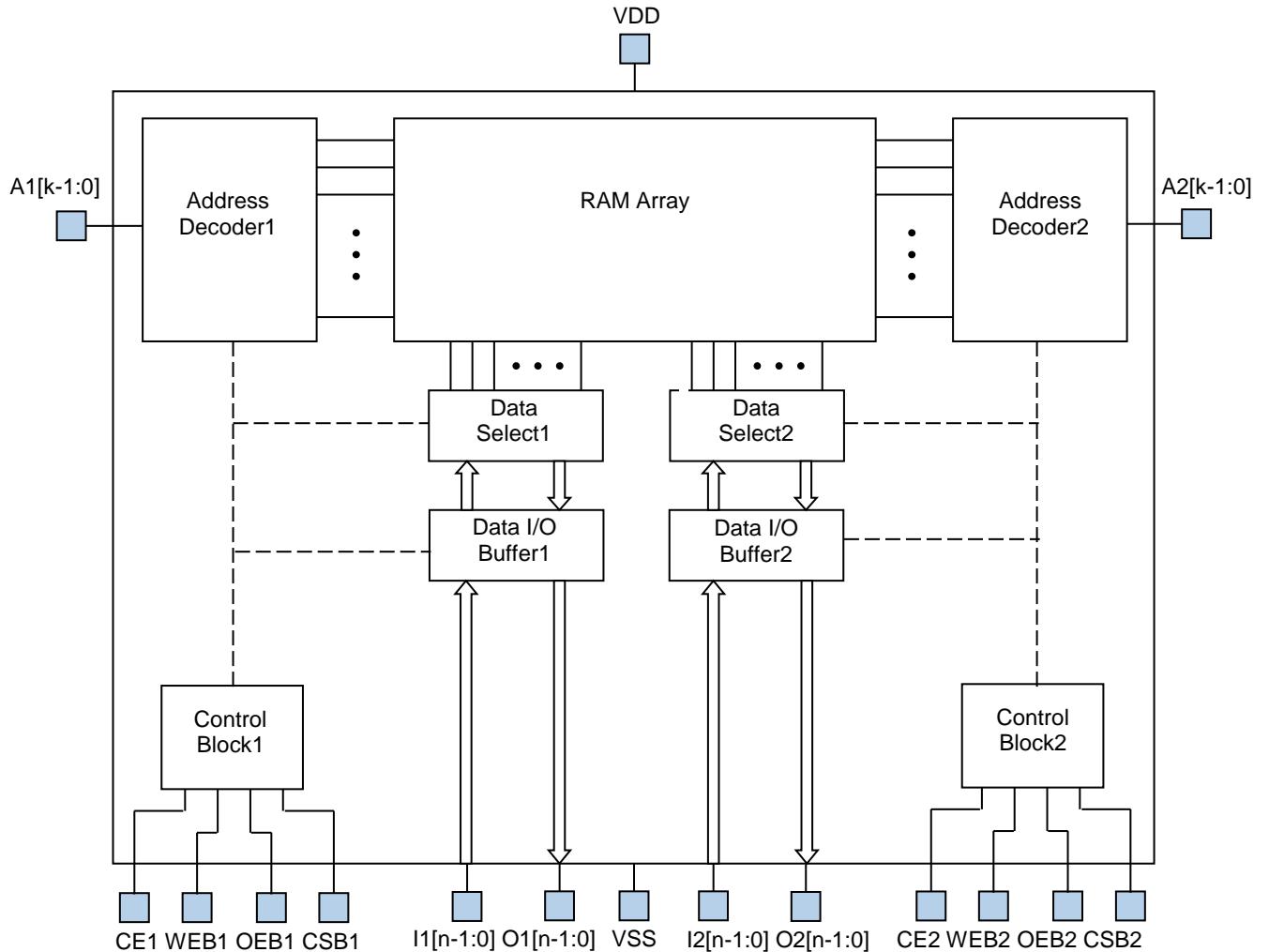


Figure 5.3. Dual port SRAMmxn block diagram

Dual port SRAMmxn Basic Operations is shown in Table 5.6.

Dual port SRAMmxn access is synchronous and triggered by the rising edge of the clock signals (CE1, CE2). Read/Write addresses (A1, A2), Input data (I1, I2), Write enable signals (WEB1, WEB2), and Chip select signals (CSB1, CSB2) are latched by the rising edge of the clocks (CE1, CE2).

The value of Chip Select signal is low (CS1/CS2=0) for read/write operation. The SRAMmxn enter read mode when CS1/CS2=0 and WEB1/WEB2=1. During read operations, data read from the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-1:0] and appear on the data output bus O1[n-1:0]/O2[n-1:0].

Table 5.6. Dual port SRAMmxn Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A1[k-1:0]	WEB1	OEB1	CSB1	I1[n-1:0]	O1[n-1:0] (t+1)	D(A1[k-1:0]) (t+1)		
X	X	0 1	1	Disabled	O1[n-1:0] (t) Z	D(A1[k-1:0]) (t)		
X	0	0 1	0	Enabled	I1[n-1:0] Z	I1[n-1:0]		
X	1	0 1	0	X	D(A1[k-1:0]) (t) Z	D(A1[k-1:0]) (t)		
A2[k-1:0]	WEB2	OEB2	CSB2	I2[n-1:0]	O2[n-1:0] (t+1)	D(A2[k-1:0]) (t+1)		
X	X	0 1	1	Disabled	O2[n-1:0] (t) Z	D(A2[k-1:0]) (t)		
X	0	0 1	0	Enabled	I2[n-1:0] Z	I2[n-1:0]		
X	1	0 1	0	X	D(A2[k-1:0]) (t) Z	D(A2[k-1:0]) (t)		

Note: O1[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O1[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A1[k-1:0]) (t) is the data in the RAM location specified on the address bus A1[k-1:0] in the previous moment of time, and D(A1[k-1:0]) (t+1) in the next moment of time.

O2[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O2[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A2[k-1:0]) (t) is the data in the RAM location specified on the address bus A2[k-1:0] in the previous moment of time, and D(A2[k-1:0]) (t+1) in the next moment of time.

Dual port SRAMmxn enter write mode when CSB1/CSB2=0 and WEB1/WEB2=0. During write mode, data on the data input bus I1[n-1:0]/I2[n-1:0] is writing into the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-2:0].

If OEB1/OEB2=1, data on the output bus O1[n-1:0]/O2[n-1:0] placed in Z state. At that time read/write operation continue. When OEB1/OEB2=0, the data appear on the output bus O1[n-a:0]/O2[n-1:0].

Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB1/CSB2=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A1[k-1:0])/D(A2[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Address contention will occur when both ports simultaneously access the same address. In this case, both ports will read the same data.

5.4.3. Dual port SRAMmxn Timing Waveforms

SRAMmxn will function according to the block-diagrams shown in Figures 5.5 – 5.7.

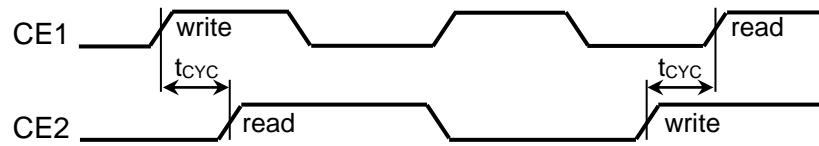


Figure 5.4. Dual port SRAMmxn Write-Read Clock Timing Waveforms

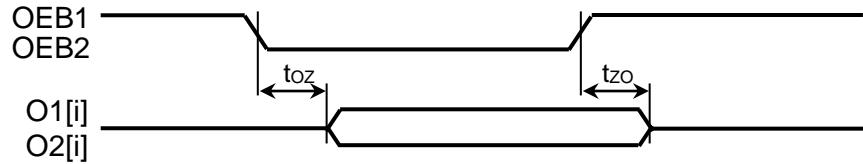


Figure 5.5. Dual port SRAMmxn Output-Enable Timing Waveforms

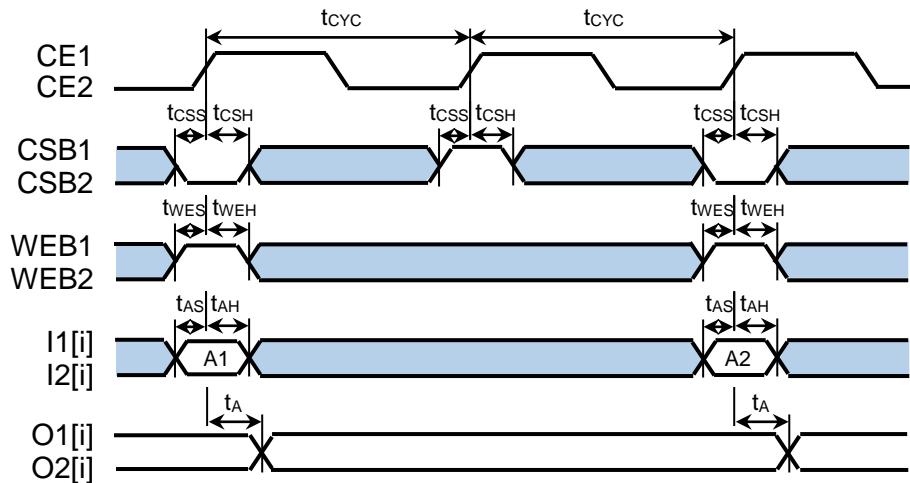


Figure 5.6. Dual port SRAMmxn Read-Cycle Timing Waveforms

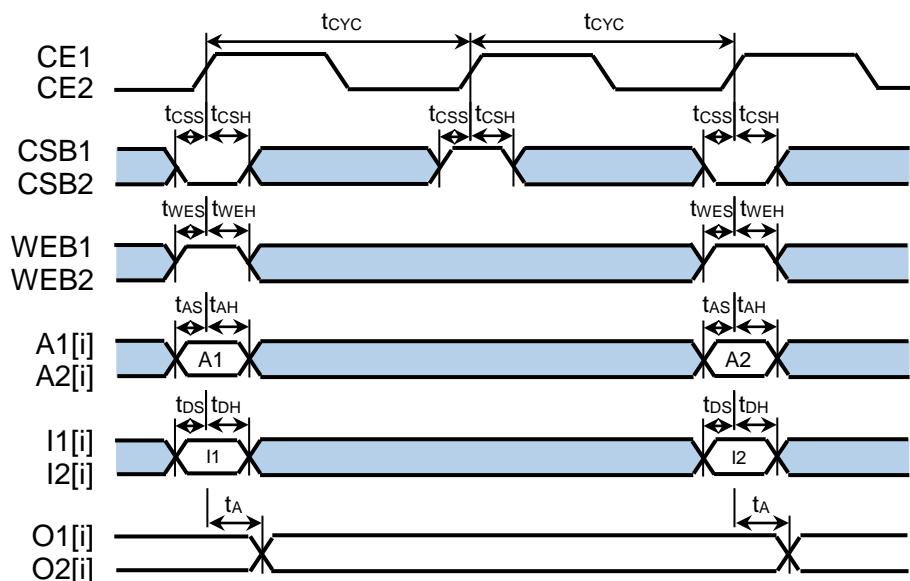


Figure 5.7. Dual port SRAMmxn Write-Cycle Timing Waveforms

5.5. Single port SRAMs

5.5.1. Basic Pins

The Basic Pins of single port SRAM1RW $n \times m$ are shown in Figure 5.8 and its descriptions are shown in Table 5.7.

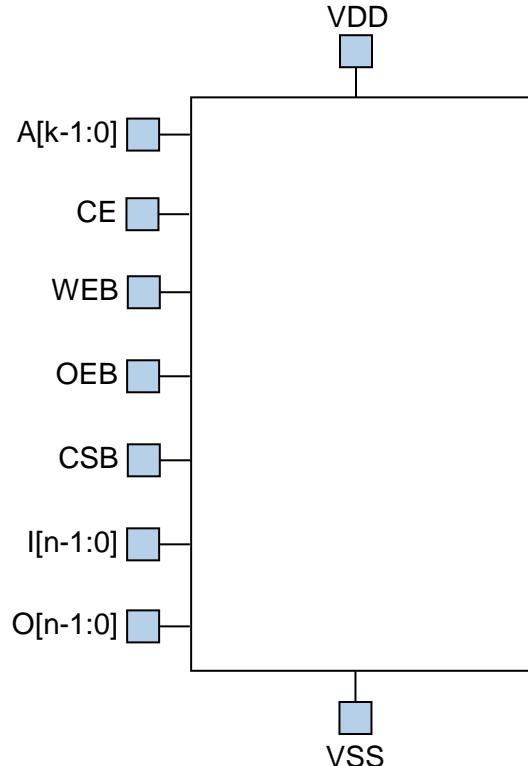


Figure 5.8. Single port SRAM1RW $m \times n$ Basic Pins

Table 5.7. Single port SRAM1RW $m \times n$ Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A	k	Input	Primary Read/Write Address
CE	1	Input	Primary Positive-Edge Clock
WEB	1	Input	Primary Write Enable, Active Low
OEB	1	Input	Primary Output Enable, Active Low
CSB	1	Input	Primary Chip Select, Active Low
I	n	Input	Primary Input data bus
O	n	Output	Primary Output data bus
VDD			Power supply
VSS			Power ground

5.5.2. Single port SRAM1RWmxn Description

The general block-diagram of single port SRAM1RWmxn is shown in Figure 5.9.

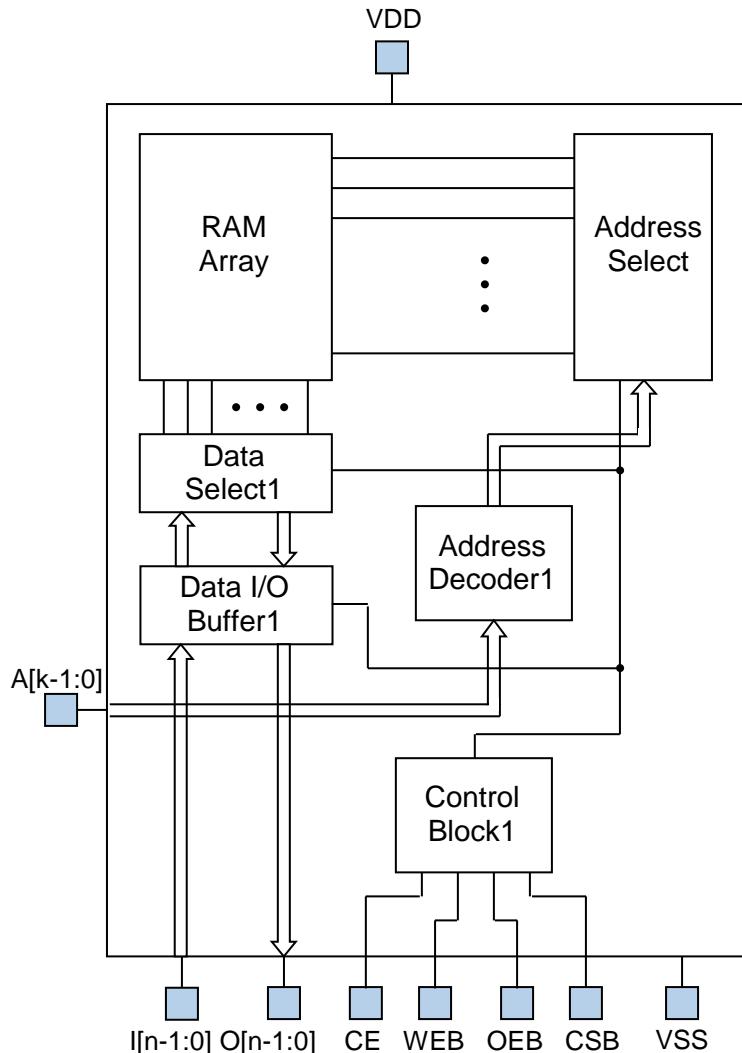


Figure 5.9. Single port SRAM1RWmxn block diagram

Single port SRAM1RWmxn Basic Operations is shown in Table 5.8.

Single port SRAM1RWmxn access is synchronous and triggered by the rising edge of the clock signals (CE). Read/Write addresses (A), Input data (I), Write enable signals (WEB), and Chip select signals (CSB) are latched by the rising edge of the clocks (CE).

The value of Chip Select signal is low (CS=0) for read/write operation. SRAM enter read mode when CS=0 and WEB=1. During read operations, data read from the memory location D(A[k-1:0]) specified on the address bus I[n-1:0] and appear on the data output bus O[n-1:0].

Table 5.8. Single port SRAM1RWmxn Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A[k-1:0]	WEB	OEB	CSB	I[n-1:0]	O[n-1:0] (t+1)	D(A[k-1:0]) (t+1)		
X	X	0	1	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I[n-1:0]	I[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A[k-1:0]) (t)	D(A[k-1:0]) (t)	No	Read
		1			Z			

Note: O[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

O[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

Single port SRAM1RWmxn enter write mode when CSB=0 and WEB=0. During write mode, data on the data input bus I[n-1:0] is writing into the memory location D(A[k-1:0]) specified on the address bus I[n-1:0].

If OEB=1, data on the output bus O[n-1:0] placed in Z state. At that time read/write operation continue. When OEB=0, the data appear on the output bus O[n-a:0].

Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

5.5.3. Single port SRAM1RWmxn Timing Waveforms

Single port SRAM1RWmxn functions according to the block-diagrams shown in Figures 5.10 – 5.12.

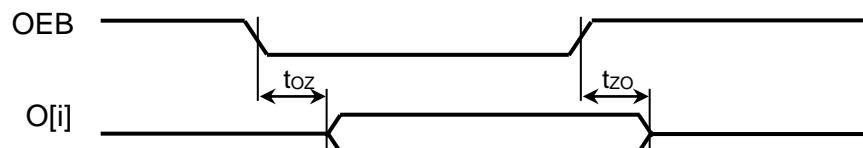


Figure 5.10. Single port SRAM1RWmxn Output-Enable Timing Waveforms

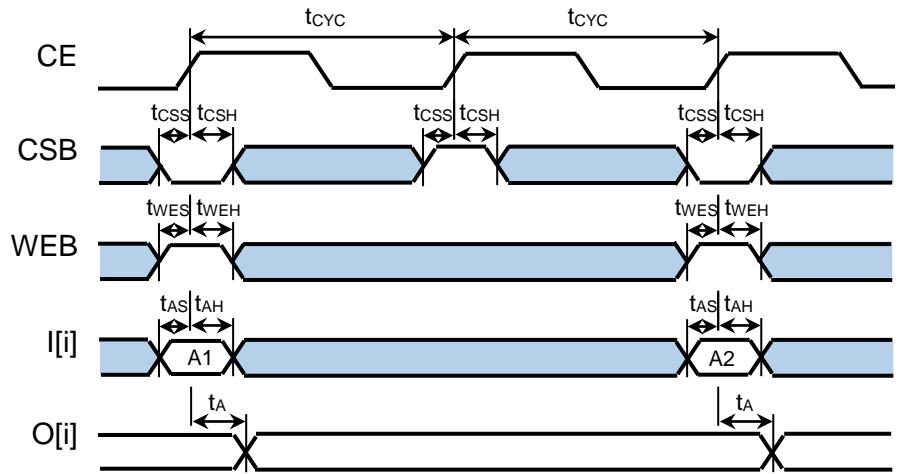


Figure 5.11. Single port SRAM1RWmxn Read-Cycle Timing Waveforms

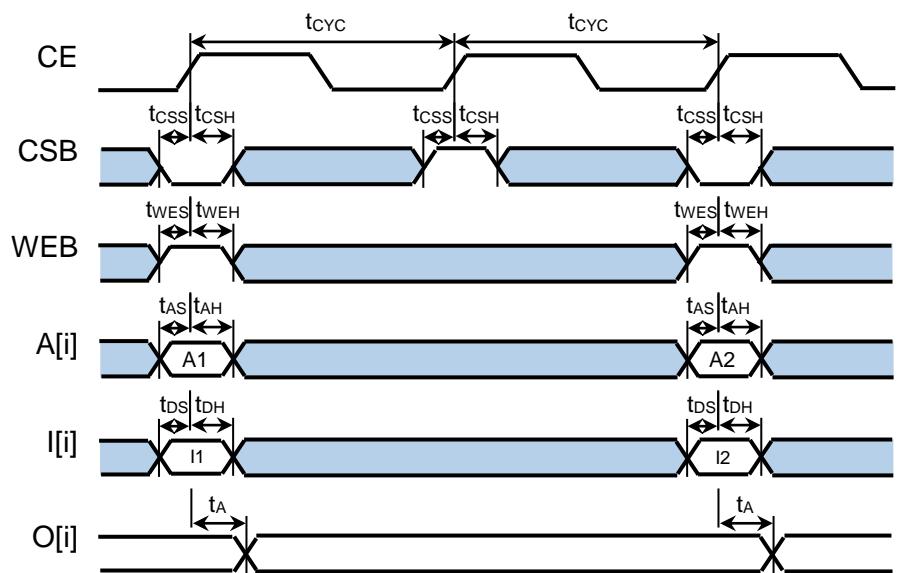


Figure 5.12. Sihgle port SRAM1RWmxn Write-Cycle Timing Waveforms

5.6. Operating conditions

The operating conditions of SAED_EDK14_FINFET_RAM set of memories are shown in Table 5.9..

Table 5.9. Operating conditions

Parameter	Min	Typ	Max	Units
Power supply (VDD) range	0.72	0.8	0.88	V
Operating Temperature	-40	+25	+125	°C
Operating Frequency (F)			1	GHz

5.7. Timing and Current Data

Table 5.10. SRAM Timing and Current Data

Parameter	Min	Max	Units
Cycle time (t _{CYC})	2		ns
Access time (t _A)		1.4	ns
A1[k-1:0]/A2[k-1:0] setup (t _{AS})	0.8		ns
A1[k-1:0]/A2[k-1:0] hold (t _{AH})	0.4		ns
CSB1/CSB2 setup (t _{CS})	0.8		ns
CSB1/CSB2 hold (t _{CSH})	0.4		ns
WEB1/WEB2 setup (t _{WE})	1.2		ns
WEB1/WEB2 hold (t _{WEH})	0.4		ns
I1[n-1:0]/I2[n-1:0] setup (t _{DS})	0.8		ns
I1[n-1:0]/I2[n-1:0] hold (t _{DH})	0.4		ns
Output enable to hi-Z (t _{OZ})		1.4	ns
Output enable active (t _{ZO})		1.4	ns
AC current (i _{AC})		0.4	mA
Standby current (i _{ACS})		0.4	mA

5.8. Characterization corners

The timing data will be given only for 3 process/voltage/temperature (PVT) conditions shown in Table 5.11.

Table 5.11. Characterization Corners

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature(°C)	Power Supply (V)	Library Name Suffix
FF	Fast – Fast	125	0.72	ff0d72v125c
FF	Fast – Fast	25	0.72	ff0d72v25c
FF	Fast – Fast	-40	0.72	ff0d72vm40c
TT	Typical – Typical	125	0.8	tt0d8v125c
TT	Typical – Typical	25	0.8	tt0d8v25c
TT	Typical – Typical	-40	0.8	tt0d8vm40c
SS	Slow – Slow	125	0.88	ss0d88v125c
SS	Slow – Slow	25	0.88	ss0d88v25c
SS	Slow – Slow	-40	0.88	ss0d88vm40c

Critical path, setup and hold analyses will be performed for the mentioned corners.

6. Set of Low Power Memories SAED_EDK14_FINFET_RAM_LP

6.1. Introduction

The SAED_EDK14_FINFET_RAM_LP set of low power memories will be designed using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V process. It will represent a set of several static RAMs (SRAMs) with small number of words (word depth – m) and bits in word (data width – n). All SRAMs, included in SAED_EDK14_FINFET_RAM_LP, will represent Synchronous Dual-Port or Single-port SRAM with Write Enable, Output Enable, Chip Select port(s). Each SRAMLPscmxn, included in the set, will have the same architecture and will differ from the rest with its $n \times m$ (width x depth) sizes. As SAED_EDK14_FINFET_RAM_LP is anticipated for the use of educational purposes, only SRAMs of the sizes, shown in Table 6.1., will be included in it. SAED_EDK14_FINFET_RAM set of memories are intended for use in low power design flow. To achieve low power consumption the following power management techniques are used:

- Reducing the supply voltage of periphery
- Reducing the supply voltage of memory core and shutting down the supply voltage of periphery
- Complete shut down of the memory during the periods of non-operation
- Switched power control (VDD power)
- Switched ground control (Vss ground)

Table 6.1. SRAMmxn Cell List

No	Data width (n)	Word depth (m)	Address width (k= $\log_2 m$)	Cell Name
1	4	16	4	SRAMLP2RWPC16x4
2	4	16	4	SRAMLP2RWGC16x4
3	4	32	5	SRAMLP2RWPC32x4
4	4	32	5	SRAMLP2RWGC32x4
5	4	64	6	SRAMLP2RWPC64x4
6	4	64	6	SRAMLP2RWGC64x4
7	4	128	7	SRAMLP2RWPC128x4
8	4	128	7	SRAMLP2RWGC128x4
9	8	16	4	SRAMLP2RWPC16x8
10	8	16	4	SRAMLP2RWGC16x8
11	8	32	5	SRAMLP2RWPC32x8
12	8	32	5	SRAMLP2RWGC32x8
13	8	64	6	SRAMLP2RWPC64x8
14	8	64	6	SRAMLP2RWGC64x8
15	8	128	7	SRAMLP2RWPC128x8
16	8	128	7	SRAMLP2RWGC128x8
17	16	16	4	SRAMLP2RWPC16x16
18	16	16	4	SRAMLP2RWGC16x16
19	16	32	5	SRAMLP2RWPC32x16
20	16	32	5	SRAMLP2RWGC32x16
21	16	64	6	SRAMLP2RWPC64x16
22	16	64	6	SRAMLP2RWGC64x16
23	16	128	7	SRAMLP2RWPC128x16
24	16	128	7	SRAMLP2RWGC128x16
25	32	16	4	SRAMLP2RWPC16x32
26	32	16	4	SRAMLP2RWGC16x32

No	Data width (n)	Word depth (m)	Address width (k= $\log_2 m$)	Cell Name
27	32	32	5	SRAMLP2RWPC32x32
28	32	32	5	SRAMLP2RWGC32x32
29	32	64	6	SRAMLP2RWPC64x32
30	32	64	6	SRAMLP2RWGC64x32
31	32	128	7	SRAMLP2RWPC128x32
32	32	128	7	SRAMLP2RWGC128x32
33	8	128	7	SRAMLP1RWPC128x8
34	8	128	7	SRAMLP1RWGC128x8
35	32	64	6	SRAMLP1RWPC64x32
36	32	64	6	SRAMLP1RWGC64x32
37	22	32	5	SRAMLP2RWPC32x22
38	22	32	5	SRAMLP2RWGC32x22
39	39	32	5	SRAMLP2RWPC32x39
40	39	32	5	SRAMLP2RWGC32x39
41	32	256	8	SRAMLP1RWPC256x32
42	32	256	8	SRAMLP1RWGC256x32
43	8	1024	10	SRAMLP1RWPC102x84
44	8	1024	10	SRAMLP1RWGC102x84
45	8	512	9	SRAMLP1RWPC512x8
46	8	512	9	SRAMLP1RWGC512x8
47	48	128	7	SRAMLP1RWPC128x48
48	48	128	7	SRAMLP1RWGC128x48
49	50	32	5	SRAMLP1RWPC32x50
50	50	32	5	SRAMLP1RWGC32x50
51	34	64	6	SRAMLP1RWPC64x34
52	34	64	6	SRAMLP1RWGC64x34
53	46	256	8	SRAMLP1RWPC256x46
54	46	256	8	SRAMLP1RWGC256x46
55	46	128	7	SRAMLP1RWPC128x46
56	46	128	7	SRAMLP1RWGC128x46
57	8	64	6	SRAMLP1RWPC64x8
58	8	64	6	SRAMLP1RWGC64x8
59	128	64	6	SRAMLP1RWPC64x128
60	128	64	6	SRAMLP1RWGC64x128
61	128	256	8	SRAMLP1RWPC256x128
62	128	256	8	SRAMLP1RWGC256x128
63	8	256	8	SRAMLP1RWPC256x8
64	8	256	8	SRAMLP1RWGC256x8
65	48	256	8	SRAMLP1RWPC256x48
66	48	256	8	SRAMLP1RWGC256x48
67	128	512	9	SRAMLP1RWPC512x128
68	128	512	9	SRAMLP1RWGC512x128
69	32	512	9	SRAMLP1RWPC512x32
70	32	512	9	SRAMLP1RWGC512x32

All memories in the set are named according to the following template (Fig. 3.1):

6.1. SRAM naming conventions



Figure 6.1. Memories naming template

The template contains symbols denoting specifics of the memory, the descriptions of the symbols are given in Table 6.2.

Table 6.2. Memories naming conventions

Symbol	Description	Values
p	Number of access ports	1,2
n	Number of words	Integer number, 2^n
w	Word size	Integer, various
sc	Supply control	pc(power control),gc(ground control)

6.2. General Information

The Synchronous Dual-Port SRAMLPscmxn will have two ports (Primary and Dual) for the same memory location. Both ports can be independently accessed for read or write operations. Single-port cells have only one port.

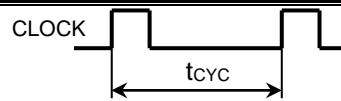
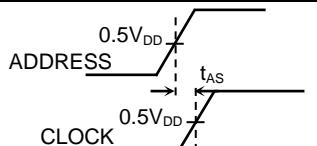
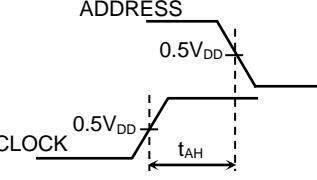
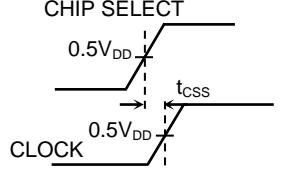
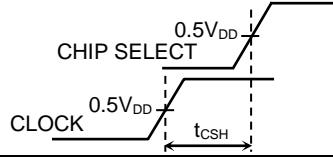
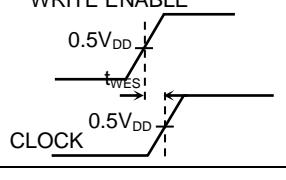
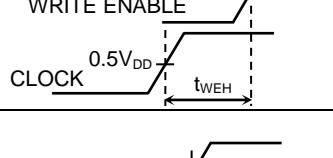
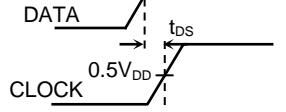
The used symbols of SRAMLPscmxn states are shown in Table 6.3.

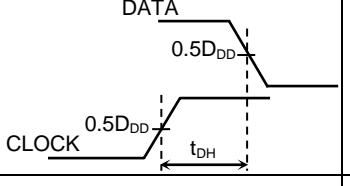
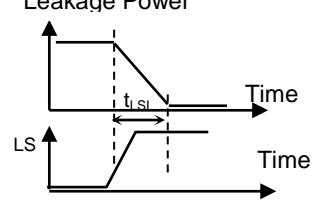
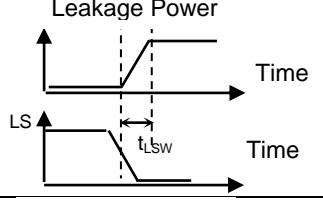
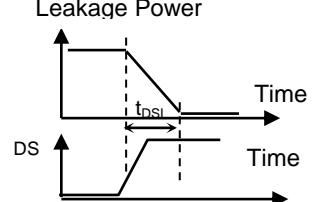
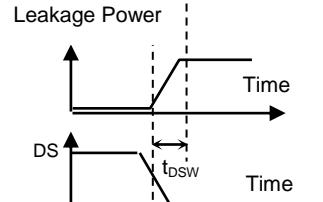
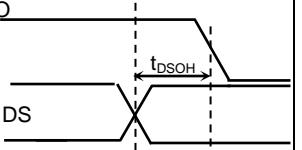
Table 6.3. Symbols of SRAMLPscmxn states

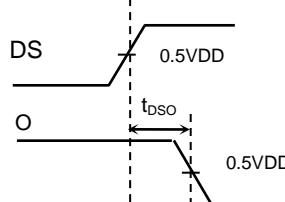
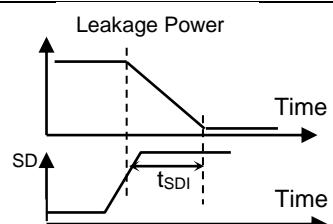
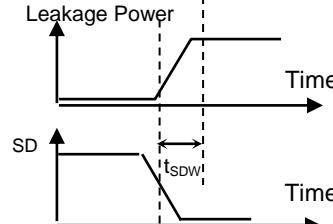
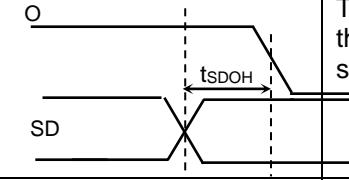
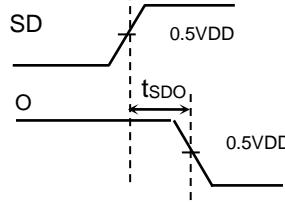
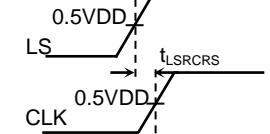
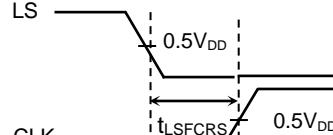
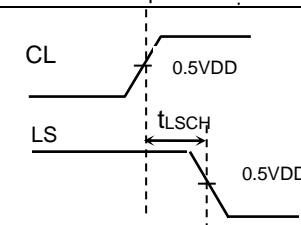
Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIGH Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

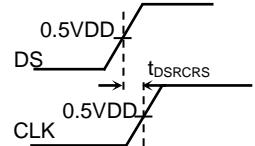
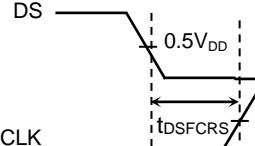
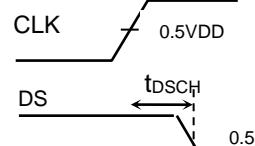
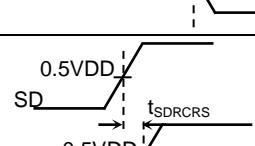
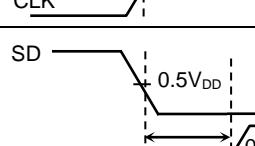
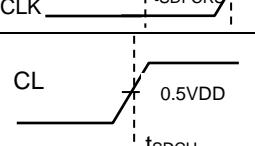
Parameters and measurement conditions of SRAMLPscmxn, included in SAED_EDK14_FINFET_RAM_LP set of memories, are shown in Table 6.4.

Table 6.4. Parameters and measurement conditions of SRAMLPscmxn

No	Parameter	Unit	Symbol	Figure	Definition
Timing parameters					
19	Cycle time	ns	t _{CYC}		The amount of time between two sequential active edges of clock signal
20	Access time	ns	t _A	None	The amount of time between applying Write/Read Enable signal and obtaining Access to Data in Memory
21	Address setup	ns	t _{AS}		The minimum amount of time in which the address to a SRAMmxn must be stable before the active edge of the clock occurs
22	Address hold	ns	t _{AH}		The minimum amount of time in which the address to a SRAMmxn must remain stable after the active edge of the clock has occurred
23	Chip select setup	ns	t _{CSS}		The minimum amount of time in which the Chip select signal to a SRAMmxn must be stable before the active edge of the clock occurs
24	Chip select hold	ns	t _{CSH}		The minimum amount of time in which the Chip select signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
25	Write enable setup	ns	t _{WES}		The minimum amount of time in which the Write enable signal to a SRAMmxn must be stable before the active edge of the clock occurs
26	Write enable hold	ns	t _{WEH}		The minimum amount of time in which the Write enable signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
27	Data setup	ns	t _{DS}		The minimum amount of time in which the input data to a SRAMmxn must be stable before the active edge of the clock occurs

No	Parameter	Unit	Symbol	Figure	Definition
28	Data hold	ns	t_{DH}		The minimum amount of time in which the input data to a SRAMmxn must remain stable after the active edge of the clock has occurred
29	Output Z state entry time	ns	t_{OZ}	None	The amount of time that takes the outputs to change to Z state after output enable signal is applied
30	Output Z state exit time	ns	t_{ZO}	None	The amount of time that takes the outputs to exit from Z state after output enable signal is applied
Low Power control measurements					
31	LS active to memory low leakage state	ns	t_{LSI}		The minimum amount of time LS signal must remain active till memory goes into low leakage mode
32	LS inactive to memory wake up from low leakage state	ns	t_{LSW}		The minimum amount of time LS signal must remain inactive till memory wakes up from low leakage mode.
33	DS active to memory low leakage state	ns	t_{DSI}		The minimum amount of time DS signal must remain active till memory goes into low leakage mode.
34	DS inactive to memory wake up from low leakage state	ns	t_{DSW}		The minimum amount of time DS signal must remain inactive till memory wakes up from low leakage mode.
35	O hold time after DS High/Low	ns	t_{DSOH}		The maximum amount of time the output remains stable after switching of DS signal.

No	Parameter	Unit	Symbol	Figure	Definition
36	DS rise to O falling delay	ns	t_{DSO}		Delay between positive edge of DS and negative edge of output.
37	SD active to memory low leakage state	ns	t_{SDI}		The minimum amount of time SD signal must remain active till memory goes into low leakage mode
38	SD inactive to memory wake up from low leakage state	ns	t_{SDW}		The minimum amount of time SD signal must remain inactive till memory wakes up from low leakage mode.
39	O hold time after SD High/Low	ns	t_{SDOH}		The maximum amount of time the output remains stable after switching of SD signal.
40	SD rise to O falling delay	ns	t_{SDO}		Delay between positive edge of SD and negative edge of output
41	LS rise setup time before CLK rises	ns	t_{LSRCRS}		The minimum amount of time in which the LS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
42	LS fall setup time before CLK rises	ns	t_{LSFCRS}		The minimum amount of time in which the LS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
43	LS hold time after CLK rises	ns	t_{LSCH}		The minimum amount of time in which the LS signal to a SRAMLPscmxn must remain stable after the active edge of the clock has occurred

No	Parameter	Unit	Symbol	Figure	Definition
44	DS rise setup time before CLK rises	ns	t_{DSRCRS}		The minimum amount of time in which the DS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
45	DS fall setup time before CLK rises	ns	t_{DSFCRS}		The minimum amount of time in which the DS signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
46	DS hold time after CLK rises	ns	t_{DSCH}		The minimum amount of time in which the DS signal to a SRAMLPscmxn must remain stable after the active edge of the clock has occurred
47	SD rise setup time before CLK rises	ns	t_{SDRCRS}		The minimum amount of time in which the SD signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
48	SD fall setup time before CLK rises	ns	t_{SDFCRS}		The minimum amount of time in which the SD signal to a SRAMLPscmxn must be stable before the active edge of the clock occurs
49	SD hold time after CLK rises	ns	t_{SDCH}		The minimum amount of time in which the SD signal to a SRAMLPscmxn must remain stable after the active edge of the clock has occurred
Power parameters					
50	AC current	mA	i_{AC}	None	Average value of dynamic current for read/write operations
51	Read AC current	mA	i_{ACR}	None	Dynamic current for read operation
52	Write AC current	mA	i_{ACW}	None	Dynamic current for write operation
53	Peak current	mA	i_{ACP}	None	Maximum value of dynamic current for read/write operations
54	Deselected current	mA	i_{ACD}	None	The value of current when SRAMLPscmxn is disabled, all addresses switch and 50% of data input switch
55	Standby current	mA	i_{ACS}	None	The value of current in standby mode when all inputs and outputs are stable

6.3. Dual port SRAMs

6.3.1. Basic Pins

The Basic Pins of dual port SRAMLPscmxn are shown in Figure 6.2 and its descriptions are shown in Table 6.5.

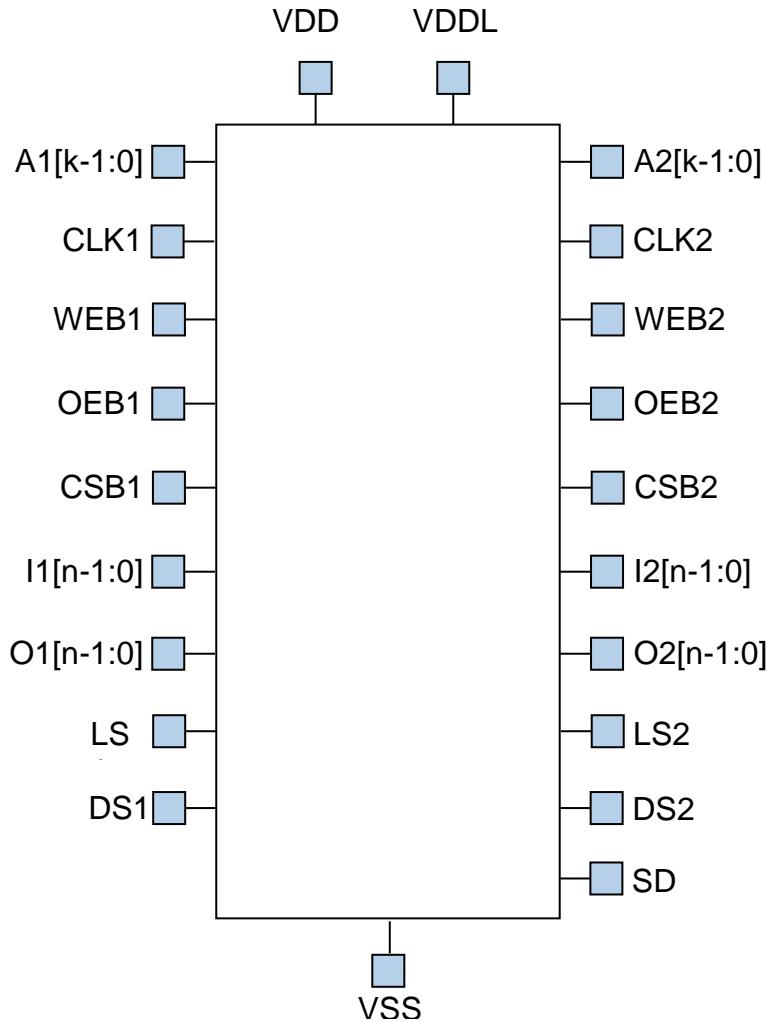


Figure 6.2. Dual port SRAMLPscmxn Basic Pins

Table 6.5. Dual port SRAMLPscmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A1	K	Input	Primary Read/Write Address
CLK1	1	Input	Primary Positive-Edge Clock
WEB1	1	Input	Primary Write Enable, Active Low
OEB1	1	Input	Primary Output Enable, Active Low
CSB1	1	Input	Primary Chip Select, Active Low
I1	N	Input	Primary Input data bus
O1	N	Output	Primary Output data bus
LS1	1	Input	Primary Light Sleep, Active High
DS1	1	Input	Primary Deep Sleep, Active High
SD1	1	Input	Primary Shut Down, Active High
A2	k	Input	Dual Read/Write Address
CLK2	1	Input	Dual Positive-Edge Clock
WEB2	1	Input	Dual Write Enable, Active Low
OEB2	1	Input	Dual Output Enable, Active Low
CSB2	1	Input	Dual Chip Select, Active Low
I2	n	Input	Dual Input data bus
O2	n	Output	Dual Output data bus
LS2	1	Input	Dual Light Sleep, Active High
DS2	1	Input	Dual Deep Sleep, Active High
SD2	1	Input	Dual Shut Down, Active High
VDD	Power supply of the memory array		
VDDL	Power supply of the periphery		
VSS	Power ground		

6.3.2. Dual port SRAMLPscmxn Description

The general block-diagram of SRAMLPscmxn is shown in Figure 6.3.

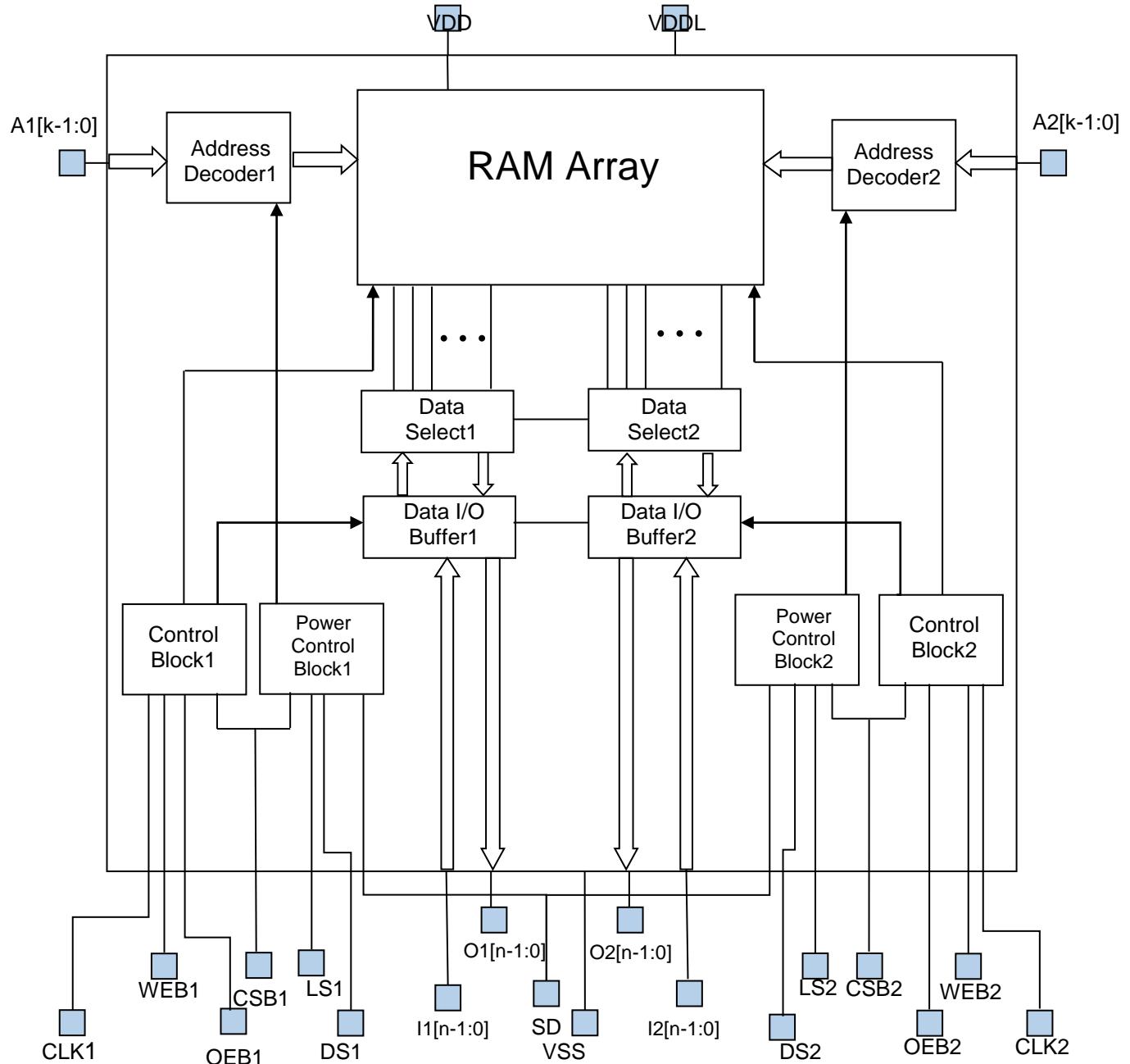


Figure 6.3. Dual port SRAMLPscmxn block diagram

Dual port SRAMLPscmxn Basic Operations is shown in Table 6.6.

Dual port SRAMLPscmxn access is synchronous and triggered by the rising edge of the clock signals (CLK1/CLK2). Read/Write addresses (A_1/A_2), Input data (I_1/I_2), Write enable (WEB1/WEB2), Light Sleep (LS1/LS2), Deep Sleep (DS1/DS2), Shut Down (SD1/SD2) and Chip select (CSB1/CSB2) signals are latched by the rising edge of the clocks (CLK1/ CLK2).

Table 6.6. Dual port SRAMLPscmxn Basic Operations

Pins									Data in Memory	Access to Memory	Operation Mode
A1[k-1:0]	WEB1	OEB1	CSB1	LS1	DS1	SD1	I1[n-1:0]	O1[n-1:0] (t+1)	D(A1[k-1:0]) (t+1)		
X	X	0	1	0	0	0	Disabled	O1[n-1:0] (t)	D(A1[k-1:0]) (t)	No	Stand by
		1		Z				Z			
X	0	0	0	0	0	0	Enabled	I1[n-1:0]	I1[n-1:0]	Yes	Write
		1		Z				Z			
X	1	0	0	0	0	0	X	D(A1[k-1:0]) (t)	D(A1[k-1:0]) (t)	No	Read
		1		Z				Z			
X	X	X	1	1	0	0	Disabled	O1[n-1:0] (t)	D(A1[k-1:0]) (t)	No	Light Sleep
X	X	X	1	0	1	0	Disabled	0	D(A1[k-1:0]) (t)	No	Deep Sleep
X	X	X	1	0	0	1	Disabled	0	Z	No	Shut Down
A2[k-1:0]	WEB2	OEB2	CSB2	LS2	DS2	SD2	I2[n-1:0]	O2[n-1:0] (t+1)	D(A2[k-1:0]) (t+1)		
X	X	0	1	0	0	0	Disabled	O2[n-1:0] (t)	D(A2[k-1:0]) (t)	No	Stand by
		1		Z				Z			
X	0	0	0	0	0	0	Enabled	I2[n-1:0]	I2[n-1:0]	Yes	Write
		1		Z				Z			
X	1	0	0	0	0	0	X	D(A2[k-1:0]) (t)	D(A2[k-1:0]) (t)	No	Read
		1		Z				Z			
X	X	X	1	1	0	0	Disabled	O2[n-1:0] (t)	D(A2[k-1:0]) (t)	No	Light Sleep
X	X	X	1	0	1	0	Disabled	0	D(A2[k-1:0]) (t)	No	Deep Sleep
X	X	X	1	0	0	1	Disabled	0	Z	No	Shut Down

Note: O1[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O1[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A1[k-1:0]) (t) is the data in the RAM location specified on the address bus A1[k-1:0] in the previous moment of time, and D(A1[k-1:0]) (t+1) in the next moment of time.

O2[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O2[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A2[k-1:0]) (t) is the data in the RAM location specified on the address bus A2[k-1:0] in the previous moment of time, and D(A2[k-1:0]) (t+1) in the next moment of time.

6.3.3. Operation modes of dual port SRAMLPscmxn

Read Mode: The value of Chip Select signal is low (CSB1/CSB2=0) for read operation. The SRAMmxn enter read mode when CS1/CS2=0 and WEB1/WEB2=1. In this mode the LS1/LS2, DS1/DS2 and SD signals are inactive. During read operations, data read from the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-1:0] and appear on the data output bus O1[n-1:0]/O2[n-1:0].

Write Mode: In Write Mode the value of Chip Select signal is low (CSB1/CSB2=0) Dual port SRAMmxn enter write mode when CSB1/CSB2=0 and WEB1/WEB2=0. In this mode the LS1/LS2, DS1/DS2 and SD signals are inactive. During write mode, data on the data input

bus I1[n-1:0]/I2[n-1:0] is being written into the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus A1[k-1:0])/D(A2[k-1:0]).

If OEB1/OEB2=1, data on the output bus O1[n-1:0]/O2[n-1:0] is placed in Z state. At that time read/write operation continues. When OEB1/OEB2=0, the data appears on the output bus O1[n-a:0]/O2[n-1:0].

Standby Mode: The Standby mode is provided to further reduce power dissipation during periods of non-operation (CSB1/CSB2=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A1[k-1:0])/D(A2[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Light Sleep Mode: When CSB1/CSB2=1 and the LS1/LS2 pin is active, the memory goes into Light Sleep mode. In this mode VDDL supply voltage of periphery is reduced down to 0.7v. In Light Sleep mode DS1/DS2, SD signals are inactive and the output state doesn't change.

Deep Sleep Mode: In this mode the value of Chip Select signal is high (CSB1/CSB2=1), and LS1/LS2 and SD signals are inactive. If DS1/DS2 pin is set, the power to periphery is shut down completely and the power to the memory core is reduced down to 0.5v. In this mode memory contents is retained, but the outputs of the memory are pulled low.

Shut Down Mode: The SRAMLPscmxn enters this mode, when the value of SD1/SD2 signal is high. When the SD pin is set, there is a complete shutdown (both the periphery and array are power gated), with no data retention, and the memory outputs are pulled low.

Address contention will occur when both ports simultaneously access the same address. In this case, both ports will read the same data.

Mentioned low power techniques differ not only with power consumption efficiency, but also with timing parameters. Table 6.10 shows the differences.

6.3.4. Dual port SRAMLPscmxn Timing Waveforms

SRAMLPscmxn will function according to the block-diagrams shown in Figures 6.5. – 6.7.

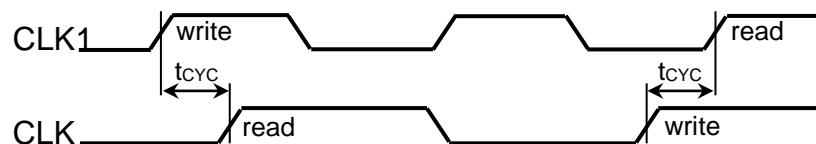


Figure 6.4. Dual port SRAMLPscmxn Write-Read Clock Timing Waveforms

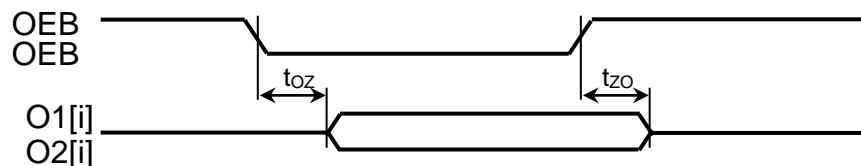


Figure 6.5. Dual port SRAMLPscmxn Output-Enable Timing Waveforms

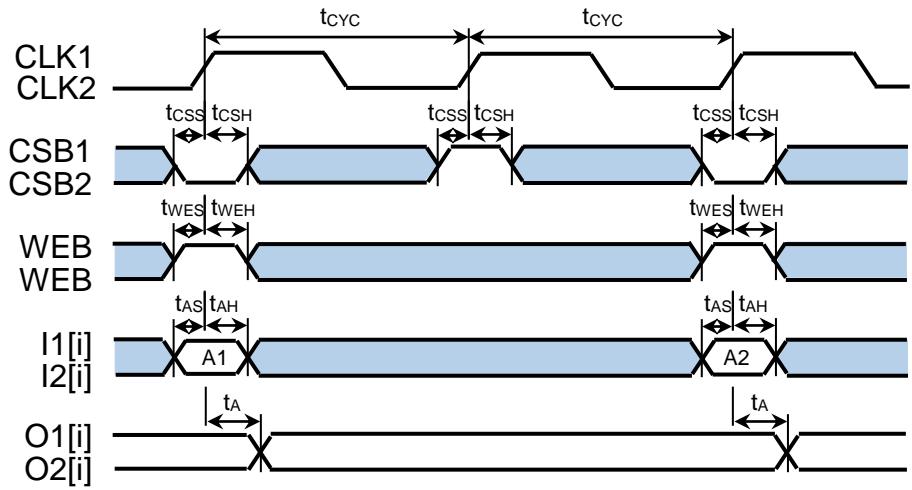


Figure 6.6. Dual port SRAMLPscmxn Read-Cycle Timing Waveforms

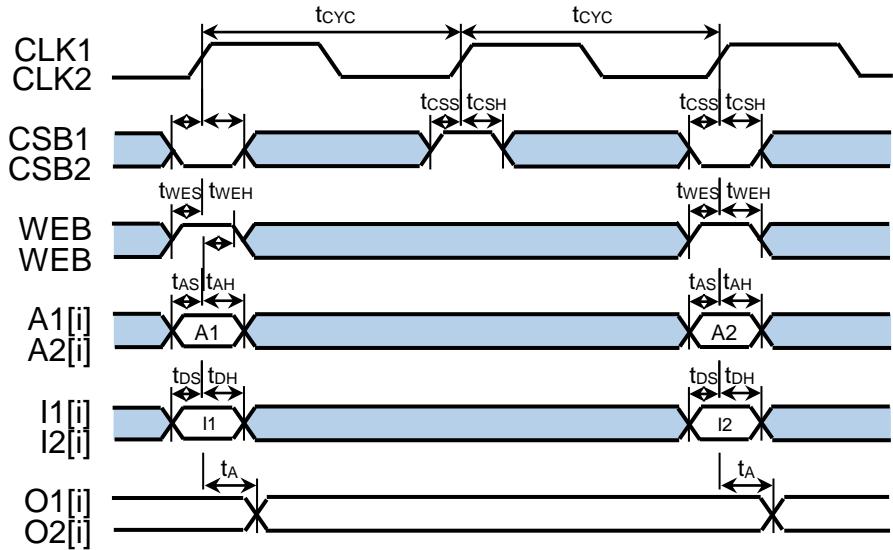


Figure 6.7. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms

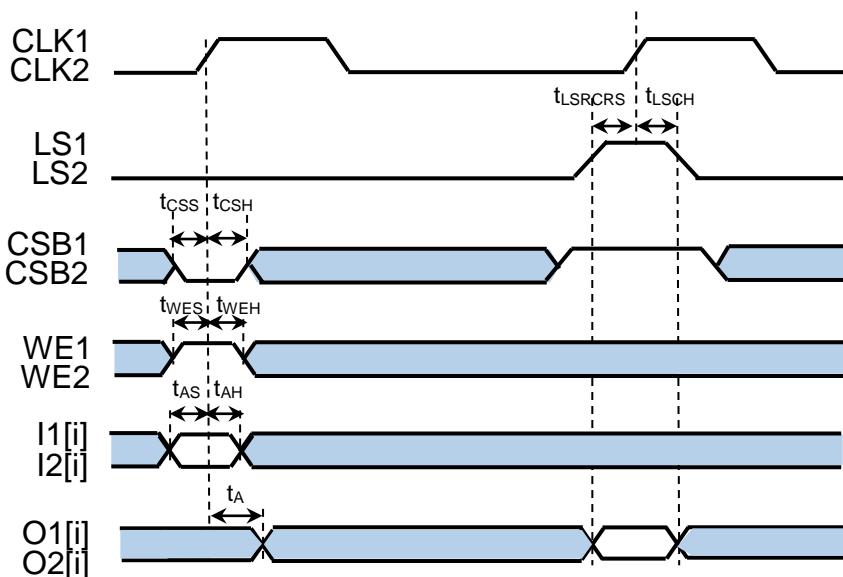


Figure 6.8. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms with Lights Sleep state

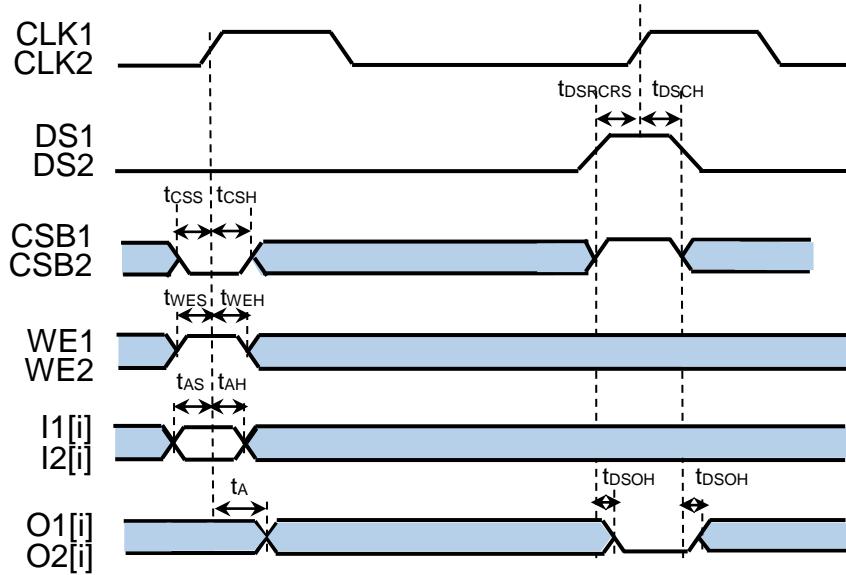


Figure 6.9. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms with Deep Sleep state

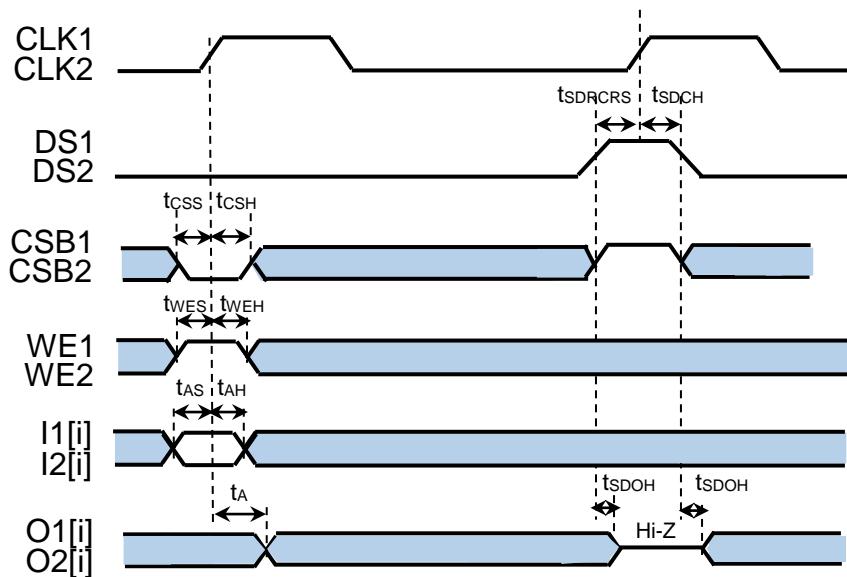


Figure 6.10. Dual port SRAMLPscmxn Write-Cycle Timing Waveforms with Shut Down state

6.4. Single port SRAMs

6.4.1. Basic Pins

The Basic Pins of single port SRAMLPscmxn are shown in Figure 6.11. and their descriptions are shown in Table 6.7.

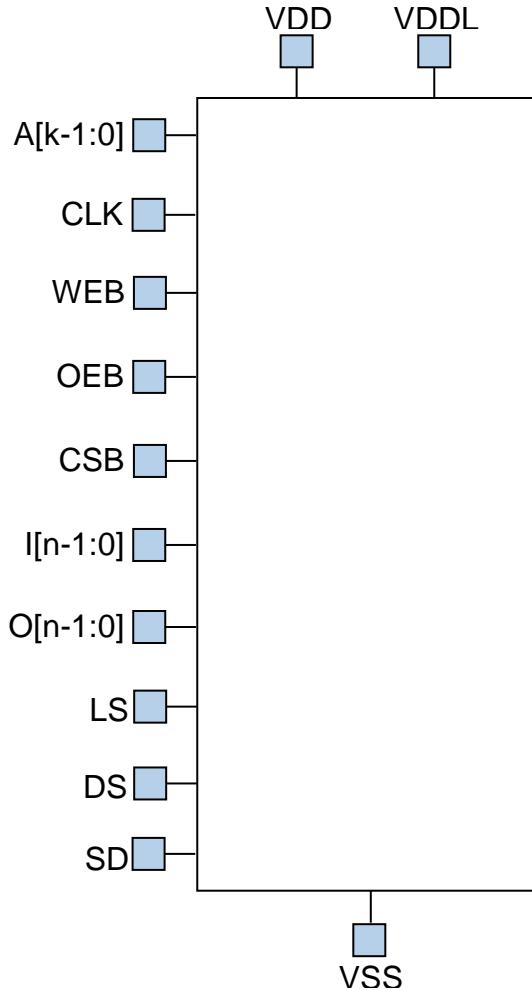


Figure 6.11 Single port SRAMLP1RWscmxn Basic Pins

Table 6.7 Single port SRAMLP1RWscmxn Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A	k	Input	Primary Read/Write Address
CLK	1	Input	Primary Positive-Edge Clock
WEB	1	Input	Primary Write Enable, Active Low
OEB	1	Input	Primary Output Enable, Active Low
CSB	1	Input	Primary Chip Select, Active Low
I	n	Input	Primary Input data bus
O	n	Output	Primary Output data bus
LS	1	Input	Primary Light Sleep, Active High
DS	1	Input	Primary Deep Sleep, Active High
SD	1	Input	Primary Shut Down, Active High
VDD	Power supply of the memory array		
VDDL	Power supply of the periphery		
VSS	Power ground		

6.4.2. Single port SRAMLP1RWscmxn Description

The general block-diagram of single port SRAMLP1RWscmxn is shown in Figure 6.12.

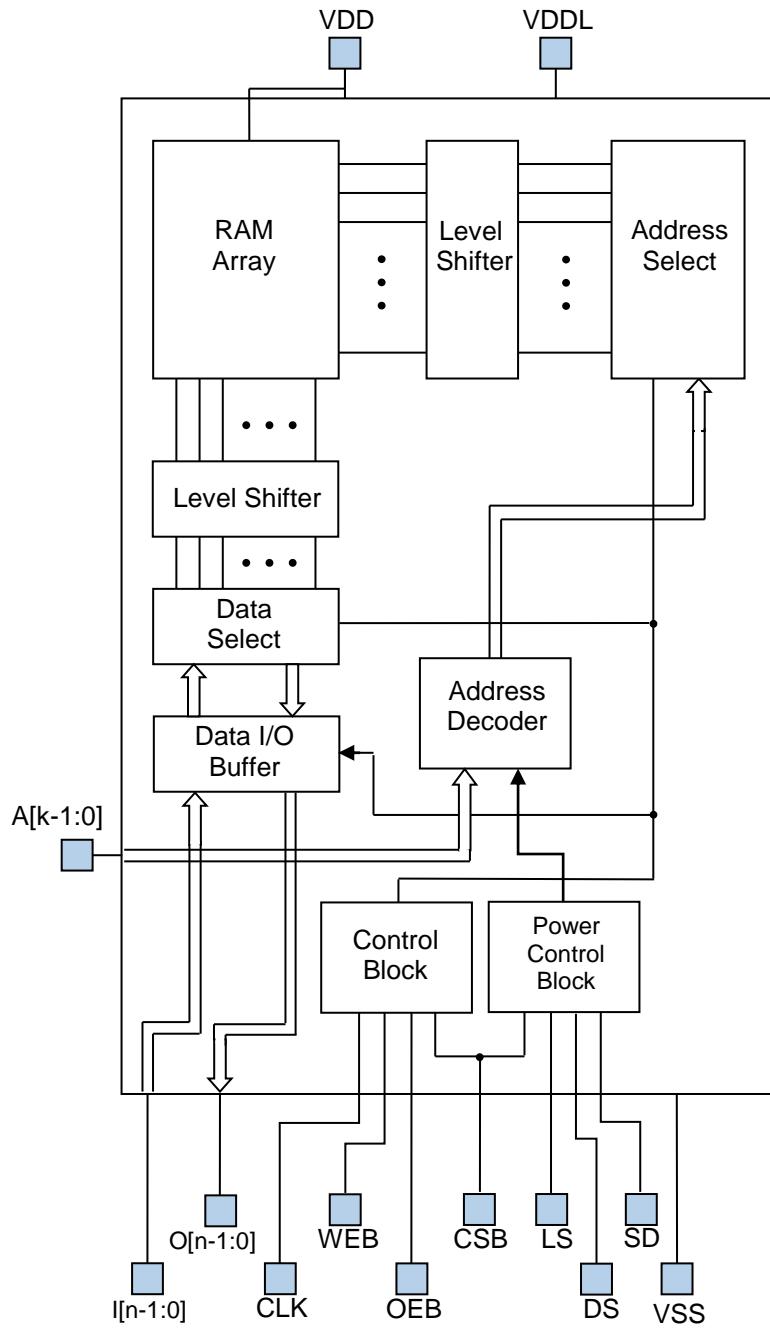


Figure 6.12. Single port SRAMLP1RWscmxn block diagram

Single port SRAMLP1RwscmxnBasic Operations is shown in Table 6.8.

Single port SRAMLP1Rwscmxnaccess is synchronous and triggered by the rising edge of the clock signal (CLK). Read/Write addresses (A), Input data (I), Write enable (WEB), Light Sleep (LS), Deep Sleep (DS), Shut Down (SD) and Chip select (CSB) signals are latched by the rising edge of the clock (CLK).

Table 6.8 Single port SRAMLP1RwscmxnBasic Operations

Pins									Data in Memory	Access to Memory	Operation	
A[k-1:0]	WEB	OEB	CSB	LS	DS	SD	I [n-1:0]	O[n-1:0] (t+1)	D(A[k-1:0]) (t+1)			
X	X	0	1	0	0	0	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Standby	
		1		Z				Z				
X	0	0	0	0	0	0	Enabled	I[n-1:0]	I[n-1:0]	Yes	Write	
		1		Z				Z				
X	1	0	0	0	0	0	X	D(A[k-1:0]) (t)	D(A[k-1:0]) (t)	No	Read	
		1		Z				Z				
X	X	X	1	1	0	0	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Light Sleep	
X	X	X	1	0	1	0	Disabled	0	D(A[k-1:0]) (t)	No	Deep Sleep	
X	X	X	1	0	0	1	Disabled	0	Z	No	Shut Down	

Note: O[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

O[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.

D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

6.4.3. Operation modes of single port SRAMLPscmxn

Read Mode: The value of Chip Select signal is low (CSB=0) for read operation. The SRAMLPscmxn enter read mode when CSB=0 and WEB=1. In this mode the LS, DS and SD signals are inactive. During read operations, data read from the memory location D(A[k-1:0]) specified on the address bus I[n-1:0] and appear on the data output bus O[n-1:0].

Normal Write Mode: In Normal Write mode the value of Chip Select signal is low (CSB=0) for write operation. Single port SRAMLPscmxn enter write mode when CSB=0 and WEB=0. In this mode the LS, DS and SD signals are inactive. During write mode, data on the data input bus I[n-1:0] is writing into the memory location D(A[k-1:0]) specified on the address bus I[n-1:0].

If OEB=1, data on the output bus O[n-1:0] placed in Z state. At that time read/write operation continues. When OEB=0, the data appear on the output bus O[n-a:0].

Standby Mode: The standby mode is provided to further reduce power dissipation during periods of non-operation (CSB=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Light Sleep Mode: When the memory is in Standby mode (CSB=1) and the LS pin is active, then the memory goes into Light Sleep mode. In this mode VDDL supply voltage of periphery is reduced down to 0.7v. In Light Sleep mode DS, SD signals are inactive and the output state doesn't change.

Deep Sleep Mode: In this mode the value of Chip Select signal is high (CSB=1) in this mode, and LS and SD signals are inactive. If DS pin is set, the power to periphery is shut down completely and the power to the memory core is reduced down to 0.5v. In this mode memory contents are retained, but the outputs of the memory are pulled low.

Shut Down Mode: The SRAMLPscmxn enters this mode, when the value of SD signal is high. When the SD pin is set, there is a complete shutdown (both the periphery and array are power gated), with no data retention, and the memory outputs are pulled low.

Mentioned low power techniques differ not only with power consumption efficiency, but also with timing parameters. The timing parameters of low power pins are shown in Table 6.10.

6.4.4. Single port SRAMLP1RwscmxnTiming Waveforms

Single port SRAMLP1Rwmxnfunctions according to the block-diagrams shown in Figures 6.13 – 6.18.

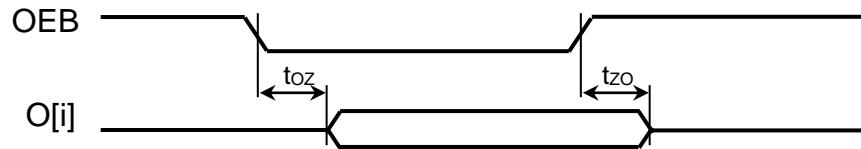


Figure 6.13. Single port SRAMLP1RwscmxnOutput-Enable Timing Waveforms

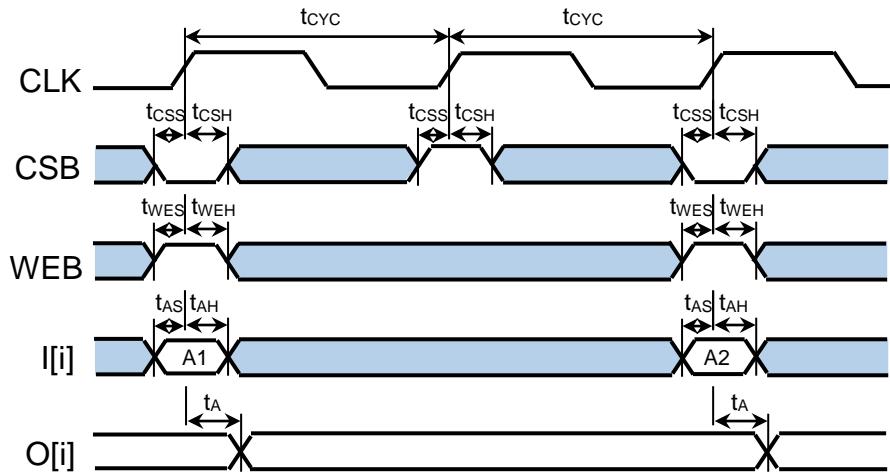


Figure 6.14. Single port SRAMLP1RWscmxn Read-Cycle Timing Waveforms

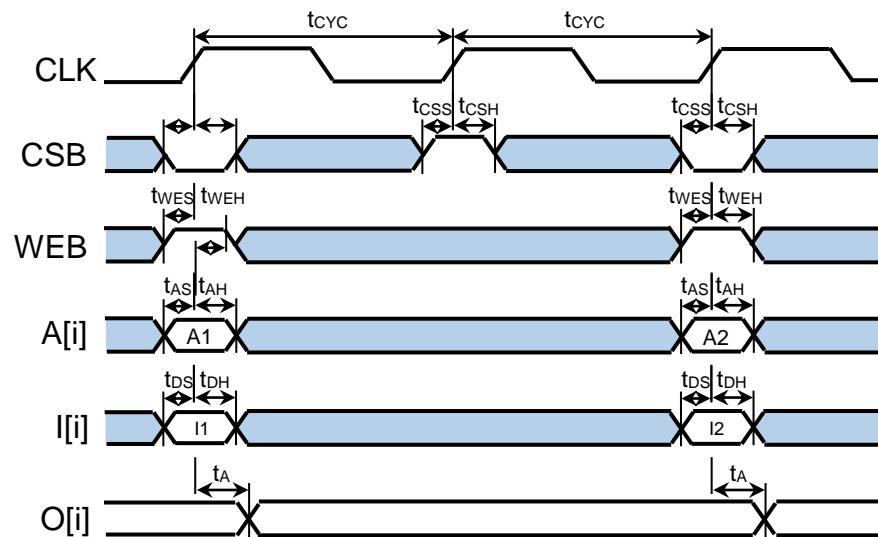


Figure 6.15. Single port SRAMLP1RWscmxn Write-Cycle Timing Waveforms

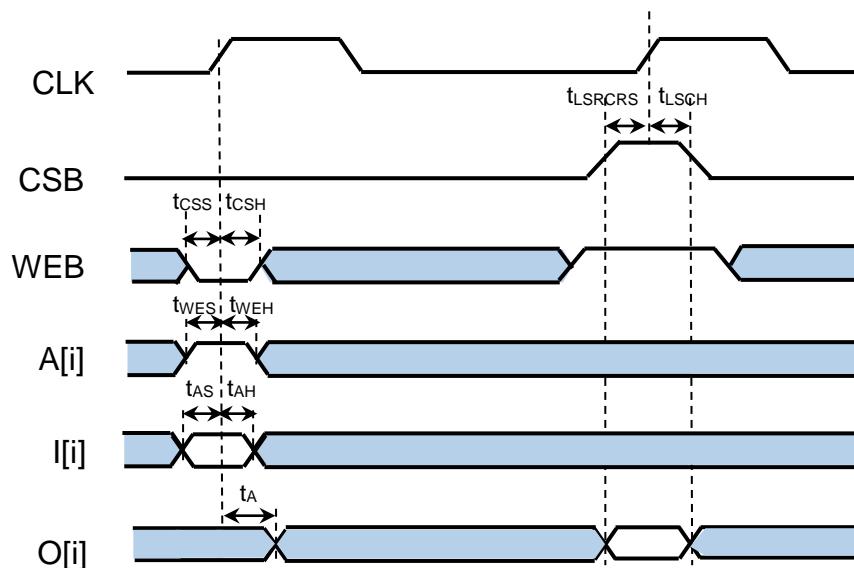


Figure 6.16. Single port SRAMLP1RWscmxn Write-Cycle Timing Waveforms with Lights Sleep state

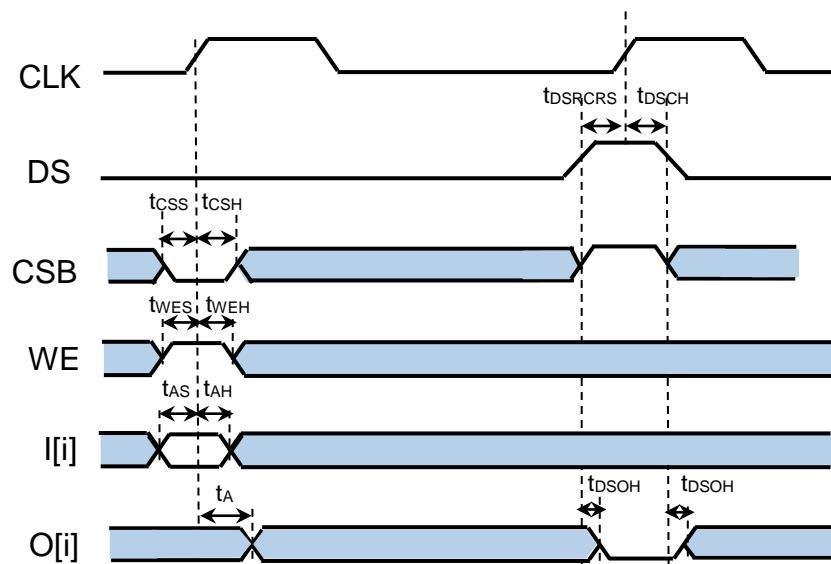


Figure 6.17. Sihgle port SRAMLP1RWscmxn Write-Cycle Timing Waveforms with Deep Sleep state

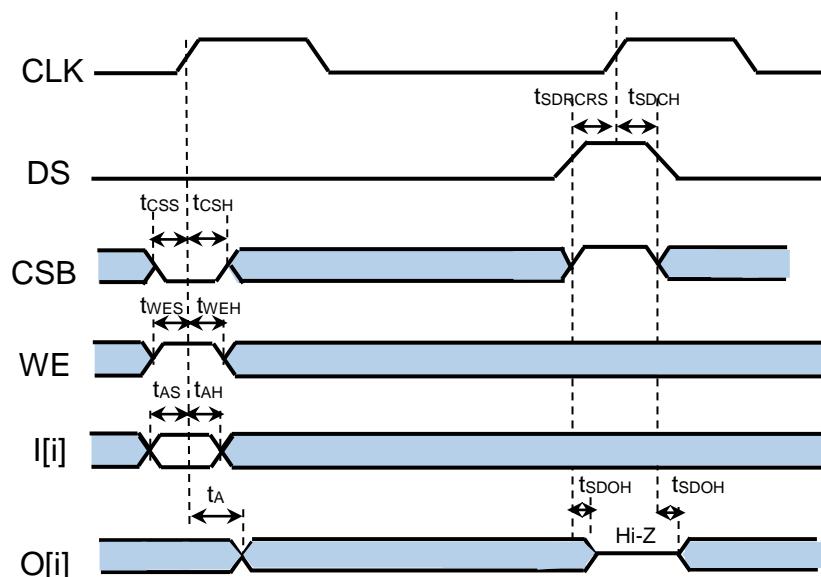


Figure 6.18. Sihgle port SRAMLP1RWscmxn Write-Cycle Timing Waveforms with Shut Down state

6.5. Operating conditions

The operating conditions of SAED_EDK14_FINFET_RAM_LP set of memories are shown in Table 6.9.

Table 6.9 Operating conditions

Parameter	Min	Typ	Max	Units
Power supply range	0.72	0.8	0.88	V
Operating Temperature	-40	+25	+125	°C
Operating Frequency (F)			1	GHz

6.6. Timing and Current Data

Table 6.10. SRAM Timing and Current Data

Parameter	Min	Max	Units
Cycle time (t_{CYC})	2		ns
Access time (t_A)		2	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.8		ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.4		ns
CSB1/CSB2 setup (t_{CSS})	0.8		ns
CSB1/CSB2 hold (t_{CSH})	0.4		ns
WEB1/WEB2 setup (t_{WES})	0.8		ns
WEB1/WEB2 hold (t_{WEH})	0.4		ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	0.8		ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.4		ns
Output enable to hi-Z (t_{OZ})		1.4	ns
Output enable active (t_{ZO})		1.4	ns
AC current (i_{AC})		0.4	mA
Standby current (i_{ACS})		0.4	mA

Table 6.11. Timing parameters of low power control pins

Description	Min	Max	Units
LS active to memory low leakage state (t_{LSI})		1.2	ns
LS inactive to memory wake up from low leakage state (t_{LSW})		1.1	ns
DS active to memory low leakage state (t_{DSI})		1.7	ns
DS inactive to memory wake up from low leakage state (t_{DSW})		1.5	ns
O hold time after DS High/Low (t_{DSOH})	0.8		ns
DS rise to O falling delay (t_{DSO})		2.6	ns
SD active to memory low leakage state (t_{SDI})		1.7	ns
SD inactive to memory wake up from low leakage state (t_{SDW})		1.6	ns
O hold time after SD High/Low (t_{SDOH})	0.8		ns
SD rise to O falling delay (t_{SDO})		2.6	ns
LS rise setup time before CLK rises (t_{LSCRCS})	0.3		ns
LS fall setup time before CLK rises (t_{LFCRS})	1.2		ns
LS hold time after CLK rises (t_{LSCH})	0.4		ns
DS rise setup time before CLK rises (t_{DSRCRS})	0.9		ns
DS fall setup time before CLK rises (t_{DSFCRS})	34		ns
DS hold time after CLK rises (t_{DSCH})	0.4		ns
SD rise setup time before CLK rises (t_{SDRCRS})	0.9		ns
SD fall setup time before CLK rises (t_{SDFCRS})	34		ns
SD hold time after CLK rises (t_{SDCH})	0.4		ns

6.7. Characterization corners

The timing data will be given only for 3 process/voltage/temperature (PVT) conditions shown in Table 6.12.

Table 6.12. Characterization Corners

#	Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Power Supply (V)	Power Supply (V)	Library Name Suffix
1	FF	ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	125
2	FF	ff0p88v125c_i0p7v	Fast-Fast	0.88	0.7	125
3	FF	ff0p7v125c_i0p7v	Fast-Fast	0.7	0.7	125
4	FF	ff0p88v25c_i0p88v	Fast-Fast	0.88	0.88	25
5	FF	ff0p88v25c_i0p7v	Fast-Fast	0.88	0.7	25
6	FF	ff0p7v25c_i0p7v	Fast-Fast	0.7	0.7	25
7	FF	ff0p88v125c_i0p88v	Fast-Fast	0.88	0.88	-40
8	FF	ff0p88v125c_i0p7v	Fast-Fast	0.88	0.7	-40
9	FF	ff0p7v125c_i0p7v	Fast-Fast	0.7	0.7	-40
10	TT	tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	125
11	TT	tt0p8v125c_i0p65v	Typical-Typical	0.8	0.65	125
12	TT	tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	125
13	TT	tt0p8v25c_i0p8v	Typical-Typical	0.8	0.8	25
14	TT	tt0p8v25c_i0p65v	Typical-Typical	0.8	0.65	25
15	TT	tt0p65v25c_i0p65v	Typical-Typical	0.65	0.65	25

#	Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Power Supply (V)	Power Supply (V)	Library Name Suffix
16	TT	tt0p8v125c_i0p8v	Typical-Typical	0.8	0.8	-40
17	TT	tt0p8v125c_i0p65v	Typical-Typical	0.8	0.65	-40
18	TT	tt0p65v125c_i0p65v	Typical-Typical	0.65	0.65	-40
19	SS	ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	125
20	SS	ss0p72v125c_i0p6v	Slow-Slow	0.72	0.6	125
21	SS	ss0p6v125c_i0p6v	Slow-Slow	0.6	0.6	125
22	SS	ss0p72v25c_i0p72v	Slow-Slow	0.72	0.72	25
23	SS	ss0p72v25c_i0p6v	Slow-Slow	0.72	0.6	25
24	SS	ss0p6v25c_i0p6v	Slow-Slow	0.6	0.6	25
25	SS	ss0p72v125c_i0p72v	Slow-Slow	0.72	0.72	-40
26	SS	ss0p72v125c_i0p6v	Slow-Slow	0.72	0.6	-40
27	SS	ss0p6v125c_i0p6v	Slow-Slow	0.6	0.6	-40

Critical path, setup and hold analyses will be performed for the mentioned corners.

7. Phase Locked Loop SAED_EDK14_FINFET_PLL

7.1. Introduction

The SAED_EDK14_FINFET_PLL phase locked loop will be designed using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V process. The SAED_EDK14_FINFET_PLL will be clock multiplier circuit that can generate a stable, high-speed clock from a slower clock signal. The SAED_EDK14_FINFET_PLL will have 3 operating modes: normal, external feedback and bypass. In the external feedback mode feedback input clock (FB_CLK) will be phase-aligned with reference input clock (REF_CLK). These aligned clocks will allow removing clock delay and skew between devices. In Bypass mode, reference clock will be bypassed to out.

7.2. General Information

Parameters and measurement conditions of the SAED_EDK14_FINFET_PLL are shown in Table 7.1.

Table 7.1. Parameters and measurement conditions of SAED_EDK14_FINFET_PLL

No	Parameter	Unit	Symbol	Figure	Definition
1	Phase error	ps	t_{PHERR}		Phase error (phase offset) is the time difference between the REF_CLK and the feedback input to the phase detector (FB) of a PLL in the lock state
2	Jitter cycle to cycle p-p	ps	$J_{\text{P-P}}$	 $J_{\text{min}} = \min_{i=1,n} \{J_i\}$ $J_{\text{max}} = \max_{i=1,n} \{J_i\}$ $J_{\text{P-P}} = J_{\text{max}} - J_{\text{min}} $	Cycle-to-cycle jitter is the difference in a clock's period from one cycle to the next
3	Bandwidth	MHz	BW		The bandwidth of a PLL is the measure of the PLL's ability to track the input clock and jitter. The closed-loop gain (A_{CL}) 3-dB frequency of the PLL determines the PLL bandwidth
4	Lock time	us	t_{LOCK}		The lock time is the minimum time required for PLL output stabilization

7.3. Operating Conditions

Operating conditions of SAED_EDK14_FINFET_PLL are shown in Table 7.2.

Table 7.2. Operating conditions

Parameter	Min	Typ	Max	Units
Analog power supply (AVDD) range	1.82	1.8	1.98	V
Digital power supply (DVDD) range	0.72	0.8	0.88	V
Operating temperature	-40	25	125	°C

7.4. Characterization corners

The characterization corners for top level are shown in Table 7.3.

Table 7.3. Characterization Corners

Corner Name	Process (NFIN proc. – PFN proc.)	Temperature (°C)	Digital Power Supply (DVDD) (V)	Analog Power Supply (AVDD) (V)	Library Name Suffix
FF	Fast – Fast	125	0.88	1.98	ff0p88v125c_1p98v
FF	Fast – Fast	25	0.88	1.98	ff0p88v25c_1p98v
FF	Fast – Fast	-40	0.88	1.98	ff0p88vm40c_1p98v
TT	Typical – Typical	125	0.8	1.8	tt0p8v25c_1p8v
TT	Typical – Typical	25	0.8	1.8	tt0p8v25c_1p8v
TT	Typical – Typical	-40	0.8	1.8	tt0p8vm40c_1p8v
SS	Slow – Slow	125	0.72	1.62	ss0p72v125c_1p62v
SS	Slow – Slow	25	0.72	1.62	ss0p72v25c_1p62v
SS	Slow – Slow	-40	0.72	1.62	ss0p72vm40c_1p62v

7.5. SAED_EDK14_FINFET_PLL Description

SAED_EDK14_FINFET_PLL will align the rising edge of the reference input clock to a feedback clock using the phase-frequency detector (PFD). The falling edges will be determined by the duty-cycle specifications. The PFD will produce an up (UP) or down (DN) signal that will determine whether the voltage controlled oscillator (VCO) will need to operate at a higher or lower frequency.

The PFD output will be applied to the Charge pump (CP) and Low pass filter (LPF), which will produce a control voltage for setting the VCO frequency. If the PFD produces an UP signal, then the VCO frequency will increase. A DN signal will decrease the VCO frequency. If the CP receives an UP signal, current will be driven into the LPF. Conversely, if it receives a DN signal, current will be drawn from the LPF.

The LPF will convert these UP and DN signals to a voltage that will be used to bias the VCO. The LPF will also remove glitches from the CP and will prevent voltage over-shoot, which will filter the jitter on the VCO.

The voltage from the LPF will determine how fast the VCO will operate. A Feedback divide counter will be inserted in the feedback loop to increase the VCO frequency above the input reference frequency. VCO frequency (f_{vco_out}) will be equal to 5 times of the input reference

clock (f_{REF_CLK}). The feedback clock (f_{FB}) applied to one input of the PFD will be locked to the f_{REF_CLK} that will be applied to the other input of the PFD.

The VCO output will feed up to two post-scale counters (Output dividers). These post-scale counters will allow a number of harmonically related frequencies to be produced within the PLL.

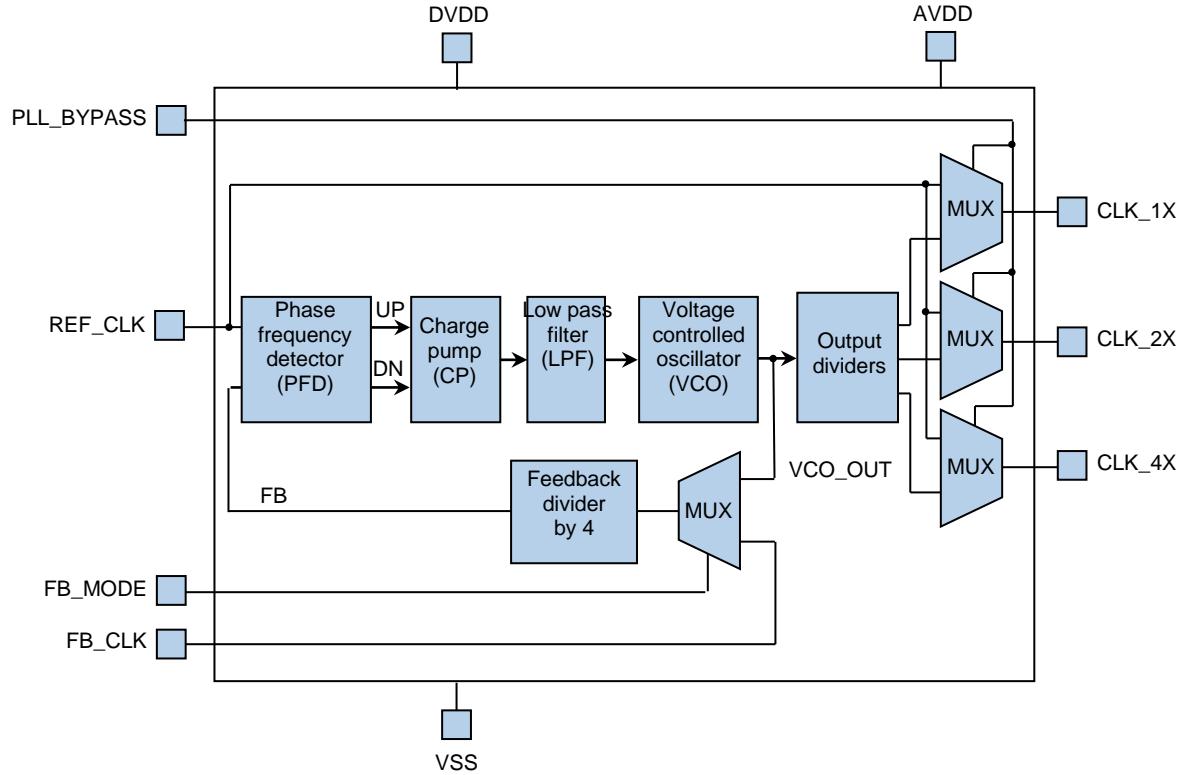


Figure 7.1. SAED_EDK14_FINFET_PLL block diagram

Electrical data of SAED_EDK14_FINFET_PLL are shown in Table 7.4.

Table 7.4. Electrical data

Parameter	Min	Typ	Max	Units
Output frequency		1800		MHz
Input frequency		450		MHz
Phase error		40	70	Ps
Jitter cycle to cycle p-p (100 cycles)			14	Ps
Analog power supply current			5	mA
Digital power supply current			3	mA
Bandwidth	1			MHz
Lock time	40	80		Us
Input duty cycle	40	50	60	%
Output duty cycle	45	50	55	%

Cell Pin Definition of SAED_EDK14_FINFET_PLL is shown in Table 7.5.

Table 7.5. Cell Pin Definition

Symbol	Name and Function
REF_CLK	Reference clock signal
FB_CLK	External feedback clock
FB_MODE	Mode selection input
PLL_BYPASS	Bypass signal
CLK_1X	1x frequency output
CLK_2X	2x frequency output
CLK_4X	4x frequency output
DVDD	Digital supply
VSS	Ground
AVDD	Analog supply

The SAED_EDK14_FINFET_PLL will be designed to generate 450 MHz (CLK_1X), 900 MHz (CLK_2X) and 1.8 GHz (CLK_4X) clock signals from a lower frequency 450 MHz clock reference signal (REF_CLK). Typical input clock source is crystal oscillator. Analog power (AVDD) will be provided.

The SAED_EDK14_FINFET_PLL will have three operation modes, shown in Table 7.6.

Table 7.6. Operation Modes

Pin	Operation Mode		
	Normal	Bypass	External feedback
PLL_BYPASS	0	1	0
FB_MODE	0	X	1
CLK_1X	450 MHz	450 MHz	450 MHz
CLK_2X	900 MHz	450 MHz	900 MHz
CLK_4X	1800 MHz	900 MHz	1800 MHz

7.6. Deliverables

Table 7.7. List of deliverables

N	Type	Description
1	.pdf	Databook / User guide, Layer usage file
2	.db, .lib	Synthesis
3	.v	Verilog simulation models
4	.cdl, .sp	LVS, HSPICE netlists
5	.spf	Extracted C and RC netlists for different corners
6	.gds	GDSII layout views
7	.lef	LEF files
8	.FRAM, .CEL	FRAM views, layout views

8. OpenSPARC Megacells SAED_EDK14_FINFET_RAM_OS

8.1. Introduction

This specification contain information about OpenSPARC Megacells that will be designed using SAED14nm FinFET 1P9M 0.8V/1.5V/1.8V technology. These megacells will include various register files, translation lookaside buffers (TLBs), content-addressable memory (CAM), Level 2 cache (L2-cache), and arrays needed for OpenSPARC processor implementation.

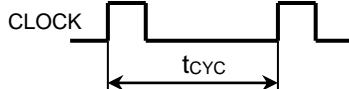
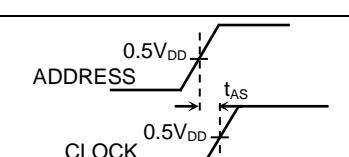
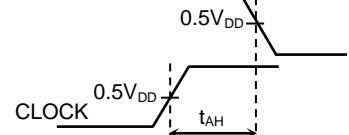
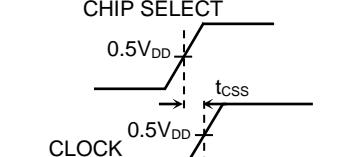
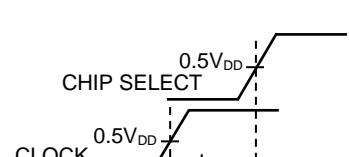
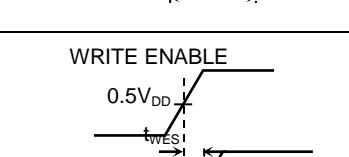
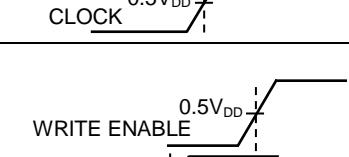
Table 8.1. OpenSPARC Megacells list

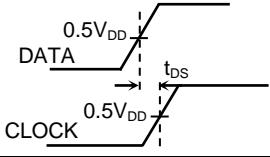
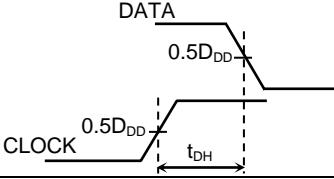
No	Functional name	Cell Name	Type	Size	Ports
1	Data Cache (Data)	br_r_dcd	SRAM	9KB = 128 entries x 4 way x 16B x 9b	1
2	FP register file	bw_r_frf	SRAM	8KB (128 x 78b)	1
3	Instruction Cache (Data)	bw_r_icd	SRAM	16KB (32B line, 4 way)	1
4	I and D cache tag	bw_r_idct	SRAM	128 entry x 33b x 4 way	1
5	Integer register file	bw_r_irf	RF	32 entry x 72bit x 4 threads	3 Read, 2 Write
6	Store buffer	bw_r_scm	CAM	Bank1: 32 entries x 38b, Bank2: 32 entries x 8b	1 look-up, 1 R/W
7	iTLB, dTLB	bw_r_tlb	CAM	64-entry x 59 bits	1
8	Reg file	bw_r_rf16x128d	RF	16 entry x 128b	1 read, 1 write
9	Reg file	bw_r_rf16x160	RF	16 entry x 160b	1 read, 1 write
10	Reg file	bw_r_rf16x32	RF	16 entry x 32b	1 read, 1 write
11	Reg file	bw_r_rf32x108	RF	32 entry x 108b	1 read, 1 write
12	Reg file	bw_r_rf32x152b	RF	32 entry x 152b	1 read, 1 write
13	Reg file	bw_r_rf32x80	RF	32 entry x 80b	1 read, 1 write
14	Reg file	bw_r_rf16x65	RF	16 entry x 65b	1 read, 1 write
15	Reg file	bw_r_rf16x81	RF	16 entry x 81b	1 read, 1 write
16	Dual port CAM	bw_r_cm_16x40	CAM	16 entry x 40bit	1 look-up, 1 Read, 1 Write port
17	Dual port CAM	bw_r_cm_16x40b	CAM	16 entry x 40bit	1 look-up, 1 Read, 1 Write port
18	Reverse directory	bw_r_dcm	CAM	64 entries x 32b	1 look-up, 1 Read, 1 write port
19	Fuse Array	bw_r_efc	SRAM	64x32	1
20	L2 data	bw_r_l2d	SRAM	3MB, 4 banks	1
21	L2 tag	bw_r_l2t	SRAM	12 ways x 1024 entries x 28b	1

8.2. General Information

Parameters and measurement conditions of megacells, included in SAED_EDK14_FINFET_RAM_OS set, are shown in Table 8.2.

Table 8.2. Parameters and measurement conditions of SRAMs

No	Parameter	Unit	Symbol	Figure	Definition
Timing parameters					
1	Cycle time	ns	t _{CYC}		The amount of time between two sequential active edges of clock signal
2	Access time	ns	t _A	None	The amount of time between applying Write/Read Enable signal and obtaining Access to Data in Memory
3	Address setup	ns	t _{AS}		The minimum amount of time in which the address to a SRAMmxn must be stable before the active edge of the clock occurs
4	Address hold	ns	t _{AH}		The minimum amount of time in which the address to a SRAMmxn must remain stable after the active edge of the clock has occurred
5	Chip select setup	ns	t _{CSS}		The minimum amount of time in which the Chip select signal to a SRAMmxn must be stable before the active edge of the clock occurs
6	Chip select hold	ns	t _{CSH}		The minimum amount of time in which the Chip select signal to a SRAMmxn must remain stable after the active edge of the clock has occurred
7	Write enable setup	ns	t _{WES}		The minimum amount of time in which the Write enable signal to a SRAMmxn must be stable before the active edge of the clock occurs
8	Write enable hold	ns	t _{WEH}		The minimum amount of time in which the Write enable signal to a SRAMmxn must remain stable after the active edge of the clock has occurred

No	Parameter	Unit	Symbol	Figure	Definition
9	Data setup	ns	t_{DS}		The minimum amount of time in which the input data to a SRAMmxn must be stable before the active edge of the clock occurs
10	Data hold	ns	t_{DH}		The minimum amount of time in which the input data to a SRAMmxn must remain stable after the active edge of the clock has occurred
11	Output Z state entry time	ns	t_{OZ}	None	The amount of time that takes the outputs to change to Z state after output enable signal is applied
12	Output Z state exit time	ns	t_{ZO}	None	The amount of time that takes the outputs to exit from Z state after output enable signal is applied

Power parameters

13	AC current	mA	i_{AC}	None	Average value of dynamic current for read/write operations
14	Read AC current	mA	i_{ACR}	None	Dynamic current for read operation
15	Write AC current	mA	i_{ACW}	None	Dynamic current for write operation
16	Peak current	mA	i_{ACP}	None	Maximum value of dynamic current for read/write operations
17	Deselected current	mA	i_{ACD}	None	The value of current when SRAMmxn is disabled, all addresses switch and 50% of data input switch
18	Standby current	mA	i_{ACS}	None	The value of current in standby mode when all inputs and outputs are stable

8.3. Operating Conditions

The operating conditions of are shown in Table 8.3.

Table 8.3. Operating conditions

Parameter	Min	Typ	Max	Units
Power supply range	0.72	0.8	0.88	V
Operating temperature	-40	25	125	°C

Table 8.4. Characterization Corners

Corner Name	Process (NFIN proc. – PFIN proc.)	Temperature (°C)	Power Supply (V)	Library Name Suffix
FF	Fast – Fast	-40	0.88	ff0p88_m40c
TT	Typical – Typical	25	0.8	tt0p8_25c
SS	Slow – Slow	125	0.72	ss0p72_125c

8.4. Deliverables

Table 8.5. List of deliverables

N	Type	Description
1	.pdf	Databook / User guide, Layer usage file
2	.db, .lib	Synthesis
3	.v	Verilog simulation models
4	.cdl, .sp	LVS, HSPICE netlists
5	.spf	Extracted C and RC netlists for different corners
6	.gds	GDSII layout views
7	.lef	LEF files
8	.FRAM, .CEL, NDM	FRAM views, layout views