Design for testability

Lab Manual

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Lab Instructions

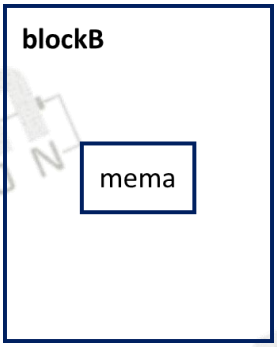
1. The recommended editor is vi or gvim editor.
2. Mentor Graphics Tessent tool is used to insert DFT logic & Questasim is used to run the test pattern simulation. [***Mentor Graphics, Tessent & Questa are the registered trademark of Mentor Graphics***]
3. The following directory structure is followed for all the lab exercises:

   libs/ - contains design, cell & simulation libraries
   design/ - contains the source either as RTL or gate-level netlist
   tsdb/ - contains sub-directories, files related to DFT flow
   simulation_outdir/ - contains simulation log files
4. We use the dofile.do script to implement the DFT flow.
5. For any technical support to do the lab exercises, please reach out to us on tech_support@maven-silicon.com

Lab - 1: Memory BIST

Objective : *Understand the DFT flow for inserting MBIST.*

Introduction : There is a blockB which is a single level of hierarchy which has a memory instance i.e memA. clkb is the functional clock for blockB.



Working Directory : Tessent_labs/Lab1/

Dofile script : dofile.do

Instructions : The following instructions have been included in the script as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT
  - This is done to set the primary context to DFT as DFT instrument has to be inserted i.e MBIST.
- ✓ Create the TSDB directory
  - This directory is created automatically during DFT flow.
- ✓ Read the cell library files
  - The I/O cell library needs to be read.
- ✓ Read the design source codes & memory files
  - The RTL & memory files needs to be read.
- ✓ Elaborate the design top
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
- ✓ Set the design level to sub-block level
  - The memory block to which MBIST is inserted is a sub-block.
- ✓ Specify the DFT requirement
  - Here the MBIST needs to be turned on and a clock needs to be added for the MBIST.
- ✓ Verify the DFT requirement
  - DRC i.e design rule check is performed to validate the DFT requirements.
- ✓ Create & report the DFT specification
  - After a successful DRC run, create DFT specification & report the same on the Tessent shell.
- ✓ Display the DFT specification
  - This is going to open the GUI interface of the DFT visualizer and you will see the specification as IJTAG network & MBIST.
- ✓ Insert the DFT instruments

- This is going to insert the DFT components and a modified RTL file is created inside the TSDB directory.

✓ Display the visualizer
- This will display the added DFT components using the DFT visualizer.

✓ Extract the ICL
- This will generate the .icl(Instrument connectivity language), .pdl(procedural description language), .sdc(synopsys design constraint) files.

✓ Create & report the pattern specification
- This will create the pattern specification & report the same.

✓ Process the patterns
- This will generate the patterns needed for simulation.

✓ Set up the simulation library
- This will set the simulation libraries needed for testbench simulations.

✓ Run & check the simulation
- This will validate the IJTAG & MBIST insertions.

DFT implementation process :

✓ Go to the directory: **cd Tessent_labs/Lab1**
✓ Run the dofile script.
✓ Observe the output

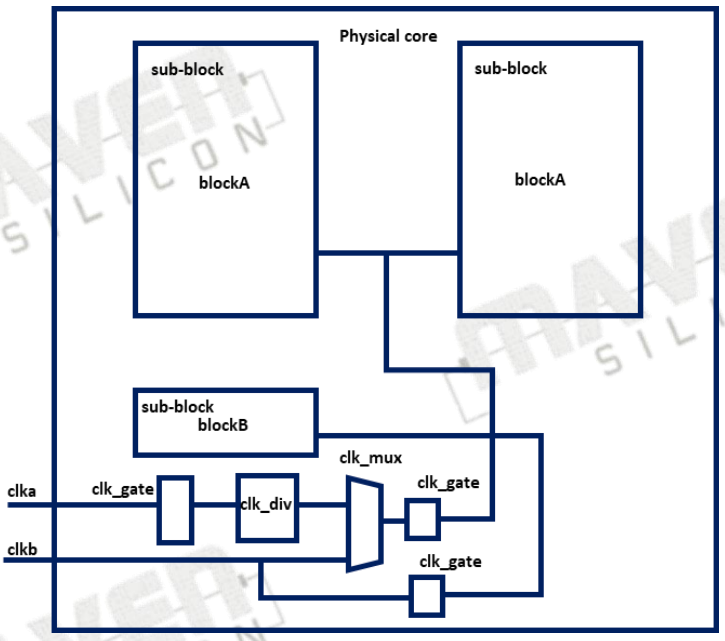
Learning outcomes :

To insert the MBIST at sub-block level using Tessent DFT flow.

Lab - 2: Clock and DRC

Objective : *Understand what could be DRC violations for MBIST.*

Introduction : There is a physical block that contains two instances of blockA and one instance of blockB. The physical block also includes a clock divider, a clock mux and clock gaters. As you go through the flow, there will be DRC violations that will need to be fixed.



Working Directory : Tessent_labs/Lab2/

Dofile script : dofile.do

Instructions : The following instructions have been included in the script as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT
  - This is done to set the primary context to DFT as DRCs are checked in the DFT flow.
- ✓ Read the cell library files
  - The I/O cell library needs to be read.
- ✓ Read the design source codes
  - The RTL files needs to be read.
- ✓ Read the TSDBs of the sub-blocks
  - The TSDBs of the sub-blocks to be opened.
- ✓ Elaborate the design top
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
- ✓ Source the PDL file of the clock divider
  - The .pdl file won't be automatically elaborated unlike the .icl file, hence needs to be sourced.
- ✓ Report the open tsdb directories

- This will display the list of tsdb directories.

✓ Report the name & location of the tsdb directories
- This will display the location of tsdb directories.

✓ Report IJTAG instances that are included in this design
- This will display the ijtag instances.

✓ Report all the ICL modules
- This will display the .icl modules loaded into the design.

✓ Report the identified clock enables
- It will report the clock enable point of the clock gaters.

✓ Set the design level to physical block level
- The memory blocks are part of a core block now.

✓ Specify the DFT requirements
- Here the MBIST needs to be turned on without adding clock so that the DRC violations will be observed.

✓ Verify the DFT requirements
- DRC i.e design rule check is performed to validate the DFT requirements.

✓ Report a specific DRC violation
- DRC violation errors about a specific violation can be reported.

✓ Analyze the violation using schematic viewer
- DRC violation errors can be viewed in GUI mode using DFT visualizer.

✓ Fixing the violation DFT_C1-1
- DRC violations are fixed.

✓ Run the DRC
- DRC i.e design rule check is performed to validate the DFT requirements.

✓ The above process is repeated till all the violations are fixed.

✓ Report the clocks
- All the clocks will be defined now.

DFT implementation process :

✓ Go to the directory: **cd Tessent_labs/Lab2**

✓ Run the dofile script.

✓ Observe the output

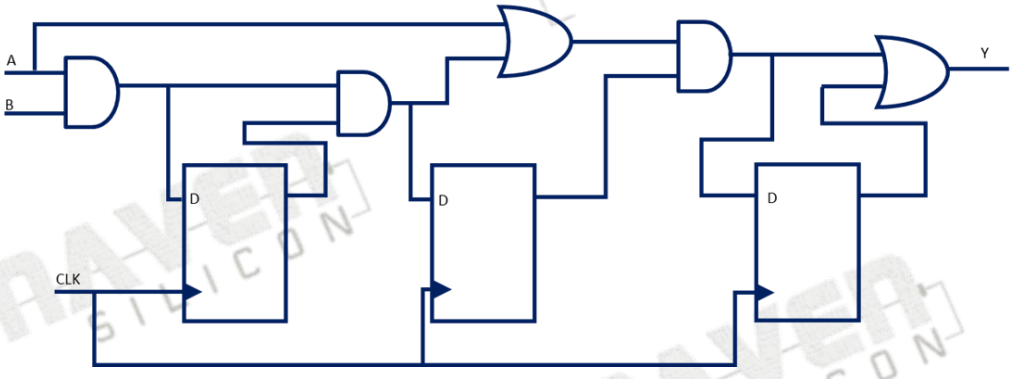
Learning outcomes :

To fix DRC violations at physical block level in a MBIST environment.

Lab - 3: Boundary scan

Objective : *Understand how to insert Boundary scan at chip level.*

Introduction : There is a gate level circuit and few DFFs for which boundary scan needs to be implemented at chip level.



Working Directory : Tessent_labs/Lab3/

Dofile script : dofile.do

Instructions : The following instructions have been included in the script as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT
  - This is done to set the primary context to DFT as DFT instrument has to be inserted i.e Boundary scan.
- ✓ Create the TSDB directory
  - This directory is created automatically during DFT flow.
- ✓ Read the cell library files
  - The I/O cell library needs to be read.
- ✓ Read the design source codes
  - The RTL files needs to be read.
- ✓ Elaborate the design top
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
- ✓ Set the design level to chip level
  - The boundary scan is always inserted at chip level.
- ✓ Specify the DFT requirement
  - Here the boundary scan needs to be turned on.
- ✓ Set attributes for the TAP controller pins
  - Here the attributes for the TAP controller pins (i.e) TDI,TCK, TMS,TRST,TDO are specified.
- ✓ Run the DRC
  - DRC i.e design rule check is performed to validate the DFT requirements.
- ✓ Create & report the DFT specification
  - After a successful DRC run, create DFT specification & report the same on the Tessent shell.
- ✓ Insert the DFT instruments
  - This is going to insert the DFT components and a modified RTL file is created inside the TSDB directory.

- ✓ Display the visualizer
  - This will display the added DFT components using the DFT visualizer.

DFT implementation process :

- ✓ Go to the directory: **cd Tessent_labs/Lab3**
- ✓ Run the dofile script.
- ✓ Observe the output

Learning outcomes :

To insert Boundary scan using Tessent shell at chip level.

Lab - 4: Scan chain insertion

Objective : *Understand how to insert scan chain into a design.*

Introduction : In this lab we have used a block level design called tracking_channel that has a single instance of a sub-module called code_gen.
Both tracking_channel and code_gen are RTL designs that have gone through previous DFT insertion steps to insert EDT into the RTL. The RTL for both of these designs was synthesized into a single file gate design with all the sequential elements mapped to scan equivalent cells.

Working Directory : Tessent_labs/Lab4/

Dofile script : dofile.do

Instructions : The following instructions have been included in the script as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT with the sub-context to scan
  - This is done to set the primary context to DFT & sub-context to scan as DFT instrument has to be inserted i.e scan cells.
- ✓ Create the TSDB directory
  - This directory is created automatically during DFT flow.
- ✓ Read the TSDBs of the sub-blocks
  - The TSDBs of the sub-blocks to be opened.
- ✓ Read the cell library files
  - The I/O cell library needs to be read.
- ✓ Read the synthesized design
  - The gate-level netlist file needs to be read.
- ✓ Load design files from the tsdb directory.
- ✓ Elaborate the design top
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
- ✓ Run the DRC
  - DRC i.e design rule check is performed to validate the DFT requirements.
- ✓ Set a chain constraint for scan chain
  - It is going to set the scan chain as per the count given and FFs will be distributed depending upon the no of chains.
- ✓ Distribute the scan elements to chain
  - This will distribute the FFs on the chain.
- ✓ Report the distribution prior to insertion
  - Reports the scan chain & cells.
- ✓ Modify the Netlist
  - Insert the test logic.
- ✓ Review the report files.

DFT implementation process :

- ✓ Go to the directory: **cd Tessent_labs/Lab4**
- ✓ Run the dofile script.
- ✓ Observe the output

Learning outcomes :

To insert the scan chain in a single mode for a given design.

Lab - 5: IJTAG Implementation

Objective : *Understand how to create ICL & PDL files.*

Introduction : In this lab we have used a PLL design file for which .icl file will be created & .pdl file for the .icl file will be generated.

Working Directory : Tessent_labs/Lab5/

Dofile script : dofile.do

Instructions : The following instructions have been included in the script as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT
  - This is done to set the primary context to DFT as .icl files are elaborated with the set_current_design.
- ✓ Read the design source codes
  - This reads the design source code.
- ✓ Elaborate the design top
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
- ✓ Create .icl file as per the syntax given:
  - <func>Port <port_name> ; where <func> describes the function of the port such a DataInPort and <port_name> is the logical name you are assigning to the port.
- ✓ Read the .icl file with a switch -force
  - This is going to read the .icl file such that tessent shell is aware of this file.
- ✓ Elaborate the design top
  - The design file top has to be elaborated to make sure that the .icl file gets elaborated.
- ✓ Create the .pdl file
- ✓ Set the context to patterns
  - The primary context should be set to patterns and sub-context should be set to ijtag.
- ✓ Set the design level to chip
- ✓ Verify the ICL ports
  - The Tessent shell will recognize the ICL ports.
- ✓ Run DRC
- ✓ Create a PDL pattern set
  - The pattern set will define how the ports are driven with values.

DFT implementation process :

- ✓ Go to the directory: **cd Tessent_labs/Lab5**
- ✓ Run the dofile script.
- ✓ Observe the output

Learning outcomes :

To create .icl & .pdl files for a design.

Lab - 6: EDT IP creation

Objective : *Understand how to insert EDT IP core using Tessent Test-kompress.*

Introduction : In this lab you start with a gate level Netlist, a non-scan Netlist, insert scan chains using Tessent scan, create Tessent Test-kompress EDT IP core.

Working Directory : Tessent_labs/Lab6/

Dofile script : dofile.do, edt_ip.do

Instructions : The following instructions have been included in the script **dofile.do** as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT scan mode
  - This is done to set the primary context to DFT & sub-context to scan mode for scan insertion.
- ✓ Read the cell library files
  - The I/O cell library needs to be read.
- ✓ Read the synthesized design
  - The gate-level netlist file needs to be read.
- ✓ Set the current design for elaboration process.
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
  - If any module descriptions are missing, design elaboration will identify them by adding **add_black_boxes -auto.**
- ✓ Identify and define control signals.
- ✓ Run DRC
- ✓ Set the scan chains count to 2
- ✓ Insert the scan logic
- ✓ Report scan chains and new test logic
- ✓ Write the scan inserted netlist
  - It creates the scan chain netlist inside the netlist directory.
- ✓ Write out atpg dofile and testproc file

The following instructions have been included in the script **edt_ip.do** as comments. Refer to the comments in the script and understand the script.

- ✓ Set the context to DFT edt mode
  - This is done to set the primary context to DFT & sub-context to edt mode for EDT ip insertion.
- ✓ Read the scan chain netlist
- ✓ Read the cell library files
  - The I/O cell library needs to be read.
- ✓ Set the current design for elaboration process.
  - The design files top has to be elaborated to make sure that the lower sub-modules are instantiated and integrated to the top module.
- ✓ Define scan chains & control signals
- ✓ Used to run the TCL procedure from the atpg.do
- ✓ Specify parameters for EDT logic
- ✓ Report EDT channels & pins

- ✓ Run DRC
- ✓ Report configuration of EDT logic
- ✓ Report required lock-up cells
- ✓ Write the EDT modified RTL

DFT implementation process :

- ✓ Go to the directory: **cd Tessent_labs/Lab6**
- ✓ Run first the dofile.do script followed by edt_ip.do script.
- ✓ Observe the output

Learning outcomes :

To insert an EDT IP core into a scan stitched netlist.