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Lab 1 Notebook

June 17, 2023

Brief Description:

In this lab we had created a bitstream for the Basys3 board, and then tested its adder functionality. We then changed the operation of the adder8.v file to allow the board to be toggled from addition and subtraction.

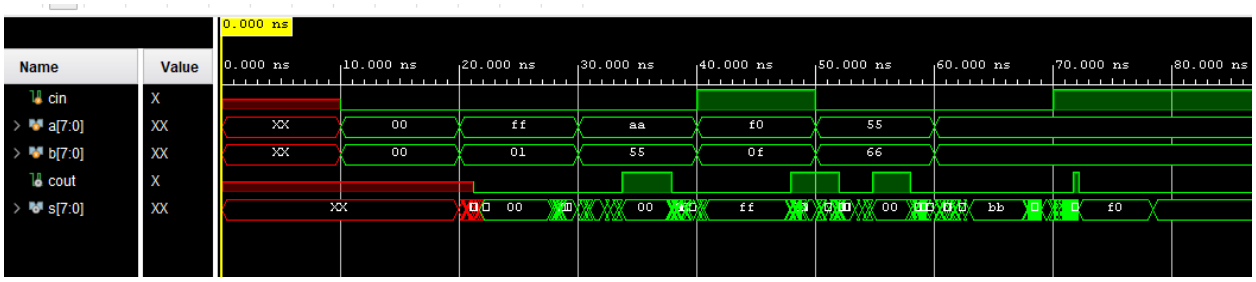
Discussion of Results:

a. I had just arbitrarily chosen a few test cases that would include all scenarios to make sure it worked. Things like making sure the carry worked, different numbers, and such.

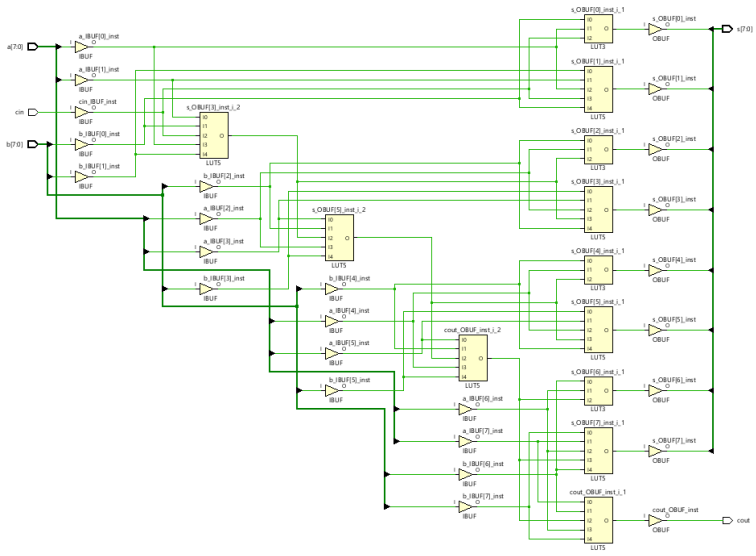
b. I had to really mess with the button configuration in order to allow the subtraction operation to work correctly.

c. Snippets:

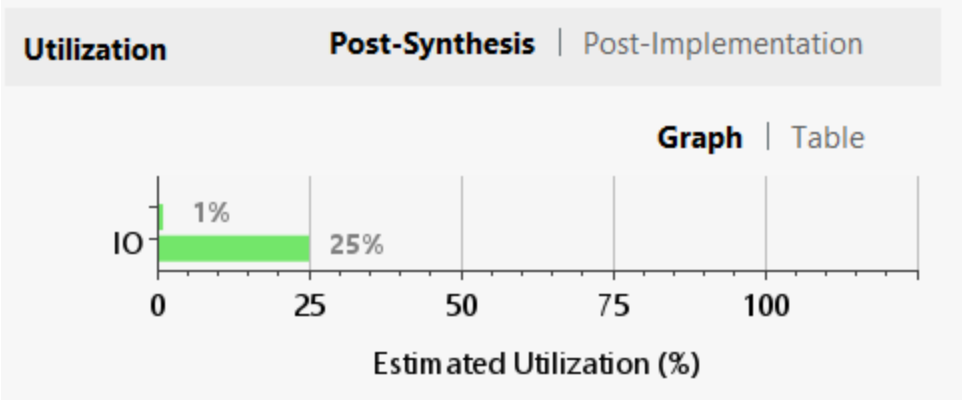
i.



ii.



iii.

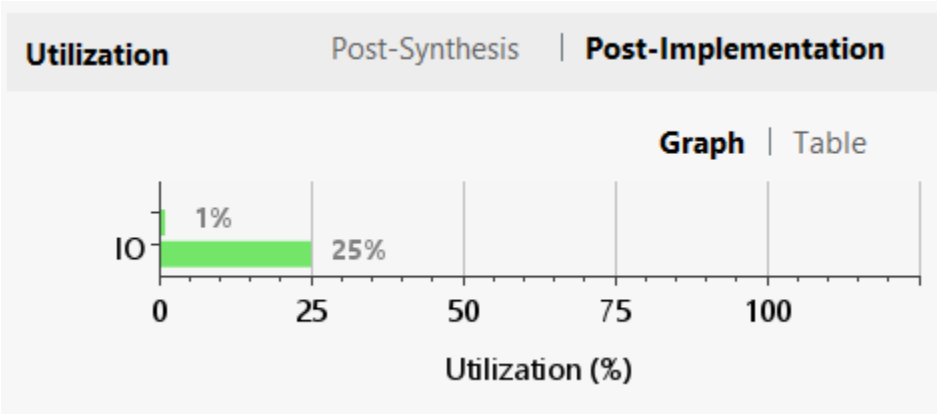


iv.

Timing Checks - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	De
Unconstrained Paths (1)														
(none) (9)														
Path 10	∞	6	5	3	a[1]	s[6]	8.486	5.485	3.000	64.6	35.4	∞	input port clock	
Path 11	∞	6	5	3	a[1]	cout	8.484	5.483	3.000	64.6	35.4	∞	input port clock	
Path 12	∞	6	5	3	a[1]	s[7]	8.474	5.474	3.000	64.6	35.4	∞	input port clock	
Path 13	∞	5	4	3	a[1]	s[4]	7.897	5.364	2.533	67.9	32.1	∞	input port clock	
Path 14	∞	5	4	3	a[1]	s[5]	7.897	5.364	2.533	67.9	32.1	∞	input port clock	
Path 15	∞	4	3	3	a[1]	s[3]	7.313	5.246	2.066	71.7	28.3	∞	input port clock	
Path 16	∞	4	3	3	a[1]	s[2]	7.305	5.238	2.066	71.7	28.3	∞	input port clock	
Path 17	∞	3	2	2	a[1]	s[1]	6.714	5.115	1.599	76.2	23.8	∞	input port clock	
Path 18	∞	3	2	3	b[0]	s[0]	6.683	5.083	1.599	76.1	23.9	∞	input port clock	

v.

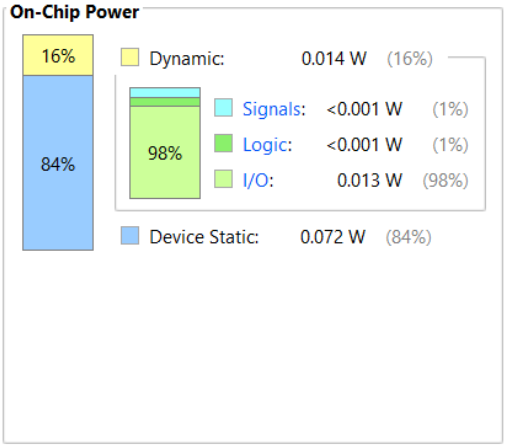


vi.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.085 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	59.6°C (11.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Key Steps:

Summary:

a. Yes, all the design goals were met. We were able to toggle it from addition and subtraction, and each operation was working.

b. Yes, getting the button to toggle between addition and subtraction caused some trouble.

c. Somehow utilize a switch other than the button to toggle the operation.

Adder8.xdc

```
# Switches
set_property PACKAGE_PIN V17 [get_ports {a[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[0]}]
set_property PACKAGE_PIN V16 [get_ports {a[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[1]}]
set_property PACKAGE_PIN W16 [get_ports {a[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[2]}]
set_property PACKAGE_PIN W17 [get_ports {a[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[3]}]
set_property PACKAGE_PIN W15 [get_ports {a[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[4]}]
set_property PACKAGE_PIN V15 [get_ports {a[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[5]}]
set_property PACKAGE_PIN W14 [get_ports {a[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[6]}]
set_property PACKAGE_PIN W13 [get_ports {a[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[7]}]
set_property PACKAGE_PIN V2 [get_ports {b[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]
set_property PACKAGE_PIN T3 [get_ports {b[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
set_property PACKAGE_PIN T2 [get_ports {b[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
set_property PACKAGE_PIN R3 [get_ports {b[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]
set_property PACKAGE_PIN W2 [get_ports {b[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[4]}]
set_property PACKAGE_PIN U1 [get_ports {b[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[5]}]
```

```
set_property PACKAGE_PIN T1 [get_ports {b[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[6]}]
set_property PACKAGE_PIN R2 [get_ports {b[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[7]}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {s[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[0]}]
set_property PACKAGE_PIN E19 [get_ports {s[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[1]}]
set_property PACKAGE_PIN U19 [get_ports {s[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[2]}]
set_property PACKAGE_PIN V19 [get_ports {s[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[3]}]
set_property PACKAGE_PIN W18 [get_ports {s[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[4]}]
set_property PACKAGE_PIN U15 [get_ports {s[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[5]}]
set_property PACKAGE_PIN U14 [get_ports {s[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[6]}]
set_property PACKAGE_PIN V14 [get_ports {s[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[7]}]
set_property PACKAGE_PIN V13 [get_ports {cout}]
    set_property IOSTANDARD LVCMOS33 [get_ports {cout}]

# Buttons
set_property PACKAGE_PIN U18 [get_ports cin]
    set_property IOSTANDARD LVCMOS33 [get_ports cin]

    # Timing Constraints
    create_clock -period 12.000 -name virtual_clock
    set_input_delay -clock [get_clocks virtual_clock] -add_delay 0.000
[get_ports -filter { NAME =~ "*" && DIRECTION == "IN" } ]
    set_output_delay -clock [get_clocks virtual_clock] -add_delay 0.000
[get_ports -filter { NAME =~ "*" && DIRECTION == "OUT" } ]
```

Adder8.v

```
module adder8(
  output cout,
  output [7:0] s,
  input [7:0] a,
  input [7:0] b,
  input cin
);
  wire [7:1] carry;
  wire [7:0] sub_b;
  full_adder FA0(carry[1], s[0], a[0], b[0], cin);
  full_adder FA1(carry[2], s[1], a[1], b[1], carry[1]);
  full_adder FA2(carry[3], s[2], a[2], b[2], carry[2]);
  full_adder FA3(carry[4], s[3], a[3], b[3], carry[3]);
  full_adder FA4(carry[5], s[4], a[4], b[4], carry[4]);
  full_adder FA5(carry[6], s[5], a[5], b[5], carry[5]);
  full_adder FA6(carry[7], s[6], a[6], b[6], carry[6]);
  full_adder FA7(cout, s[7], a[7], sub_b[7], carry[7]);  // Use sub_b instead of b for
subtraction

  assign sub_b = cin ? (~b + 1'b1) : b;  // Perform subtraction if toggle is active, else use b
directly
endmodule
```

Relevant Output Files: