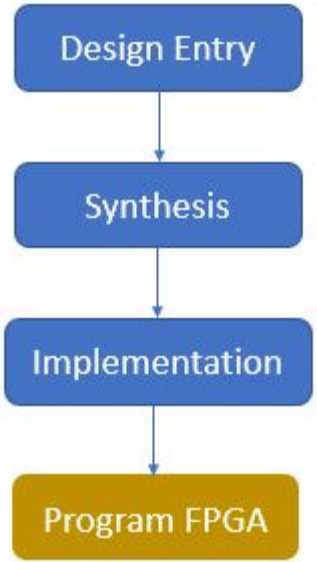
Lab - 2

Implementation and Timing Analysis

Review - FPGA Flow

- It is a Multi-step process



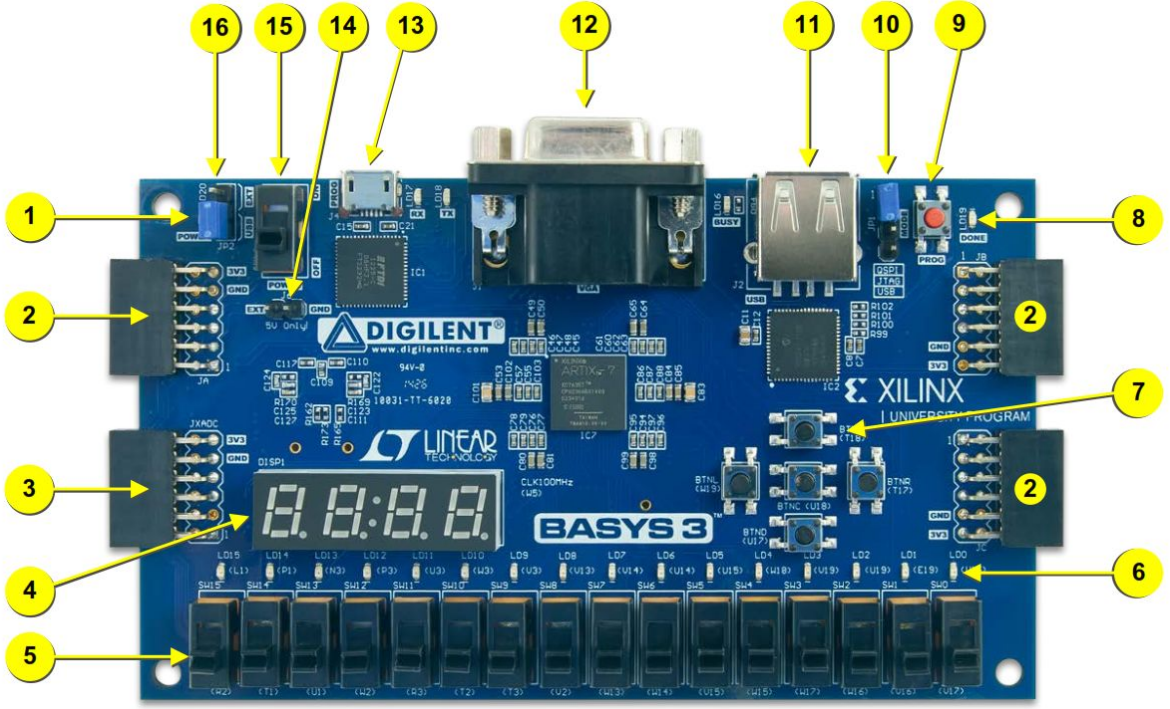
Implementation

- It is a Multi-step process
  - Translate
  - Map
  - Place and Route

Translate

- Combines all the input netlists and constraints to a logic design file.
- Defining constraints -
  - assigning the ports in the design to the physical elements
  - specifying time requirements of the design
- Stored in a file named UCF (User Constraints File).

FPGA Kit/Board



Pacakge


Package
Device
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
A B C D E F G H J K L M N P R T U V W
Pin: U19 (User IO)
Site Type: IO_L15P_T2_DQS_RDWR_B_14
Bank: 14 (High Range)

Constraints

```
10
11 ## Switches
12 set_property PACKAGE_PIN V17 [get_ports {inNum[0]}]
13 set_property IOSTANDARD LVCMOS33 [get_ports {inNum[0]}]
14 set_property PACKAGE_PIN V16 [get_ports {inNum[1]}]
15 set_property IOSTANDARD LVCMOS33 [get_ports {inNum[1]}]
16 set_property PACKAGE_PIN W16 [get_ports {inNum[2]}]
17 set_property IOSTANDARD LVCMOS33 [get_ports {inNum[2]}]
18 set_property PACKAGE_PIN W17 [get_ports {inNum[3]}]
19 set_property IOSTANDARD LVCMOS33 [get_ports {inNum[3]}]
20 set_property PACKAGE_PIN W15 [get_ports {inNum[4]}]
21 set_property IOSTANDARD LVCMOS33 [get_ports {inNum[4]}]
22 set_property PACKAGE_PIN V15 [get_ports {inNum[5]}]
23 set_property IOSTANDARD LVCMOS33 [get_ports {inNum[5]}]
```

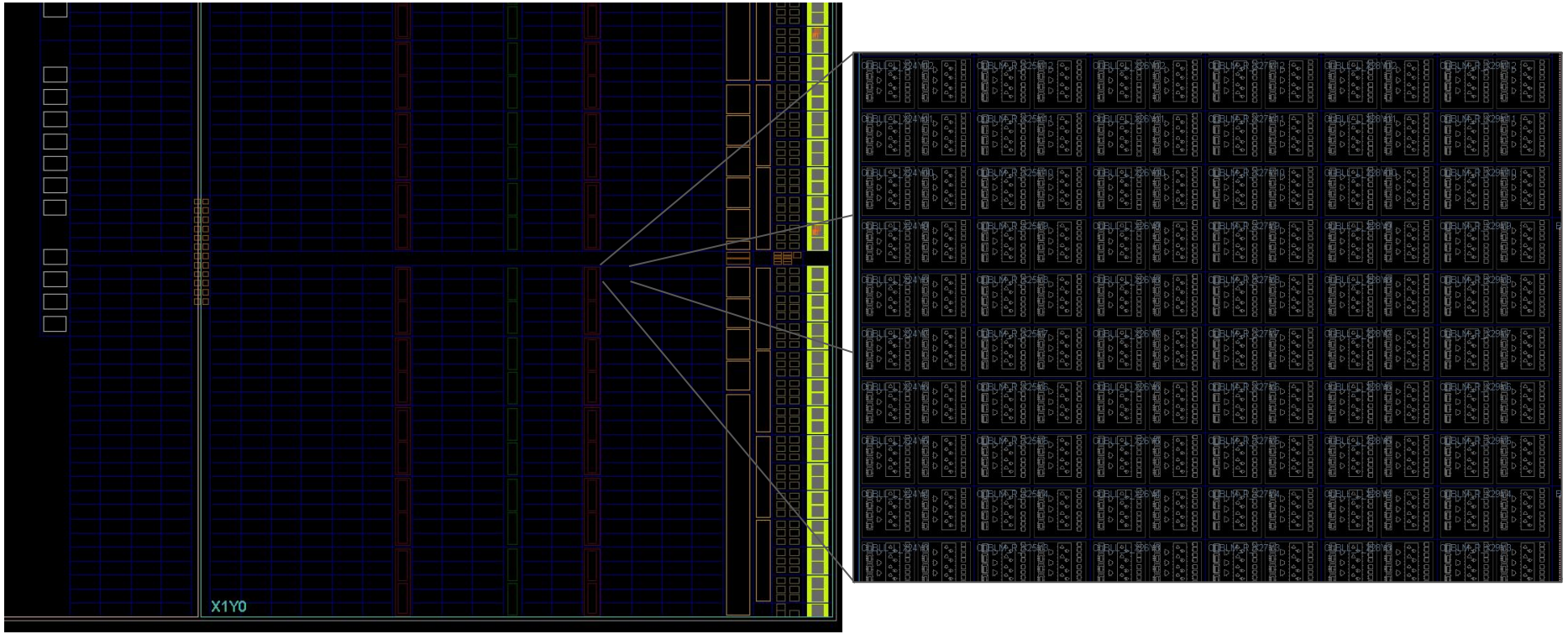
Map

- Divides the whole circuit with logical elements into sub blocks such that they can be fit into the FPGA logic blocks
- FPGA elements
    - Combinational Logic Blocks (CLB),
    - Input Output Blocks (IOB))

Place and Route

- Strategies
    - Power Driven
    - Timing Driven
    - Area Driven
    - Wire Length Driven
- Tool runs several optimization algorithms to find a balance between these

“At the End it is all a tradeoff between these Parameters”


X1Y0

Post-Implementation

- Reports and Analysis
  - Power
  - Timing
    - Different from Synthesis, why?
  - Utilization, more than what was in synthesis?
- Functional and Timing Simulations
- DRC violations (for complex designs, RF and Analog Designs)

Schematic of a design after Elaboration, Synthesis and Implementation are all different, why?

END

Any Questions?