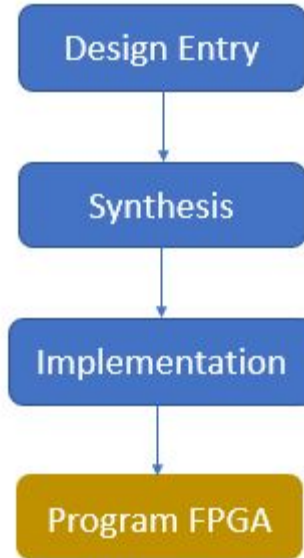


# Lab - 3

Downloading to the FPGA Board

# Review - FPGA Flow

- It is a Multi-step process



# Bitstream Generation

- Design must be converted to a format so that the FPGA can accept it.
- Contains information to configure the FPGA to required Digital Logic.

# Programming the FPGA

- Can be done in 3 different ways
  - Quad-SPI (Serial Peripheral Interface)
  - JTAG
  - USB

•

# Quad-SPI

It is a two step process (slower)

- Upload the program to the Flash Memory
- FPGA loads the configurations from the Flash Memory upon “Power On” or “Reset”.
  
- JP1 in QSPI Position
- Requires a **.bin** file
- “Be careful with the Memory Device Selection”
  - If IC has inscription MXIC - choose `mx25l3233f-spi-x1_x2_x4` / `mx25l3273f-spi-x1_x2_x4`
  - If IC has inscription Spansion - choose `s25fl032p-spi-x1_x2_x4`

For deploying Applications



# JTAG

It is a faster way of programming the FPGA

- JP1 in JTAG Position
- Requires a **.bit** file
- **FPGA loses configurations upon “Reset”**

Used for developing applications (constant/incremental design changes)



UNIVERSITY OF MINNESOTA

**Driven to Discover**<sup>SM</sup>

# USB

Similar to JTAG but using a USB Stick

- JP1 in USB Position
- USB device that you select to program the Basys3 must be formatted in Fat32
- Only look through the USB's root for a file with a .bit extension
  - So it is important that the **only .bit file** in root is the one that you want to be used to program the Basys3.



UNIVERSITY OF MINNESOTA

Driven to Discover<sup>SM</sup>

# References

[1] [Basys 3 Programming Guide](#)



UNIVERSITY OF MINNESOTA  
**Driven to Discover<sup>SM</sup>**



# END

Any Questions?

