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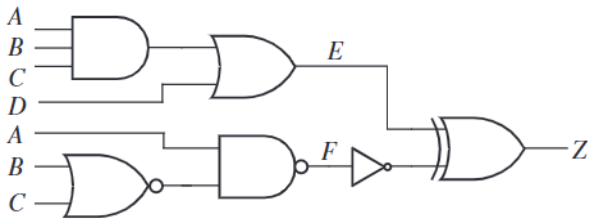
Homework 1

EE 4301

2.4 Write a Verilog description of the following combinational circuit using concurrent statements. Each gate has a 5-ns delay, excluding the inverter, which has a 2-ns delay.




```
module question1(A,B,C,D,Z)
    input A, B, C, D;
    output Z;
    wire E, F, G, H, I;
    assign #5 G = A & B & C;
    assign #5 H = ~(B | C);
    assign #5 E = D | G;
    assign #5 F = ~(A & H);
    assign #2 I = ~F;
    assign #5 Z = I ^ E;
end module
```

2.8 **(a)** What device does the following Verilog code represent?

```
always @(CLK, Clr, Set)
begin
  if(Clr == 1'b1)
    Q <= 1'b0;
  else if(Set == 1'b1)
    Q <= 1'b1;
  else if(CLK == 1'b0)
    Q <= D;
  else begin
  end
end
```

(b) What happens if *Clr* = *Set* = 1 in the device in part a?

```
a.  Falling edge flip-flop that has asynch active high clear and set

b.  Since Q has less priority than Clr, Q will be 0
```

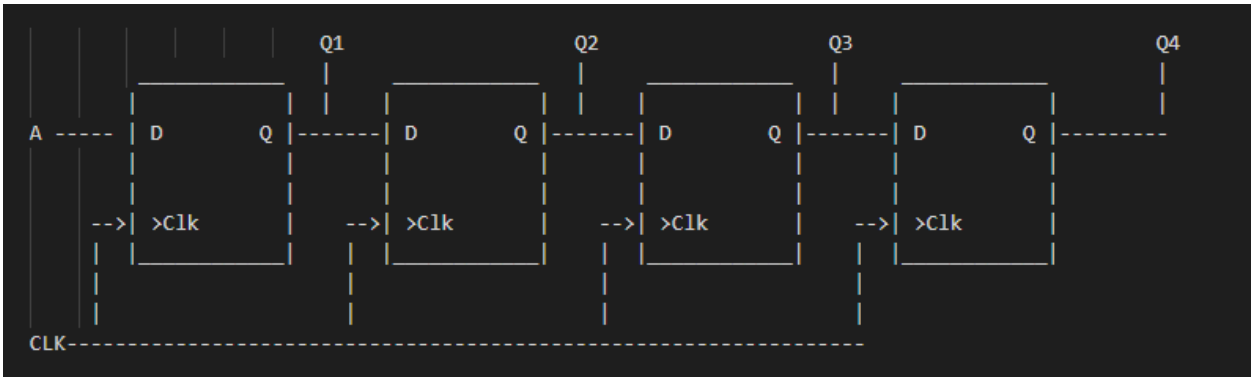
2.14 In the following Verilog process A, B, C, and D are all registers that have a value of 0 at time = 10 ns. If E changes from 0 to 1 at time = 20 ns, specify the time(s) at which each signal will change and the value to which it will change. List these changes in chronological order.

```
always @(E)
begin
    A <= #5 1;
    B <= A + 1;
    C <= #10 B;

    D <= #3 B;
    A <= #15 A + 5;
    B <= B 1 7;
end
```

Time	10ns	20ns	20ns + D	23ns	25ns	35ns
Variable						
A	0	0	0	0	1	5
B	0	0	7	7	7	7
C	0	0	0	0	0	0
D	0	0	0	0	0	0
E	0	1	1	1	1	1

2.21 Draw the hardware obtained if the following code is synthesized:

```
module  reg3 (Q1,Q2,Q3,Q4, A,CLK);
input   A;
input   CLK;
output  Q1,Q2,Q3,Q4;

reg     Q1,Q2,Q3,Q4;

always @(posedge CLK)
begin
  Q4 = Q3;
  Q3 = Q2;
  Q2 = Q1;
  Q1 = A;
end

endmodule
```



2.24 (a) Assume D_1=0, D_2=5, and D_1 changes to 1 at time=10ns. What are the values of D_1 and D_2 after the following code has been executed once? Do the values of D_1 and D_2 swap?

```
always @ (D1)
begin
    D2 <= D1;
    D1 <= D2;
End
```

(b) Assume D_1=0, D_2=5, and D_1 changes to 1 at time=10ns. What are the values of D_1 and D_2 after the following code has been executed once? Do the values of D_1 and D_2 swap?

```
always @ (D1)
begin
    D2 = D1;
    D1 = D2;
end
```

(c) How many latches will result when the following code is synthesized? Assume B is 3 bits long.

```
always @ (State) begin
       case(State)
       2'b00: B = 5;
       2'b01: B = 3;
       2'b10: B = 0;
       endcase
end
```

Circle the correct choice:

i. 1 latch because 1 case is missing
ii. 2 latches because state is 2 bits
iii. 3 latches because B is 3 bits
iv. 5 latches because B is 3 bits and state is 2 bits
v. None of the above. But it results in _____ latches.

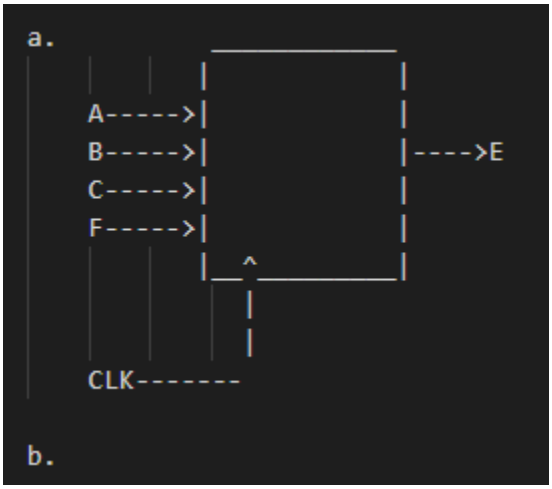
```
a. Yes they do swap, D1 = 5 and D2 = 1

b. No they do not swap, D1 = 1 = D2

c. Option iii
```

2.34 Consider the following Verilog code:

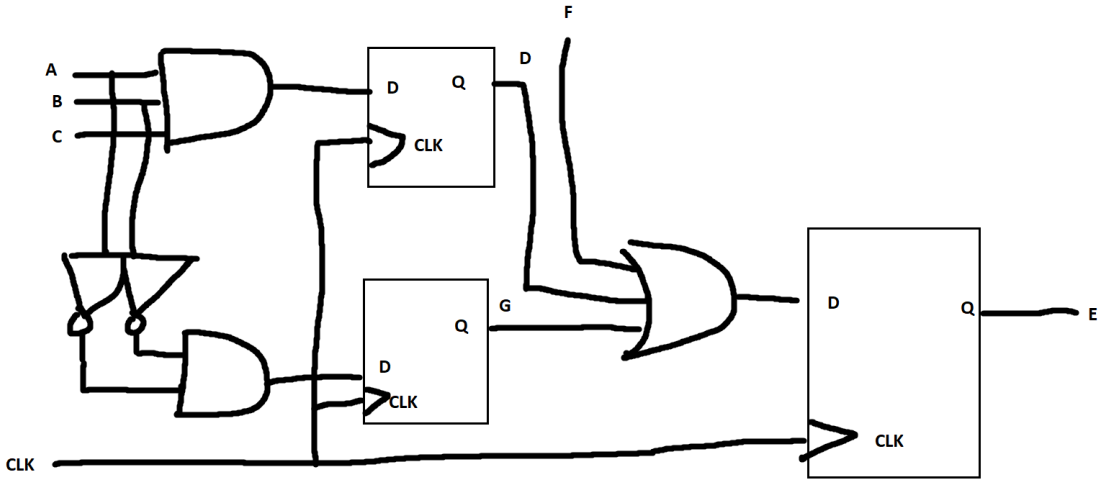
```
module Q3(A,B,C,F,Clk,E);
input A,B,C,F,Clk;
output reg E;

reg D,G;

initial
begin
    E = 1'b0;
    D = 1'b0;
    G = 1'b0;
end

always @(posedge Clk)
begin
    D <= A & B & C;
    G <= ~A & ~B;
    E <= D | G | F;
end
endmodule
```

(a) Draw a block diagram for the circuit (no gates and at block level only).
(b) Give the circuit generated by the preceding code (at the gate level).

a.



b.


A
B
C
D
Q
CLK
D
F
G
Q
D
CLK
D
Q
E
CLK
CLK