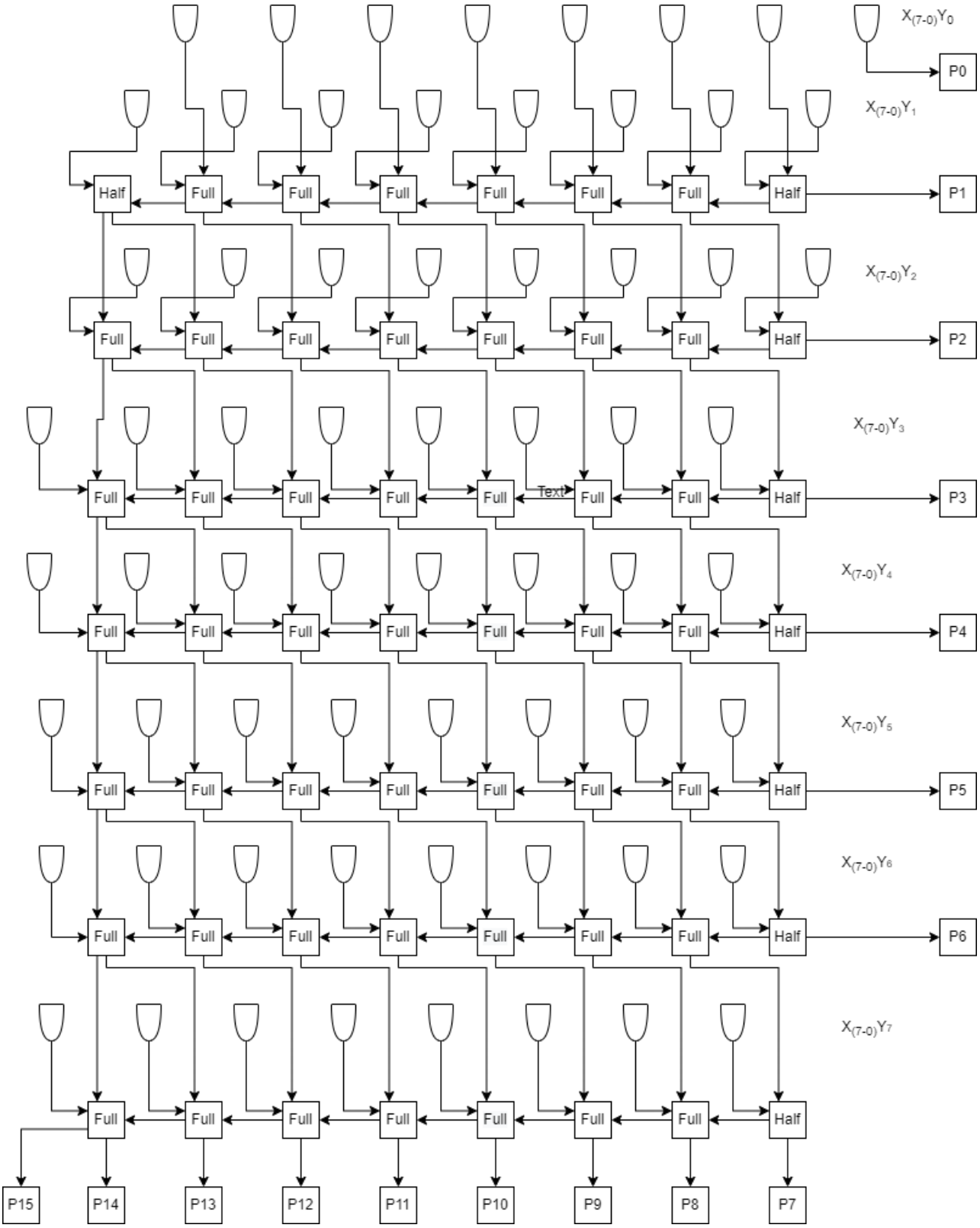
Vincent Han

Homework 4

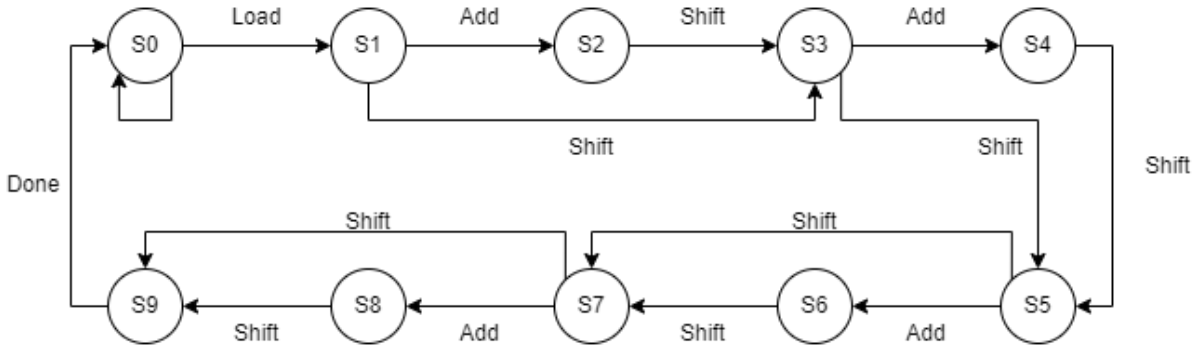
July 19, 2023

```
1.

a. There are going to be 64 and gates, 48 full adders, and then 8 half adders.
```


$X_{(7-0)}Y_0$
P0
$X_{(7-0)}Y_1$
Half
Full
P1
$X_{(7-0)}Y_2$
P2
$X_{(7-0)}Y_3$
Text
P3
$X_{(7-0)}Y_4$
P4
$X_{(7-0)}Y_5$
P5
$X_{(7-0)}Y_6$
P6
$X_{(7-0)}Y_7$
P15
P14
P13
P12
P11
P10
P9
P8
P7

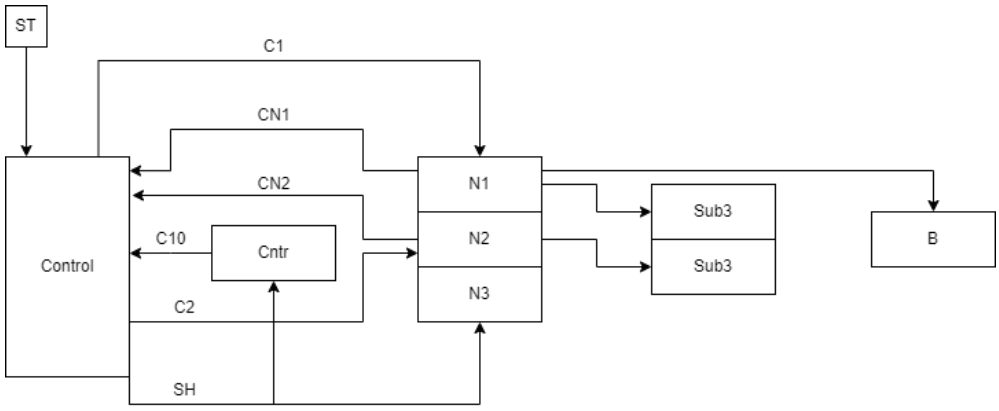
b.



2.

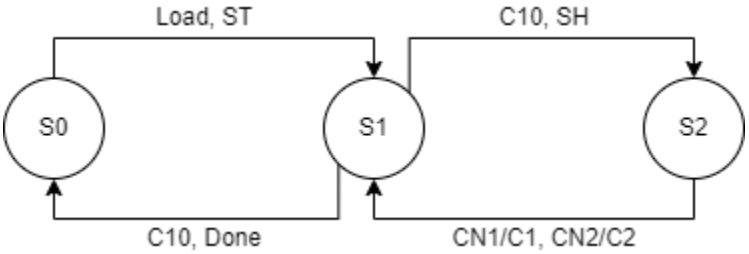
a.

Register A	Register B	Operation
100001010111	0000000000	Shift
010000101011	1000000000	Make correct
010000101000	1000000000	Shift
001000010100	0100000000	Shift w/o correct
000100001010	0010000000	Make correct
000100000111	0010000000	Shift
000010000011	1001000000	Make correct
000001010011	1001000000	Shift
000000101001	1100100000	Make correct
000000100110	1100100000	Shift
000000010011	0110010000	Shift w/o correct
000000001001	1011001000	Make correct
000000000110	1011001000	Shift until done
000000000000	1101011001	Result



b.

c.



d.

```
d.


module ques2(BCDin, St, clk, B, done);
    input [11:0] BCDin;
    input St, clk;
    output reg [9:0] B;
    output reg done;
    reg [11:0] N;
    reg load, C1, C2, Sh;
    reg [1:0] State, Nstate;
    integer ctr;
    wire [3:0] sub3_2, sub3_1;

    initial begin

        B = 0;
        done = 0;
        N = 0;
        load = 0;
        C1 = 0;
        C2 = 0;
        Sh = 0;
        State = 0;
        Nstate = 0;
        ctr = 0;
    end

    assign sub3_2 = N[7:4] + 4'b1101;
    assign sub3_1 = N[3:0] + 4'b1101;
```