EE 4301 Homework 1 due June 21st at 4:30 pm

Chapter 2 – text book

2.4 , 2.8 , 2.14 , 2.21 , 2.24 , 2.34

Solutions:

2.4 (4 points)

Prob 2.4

```
module prob2_4( A,B,C,D,Z);
        input A, B, C, D;
        output Z;
        wire E,F,G,H,I
        assign #5 G = A & B & C ;
        assign #5 E = D | G  ;
        assign #5 H = ~( B | C );
        assign #5 F = ~( A & H );
        assign #2 I = ~F ;
        assign #5 Z = I ^ E
endmodule
```

2.8 a) (2 Points)

A falling edge triggered flip-flop with
asynchronous active high clear
asynchronous active high set

b) (1 point)

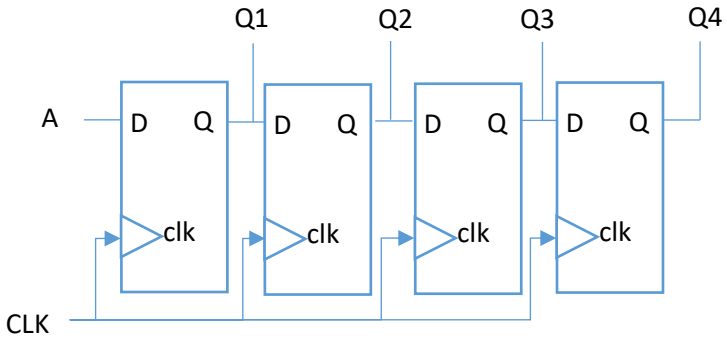
Q will be set to 0 as Clr has priority over Q

2.14 (3 points)

Variable/time	10ns	20ns	20ns+delta	23ns	25ns	35
A	0	0	0	0	1	5
B	0	0	7	7	7	7
C	0	0	0	0	0	0
D	0	0	0	0	0	0
E	0	1	1	1	1	1

2.21 (3 points)

4 bit shift register



2.24 (3 points)

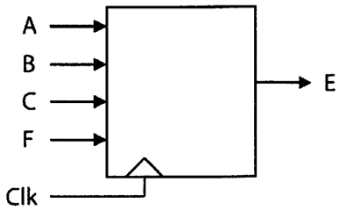
a) D1 and D2 swap, D1 =5 D2 =1

b) D1 and D2 do not swap, D1 =D2 =1

c) iii. 3 latches because B is 3 bits

2.34

a) (1 points)



b) (3 points)