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Lab 1 Notebook

June 16, 2023

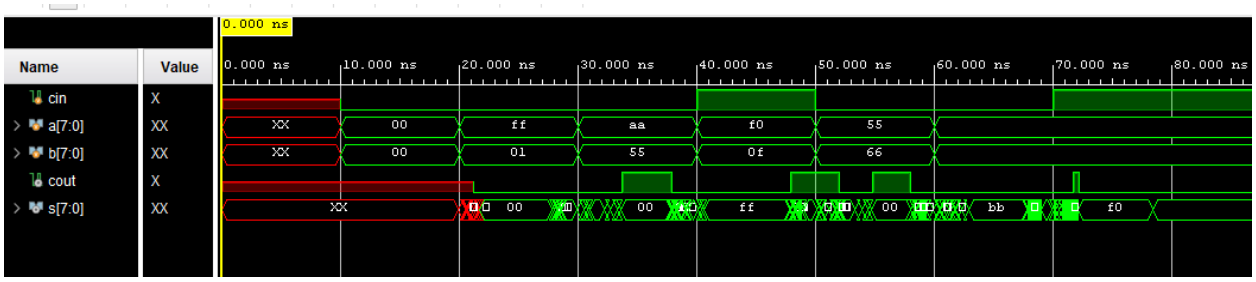
Brief Description:

In this lab we got exposure to the use of a constraint file. In the constraint file, we had allocated and assigned the LEDs, the switches, and a timing constraint. We then saw the physical mapping using the net panel in Vivado. We then also compared two implementations by looking at their utilization as well as their power usage.

Discussion of Results:

a. Snippets

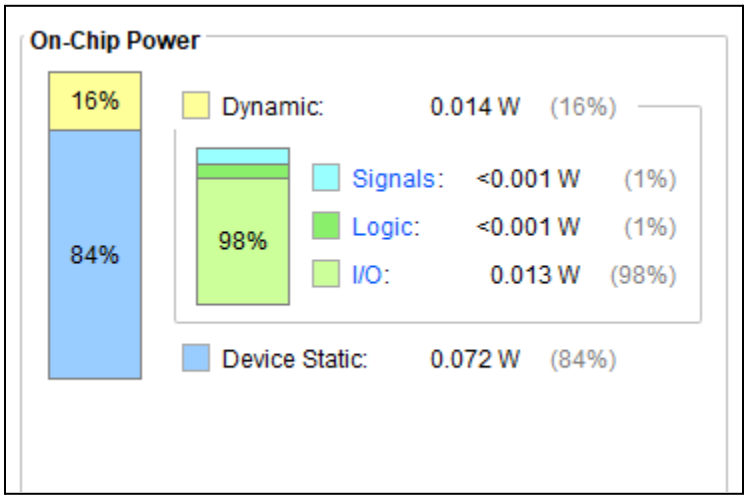
i.



ii.

Resource	Utilization	Available	Utilization %
LUT	8	20800	0.04
IO	26	106	24.53

iii.



Key Steps:

Summary:

a. Yes, since we were able to add the constraints to the board and then synthesize and run the implementation.
b. Loading the second implementation was a little difficult. It kept defaulting to the first one. Additionally, I'm not sure if I can see the differences between the first and second implementation.
c. Nothing I would change.

The adder8 and full adder is the same from lab 1.

adder8.xdc

```
# This file is the .xdc for the Basys3 rev B board used with lab1

# Switches
set_property PACKAGE_PIN V17 [get_ports {a[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[0]}]
set_property PACKAGE_PIN V16 [get_ports {a[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[1]}]
set_property PACKAGE_PIN W16 [get_ports {a[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[2]}]
set_property PACKAGE_PIN W17 [get_ports {a[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[3]}]
set_property PACKAGE_PIN W15 [get_ports {a[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[4]}]
set_property PACKAGE_PIN V15 [get_ports {a[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[5]}]
set_property PACKAGE_PIN W14 [get_ports {a[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[6]}]
set_property PACKAGE_PIN W13 [get_ports {a[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {a[7]}]
set_property PACKAGE_PIN V2 [get_ports {b[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]
set_property PACKAGE_PIN T3 [get_ports {b[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
set_property PACKAGE_PIN T2 [get_ports {b[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
set_property PACKAGE_PIN R3 [get_ports {b[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]
set_property PACKAGE_PIN W2 [get_ports {b[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[4]}]
set_property PACKAGE_PIN U1 [get_ports {b[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[5]}]
set_property PACKAGE_PIN T1 [get_ports {b[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[6]}]
set_property PACKAGE_PIN R2 [get_ports {b[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {b[7]}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {s[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[0]}]
set_property PACKAGE_PIN E19 [get_ports {s[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[1]}]
set_property PACKAGE_PIN U19 [get_ports {s[2]}]
```

```
    set_property IOSTANDARD LVCMOS33 [get_ports {s[2]}]
set_property PACKAGE_PIN V19 [get_ports {s[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[3]}]
set_property PACKAGE_PIN W18 [get_ports {s[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[4]}]
set_property PACKAGE_PIN U15 [get_ports {s[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[5]}]
set_property PACKAGE_PIN U14 [get_ports {s[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[6]}]
set_property PACKAGE_PIN V14 [get_ports {s[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {s[7]}]
set_property PACKAGE_PIN V13 [get_ports {cout}]
    set_property IOSTANDARD LVCMOS33 [get_ports {cout}]

# Buttons
set_property PACKAGE_PIN U18 [get_ports cin]
    set_property IOSTANDARD LVCMOS33 [get_ports cin]

    # Timing Constraints
    create_clock -period 12.000 -name virtual_clock
    set_input_delay -clock [get_clocks virtual_clock] -add_delay 0.000
[get_ports -filter { NAME =~ "*" && DIRECTION == "IN" } ]
    set_output_delay -clock [get_clocks virtual_clock] -add_delay 0.000
[get_ports -filter { NAME =~ "*" && DIRECTION == "OUT" } ]
```

Relevant Output Files: