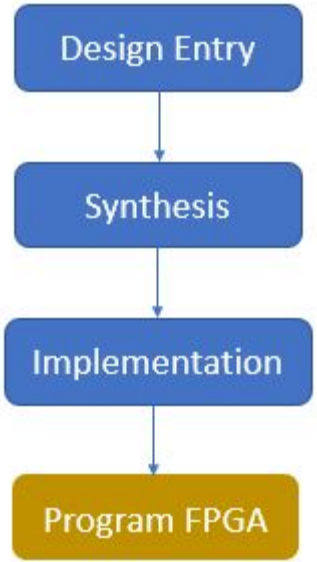
Lab - 1

Verilog Design Entry, Synthesis and Behavioral Simulation

FPGA Flow

- It is a Multi-step process



Design Entry

- Can be done using various techniques,
  - Schematic
    - Draw your design on computer using gates and wires
  - Hardware Descriptive Language (HDL)
    - Fast, language-based process
    - no need to design in lower level hardware
  - State-Machine
    - Complex and deprecated

Hardware Descriptive Languages (HDLs)

- Used to describe the structure and behavior of electronic circuits (mostly digital logic circuits).
- There are lot of HDLs,
  - Verilog
  - VHDL
  - SystemVerilog
  - Scala - Chisel

Synthesis

- Code is translated into an actual circuit with elements such as gates, flip flops, multipliers, etc.
- It is a multi-step process
  - Process begins with a syntax check
  - Optimizes - reduction of logic, elimination of redundant logic, reduction of the size of the design
  - Connect the design to Logic (Wiring up)
  - Accumulation of Design Netlist

```
module and2 (c, b, a);
output c; input a,b;
assign c = a&b;
endmodule
```

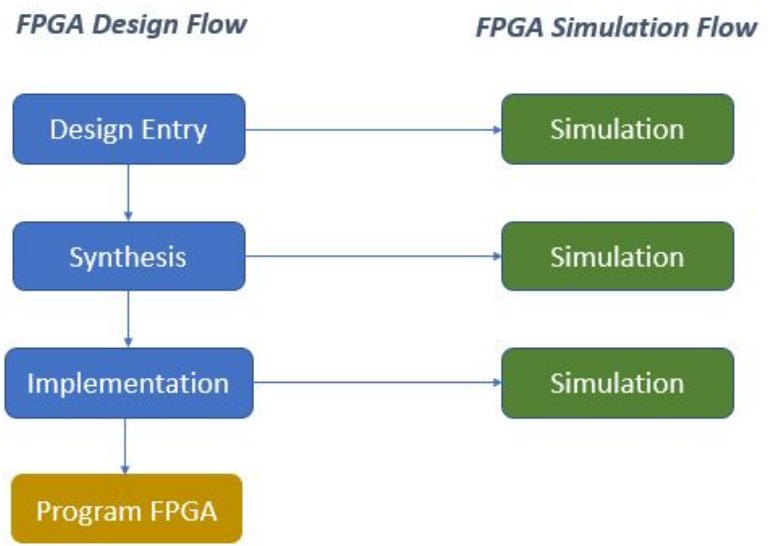
AND gate using Verilog

Synthesized AND gate

Vivado has its own proprietary tool to synthesize the design

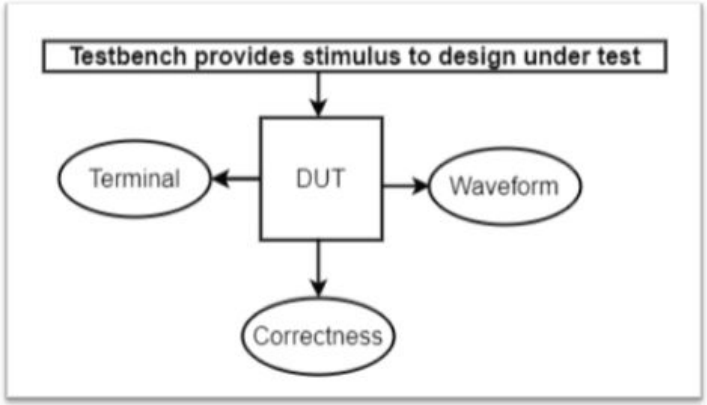
FPGA Verification and Simulation

- At the end of each step in the FPGA design flow, you have the opportunity to simulate and test you design.
- verifying that the implemented design performs the required functionality an important part of the FPGA design flow.



Behavioral Simulation (After Design Entry)

- Also called RTL simulation, is performed before synthesis
- Used to check the functionality of the design without constraints
- Test your code and find logic errors.
- Need to write a testbench to Simulate.



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Any Questions?