**University of Minnesota**

**EE4301**: **Summer Session 2023**

# Digital Design with Programmable Logic (Verilog HDL)

**Instructor:** **Dr.** **A B (Bob)Mahmoodi, KHKH 5-167, (612) 625-1574, mahmo006@umn.edu**

**Time & Location: 12:20 pm – 2:15 KLH 3-125 (and uploaded video lecture)**

**Office Hours: M & W (10 am -11:30 am)**

**Teaching Assistants: TBA**

**Lab TA : TBA**

**Catalog Description:**

EE 4301. Digital Design With Programmable Logic.

(4.0 cr.; prereq 2301, [1301 or CSCI 1113 or CSCI 1901]; fall, summer, every year)

Introduction to system design/simulation. Design using Verilog code/synthesis. Emulation using Verilog code.

**Course Web Page:** Canvas site

Updated administrative information, homework, quiz and exam solutions, and

Supplemental information and links will be posted on the course webpage.

**Required Text:** (available at the Bookstore in Coffman Union)

C. H. Roth, L. K. John, and B. K. Lee, *Digital Systems Design Using Verilog*, Cengage Learning, 2016. ISBN 978-1-285-05107-9.

**Prerequisites:** EE2301 or equivalent and familiarity with a programming language such as C.

**Grading Components:**

Homework 10 %

Lab 30 %

Exam 1 30 %

Exam 2 30 %

**Exam 1** **Friday July 7th (duration two hours)**

**Exam 2 Friday July 28th (duration two hours)**

**No Class on Monday June 19th.**

**For Monday July 3rd I will record the lectures so you can have an extended July4th weekend (Saturday thru Tuesday)**

**Laboratory:**

There is a laboratory associated with the class that meets twice every week. **(Tuesday & Thursdays)**

**Lab sessions will begin as of Tuesday June 8th**. The lab is an integral part of the course, and will be conducted online. The lab kit consists of the Digilent Basys 3 board and can be ordered online from [www.digilentinc.com](http://www.digilentinc.com/) . The Basys 3 is the same as used in EE2301.

**Course Outline:**

We plan to cover most of the Verilog related material in the text in varying levels of detail, and also some material beyond the text. Note that chapter 1 of the text is review material. An approximate outline for the topics to be covered is listed below. Please note that this is approximate and subject to change.

Week 1 (June 5, 7, 9) Overview, Introduction to Verilog

Basic methods for circuit specification – Text book chapters 1 & 2

Week 2(June 12, 14, 16) Design and specification of simple circuits

Programmable logic devices and FPGAs – Text book chapters 3 & 4

Week 3 (June 21, 23) Advanced Design and Synthesis – Chapter 4 & 5

Week 4 (June 26, 28 , 30) Advanced Design, Examples – Chapter 6

Week 5 (July 5, 7) ALU - Adder – Chapter 7 ( For July 3rd we have a recorded video )

**Exam 1 – Friday July 7th)**

Week 6 (July 10, 12, 14) Arithmetic unit design: Multipliers, Dividers –Chapter 8

Week 7 (July 17, 19, 21) Design Examples, Verilog Functions, Testing strategies. Chapter 9

Week 8 (July 24, 26) Testing sequential logic **–** Chapter 10

**Exam 2 – Friday July 28th.**

References and links for material covered in lecture which is not in the textbook will be provided.

**Homework**:

Homework will be assigned approximately once every week unless otherwise announced. Homework may require the use of CAD tools.

Homework must have your name and ID number. Only selected homework problems will be graded.

**You should check the class webpage on a regular basis for the latest information about EE4301**

**Policies and Bureaucratic Matters**

* Use of cell phones and similar electronic devices is not permitted in lecture, lab, or recitation.
* No "Incomplete" grades will be given for the course, except under extreme circumstances. The following is the University Senate statement with regard to a grade of "I": *The "I" shall be assigned at the discretion of the instructor when, due to extraordinary circumstances, the student was prevented from completing the work of the course on time. The assignment of an "I" grade requires a written agreement between the instructor and student specifying the time and manner in which the student will complete the course requirements. In no event may any such written agreement allow a period of longer than one year to complete the course requirements.*

Any "extraordinary circumstances" must be verifiable.

* You are not permitted to submit extra work in an attempt to raise your grade.
* You are responsible for all assigned readings and information presented in class, including due dates, assignments, exams and so forth. Moreover, you are expected to attend all class meetings. You should regularly check your email and the class web page for announcements.
* Students with disabilities that affect their ability to fully participate in class or meet all course requirements are encouraged to bring this to the attention of the instructor at the beginning of the semester so that appropriate accommodations may be arranged. Further information is available from disability services, Suite 180, McNamara Alumni Center, 200 Oak St. SE, 612-626-1333 (V/TDD).
* Any changes and/or updates to the information on this syllabus will be posted to the class webpage. You are responsible for information posted or **Exam 1**updated on the class webpage.

**Student Academic Integrity and Scholastic Dishonesty**

Academic Integrity is essential to a positive teaching and learning environment. All students enrolled in University courses are expected to complete coursework responsibilities with fairness and honesty. Failure to do so by seeking unfair advantage over others or misrepresenting someone else's work as your own, can result in disciplinary action. The University Student Conduct Code defines scholastic dishonesty as follows: *Scholastic Dishonesty: submission of false records or academic achievement; cheating on assignments or examinations; plagiarizing; altering, or acquiring, or using test materials without faculty permission; acting alone or in cooperation with another to falsify records or to obtain dishonestly grades, honors, awards, or professional endorsement.*

Within this course, a student responsible for scholastic dishonesty can be assigned a penalty up to and including an "F" or "N" for the course. If you have any questions regarding the expectations for a specific assignment or exam, ask. **See also the Office of Student Conduct and Academic Integrity (OSCAI) web pages at** [**www.oscai.umn.edu.**](http://www.oscai.umn.edu/)