



Bài Thi Cuối Kỳ Môn Kiến Trúc Máy Tính và Hợp Ngữ

Kiến trúc máy tính _ hợp ngữ (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

Thi Online KTMT&HN nhóm lẻ

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Question 1

Complete

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0.50

In multiplication instruction, the upper half of the result is nonzero implies which state of Carry flag and Overflow flag?

Select one or more:

- ☐ OF=1
- ☐ CF=1
- ☒ OF=0
- ☒ CF=0

Question 2

Complete

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1.00

Which is correct about dual-layer DVD?

Select one:

- ☐ the same as double-sided DVD
- ☐ contains layers on both sides of the disk for writing data to
- ☒ contains two layers on a single side for writing data to
- ☐ DVD drives has double laser head for reading from or writing to this disk

Question 3

Complete

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1.00

For better speed, in CPU design, engineers make use of the following techniques:

Select one or more:

- ☒ Pipelining
- ☒ Branch prediction
- ☐ Faster CPU internal bus
- ☒ Speculative execution

Question 4

Complete

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1.00

Consider the following assembly instruction sequence

```
XOR BX, BX
CMP DL, 5
JLE a_label
CMP DL, 17h
JGE a_label
MOV BX, 10h
```

a_label:

```
INC BX
```

watch point:

...

Choose correct value of BX register at watch point for different value of DL?

DL=0Ah

01h ▼

DL=0FFh

11h ▼

DL=10

01h ▼

DL=17h

11h ▼

Question 5

Complete

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1.00

Consider a 16-bit microprocessor, with a 16-bit external data bus, driven by an 10-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain?

Select one:

- ☒ 4 MB/s
- ☐ 1 MB/s
- ☐ 5 MB/s
- ☐ 10 MB/s

Question 6

Complete

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1.00

Select correct definition of seek time, rotational delay, access time, transfer time for hard drives with moveable-head system:

rotational delay

time for the sector in the request track to reach the head ▼

seek time

time for the head to settle at the request track ▼

access time

access time + settle time ▼

Question 7

Complete

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0.50

Which are the correct actions for LODSW string operation if DF is reset (=0)

Select one or more:

- ☐ decrease DI by 2
- ☐ Load 16-bit value at memory location pointed by ES:[DI] into AX
- ☒ Load 16-bit value at memory location pointed by DS:[SI] into AX
- ☒ increase SI by 2

Question 8

Complete

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1.00

In computer organization, the CPU transfer rate is much higher than that of memory. It is easy to match performance of these components by:

Select one:

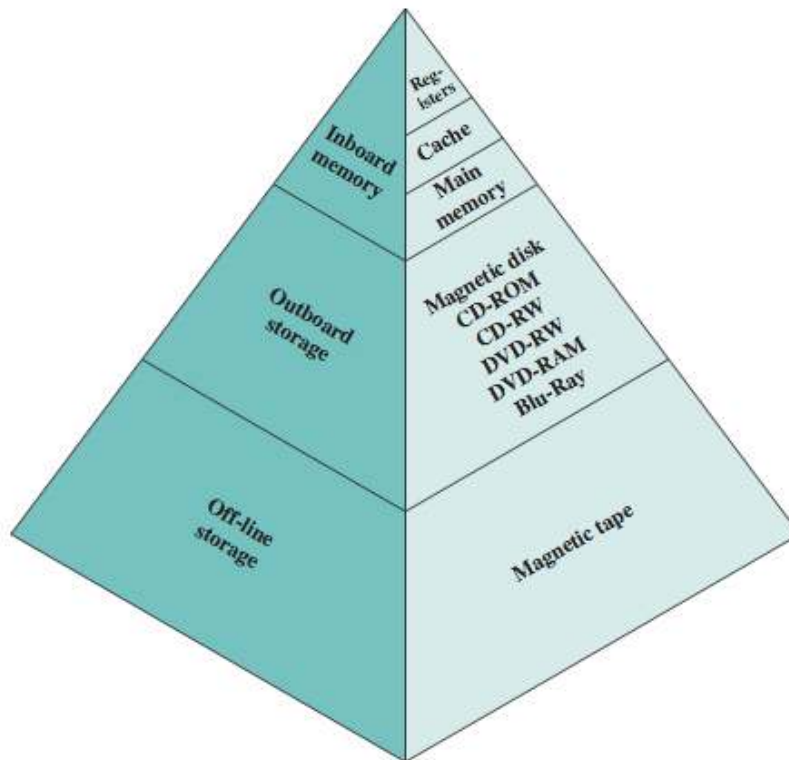
- ☐ increase the bus speed
- ☐ producing faster memory module
- ☒ Introducing cache memory
- ☐ increase I/O speed

Question 9

Complete

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1.00

For memory hierarchy below, which relationship hold when moving downward



Select one or more:

- ☒ Decreasing cost per bit
- ☒ the processor accesses more often
- ☐ Increasing access time
- ☒ Decreasing frequency of access by the processor
- ☒ Increasing capacity

Question 10

Complete

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0.50

Which of the following instructions are not valid?

Select one or more:

- ☒ MOV DS, B800h
- ☐ MOV AX, SI
- ☒ MOV AX, [BP+2]
- ☐ MOV SP, SS:[SI+2]

Question 11

Complete

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0.50

Sign-extend number 1011 0101 (8-bit binary) to 16-bit

Answer: 1111 1111 1011 0101

Question 12

Complete

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1.00

The principle of cache memory relies on key features: locality of reference which involves spatial and temporal locality. Match the definition to keywords on the left

Temporal
locality

the tendency for a processor to access memory locations that have been used recently ▼

Spatial
locality

the tendency of execution to involve a number of memory locations that are clustered ▼

tendency to use large cache and prefetch mechanism ▼

Question 13

Complete

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1.00

Which ones are not correct for static RAM?

Select one or more:

- ☒ faster than dynamic RAM because they are made from capacitor
- ☐ Cheaper than dynamic RAM because simpler chip controller
- ☒ Cost per bit is higher than dynamic RAM
- ☐ Cost per bit is lower than dynamic RAM

Question 14

Complete

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1.00

Which of the following instructions are not legal addressing?

Select one or more:

- ☐ MOV AX, [DI]
- ☐ MOV CX, [SI]
- ☒ MOV AX, [BX+SP]
- ☒ MOV AX, [SP+1]

Question 15

Complete

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1.00

Structural components of computer include:

Select one or more:

- ☒ I/O
- ☐ DMA
- ☒ System interconnection
- ☐ Interrupt
- ☒ Central processing unit
- ☒ Memory

Question 16

Complete

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1.00

A memory chip has 12 address pins, determine the maximum memory words of this chip?

Select one:

- ☒ 4096
- ☐ 2048
- ☐ 2048K
- ☐ 4000

Question 17

Complete

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1.00

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity

Answer:

KB ▼

Question 18

Complete

Marked out of
1.00

Choose correct features for SRAM and DRAM

SRAM ▼DRAM ▼**Question 19**

Complete

Marked out of
1.00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

MOV AX,0020

MOV CX,0010

MUL CL

watch point:

DX ▼AX = ▼CX = ▼**Question 20**

Complete

Marked out of
1.00

Which statements are correct for HDDs?

Select one or more:

- ☐ a. Bits are store randomly on disk surfaces
- ☐ b. Head, Track, Cylinder are key parameters for access data on hard disk
- ☒ c. Bits are stored on tracks
- ☒ d. Head, Track, Sector are key parameters for access data on hard disk

Question 21

Complete

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0.50

Which are the correct inputs for XLAT instruction

Select one or more:

- ☐ look-up index must be loaded into DL
- ☐ DS:[BX] pointed to look-up table
- ☒ look-up index must be loaded into AL
- ☐ DS:[SI] pointed to look-up table

Question 22

Complete

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1.00

What is the correct value of SI, AL (in hex) at watch point:

```

01:      MOV SI, 300h
02:      MOV AL, 10h
03:      MOV CX, 7
04: Loop_label:
05:      MOV [SI], AL
06:      ADD AL, 10h
07:      INC SI
08:      LOOP Loop_label

```

watch point:

SI AL = **Question 23**

Complete

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1.00

To evaluate processor performance, the following indicators and formulas are used:

Cycles per instruction
$$CPI = \frac{\sum_{i=1}^n (CPI_i \times I_i)}{I_c}$$

Time to execute a program
$$T = I_c \times CPI \times \tau$$

Or
$$T = I_c \times [p + (m \times k)] \times \tau$$

In which:

p: the number of processor cycles needed to decode and execute the instruction

m: the number of memory references needed

k: the ratio between memory cycle time and processor cycle time

 τ : cycle time = $1/f$ Which of the following system attributes affects cycle time τ

Select one or more:

- ☒ Instruction set architecture
- ☒ Cache and memory hierarchy
- ☐ Compiler technology
- ☐ Processor implementation

Question 24

Complete

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0.50

To encrypt a byte value, use _____ instruction.

Select one:

- ☒ XOR
- ☐ AND
- ☐ NOT
- ☐ OR

Question 25

Complete

Marked out of
0.50

In multiplication instruction, when the source operand is 8 bit, _____ will be multiplied with source.

Select one:

- ☐ AX
- ☒ AL
- ☐ Whatever general purpose register
- ☐ BX

Question 26

Complete

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1.50

A system programmer needs to compute $449/2 + 358/4$ (decimal). Instruct him to code in debug (number must be in hex) with the least number of instruction counts.

Step 1: Step 2: Step 3: Step 4: Step 5: Step 6: **Question 27**

Complete

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1.00

Convert 0.1015625 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa)

Answer: **Question 28**

Complete

Marked out of
0.50

The instruction that loads the AH register with the lower byte of the flag register is

Select one:

- ☒ LAHF
- ☐ PUSHF
- ☐ AH
- ☐ SAHF

Question 29

Complete

Marked out of
1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL, 0F

ADD AL, F1

watch point:

Zero flag (OF) = Carry flag (CF) = **Question 30**

Complete

Marked out of
1.50

Which are correct about 32 bit index registers of IA-32 processors:

Select one or more:

- ☒ ESI: 32 bit pointer to source memory in data movement instructions
- ☐ ESH,EDH: 16 bit pointers to higher memory above 1M
- ☒ SI: 16 bit pointer to source memory in data movement instructions
- ☒ EDI: 32 bit pointer to destination memory in data movement instructions
- ☒ DI: 16 bit pointer to destination memory in data movement instructions

Question 31

Complete

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1.00

Select the correct sequence of instructions to compute -1024/128 (all values are in hex).

Step 1: Step 2: Step 3: Step 4: **Question 32**

Complete

Marked out of
1.50

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Calculate MIPS rate for this program

Given:

$$\text{MIPS rate} = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

$$CPI = \frac{\sum_{i=1}^n (CPI_i \times I_i)}{I_c}$$

Answer:

Question 33

Complete

Marked out of
1.20

What is the correct sequence of instruction cycle?

- Step 6 ▼
- Step 4 ▼
- Step 1 ▼
- Step 5 ▼
- Step 2 ▼
- Step 3 ▼

Question 34

Complete

Marked out of
1.00

Convert the 32-bit floating point number C4361000 (in hex) to decimal.

Answer: **Question 35**

Complete

Marked out of
0.50

Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit).

Answer: **Question 36**

Complete

Marked out of
0.50

8088 is 16 bit processor, the maximum addressable memory is:

Select one:

- ☐ 640M
- ☐ 640K
- ☐ 1024K
- ☒ 64M

Question 37

Complete

Marked out of
0.50

Write mask byte (in hex) to set bit 6th, 4th of a byte value with OR instruction (LSB is the 1st bit).

Answer: **Question 38**

Complete

Marked out of
0.50

the instruction, CMP to compare source and destination operands by _____

Select one:

- ☒ subtracting
- ☐ adding
- ☐ dividing
- ☐ comparing

Question 39

Complete

Marked out of
1.00

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Calculate the execution time for this program.

Given:

$$T = I_c \times CPI \times \tau$$

$$CPI = \frac{\sum_{i=1}^n (CPI_i \times I_i)}{I_c}$$

Answer:

Question 40

Complete

Marked out of
1.00

Part of computer memory is shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction **MOV AX, [1D4B]** executed

Answer:

Question 41

Complete

Marked out of
1.00

Select correct level for contemporary computer multilevel machine

- Level 3
- Level 5
- Level 6
- Level 1
- Layer 4
- Level 2
- Level 0

Question 42

Complete

Marked out of
1.00

the memory stack area of a program shown in figure

Address	1D50	1D51	1D52	1D53
Value	AF	90	71	DA

The value of SP register is 1D50. What is the value of SP follows the execution of **PUSH SI**

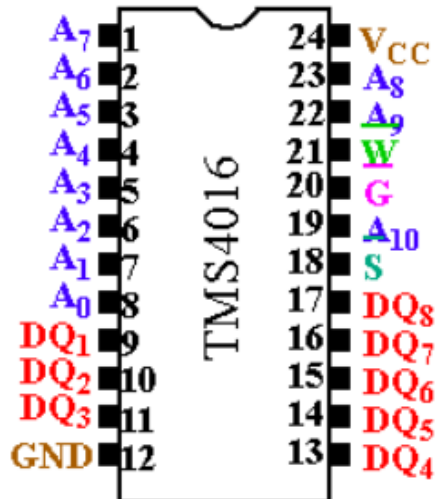
Answer: 1D48

Question 43

Complete

Marked out of
1.00

Choose the correct structure of memory chip as shown below



Note:

DQ: Data pinout

Select one:

- ☐ DRAM 2Kx8-bit
- ☐ SRAM 1Kx16-bit
- ☒ SRAM 2Kx8-bit
- ☐ DRAM 1Kx16-bit

Question 44

Complete

Marked out of
1.00

Given 8-bit floating-point binary format:

1 (sign) + 3 (exponent) + 4 (mantissa)

Convert the 8-bit floating point number 68 (in hex) to decimal.

Answer: 12.0

Question 45

Complete

Marked out of
2.00

Choose correct RAID volume definitions for a request 2T storage.

RAID 0 -
Striped
volume

2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails

RAID5
Volume

At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time

RAID 1 -
Mirror
volume

2 x 2T HDDs are needed, no data lost when the primary storage fails

Spanned
Volume

2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails

◀ Announcements

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