Link Street® 88E6350R/88E6350/88E6351

7 Port AVB Gigabit Ethernet Switch with 5 Integrated PHYs and Synchronous Ethernet

Datasheet Part 3 of 3: Gigabit PHYs

Doc. No. MV-S106031-03, Rev. --
June 4, 2009
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Document Classification: Proprietary Information

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Doc Status: Draft	Technical Publication: 0.03

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Preface

About this Document

The 88E6350R/88E6350/88E6351 datasheet is a three-part set that includes the following documents:

- **88E6350R/88E6350/88E6351 Datasheet Part 1: Overview, Pinout, Applications, Mechanical and Electrical Specifications**

  Provides a feature list and overview describing the 88E6350R/88E6350/88E6351. It also provides the pin description, pin map, mechanical drawings, and electrical specifications.

- **88E6350R/88E6350/88E6351 Datasheet Part 2: Switch Core**

  Provides a description of the switch core of the 88E6350R/88E6350/88E6351 and related register tables.

- **88E6350R/88E6350/88E6351 Datasheet Part 3: Gigabit PHYs**

  Provides a description of the Gigabit PHYs of the 88E6350R/88E6350/88E6351 and related register tables.

Table 1 shows the 88E6350R/88E6350/88E6351 devices feature differences.

Table 1: 88E6350R/88E6350/88E6351 Device Feature Differences

		88E6350R	88E6350	88E6351
Features	GE Switch Ports	7	7	7
	# GE PHYs	5	5	5
	RGMII/MII	2	2	2
	# GMII/MII (Shared w/RGMII)	0	2 (Indicated by BLUE text in Figure 1)	2
	Jumbo Frame Support	10K bytes	10K bytes	10K bytes
	Packet Buffer Memory	1 Mbit	1 Mbit	1 Mbit
	# MAC Addresses	1K	1K	8K
AVB	802.1AS/Qat/Qav/1588	Yes	Yes	Yes
	Timing Application Interface (TAI)	No	Yes	Yes
	Synchronous Ethernet	No	No	Yes
QoS	Queues per Port	4	4	4
	802.1p, Port, TOS/DS, IPv6, TC, MAC	Yes	Yes	Yes
	Programmable Weighting	No	No	Yes
VLAN	Port -based VLANs	Yes	Yes	Yes
	802.1Q VLANs	64	64	4096
	Double Tagging (Q in Q)	Yes	Yes	Yes
Management	Remote Management/Ethertype DSA	Yes	Yes	Yes
	Layer 2 Policy Control Lists (PCL)	No	No	Yes
	802.1D/w/s Spanning Tree	Yes	Yes	Yes
	Port Mirroring/Port Trunking	Yes	Yes	Yes
	IPv4 IGMP & IPv6 MLD Snooping	Yes	Yes	Yes
Other	Ingress Rate Limiting Resources	2/port	5/port	5/port
	Egress Rate Shaping	Enhanced	Enhanced	Enhanced
	802.1X Port and MAC-based Authentication	Yes	Yes	Yes
	GPIO Pins	2	7	7
	Package	128-pin TQFP	176-pin LQFP	176-pin LQFP

Figure 1 shows the overall block diagram for the 88E6350R/88E6350 devices.

Figure 1: 88E6350R/88E6350 Block Diagram

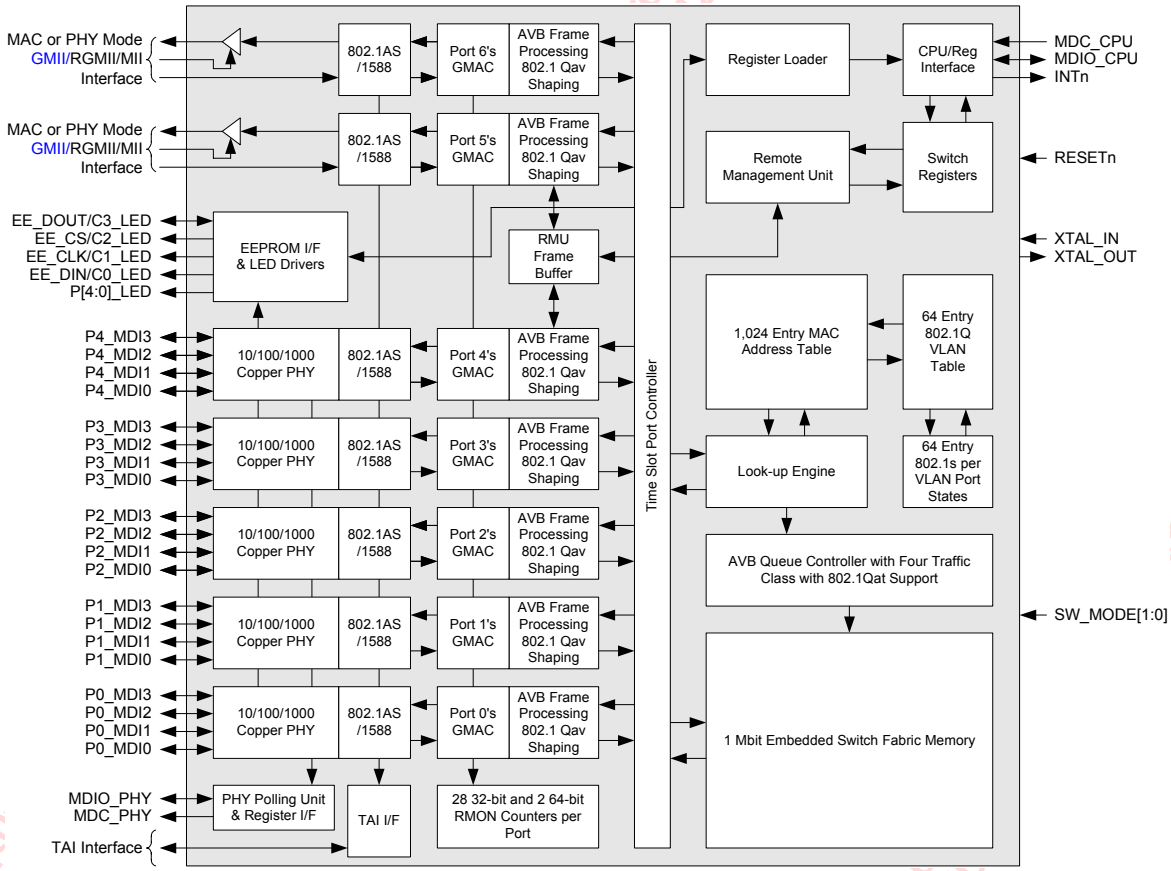
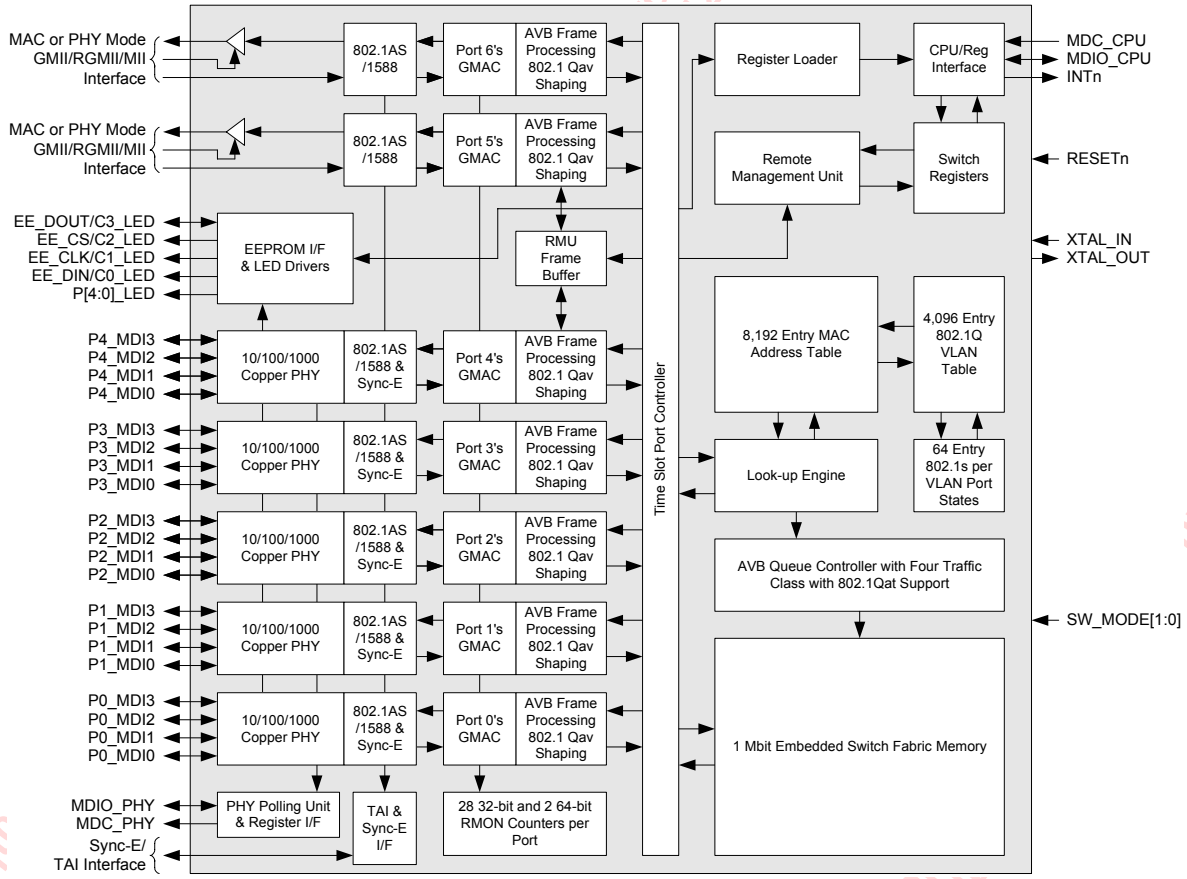


Figure 2 shows the overall block diagram for the 88E6351 device.

Figure 2: 88E6351 Block Diagram



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1 Integrated Gigabit PHY Functional Description

The 88E6350R/88E6350/88E6351 device contains five integrated 10/100/1000BASE-T Gigabit Ethernet transceivers, and integrates two GMII/RGMII/MII ports. The two GMII/RGMII/MII ports (Port 5 and Port 6) can interface with Marvell Alaska Gigabit PHYs and can be optionally configured GMII Mode (full-duplex), MII-MAC Mode (Forward) MII-PHY Mode (Reverse - full-duplex), RGMII-MAC Mode, or RGMII-PHY mode interface option (refer to Part 1 of this datasheet for information on these non-PHY mode interface options).

The 88E6350R/88E6350/88E6351 Gigabit Ethernet Transceiver contains integrated termination resistors.

1.1 Copper Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation.

The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the magnetics. The resistors have to be very accurate to meet the strict IEEE return loss requirements. Typically ± 1% accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements.

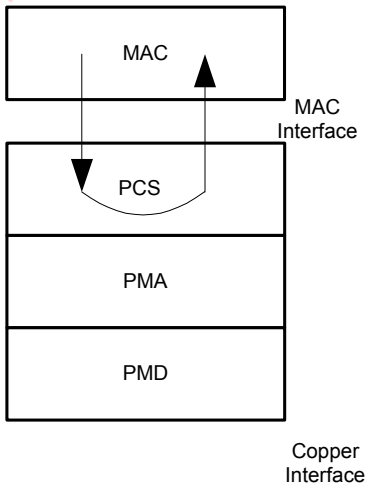
1.2 Loopback for Copper PHYs

1.2.1 MAC Interface Loopback for Copper PHYs

The functionality, timing, and signal integrity of the MAC interface can be tested by placing the 88E6350R/88E6350/88E6351 device in MAC interface loopback mode. This can be accomplished by setting register 0.14 = 1. In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. During loopback, link will be lost and packets will not be received.

If while auto-negotiating and loopback is enabled, FLP Auto-Negotiation codes will be transmitted. If in forced 10BASE-T mode and loopback is enabled, 10BASE-T idle link pulses will be transmitted on the copper side. If in forced 100BASE-T mode and loopback is enabled, 100BASE-T idles will be transmitted on the copper side.

Figure 3: MAC Interface Loopback Diagram



The speed of the interface is determined by register 21_2.2:0.

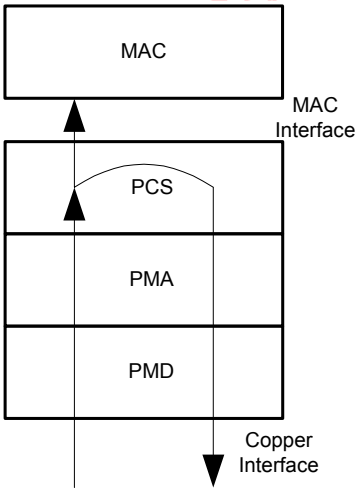
Table 2: MAC Interface Speed Settings

Control Register - MAC					
Register	**Function**	**Setting**	**Mode**	**HW Rst**	**SW Rst**
21_2.2:0	Default MAC interface speed	Bit Speed 000 = Reserved 001 = Reserved 01X = Reserved 100 = 10 Mbps 101 = 100 Mbps 110 = 1000 Mbps 111 = Reserved	R/W	110	Update

1.2.2 Copper Line Loopback

Line loopback allows a link partner to send frames into the 88E6350R/88E6350/88E6351 device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. Refer to Figure 4. This allows the link partner to receive its own frames.

Figure 4: Line Loopback Data Path



Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, both link partners should advertise the same speed and full-duplex. If Auto-Negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, enable the line loopback mode by writing to register 21_2.14

- 21_2.14 = 1 (Enable line loopback)
- 21_2.14 = 0 (Disables line loopback)

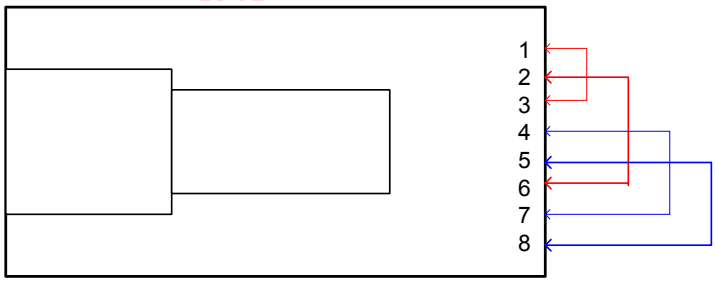
1.2.3 Copper External Loopback

For production testing, an external loopback stub allows testing of the complete data path.

For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, register 16_6.5 must be set to 1 to enable the external loopback. All copper modes require an external loopback stub.

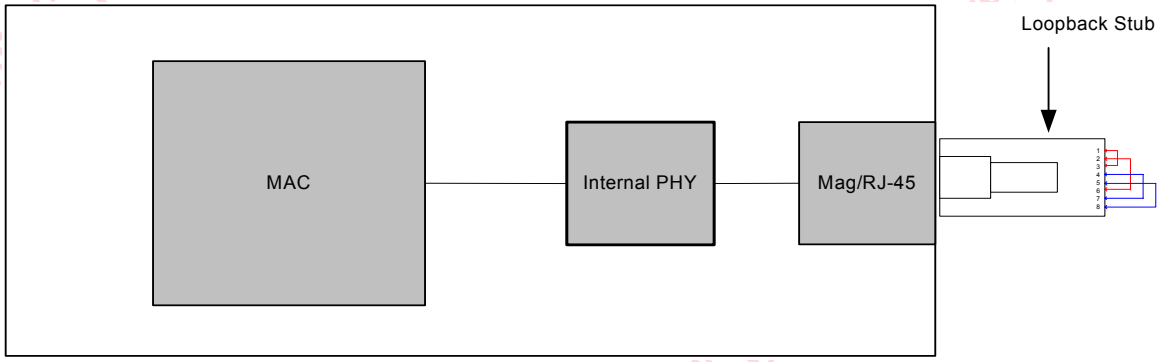
The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 5.

Figure 5: Loopback Stub (Top View with Tab up)



The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 1000 Mbps. It also allows the actual external loopback. See Figure 6. The MAC should see the same packets it sent, looped back to it.

Figure 6: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub



1.3 Synchronizing FIFO

The 88E6350R/88E6350/88E6351 device has transmit and receive synchronizing FIFOs to reconcile frequency differences between the clocks of the MAC interface and the media side.

1.4 Copper Media Transmit and Receive Function

The transmit and receive paths for the 88E6350R/88E6350/88E6351 device are described in the following sections.

1.4.1 Transmit Side Network Interface

1.4.1.1 Multi-mode TX Digital to Analog Converter

The 88E6350R/88E6350/88E6351 device incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

1.4.1.2 Slew Rate Control and Waveshaping

In 1000BASE-T mode, partial response filtering and slew rate control is used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

1.4.2 Encoder

1.4.2.1 1000BASE-T

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM 5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple 88E6350R/88E6350/88E6351 device from outputting the same sequence during idle, which helps to reduce EMI.

1.4.2.2 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled.

1.4.2.3 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

1.4.3 Receive Side Network Interface

1.4.3.1 Analog to Digital Converter

The 88E6350R/88E6350/88E6351 device incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

1.4.3.2 Active Hybrid

The 88E6350R/88E6350/88E6351 device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

1.4.3.3 Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The 88E6350R/88E6350/88E6351 device employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

1.4.3.4 NEXT Canceller

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The 88E6350R/88E6350/88E6351 device employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

1.4.3.5 Baseline Wander Canceller

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The 88E6350R/88E6350/88E6351 device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

1.4.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

1.4.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the 88E6350R/88E6350/88E6351 device, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

1.4.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDIP/N pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16_0.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16_0.10 has no effect.

1.4.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDIP/N pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

1.4.4 Decoder

1.4.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of Auto-Negotiation.

1.4.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

1.4.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

1.5 Power Management

The 88E6350R/88E6350/88E6351 device supports several advanced power management modes that conserve power.

1.5.1 Low Power Modes

Three low power modes are supported in the 88E6350R/88E6350/88E6351 device.

- IEEE 22.2.4.1.5 compliant power down
- Energy Detect (Mode 1)
- Energy Detect+™ (Mode 2)

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect (Mode 1) allows the 88E6350R/88E6350/88E6351 device to wake up when energy is detected on the wire.

Energy Detect+™ (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Details of each mode are described below.

1.5.2 Low Power Operating Modes

1.5.2.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 0.11 = 1. In this mode, the PHY does not respond to any activity on the copper or fiber media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 0.11 = 0 and 16_0.2 = 0.

Upon deassertion of hardware reset, Register 0.11 and 16_0.2 are set to 1 to default the 88E6350R/88E6350/88E6351 device to a power down state.

Register 0.11 and 16_0.2 are logically ORed to form a power down control.

1.5.2.2 Energy Detect Power Down Modes

The 88E6350R/88E6350/88E6351 device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The energy detect modes only apply to the copper media. The status of the energy detect is reported in register 17_0.4 and the energy detect changes are reported in register 19_0.4.

1.5.2.3 Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 16_0.9:8 to 10.

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal 10/100/1000 Mbps operation. If during normal operation the link is lost, the PHY will re-start Auto-Negotiation. If no energy is detected after 5 seconds, the PHY goes back to monitoring receive energy.

1.5.2.4 Energy Detect+™ (Mode 2)

Energy Detect (Mode 2) is entered by setting register 16_0.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the 88E6350R/88E6350/88E6351 device is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the 88E6350R/88E6350/88E6351 device is in Mode 2, then it can wake a connected device.

1.5.2.5 Normal 10/100/1000 Mbps Operation

Normal 10/100/1000 Mbps operation can be entered by turning off energy detect mode by setting register 16_0.9:8 to 00.

1.5.2.6 Power State Upon Exiting Power Down

When the PHY exits power down (register 0.11 or 16_0.2) the active state will depend on whether the energy detect function is enabled (register 16_0.9:8 = 1x). If the energy detect function is enabled, the PHY will transition to the energy detect state first and will wake up only if there is a signal on the wire.

Table 3: Power State after Exiting Power Down

Register 0.11	Register 16_0.2	Register 16_0.9:8	Behavior
1	x	xx	Power down
x	1	xx	Power down
1 to 0	0	00	Transition to power up
0	1 to 0	00	Transition to power up
1 to 0	0	1x	Transition to energy detect state
0	1 to 0	1x	Transition to energy detect state

1.6 Copper Auto-Negotiation

Auto-Negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and Master/Slave preference during a link session.

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (Register 0.15)
- Restart Auto-Negotiation (Register 0.9)
- Transition from power down to power up (Register 0.11)
- The link goes down

The following sections describe each of the Auto-Negotiation modes in detail.

1.6.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T Auto-Negotiation (AN) is based on Clause 28 and 40 of the IEEE802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once Auto-Negotiation is initiated, the 88E6350R/88E6350/88E6351 device determines whether or not the remote device has Auto-Negotiation capability. If so, the 88E6350R/88E6350/88E6351 device and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, the 88E6350R/88E6350/88E6351 device uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of Auto-Negotiation.

After hardware reset, 10/100/1000BASE-T Auto-Negotiation can be enabled and disabled via Register 0.12. Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently. When Auto-Negotiation is disabled, the speed and duplex can be set via registers 0.13, 0.6, and 0.8 respectively. When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 4 and 9.

Changes to registers 0.12, 0.13, 0.6 and 0.8 do not take effect unless one of the following takes place:

- Software reset (registers 0.15)
- Restart Auto-Negotiation (register 0.9)
- Transition from power down to power up (register 0.11)
- The copper link goes down

To enable or disable Auto-Negotiation, Register 0.12 should be changed simultaneously with either register 0.15 or 0.9. For example, to disable Auto-Negotiation and force 10BASE-T half-duplex mode, register 0 should be written with 0x8000.

Registers 4 and 9 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. Hence, a write into Register 4 or 9 has no effect once the 88E6350R/88E6350/88E6351 device begins to transmit Fast Link Pulses (FLPs).This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7 is treated in a similar way as registers 4 and 9 during additional next page exchanges.

If 1000BASE-T mode is advertised, then the 88E6350R/88E6350/88E6351 device automatically sends the appropriate next pages to advertise the capability and negotiate master/slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set register 4.15 to one, and send and receive additional next pages via registers 7and 8, respectively. The 88E6350R/88E6350/88E6351 device stores the previous results from register 8 in internal registers, so that new next pages can overwrite register 8.

Note that 1000BASE-T next page exchanges are automatically handled by the 88E6350R/88E6350/88E6351 device without user intervention, regardless of whether or not additional next pages are sent.

Once the 88E6350R/88E6350/88E6351 device completes Auto-Negotiation, it updates the various status in registers 1, 5, 6, and 10. Speed, duplex, page received, and Auto-Negotiation completed status are also available in registers 17 and 19.

See Section 2, Gigabit PHY Register Description, on page 35.

1.7 Copper Downshift Feature

Without the downshift feature enabled, connecting between two Gigabit link partners requires a four-pair RJ-45 cable to establish 10, 100, or 1000 Mbps link. However, there are existing cables that have only two-pairs, which are used to connect 10 Mbps and 100 Mbps Ethernet PHYs. With the availability of only pairs 1, 2 and 3,6, Gigabit link partners can Auto-Negotiate to 1000 Mbps, but fail to link. The Gigabit PHY will repeatedly go through the Auto-Negotiation but fail 1000 Mbps link and never try to link at 10 Mbps or 100 Mbps.

With the Marvell® downshift feature enabled, the 88E6350R/88E6350/88E6351 device is able to Auto-Negotiate with another Gigabit link partner using cable pairs 1,2 and 3,6 to downshift and link at 10 Mbps or 100 Mbps, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In the case of a three pair cable (additional pair 4,5 or 7,8 - but not both) the same downshift function for two-pair cables applies.

By default, the downshift feature is turned off. Refer to register 16_0.14:11 which describe how to enable this feature and how to control the downshift algorithm parameters.

To enable the downshift feature, the following registers must be set:

- Register 16_0.11 = 1 - enables downshift
- Register 16_0.14:12 - sets the number of link attempts before downshifting

1.8 Fast 1000BASE-T Link Down Indication

Per the IEEE 802.3 Clause 40 standard, a 1000BASE-T PHY is required to wait 750 milliseconds or more to report that link is down after detecting a problem with the link. For Metro Ethernet applications, a Fast Failover in 50 ms is specified, which cannot be met if the PHY follows the 750 ms wait time. This delay can be reduced by intentionally violating the IEEE standard by setting register 26_0.9 to 1.

The delay at which link down is to be reported can be selected by setting register 26_0.11:10. 00 = 0ms, 01 = 10 ± 2 ms, 10 = 20 ± 2ms, 11 = 40 ± 2ms.

1.9 Advanced Virtual Cable Tester®

The 88E6350R/88E6350/88E6351 device Advanced Virtual Cable Tester feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The 88E6350R/88E6350/88E6351 device transmits a signal of known amplitude (+1V) down each of the four pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the MDI_0_0P/N, MDI_0_1P/N, MDI_0_2P/N, and MDI_0_3P/N pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection.

The Advanced VCT™ has 4 modes of operation that is programmable via register 23_5.7:6. The first mode returns the peak with the maximum amplitude that is above a certain threshold. The second mode returns the first peak detected that is above a certain threshold. The third mode measures the systematic offset at the receiver. The fourth mode measures the amplitude seen at a certain specified distance.

The VCT test is initiated by setting register 23_5.15 to 1. This bit will self clear when the test is completed. Register 23_5.14 will be set to a 1 indicating that the TDR results in the registers are valid.

Each point in the VCT reflected waveform is sampled multiple times and averaged. The number of samples to take is programmable via register 23_5.10:8.

Each time the VCT test is enable, the results seen on the four receive channels are reported in registers 16_5, 17_5, 18_5, and 19_5. Register 23_5.13:11 selects which channel transmits the test pulse.

When register 23_5.13:11 is set to 000 the same channel reflection is recorded. In other words, channel 0 transmits a pulse and the reflection seen on channel 0 receiver is reported. Channel 1 transmits a pulse and the reflection seen on channel 1 receiver is reported. The same for channel 2 and channel 3.

When register 23_5.13:11 is set to 100 all 4 receive channels report the reflection seen by a pulse transmitted by channel 0.

When register 23_5.13:11 is set to 101 all 4 receive channels report the reflection seen by a pulse transmitted by channel 1.

When register 23_5.13:11 is set to 110 all 4 receive channels report the reflection seen by a pulse transmitted by channel 2.

When register 23_5.13:11 is set to 111 all 4 receive channels report the reflection seen by a pulse transmitted by channel 3.

Hence, if only the reflection seen on the same channel is desired the VCT test should be run with 23_5.13:11 = 000. If all same channel and cross channel combinations are desired then the VCT test must be run 4 times with 23_5.13:11 set to 100, 101, 110, and 111 for the 4 runs. Registers 16_5, 17_5, 18_5, and 19_5 should be read and stored between each run.

1.9.1 Maximum Peak

When register 23_5.7:6 is set to 00, the maximum peak above a certain threshold is reported. Pulses are sent out and recorded according to the setting of register 25_5.13:11.

There are 5 threshold settings for same channel reflections are specified by registers 26_5.6:0, 26_5.14:8, 27_5.6:0, 27_5.14:8, and 28_5.6:0. These settings correspond to the amplitude threshold the reflected signal has to exceed before it is counted. Any reflected signal below this threshold level is ignored. The 5 threshold settings are based on cable length with the breakpoints at 10 m, 50 m, 110 m, and 140 m.

There are 2 threshold settings for cross-channel specified by registers 25_5.6:0 and 25_5.14:8 and are based on cable length with the breakpoint at 10 m.

The default values are targeted to 85 ohm to 115 ohms. However these threshold settings should be calibrated for the desired impedance setting on the target system.

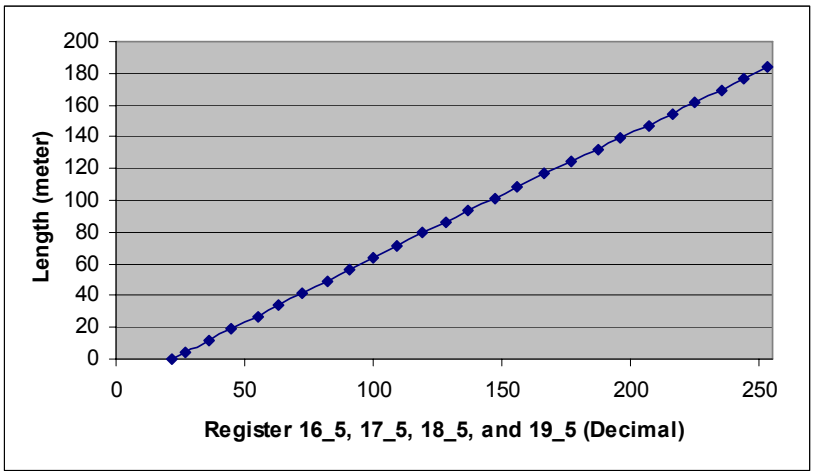
The results are stored in registers 16_5, 17_5, 18_5, and 19_5. Bits 7:0 report the distance of the peak. The distance can be converted to using the trend line in Figure 7. Bits 14:8 report the reflected amplitude. Bit 15 reports whether the reflected amplitude was positive or negative. When bits 15:8 return a value of 0x80, it means there was no peak detected above the threshold. If bits 15:8 return a value of 0x00 then the test failed.

Register 28_5.7 controls the exact distance that is reported. When set to 0 the distance where the amplitude falls to 50% of the peak amplitude is reported. When set to 1 the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude is reported in bits 14:8.

In the maximum peak mode, register 24_5.7:0 is used to set the starting distance of the sweep. Normally this value should be set to 0. If this value is set to a non-zero value, any reflection below the starting distance is ignored. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

Figure 7: Cable Fault Distance Trend Line



1.9.2 First Peak

When register 23_5.7:6 is set to 01, the first peak above a certain threshold is reported. The first peak operates in exactly the same way as the maximum peak except that there has to be some qualification as to what constitutes a peak since the first peak is not necessarily the maximum peak. The first peak is defined as the maximum amplitude seen before the reflected amplitude drops by some value below this peak. This hysteresis value is defined by register 23_5.5:0.

For example, in Figure 8, if Pa is greater than the hysteresis value in 23_5.5:0 and Va is above the threshold value, then Va and Da are reported since it is the first peak that is above the threshold.

If Pa is less than the hysteresis value in 23_5.5:0, then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

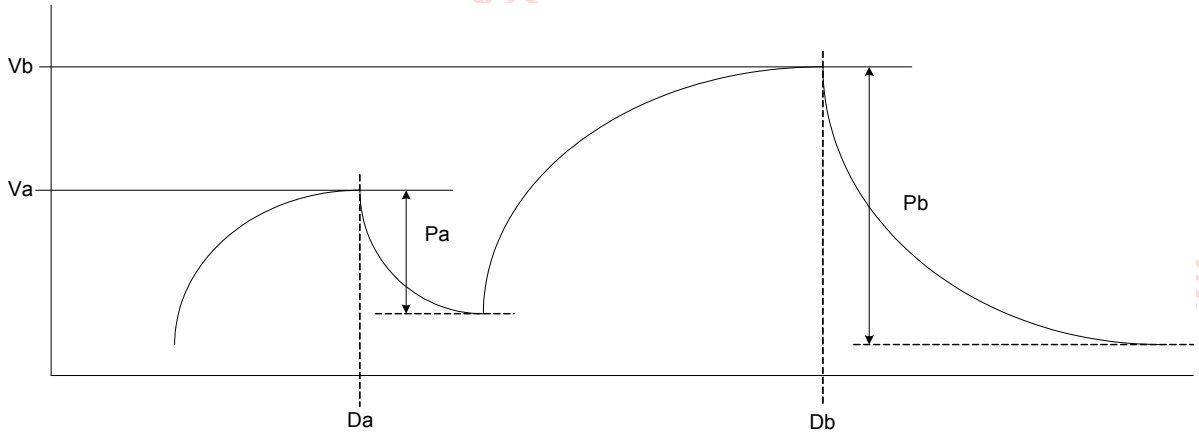
If Pa is greater than the hysteresis value in 23_5.5:0 but Va is below the threshold value then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

Register 28_5.7 controls the exact distance that is reported. When set to 0 the distance where the amplitude falls below the peak amplitude minus the hysteresis level as defined in register 23_5.5:0 is reported. When set to 1 the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude of the first peak is reported in bits 14:8.

In the first peak mode register 24_5.7:0 is used to set the starting distance of the sweep. Normally, this value should be set to 0. If this value is set to a non-zero value, any reflection below the starting distance is ignored. This may be useful to ignore reflections at the transformer that are reported as the first peak. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

Figure 8: First Peak Example



1.9.3 Offset

The offset reports the offset seen at the receiver. This is a debug mode. Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 have no meaning. When bits 15:8 return a value of 0x80 it means there is zero offset. If bit 15:8 returns a value of 0x00 then the test failed.

Note that in the maximum peak, first peak, and sample point modes, the systematic offset is automatically subtracted from the results.

1.9.4 Sample Point

When register 20_8.7:6 is set to 11, the amplitude of the reflected pulse at a particular distance on the cable is reported. Unlike the maximum peak and first peak modes which only measures up to about 200 meters of cable, the sample point mode can measure up to 400 meters of cable.

The sample point returns the amplitude of the reflected pulse at a particular distance on the cable. The distance is set by register 24_5.8:0. The threshold registers 25_5, 26_5, 27_5, and 28_5.6:0 are ignored.

Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 return the same value as 24_5.7:0. Note that register 24_5.8 is not returned. Bits 14:8 return the amplitude, and bit 15 the sign of the amplitude. If the test failed bits 15:8 will return 00000000 (zero amplitude will always return as 10000000).

By programming register 24_5.8:0 from 0x000 to 0x1FF and running the sample point test at each distance it is possible to reconstruct the reflected amplitude. Note that since the threshold is ignored, it is possible that some small reflections in the same channel measurements will be reported at short cable lengths when there are none. This is because the analog hybrid does not 100% cancel out the transmitted signal.

1.9.5 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via registers 28_5.9:8 and 28_5.11:10 respectively. They should normally be set to full amplitude and full pulse width.

1.9.6 Drop Link

When register 28_5.12 is set to 0 the circuit will wait 1.5 seconds to break the link before starting VCT™. When set to 1 this delay is bypassed.

1.9.7 VCT™ with Link Up

The following status requires the PHY to link up with a link partner.

- Register 20_5 reports the pair skew of each pair of wires relative to each other.
- Register 21_5.3:0 reports the polarity of each pair of wires.
- Register 21_5.6:5 reports the crossover status
- Register 20_5 and 21_5 are not valid unless register 21_5.6 is set to 1.

1.10 Data Terminal Equipment (DTE) Detect

The 88E6350R/88E6350/88E6351 device supports the Data Terminal Equipment (DTE) power function. The DTE power function is used to detect if a link partner requires power supplied by the 88E6350R/88E6350/88E6351 device.

The DTE power function can be enabled by writing to register 26_0.8. When DTE is enabled, the 88E6350R/88E6350/88E6351 device will first monitor for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and power from the 88E6350R/88E6350/88E6351 device is not required. If there is no activity coming from the link partner, DTE power engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner will be detected as requiring DTE power.

The DTE power status register (Register 17_0.2) immediately comes up as soon as link partner is detected as a device requiring DTE power. Register 19_0.2 is a stray bit that reports the DTE power status has changed states.

If a link partner that requires DTE power is unplugged, the DTE power status (register 17_0.2) will drop after a user controlled delay (default is 20 seconds - Register 26_0.7:4) to avoid DTE power status register drop during the link partner powering up (for most applications), since the low pass filter (or similar fixture) is removed during power up. If DTE power status drop is desired to be reported immediately, write register 26_0.7:4 to 4'b0000.

A detailed description of the register bits used for DTE power detection for the 88E6350R/88E6350/88E6351 device are shown in Table 4.

Table 4: Registers for DTE Power

Register	Description
26_0.8 - Enable power over Ethernet detection	1 = Enable DTE detect 0 = Disable DTE detect A soft reset is required to enable this feature HW reset: 0 SW reset: Update
17_0.2 - Power over Ethernet detection status	1 = Need power 0 = Do not need power HW reset: 0 SW reset: 0
19_0.2 - Power over Ethernet detection state changed	1 = Changed 0 = No change HW reset: 0 SW reset: 0
26_0.7:4 - DTE detect status drop	Once the PHY no longer detects that the link partner filter, the PHY will wait a period of time before clearing the power over Ethernet detection status bit (17_0.2). The wait time is 5 seconds multiplied by the value of these bits. Example: (5 * 0x4 = 20 seconds) Default at HW reset: 0x4 At SW reset: retain

1.11 Copper Interface CRC Error Counter and Frame Counter

The CRC counter and frame counters, normally found in MACs, are available in the PHYs of the 88E6350R/88E6350/88E6351 device. The error counter and frame counter features are enabled through register writes and each counter is stored in eight register bits.

1.11.1 Enabling the Copper PHY CRC Error Counter and Frame Counter

To enable both counters to count, set 16_6.4 to 1.

To disable and clear both counters, set 16_6.4 to 0.

To read the CRC counter and frame counter, read register 17_6.

17_6.15:8 (Frame count is stored in these bits)

17_6.7:0 (CRC error count is stored in these bits)

The counter does not clear on a read command. To clear the CRC error counter, disable and enable the counters.

1.12 Copper Packet Generator

The 88E6350R/88E6350/88E6351 device contains a very simple packet generator. Table 46 lists the 88E6350R/88E6350/88E6351 device Packet Generator register details.

Once enabled, a fixed length packet of 64 or 1518 byte frame (including CRC) will be transmitted separated by 12 bytes of IPG.The preamble length will be 8 bytes. The payload of the frame is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the frame. An error packet can also be generated.

The registers are as follows:

16_6.3 Packet generation enable. 0 = Normal operation, 1 = Enable internal packet generator

16_6.2 Payload type. 0 = Pseudo random, 1 = Fixed 5A, A5, 5A, A5,...

16_6.1 Packet length. 0 = 64 bytes, 1 = 1518 bytes

16_6.0 Error packet. 0 = Good CRC, 1 = Symbol error and corrupt CRC.

16_6.15:8 Packet Burst Size. 0x00 = Continuous, 0x01 to 0xFF = Burst 1 to 255 packets.

If register 16_6.15:8 is set to a non-zero value, then register 16_6.3 will self clear once the required number of packets are generated. Note that if register 16_6.3 is manually set to 0 while packets are still bursting, the bursting will cease immediately once the current active packet finishes transmitting. The value in register 16_6.15:8 should not be changed while 16_6.3 is set to 1.

1.13 MDI/MDIX Crossover

The 88E6350R/88E6350/88E6351 device automatically determines whether or not it needs to cross over between pairs as shown in Table 5 so that an external crossover cable is not required. If the 88E6350R/88E6350/88E6351 device interoperates with a device that cannot automatically correct for crossover, the 88E6350R/88E6350/88E6351 device makes the necessary adjustment prior to commencing Auto-Negotiation. If the 88E6350R/88E6350/88E6351 device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the 88E6350R/88E6350/88E6351 device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the 88E6350R/88E6350/88E6351 device follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E6350R/88E6350/88E6351 device uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16_0.6:5.

The pin mapping in MDI and MDIX modes is shown in Table 5.

Table 5: Media Independent Interface Pin Mapping

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note Table 5 assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17_0.6. This bit indicates whether the receive pairs (3,6) and (1,2) are crossed over. In 1000BASE-T operation, the 88E6350R/88E6350/88E6351 device can correct for crossover between pairs (4,5) and (7,8) as shown in Table 5. However, this is not indicated by Register 17_0.6.

If 1000BASE-T link is established, pairs (1,2) and (3,6) crossover is reported in register 21_5.4, and pairs (4,5) and (7,8) crossover is reported in register 21_5.5.

1.14 Polarity Correction

The 88E6350R/88E6350/88E6351 device automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17_0.1. This bit indicates whether the receive pair (3,6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1,2) and Register 17_0.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17_0.1 only indicates polarity reversal on the pairs described above.

If 1000BASE-T link is established register 21_5.3:0 reports the polarity on all 4 pairs.

Polarity correction can be disabled by register write 16_0.1 = 1. Polarity will then be forced in normal 10BASE-T mode.

1.15 Exchange Complete with No Link

Sometimes when link does not come up, it is difficult to determine whether the failure is due to the auto-negotiation FLP not completing or from the 10/100/1000BASE-T link not being able to come up.

Register 19_0.3 is a sticky bit that gets set to 1 whenever the FLP exchange is completed but the link cannot be established for some reason. Once the bit is set, it can be cleared only by reading the register.

This bit will not be set if the FLP exchange is not completed, or if link is established.

1.16 Copper PHY LED

LED behavior is highly configurable with registers, which are described in Part 2 of the 88E6350R/88E6350/88E6351 datasheet. See Switch Per-port Registers, LED Control, LED 0 &1 Control, and LED 2 & 3 Control for LED register details.

1.17 Synchronous Clocking Support (88E6351 Only)

Synchronous clocking support is provided when the device is operating in the following modes: 1000BASE-T, or 100BASE-TX on the line interface. There are two components to synchronous clocking support. The first is to output a recovered clock. The second is to select between the local reference clock and a cleaned up recovered clock.

1.17.1 Recovered Clock

The SE_RCLK0 and SE_RCLK1 pins of the chip output either a 125 MHz or 25 MHz clock that is based on the 125 MHz recovered clock on the receive path when linked to 1000BASE-T or 100BASE-TX. If a 25 MHz clock is selected, the 125 MHz recovered clock is internally divided by 5 with 60% low and 40% high.

Register 16_2.11 selects whether SE_RCLK outputs 25 MHz XTAL clock or drives LOW when the link is down or when the copper receiver is linked to 10BASE-T.

- 0 = SE_RCLK outputs 25 MHz XTAL clock during link down or 10BASE-T
- 1 = SE_RCLK drives LOW during link down or 10BASE-T

The SE_RCLK0 pin is enabled when register 16_2.8 is set to 1, and SE_RCLK1 pin is enabled when register 16_2.9 is set to 1. Each of these bits should be set to 1 for only one port (i.e. 16_2.8 set to 1 in port 0 and 16_2.9 set to 1 for port 1). If the bit is set high for multiple ports then the highest numbered physical port that is enabled is selected. The highest numbered physical port is defined to be the port connected to MDIP/N3 and not necessarily the port with the highest PHYAD[4:0] value. (i.e. the PHY_ORDER setting affects the PHYAD[1:0] setting.)

Register 16_2.12 selects whether SE_RCLK outputs 25 MHz or 125 MHz. 0 = 25 MHz, 1 = 125 MHz.

1.17.2 Reference Clock Select

The 25 MHz reference clock source to the copper unit is independently selectable per port. On hardware reset the XTAL_IN is selected as the reference clock source for all ports. SE_SCLK can be selected as the reference clock source on a per port basis.

Register 16_2.7 selects whether the reference clock for the copper interface is based on XTAL_IN or SCLK. 0 = XTAL_IN, 1 = SE_SCLK.

Register 16_2.6 selects whether the reference clock for the 1.25 GHz SERDES interface is based on XTAL_IN or SE_SCLK. 0 = XTAL_IN, 1 = SE_SCLK.

Register 26_4.14 selects whether the reference clock for the QSGMII is based on XTAL_IN or SE_SCLK. 0 = XTAL_IN, 1 = SE_SCLK.

The CLK_SEL[1:0] must be set to 11 in order to do the reference clock selection.

Since changing the reference clocks disturbs the PHY, a software reset must be issued before any change to the clock select takes place.

1.18 Interrupt

The INT pin supports the interrupt function. INT is active low.

Registers 18_0 and 18_2 are the Interrupt Enable registers for the copper media and the MAC interfaces, respectively.

Registers 19_0 and 19_2 are the Interrupt Status registers for the copper media and the MAC interfaces, respectively.

Registers 23_0 and 23_2 are the Interrupt Status summary registers. Registers 23_0 and 23_2 are physically the same registers. Register 23 lists the ports that have active interrupts. Register 23 provides a quick way to isolate the interrupt so that the MAC or switch does not have to poll register 19 for all ports. Reading register 23 does not de-assert the INTn pin. Note that register 23 can be accessed by reading register 23 using the PHY address of any of the four ports.

The various pages of register 18 are used to select the interrupt events that can activate the interrupt pin. The interrupt pin will be activated if any of the selected events on any page of register 18 occurs.

If a certain interrupt event is not selected by register 18, it will still be indicated by the corresponding register 19 bits if the interrupt event happens. However, the unselected events will not cause the Interrupt pin to be activated.

1.19 Temperature Sensor

The 88E6350R/88E6350/88E6351 device contains an internal temperature sensor. The procedure to read the temperature sensor is as follows:

1. Enable the Temperature Sensor through Port 0 (Register 26_6.5 = 1).
2. Disable the Temperature Sensor through Port 0 (Register 26_6.5 = 0).
3. Read the Temperature Sensor data - can be read from Port 0 to Port 4 - (Register 26_6.4:0).

See the latest Release Notes for details on how to convert register values read to junction temperature.

2 Gigabit PHY Register Description

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 0 to 21, and 23 to 28 register 22 bits 7 to 0 are used to specify the page. For registers 30 and 31 register 29 bits 5:0 are used to specify the page. There is no paging for registers 22 and 29.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 16 page 2 bits 5 to 2 is specified as 16_2.5:2.

Register 16 page 2 bits 5 is specified as 16_2.5.

Register 2 bit 3 to 0 is specified as 2.3:0.

Note that In this context the setting of the page register (register 22) has no effect.

Register 2 bit 3 is specified as 2.3.

Note that in order for the paging mechanism to work correctly register 22.15 must be set to 0 to disable the automatic medium register selection.

These registers can be accessed through the PHY SMI Command registers as described in Part 2 of the 88E6350R/88E6350/88E6351 datasheet. See Multi-Chip Addressing Mode, SMI Command Register and SMI Data Register for details.

Table 6 below defines the register types used in the register map.

Table 6: Register Types

Type	Description
C	Clear after read.
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
Retain	The register value is retained after software reset is executed.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROS	Read only, Set high after read.
ROC	Read only clear. After read, register field is cleared.
RW	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All field bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
RWR	Read/Write clear on read. All field bits are readable and writable. After reset, register field is cleared to 0.
RWS	Read/Write set. All field bits are readable and writable. After reset, register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field doesn't take effect until soft reset is executed.
WO	Write only. Reads to this type of register field return undefined data.

For all binary equations appearing in the register map, the symbol | is equal to a binary OR operation.

Table 7: 88E6350R/88E6350/88E6351 Device Register Map Summary

Register Address	Page Address 0	1	2	3	4	5	6	7 to 254	255
0	Control Register								
1	Status Register								
2	PHY Identifier 1								
3	PHY Identifier 2								
4	Autonegotiation Copper Advertisement Register								
5	Autonegotion Copper Link Partner Ability Register - Base Page								
6	Autonegotiation Copper Expansion Register								
7	Autonegotiation Copper Next Page Transmit Register								
8	Autonegotiation Copper Link Partner Next Page Register								
9	1000BASE-T Control Register								
10	1000BASE-T Status Register								
11	Reserved								
12	Reserved								
13	Reserved								
14	Reserved								
15	Extended Status Register								
16	Copper Specific Control Register 1		MAC Specific Control Register 1			Advanced VCT TX to MDI[0] Rx Coupling	Packet Generation/ Line Loopback		Factory Test Modes
17	Copper Specific Status Register 1		MAC Specific Status Register 1			Advanced VCT TX to MDI[1] Rx Coupling	CRC checker		Factory Test Modes
18	Copper Specific Interrupt Enable Register		MAC Specific Interrupt Enable Register			Advanced VCT TX to MDI[2] Rx Coupling			Factory Test Modes
19	Copper Specific Status Register 2		MAC Specific Status Register 2			Advanced VCT TX to MDI[3] Rx Coupling			
20	Copper Specific Status Register 3					1000BASE-T Pair Skew			
21	Receive Error Counter		MAC Specific Control Register 2			1000BASE-T Pair Swap and Polarity			
22	Page Address								
23	Global Interrupt Status		Global Interrupt Status			Advance VCT Control			Factory Test Modes
24						Advanced VCT Sample Point Distance			Factory Test Modes
25						Advanced VCT Cross Pair Threshold			Factory Test Modes
26	Copper Specific Control Register 2		MAC Specific Control Register 2			Advanced VCT Same Pair Impedance Threshold 0 and 1	Misc Test		
27						Advanced VCT Same Pair Impedance Threshold 2 and 3			
28						Advanced VCT Same Pair Impedance Threshold 4 and Transmit Pulse Control			
29	Factory Test Modes								
30	Factory Test Modes								
31	Factory Test Modes								

Table 8: Register Map

Table 9: Control Register
Offset: Page Any, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by Registers 21_2.2:0. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation If Register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 is set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

Table 9: Control Register (Continued)
Offset: Page Any, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Power Down	R/W	See Descr	Retain	Power down is controlled via register 0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_15) and Restart Auto-Negotiation (0.9) are not set by the user. IEEE power down shuts down the chip except for the GMII interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the GMII interface also shuts down. 1 = Power down 0 = Normal operation
10	Reserved	RO	0x0	0x0	Reserved.
9	Restart Copper Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Copper Duplex Mode	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex
7	Reserved	RO	0x0	0x0	Reserved.
6	Speed Selection (MSB)	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	Always 000000	Always 000000	Will always be 0.

Table 10: Status Register
Offset: Page Any, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	Always 1	Always 1	1 = PHY able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	Always 1	Always 1	1 = PHY able to perform half-duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	Always 1	Always 1	1 = PHY able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 1	Always 1	1 = PHY able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Copper Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	Always 1	Always 1	1 = PHY able to perform Auto-Negotiation
2	Copper Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO,LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 11: PHY Identifier 1
Offset: Page Any, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 12: PHY Identifier 2
Offset: Page Any, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24
9:4	Model Number	RO	Always 100111	Always 100111	Model Number 100111
3:0	Revision Number	RO	See Descr	See Descr	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 13: Auto-Negotiation Advertisement Register
Offset: Page Any, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	Always 0	Always 0	Must be 0.
13	Remote Fault	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down Reserved bit is R/W to allow for forward compatibility with future IEEE standards.
11	Asymmetric Pause	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Asymmetric Pause 0 = No asymmetric Pause

Table 13: Auto-Negotiation Advertisement Register (Continued)
Offset: Page Any, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Pause	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	R/W	0x0	Retain	0 = Not capable of 100BASE-T4
8	100BASE-TX Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised
7	100BASE-TX Half-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised

Table 13: Auto-Negotiation Advertisement Register (Continued)
Offset: Page Any, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
6	10BASE-TX Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised
5	10BASE-TX Half-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised
4:0	Selector Field	R/W	0x01	Retain	Selector Field mode 00001 = 802.3

Table 14: Link Partner Ability Register - Base Page
Offset: Page Any, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
13	Remote Fault	RO	0x0	0x0	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability Field	RO	0x0	0x0	Received Code Word Bit 12
11	Asymmetric Pause	RO	0x0	0x0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause Capable	RO	0x0	0x0	Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
9	100BASE-T4 Capability	RO	0x0	0x0	Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
7	100BASE-TX Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
6	10BASE-T Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
5	10BASE-T Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
4:0	Selector Field	RO	0x00	0x00	Selector Field Received Code Word Bit 4:0

Table 15: Auto-Negotiation Expansion Register
Offset: Page Any, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
4	Parallel Detection Fault	RO,LH	0x0	0x0	Register 6.4 is not valid until the Auto-Negotiation complete bit (Reg 1.5) indicates completed. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	Link Partner Next page Able	RO	0x0	0x0	Register 6.3 is not valid until the Auto-Negotiation complete bit (Reg 1.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	Register 6.2 is not valid until the Auto-Negotiation complete bit (Reg 1.5) indicates completed. 1 = Local Device is Next Page able 0 = Local Device is not Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6.1 is not valid until the Auto-Negotiation complete bit (Reg 1.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	Register 6.0 is not valid until the Auto-Negotiation complete bit (Reg 1.5) indicates completed. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 16: Next Page Transmit Register
Offset: Page Any, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 17: Link Partner Next Page Register
Offset: Page Any, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 18: 1000BASE-T Control Register
Offset: Page Any, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
12	MASTER/SLAVE Manual Configuration Enable	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/SLAVE Configuration Value	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
10	Port Type	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Register 9.10 is ignored if Register 9.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised

Table 18: 1000BASE-T Control Register (Continued)
Offset: Page Any, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
8	1000BASE-T Half-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Advertise 0 = Not advertised
7:0	Reserved	R/W	0x00	Retain	0

Table 19: 1000BASE-T Status Register
Offset: Page Any, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/SLAVE Configuration Fault	RO,LH	0x0	0x0	This register bit will clear on read. 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex
9:8	Reserved	RO	0x0	0x0	Reserved
7:0	Idle Error Count	RO, SC	0x00	0x00	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 20: Extended Status Register
Offset: Page Any, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	Always 0	Always 0	0 = Not 1000BASE-X full-duplex capable
14	1000BASE-X Half-Duplex	RO	Always 0	Always 0	0 = Not 1000BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	Always 1	Always 1	1 = 1000BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	Always 1	Always 1	1 = 1000BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

Table 21: Copper Specific Control Register 1
Offset: Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable Link Pulses	R/W	0x0	0x0	1 = Disable Link Pulse 0 = Enable Link Pulse
14:12	Downshift counter	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1x, 2x, ...8x is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. 000 = 1x 100 = 5x 001 = 2x 101 = 6x 010 = 3x 110 = 7x 011 = 4x 111 = 8x
11	Downshift Enable	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Enable downshift. 0 = Disable downshift.
10	Force Copper Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation
9:8	Energy Detect	R/W	See Descr.	Update	0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP (Energy Detect+™)
7	Enable Extended Distance	R/W	0x0	Retain	When using cable exceeding 100m, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold
6:5	MDI Crossover Mode	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	R/W	0x0	Retain	Write 0
3	Copper Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable

Table 21: Copper Specific Control Register 1 (Continued)
Offset: Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Power Down	R/W	0x0	Retain	Power down is controlled via register 0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_15) and Restart Auto-Negotiation (0.9) are not set by the user. IEEE power down shuts down the chip except for the GMII interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the GMII interface also shuts down. 1 = Power down 0 = Normal operation
1	Polarity Reversal Disable	R/W	0x0	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled The detected polarity status is shown in Register 17_0.1, or in 1000BASE-T mode, 21_5.3:0.
0	Disable Jabber	R/W	0x0	Retain	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

Table 22: Copper Specific Status Register 1
Offset: Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x2	Retain	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved
10	Copper Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
8	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
7	Reserved	RO	0x0	0x0	0
6	MDI Crossover Status	RO	0x1	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
5	Downshift Status	RO	0x0	0x0	1 = Downshift 0 = No Downshift

Table 22: Copper Specific Status Register 1
Offset: Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Copper Energy Detect Status	RO	0x0	0x0	1 = Sleep 0 = Active
3	Global Link Status	RO	0x0	0x0	1 = Copper link is up 0 = Copper link is down
2	DTE power status	RO	0x0	0x0	1 = Link partner needs DTE power 0 = Link partner does not need DTE power
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal Polarity reversal can be disabled by writing to Register 16_0.1. In 1000BASE-T mode, polarity of all pairs are shown in Register 21_5.3:0.
0	Jabber (real time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 23: Copper Specific Interrupt Enable Register
Offset: Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	Reserved	R/W	0x0	Retain	0
6	MDI Crossover Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Downshift Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
4	Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	FLP Exchange Complete but no Link Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	DTE power detection status changed interrupt enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 24: Copper Specific Status Register 2
Offset: Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error	RO,LH	0x0	0x0	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
14	Copper Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Copper Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Copper Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Copper Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Copper Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Copper Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	Copper False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	Reserved	RO	Always 0	Always 0	0
6	MDI Crossover Changed	RO,LH	0x0	0x0	1 = Crossover changed 0 = Crossover not changed
5	Downshift Interrupt	RO,LH	0x0	0x0	1 = Downshift detected 0 = No down shift
4	Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected
3	FLP Exchange Complete but no Link	RO,LH	0x0	0x0	1 = FLP Exchange Completed but Link Not Established 0 = No Event Detected
2	DTE power detection status changed interrupt	RO,LH	0x0	0x0	1 = DTE power detection status changed 0 = No DTE power detection status change detected
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity Changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 25: Copper Specific Control Register 3
Offset: Page 0, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	R/W	0x000	Retain	Write all 0s
3	Reverse MDIP/N[3] Transmit Polarity	R/W	0x0	Retain	1 = Reverse Transmit Polarity 0 = Normal Transmit Polarity
2	Reverse MDIP/N[2] Transmit Polarity	R/W	0x0	Retain	1 = Reverse Transmit Polarity 0 = Normal Transmit Polarity
1	Reverse MDIP/N[1] Transmit Polarity	R/W	0x0	Retain	1 = Reverse Transmit Polarity 0 = Normal Transmit Polarity
0	Reverse MDIP/N[0] Transmit Polarity	R/W	0x0	Retain	1 = Reverse Transmit Polarity 0 = Normal Transmit Polarity

Table 26: Receive Error Counter Register
Offset: Page 0, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 27: Page Address
Offset: Page Any, Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	00000000
7:0	Page select for registers 0 to 28	R/W	0x00	Retain	Page Number

Table 28: Global Interrupt Status
Offset: Page 0,2, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	Always 0s	Always 0s	0
3:0	Port X Interrupt	RO	0x0	0x0	Depending on how many ports there are bit 0 to n correspond to the port number that has the interrupt. 1 = Interrupt active on port X 0 = No interrupt active on port X

Table 29: Copper Specific Control Register 2
Offset: Page 0, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000 BASE-T Transmitter type	R/W	See Desc.	Retain	1 = Class A 0 = Class B
14:13	Reserved	R/W	0x0	Retain	Write 0.
12	100 BASE-T Transmitter type	R/W	0x0	Retain	1 = Class A 0 = Class B
11:10	Gigabit Link Down Delay	R/W	0x0	Retain	This register only has an effect if register 26_0.9 is set to 1. 00 = 0ms 01 = 10 ± 2ms 10 = 20 ± 2ms 11 = 40 ± 2ms
9	Speed Up Gigabit Link Down Time	R/W	0x0	Retain	1 = Enable faster gigabit link down 0 = Use IEEE gigabit link down
8	DTE detect enable	R/W	0x0	Update	1 = Enable DTE detection 0 = Disable DTE detection
7:4	DTE detect status drop hysteresis	R/W	0x4	Retain	0000: report immediately 0001: report 5s after DTE power status drop ... 1111: report 75s after DTE power status drop
3:2	100 MB test select	R/W	0x0	Retain	0x = Normal Operation 10 = Select 112 ns sequence 11 = Select 16 ns sequence
1	10 BT polarity force	R/W	0x0	Retain	1 = Force negative polarity for Receive only 0 = Normal Operation
0	Reserved	R/W	0x0	Retain	Write 0

Table 30: MAC Specific Control Register 1
Offset: Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Transmit FIFO Depth	R/W	See Descr.	Retain	1000BASE-T 00 = ± 16 Bits 01 = ± 24 Bits 10 = ± 32 Bits 11 = ± 40 Bits
13	Reserved	R/W	0x0	Update	Set to 0
12	RCLK Frequency Select	R/W	0x0	Retain	0 = 25 MHz 1 = 125 MHz
11	RCLK Link Down Disable	R/W	0x0	Retain	0 = RCLK outputs 25 MHz XTAL clock during link down and 10BASE-T. 1 = RCLK low during link down and 10BASE-T.
10	Reserved	R/W	0x0	Retain	Set to 0
9	SE_RCLK1 Select	R/W	0x0	Retain	The highest numbered port with this bit set will output the clock. The 125 MHz recovered clock is output as is or divided by 5 and output on SE_RCLK1 depending on the setting of 16_2.12. 1 = Output recovered clock on SE_RCLK1 0 = Do not output recovered clock on SE_RCLK1
8	SE_RCLK0 Select	R/W	0x0	Retain	The highest numbered port with this bit set will output the clock. The 125 MHz recovered clock is output as is or divided by 5 and output on SE_RCLK0 depending on the setting of 16_2.12. 1 = Output recovered clock on SE_RCLK0 0 = Do not output recovered clock on SE_RCLK0
7	Copper Reference Clock Source Select	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 1 = Use SE_SCLK as 25 MHz source 0 = Use XTAL1 as 25 MHz source
6	Pad Odd Nibble Preambles	R/W	0x1	Update	1 = Pad odd nibble preambles in copper receive packets. 0 = Do not pad odd nibble preambles in copper receive packets.
5:4	Reserved	R/W	0x0	Retain	Write 0

Table 30: MAC Specific Control Register 1
Offset: Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
3	GMII Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether the GMII RX_CLK powers down when Register 0.11, 16_0.2 are used to power down the device or when the PHY enters the energy detect state. 1 = Always power up 0 = Can power down
2:0	Reserved	R/W	0x0	Update	Write 0

Table 31: MAC Specific Interrupt Enable Register
Offset: Page 2, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	000000000
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:4	Reserved	R/W	0x0	Retain	000
3	FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1:0	Reserved	R/W	0x0	Retain	00

Table 32: MAC Specific Status Register
Offset: Page 2, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	00000000
7	FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:4	Reserved	RO	Always 0	Always 0	000
3	FIFO Idle Inserted	RO,LH	0x0	0x0	1 = Idle Inserted 0 = No Idle Inserted
2	FIFO Idle Deleted	RO,LH	0x0	0x0	1 = Idle Deleted 0 = Idle not Deleted
1:0	Reserved	RO	Always 0	Always 0	00

Table 33: MAC Specific Control Register 2
Offset: Page 2, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	0
14	Line Loopback	R/W	0x0	0x0	1 = Enable Line Loopback 0 = Normal Operation
13:12	Reserved	R/W	0x1	Update	1
11:7	Reserved	R/W	0x00	0x00	00000
6	Reserved	R/W	0x1	Update	1
5:4	Reserved	R/W	0x0	Retain	0
3	Block Carrier Extension Bit	R/W	0x0	Retain	1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
2:0	Default MAC interface speed	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. MAC Interface Speed during Link down while Auto-Negotiation is enabled. TX_CLK Speed Bit Speed Link Down 1000BASE-T 000 = 10 Mbps 2.5 MHz 0 MHz 001 = 100 Mbps 25 MHz 0 MHz 01X = 1000 Mbps 0 MHz 0 MHz 100 = 10 Mbps 2.5 MHz 2.5 MHz 101 = 100 Mbps 25 MHz 25 MHz 110 = 1000 Mbps 2.5 MHz 2.5 MHz 111 = 1000 Mbps 25 MHz 25 MHz

Table 34: Advanced VCT™ TX to MDI[0] Rx coupling
Offset: Page 5, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. when 23_5.7 = 0 and 23_5.13:11 = 000 or 100 the reflected amplitude below the threshold specified in registers 26_5, 27_5, and 28_5.6:0 are reported as 0 mV. when 23_5.7 = 0 and 23_5.13:11 is not 000 or 100 the reflected amplitude below the threshold specified in register 25_5 are reported as 0 mV. when 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, and 28_5 are ignored. The amplitude value is valid only when 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note

This register reports the reflection see based on the setting of register 23_5.13:11
000 = MDI[0] Tx to MDI[0] Rx
100 = MDI[0] Tx to MDI[0] Rx
101 = MDI[1] Tx to MDI[0] Rx
110 = MDI[2] Tx to MDI[0] Rx
111 = MDI[3] Tx to MDI[0] Rx

Table 35: Advanced VCT™ TX to MDI[1] Rx coupling
Offset: Page 5, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. when 23_5.7 = 0 and 23_5.13:11 = 000 or 101 the reflected amplitude below the threshold specified in registers 26_5, 27_5, and 28_5.6:0 are reported as 0 mV. when 23_5.7 = 0 and 23_5.13:11 is not 000 or 101 the reflected amplitude below the threshold specified in register 25_5 are reported as 0 mV. when 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, and 28_5 are ignored. The amplitude value is valid only when 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note

This register reports the reflection see based on the setting of register 23_5.13:11
000 = MDI[1] Tx to MDI[1] Rx
100 = MDI[0] Tx to MDI[1] Rx
101 = MDI[1] Tx to MDI[1] Rx
110 = MDI[2] Tx to MDI[1] Rx
111 = MDI[3] Tx to MDI[1] Rx

Table 36: Advanced VCT™ TX to MDI[2] Rx coupling
Offset: Page 5, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. when 23_5.7 = 0 and 23_5.13:11 = 000 or 110 the reflected amplitude below the threshold specified in registers 26_5, 27_5, and 28_5.6:0 are reported as 0 mV. when 23_5.7 = 0 and 23_5.13:11 is not 000 or 110 the reflected amplitude below the threshold specified in register 25_5 are reported as 0 mV. when 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, and 28_5 are ignored. The amplitude value is valid only when 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note

This register reports the reflection see based on the setting of register 23_5.13:11
000 = MDI[2] Tx to MDI[2] Rx
100 = MDI[0] Tx to MDI[2] Rx
101 = MDI[1] Tx to MDI[2] Rx
110 = MDI[2] Tx to MDI[2] Rx
111 = MDI[3] Tx to MDI[2] Rx

Table 37: Advanced VCT™ TX to MDI[3] Rx coupling
Offset: Page 5, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. when 23_5.7 = 0 and 23_5.13:11 = 000 or 111 the reflected amplitude below the threshold specified in registers 26_5, 27_5, and 28_5.6:0 are reported as 0 mV. when 23_5.7 = 0 and 23_5.13:11 is not 000 or 111 the reflected amplitude below the threshold specified in register 25_5 are reported as 0 mV. when 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, and 28_5 are ignored. The amplitude value is valid only when 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note

This register reports the reflection see based on the setting of register 23_5.13:11
000 = MDI[3] Tx to MDI[3] Rx
100 = MDI[0] Tx to MDI[3] Rx
101 = MDI[1] Tx to MDI[3] Rx
110 = MDI[2] Tx to MDI[3] Rx
111 = MDI[3] Tx to MDI[3] Rx

Table 38: 1000 BASE-T Pair Skew Register
Offset: Page 5, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 7,8 (MDI[3]±)	RO	0x0	0x0	Skew = bit value x 8 ns. Value is correct to within ± 8 ns. The contents of 20_5.15:0 are valid only if Register 21_5.6 = 1
11:8	Pair 4,5 (MDI[2]±)	RO	0x0	0x0	Skew = bit value x 8 ns. Value is correct to within ± 8 ns.
7:4	Pair 3,6 (MDI[1]±)	RO	0x0	0x0	Skew = bit value x 8 ns. Value is correct to within ± 8 ns.
3:0	Pair 1,2 (MDI[0]±)	RO	0x0	0x0	Skew = bit value x 8 ns. Value is correct to within ± 8 ns.

Table 39: 1000 BASE-T Pair Swap and Polarity
Offset: Page 5, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	
6	Register 20_5 and 21_5 valid	RO	0x0	0x0	The contents of 21_5.5:0 and 20_5.15:0 are valid only if Register 21_5.6 = 1 1= Valid . 0 = Invalid
5	C, D Crossover	RO	0x0	0x0	1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]±
4	A, B Crossover	RO	0x0	0x0	1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]±
3	Pair 7,8 (MDI[3]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]±) Polarity		0x0	0x0	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
0	Pair 1,2 (MDI[0]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive

Table 40: Advance VCT™ Control
Offset: Page 5, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable Test	R/W, SC	0x0	0x0	1 = Enable test 0 = Disable test This bit will self clear when the test is completed
14	Test status	RO	0x0	0x0	0 = Test not started/in progress, 1 = test completed
13:11	Transmitter Channel Select	R/W	0x0	0x0	000 - Tx 0 => Rx 0, Tx 1 => Rx 1, Tx 2 => Rx 2, Tx 3 => Rx 3. 100 - Tx 0 => Rx 0, Tx 0 => Rx 1, Tx 0 => Rx 2, Tx 0 => Rx 3. 101 - Tx 1 => Rx 0, Tx 1 => Rx 1, Tx 1 => Rx 2, Tx 1 => Rx 3. 110 - Tx 2 => Rx 0, Tx 2 => Rx 1, Tx 2 => Rx 2, Tx 2 => Rx 3. 111 - Tx 3 => Rx 0, Tx 3 => Rx 1, Tx 3 => Rx 2, Tx 3 => Rx 3. 01x - Reserved 0x1 - Reserved
10:8	Number of Sample Averaged	R/W	6	Retain	0 = 2 samples 1 = 4 samples 2 = 8 samples 3 = 16 samples 4 = 32 samples 5 = 64 samples 6 = 128 samples 7 = 256 samples
7:6	Mode	R/W	0x0	Retain	00 = Maximum peak above threshold 01 = First peak above threshold 10 = Offset 11 = Sample point at distance set by 24_5.7:0
5:0	Peak Detection Hysteresis	R/W	0x03	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x3F = ± 492 mv

Table 41: Advanced VCT Sample Point Distance
Offset: Page 5, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	RO	0x00	0x00	0
8:0	Distance to measure/ Distance to start	R/W	0x000	Retain	When 23_5.7:6 = 11 the measurement is taken at this distance. (00 to 1FF) When 23_5.7:6 = 0x any distance below this distance is not considered (00 to FF). Bit 8 is ignored.

Table 42: Advanced VCT™ Cross Pair Threshold
Offset: Page 5, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14:8	Cross Pair Threshold > 30m	R/W	0x01	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 9.92 mv
7	Reserved	RO	0x0	0x0	0
6:0	Cross Pair Threshold < 30m	R/W	0x04	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 992 mv

Table 43: Advanced VCT Same Pair Impedance Threshold 0 and 1
Offset: Page 5, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14:8	Same-Pair Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 9.92 mv
7	Reserved	RO	0x0	0x0	0
6:0	Same-Pair Threshold < 10m	R/W	0x12	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 9.92 mv

Table 44: Advanced VCT Same Pair Impedance Threshold 2 and 3
Offset: Page 5, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14:8	Same-Pair Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 9.92 mv
7	Reserved	RO	0x0	0x0	0
6:0	Same-Pair Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 9.92 mv

Table 45: Advanced VCT Same Pair Impedance Threshold 4 and Transmit Pulse Control
Offset: Page 5, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0
12	Break Link Prior to Measurement	R/W	0x0	Retain	1 = Do not wait 1.5s to break link before starting VCT 0 = Wait 1.5s to break link before starting VCT
11:10	Transmit Pulse Width	R/W	0x0	Retain	00 = Full pulse (128 ns) 01 = 3/4 pulse 10 = 1/2 pulse 11 = 1/4 pulse
9:8	Transmit Amplitude	R/W	0x0	Retain	00 = Full amplitude 01 = 3/4 amplitude 10 = 1/2 amplitude 11 = 1/4 amplitude

7	Distance Measurement Point	R/W	0x0	Retain	If 23_5.7:6 = 00 then
					0 = Measure distance when amplitude drops to 50% of peak amplitude
					1 = Measure distance at actual maximum amplitude
					
					If 23_5.7:6 = 01 then
					0 = Measure distance when amplitude drops below hysteresis
					1 = Measure distance at actual maximum amplitude
					
					If 23_5.7:6 = 1X then this bit is ignored.

6:0	Same-Pair Threshold > 140m	R/W	0x06	Retain	0x00 = ± 0 mV, 0x01 = ± 7.81 mV, ..., 0x7F = ± 992 mv

Table 46: Packet Generation
Offset: Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7:6	Reserved	R/W	0x0	Retain	Set to 00
5	Enable Stub Test	R/W	0x0	Retain	1 = Enable stub test 0 = Normal Operation
4	Enable CRC checker	R/W	0x0	Retain	1 = Enable CRC checker 0 = Disable/reset CRC checker
3	Enable Packet Generator	R/W, SC	0x0	Retain	1 = Enable packet generator 0 = Normal Operation
2	Payload of packet to transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of packet to transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 47: CRC Counters
Offset: Page 6, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	CRC Packet Count	RO	0x00	Retain	0x00 = No packets received 0xFF = 256 packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00 = No CRC errors detected in the packets received. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.

Table 48: Misc Test
Offset: Page 6, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TX_TCLK Enable	R/W	0x0	0x0	The highest numbered enabled port will drive the transmit clock to the HSDACP/N pin. 1 = Enable 0 = Disable
14:6	Reserved	R/W	0x000	Retain	Set to 0
5	Temperature Sensor Enable	R/W	0x0	Retain	1 = Enable 0 = Disable. When the temperature sensor is not needed, it should be disabled to save power.
4:0	Temperature Sensor	RO	xxxxx	xxxxx	Refer to Section 1.19.

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