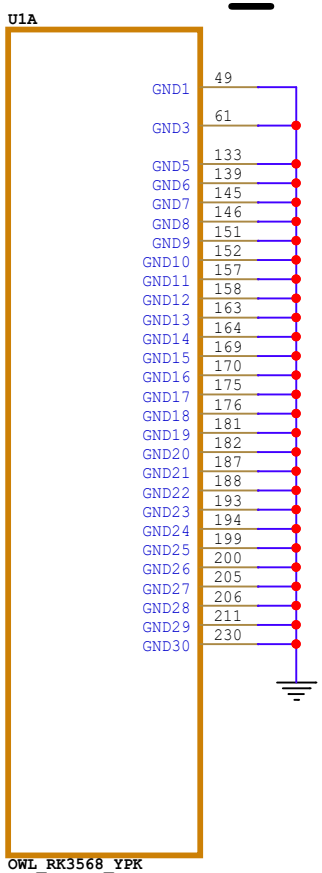
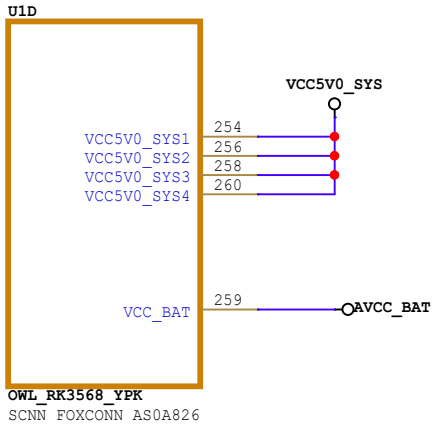
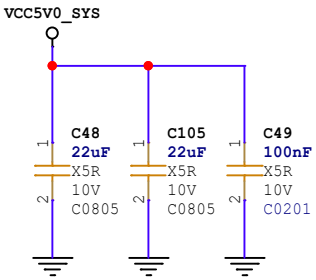
# Hinlink-RK3568

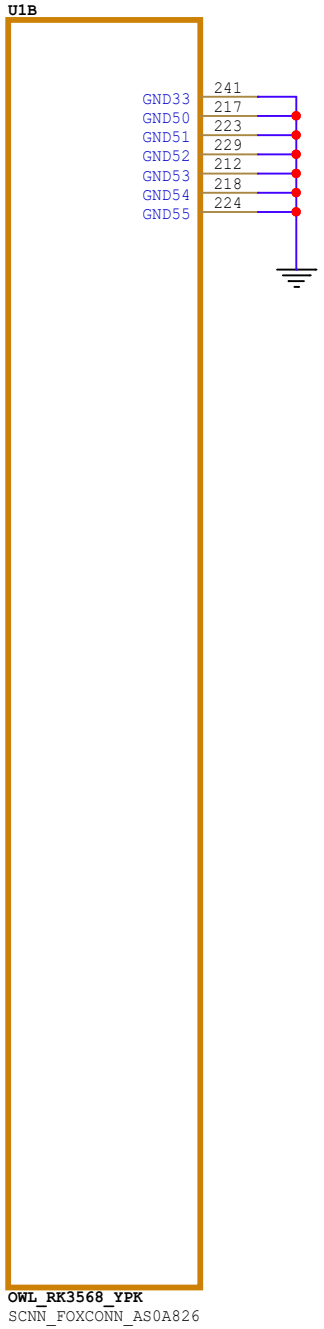
| | | | |
|---|---|---|---|
| OWLVisionTech | | | |
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 00.Cover Page | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | OWLVisionTech | Sheet: | 1 of 20 |

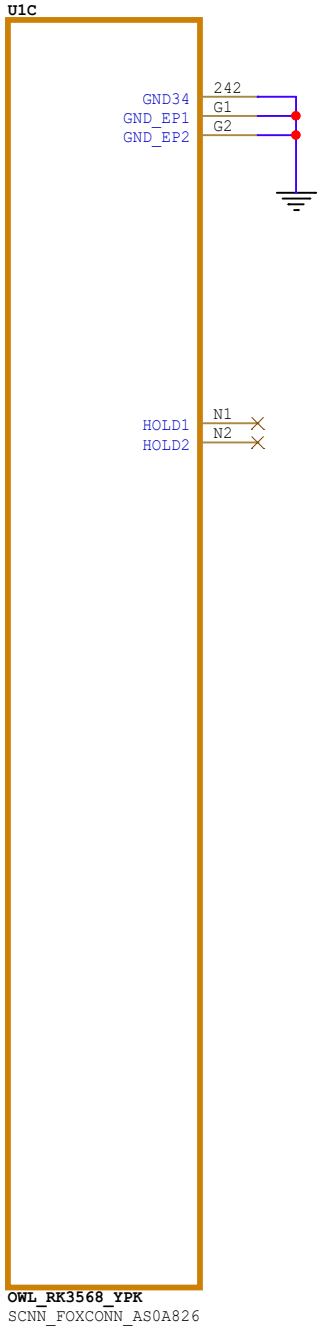
# RK3568_ABCDE (Power&Gnd)

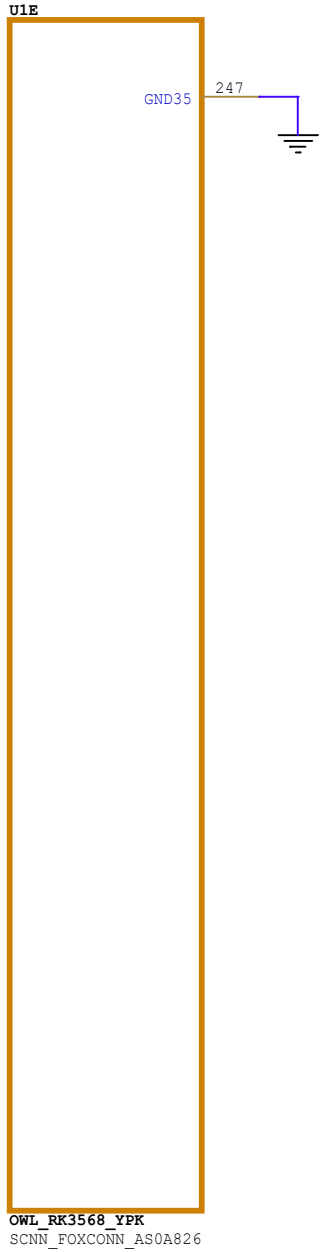
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| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 02.RK3568_Power/GND | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | OWLVisionTech | Sheet: | 2 of 20 |

# RK3568_F (DDR PHY)

U1F

| DDR4 | LPDDR4 | DDR3 | LPDDR3 |
|---|---|---|---|
| DDR4_DQL0_A | LPDDR4_DQ0_A | DDR3_DQ0 | LPDDR3_DQ15 |
| DDR4_DQL2_A | LPDDR4_DQ1_A | DDR3_DQ1 | LPDDR3_DQ14 |
| DDR4_DQL4_A | LPDDR4_DQ2_A | DDR3_DQ2 | LPDDR3_DQ10 |
| DDR4_DQL6_A | LPDDR4_DQ3_A | DDR3_DQ3 | LPDDR3_DQ9 |
| DDR4_DQL7_A | LPDDR4_DQ4_A | DDR3_DQ4 | LPDDR3_DQ13 |
| DDR4_DQL5_A | LPDDR4_DQ5_A | DDR3_DQ5 | LPDDR3_DQ12 |
| DDR4_DQL3_A | LPDDR4_DQ6_A | DDR3_DQ6 | LPDDR3_DQ8 |
| DDR4_DQL1_A | LPDDR4_DQ7_A | DDR3_DQ7 | LPDDR3_DQ11 |
| DDR4_DML_A | LPDDR4_DM0_A | DDR3_DM0 | LPDDR3_DM1 |
| DDR4_DQSL_P_A | LPDDR4_DQS0P_A | DDR3_DQS0P | LPDDR3_DQS1P |
| DDR4_DQSL_N_A | LPDDR4_DQS0N_A | DDR3_DQS0N | LPDDR3_DQS1N |
| DDR4_DQU3_A | LPDDR4_DQ8_A | DDR3_DQ8 | LPDDR3_DQ25 |
| DDR4_DQU1_A | LPDDR4_DQ9_A | DDR3_DQ9 | LPDDR3_DQ24 |
| DDR4_DQU7_A | LPDDR4_DQ10_A | DDR3_DQ10 | LPDDR3_DQ28 |
| DDR4_DQU5_A | LPDDR4_DQ11_A | DDR3_DQ11 | LPDDR3_DQ29 |
| DDR4_DQU2_A | LPDDR4_DQ12_A | DDR3_DQ12 | LPDDR3_DQ26 |
| DDR4_DQU4_A | LPDDR4_DQ13_A | DDR3_DQ13 | LPDDR3_DQ31 |
| DDR4_DQU6_A | LPDDR4_DQ14_A | DDR3_DQ14 | LPDDR3_DQ30 |
| DDR4_DQU0_A | LPDDR4_DQ15_A | DDR3_DQ15 | LPDDR3_DQ27 |
| DDR4_DMU_A | LPDDR4_DM1_A | DDR3_DM1 | LPDDR3_DM3 |
| DDR4_DQSU_P_A | LPDDR4_DQS1P_A | DDR3_DQS1P | LPDDR3_DQS3P |
| DDR4_DQSU_N_A | LPDDR4_DQS1N_A | DDR3_DQS1N | LPDDR3_DQS3N |
| DDR4_DQU7_B | LPDDR4_DQ0_B | DDR3_DQ16 | LPDDR3_DQ1 |
| DDR4_DQU5_B | LPDDR4_DQ1_B | DDR3_DQ17 | LPDDR3_DQ5 |
| DDR4_DQU3_B | LPDDR4_DQ2_B | DDR3_DQ18 | LPDDR3_DQ6 |
| DDR4_DQU1_B | LPDDR4_DQ3_B | DDR3_DQ19 | LPDDR3_DQ4 |
| DDR4_DQU0_B | LPDDR4_DQ4_B | DDR3_DQ20 | LPDDR3_DQ2 |
| DDR4_DQU6_B | LPDDR4_DQ5_B | DDR3_DQ21 | LPDDR3_DQ3 |
| DDR4_DQU4_B | LPDDR4_DQ6_B | DDR3_DQ22 | LPDDR3_DQ7 |
| DDR4_DQU2_B | LPDDR4_DQ7_B | DDR3_DQ23 | LPDDR3_DQ0 |
| DDR4_DMU_B | LPDDR4_DM0_B | DDR3_DM2 | LPDDR3_DM0 |
| DDR4_DQSU_P_B | LPDDR4_DQS0P_B | DDR3_DQS2P | LPDDR3_DQS0P |
| DDR4_DQSU_N_B | LPDDR4_DQS0N_B | DDR3_DQS2N | LPDDR3_DQS0N |
| DDR4_DQL0_B | LPDDR4_DQ8_B | DDR3_DQ24 | LPDDR3_DQ18 |
| DDR4_DQL2_B | LPDDR4_DQ9_B | DDR3_DQ25 | LPDDR3_DQ19 |
| DDR4_DQL4_B | LPDDR4_DQ10_B | DDR3_DQ26 | LPDDR3_DQ22 |
| DDR4_DQL6_B | LPDDR4_DQ11_B | DDR3_DQ27 | LPDDR3_DQ23 |
| DDR4_DQL7_B | LPDDR4_DQ12_B | DDR3_DQ28 | LPDDR3_DQ16 |
| DDR4_DQL5_B | LPDDR4_DQ13_B | DDR3_DQ29 | LPDDR3_DQ17 |
| DDR4_DQL1_B | LPDDR4_DQ14_B | DDR3_DQ30 | LPDDR3_DQ20 |
| DDR4_DQL3_B | LPDDR4_DQ15_B | DDR3_DQ31 | LPDDR3_DQ21 |
| DDR4_DML_B | LPDDR4_DM1_B | DDR3_DM3 | LPDDR3_DM2 |
| DDR4_DQSL_P_B | LPDDR4_DQS1P_B | DDR3_DQS3P | LPDDR3_DQS2P |
| DDR4_DQSL_N_B | LPDDR4_DQS1N_B | DDR3_DQS3N | LPDDR3_DQS2N |
| DDR4_ECC_DQ7 | -- | DDR3_ECC_DQ0 | |
| DDR4_ECC_DQ0 | -- | DDR3_ECC_DQ1 | |
| DDR4_ECC_DQ2 | -- | DDR3_ECC_DQ2 | |
| DDR4_ECC_DQ1 | -- | DDR3_ECC_DQ3 | |
| DDR4_ECC_DQ6 | -- | DDR3_ECC_DQ4 | |
| DDR4_ECC_DQ4 | -- | DDR3_ECC_DQ5 | |
| DDR4_ECC_DQ3 | -- | DDR3_ECC_DQ6 | |
| DDR4_ECC_DQ5 | -- | DDR3_ECC_DQ7 | |
| DDR4_ECC_DM | -- | DDR3_ECC_DM | |
| DDR4_ECC_DQS_P | -- | DDR3_ECC_DQS_P | |
| DDR4_ECC_DQS_N | -- | DDR3_ECC_DQS_N | |

| DDR4 | LPDDR4 | DDR3 | LPDDR3 |
|---|---|---|---|
| DDR4_A0 | **LPDDR4_CLKP_B** | DDR3_A9 | --- |
| DDR4_A1 | --- | DDR3_A2 | --- |
| DDR4_A2 | LPDDR4_A1_A | DDR3_A4 | LPDDR3_A6 |
| DDR4_A3 | LPDDR4_CKE1_A | DDR3_A3 | --- |
| DDR4_A4 | LPDDR4_A3_B | DDR3_BA1 | LPDDR3_A3 |
| DDR4_A5 | LPDDR4_A5_B | DDR3_A11 | LPDDR3_A2 |
| DDR4_A6 | LPDDR4_A1_B | DDR3_A13 | LPDDR3_A1 |
| DDR4_A7 | LPDDR4_ODT0_CA_B | DDR3_A8 | --- |
| DDR4_A8 | LPDDR4_ODT0_CA_A | DDR3_A6 | LPDDR3_A9 |
| DDR4_A9 | **LPDDR4_CLKN_B** | DDR3_A5 | --- |
| DDR4_A10 | LPDDR4_CKE0_B | DDR3_A10 | --- |
| DDR4_A11 | LPDDR4_A0_A | DDR3_A7 | LPDDR3_A8 |
| DDR4_A12 | LPDDR4_A3_A | DDR3_BA2 | --- |
| DDR4_A13 | LPDDR4_A0_B | DDR3_A14 | LPDDR3_A0 |
| DDR4_A14_WEn | LPDDR4_A4_A | DDR3_A15 | LPDDR3_A5 |
| DDR4_A15_CASn | LPDDR4_A2_A | DDR3_A0 | --- |
| DDR4_A16_RASn | LPDDR4_A5_A | DDR3_RASn | LPDDR3_A7 |
| DDR4_ACTn | LPDDR4_CKE1_B | DDR3_CASn | --- |
| DDR4_BA0 | LPDDR4_A2_B | DDR3_A1 | --- |
| DDR4_BA1 | LPDDR4_A4_B | DDR3_A12 | LPDDR3_A4 |
| DDR4_BG0 | LPDDR4_ODT1_CA_B | DDR3_WEn | --- |
| DDR4_BG1 | LPDDR4_ODT1_CA_A | DDR3_BA0 | --- |
| DDR4_CKE | LPDDR4_CKE0_A | DDR3_CKE | LPDDR3_CKE |
| **DDR4_CLKP** | **LPDDR4_CLKP_A** | **DDR3_CLKP** | **LPDDR3_CLKP** |
| **DDR4_CLKN** | **LPDDR4_CLKN_A** | **DDR3_CLKN** | **LPDDR3_CLKN** |
| DDR4_CS0n | LPDDR4_CS0n_A | DDR3_ODT1 | LPDDR3_ODT0 |
| DDR4_CS1n | LPDDR4_CS1n_A | DDR3_CS1n | LPDDR3_ODT1 |
| DDR4_ODT0 | LPDDR4_CS1n_B | DDR3_ODT0 | LPDDR3_CS1n |
| DDR4_ODT1 | LPDDR4_CS0n_B | DDR3_CS0n | LPDDR3_CS0n |
| DDR4_RESETn | LPDDR4_RESETn | DDR3_RESETn | --- |

Note: Sequences can not be swap

GND31 235

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x =1.1V

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x **=0.6V**

Note:
Except DDR3, other DQ sequences can not be swap

**OWL_RK3568_YPK**
SCNN_FOXCONN_AS0A826

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| | | | |
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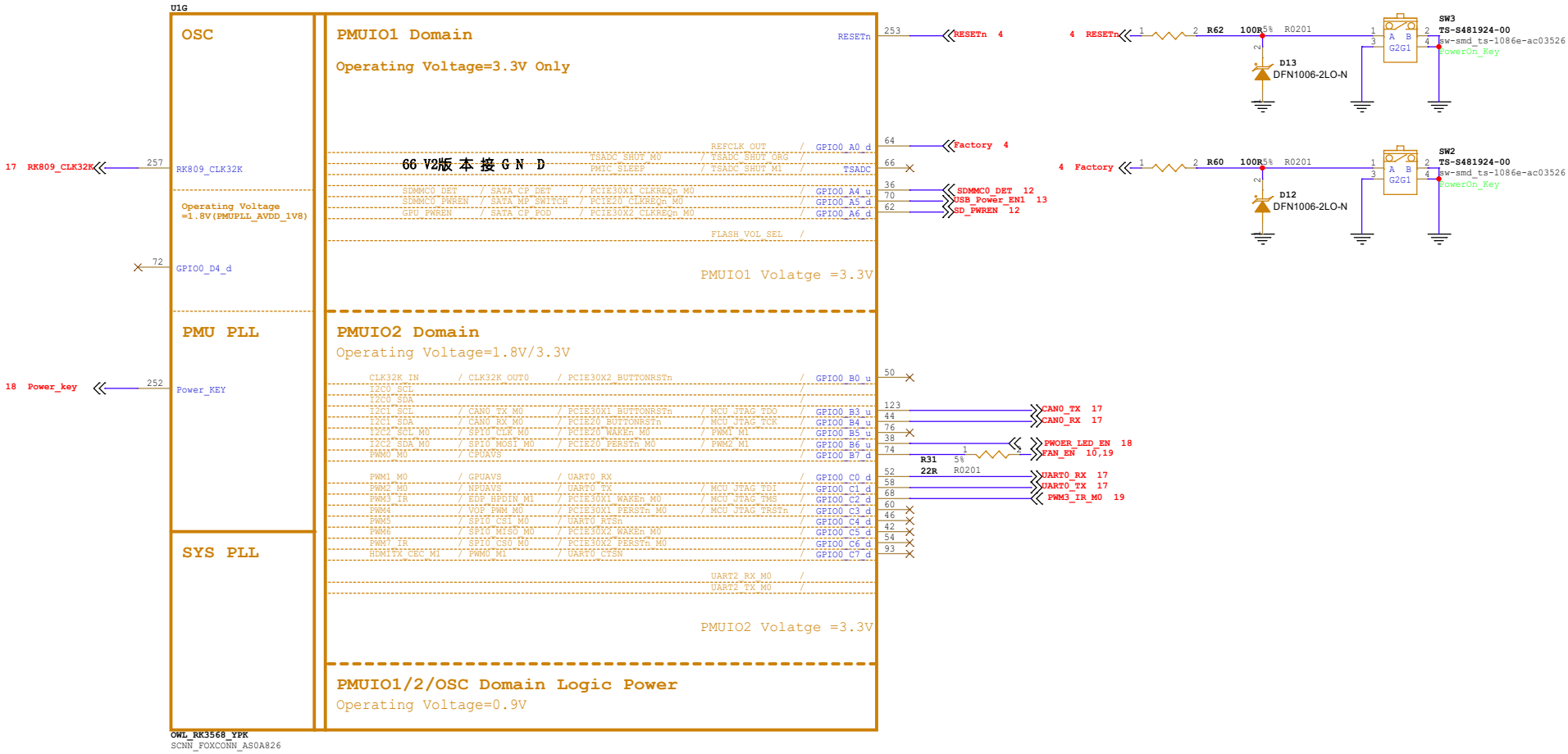
| OWLVisionTech | | | |
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 03.RK3568_DDR PHY | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | OWLVisionTech | Sheet: | 3 of 20 |

# RK3568_G(OSC/PLL/PMUIO1/2)




**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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|---|---|---|---|
| Project: | RK3568_OPC_MINI | | |
| File: | 04.RK3568_OSC/PLL/PMUIO | | OWLVisionTech |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 4 of 20 |

# RK3568_I(VCCIO2 Domain)

U1I

**VCCIO2 Domain**

Operating Voltage=1.8V/3.3V

| | | | |
|---|---|---|---|
| EMMC_D0 | / FLASH_D0 / | Update | 55 |
| EMMC_D1 | / FLASH_D1 / | | |
| EMMC_D2 | / FLASH_D2 / | | |
| EMMC_D3 | / FLASH_D3 / | | |
| EMMC_D4 | / FLASH_D4 / | | |
| EMMC_D5 | / FLASH_D5 / | | |
| EMMC_D6 | / FLASH_D6 / | | |
| EMMC_D7 | / FLASH_D7 / | | |
| EMMC_CMD | / FLASH_WRn / | | |
| EMMC_CLKOUT | / FLASH_DQS / | | |
| EMMC_DATA_STROBE | / FSPI_CS1n / FLASH_CLE / | | |
| EMMC_RSTn | / FSPI_D2 / FLASH_WPn / | | |
| | FSPI_CLK / FLASH_ALE / | | |
| | FSPI_D0 / FLASH_RDY / | | |
| | FSPI_D1 / FLASH_RDn / | | |
| | FSPI_CS0n / FLASH_CS0n / | | |
| | FSPI_D3 / FLASH_CS1n / | | |

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

GND32 236

VCCIO2 Volatge =1.8V

OWL_RK3568_YPK
SCNN_FOXCONN_AS0A826

Update 55 → Update 5

5 Update ← 1 R58 20K 5% R0201 2 → SW1 TS-S481924-00 (A B / G2G1) 3 4 sw-smd_ts-1086e-ac03526 PowerOn_Key

# RK3568_J(VCCIO3 Domain)

U1J

**VCCIO3 Domain**

Operating Voltage=1.8V/3.3V

| | | | |
|---|---|---|---|
| SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1 / PWM8_M1 / | GPIO1_D5_u | 6 | SDMMC0_D0 12 |
| SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1 / PWM9_M1 / | GPIO1_D6_u | 4 | SDMMC0_D1 12 |
| SDMMC0_D2 / ARMJTAG_TCK / UART5_CTSn_M0 / | GPIO1_D7_u | 8 | SDMMC0_D2 12 |
| SDMMC0_D3 / ARMJTAG_TMS / UART5_RTSn_M0 / | GPIO2_A0_u | 2 | SDMMC0_D3 12 |
| SDMMC0_CMD / PWM10_M1 / UART5_RX_M0 / CAN0_TX_M1 / | GPIO2_A1_u | 25 | SDMMC0_CMD 12 |
| SDMMC0_CLK / TEST_CLKOUT / UART5_TX_M0 / CAN0_RX_M1 / | GPIO2_A2_d | 27 | SDMMC0_CLK 12 |

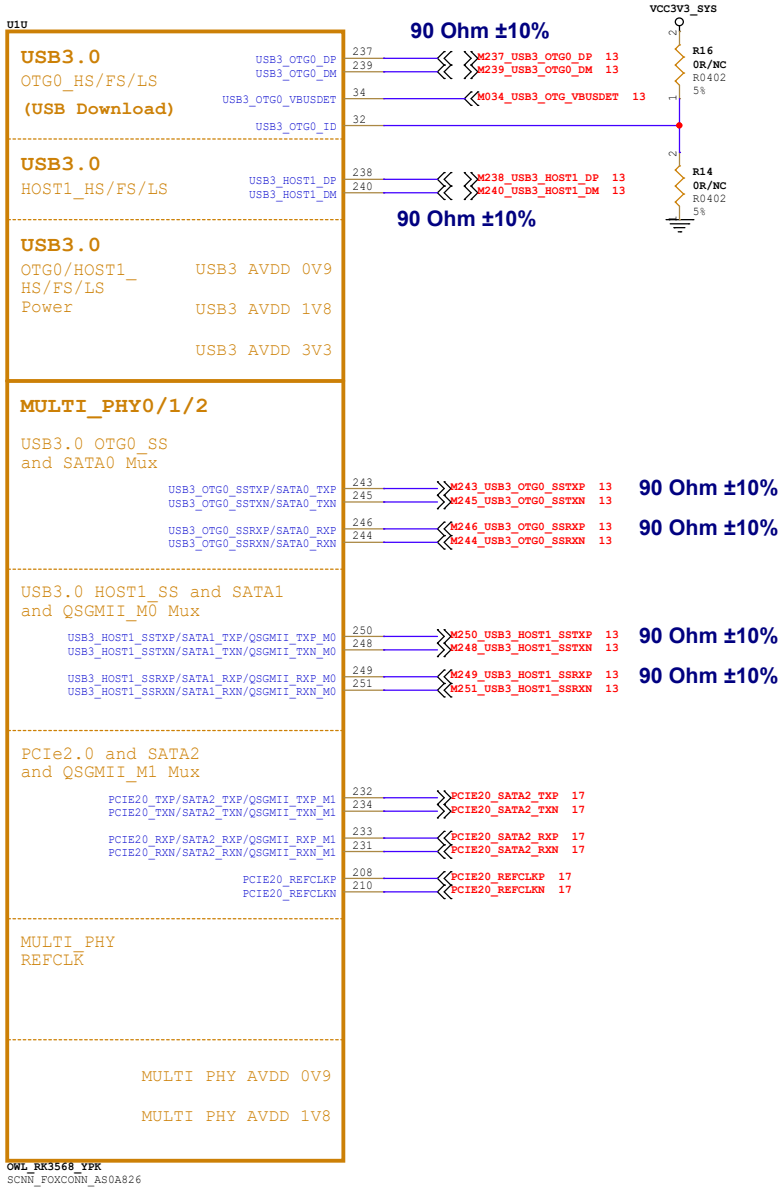
VCCIO3 Volatge =3.3V

OWL_RK3568_YPK
SCNN_FOXCONN_AS0A826

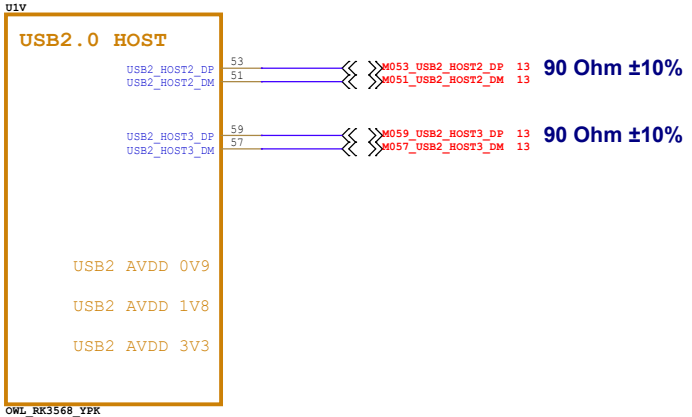
**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package

| | | | |
|---|---|---|---|
| OWLVisionTech | | | |
| Project: | RK3568_OPC_MINI | | |
| File: | 05.RK3568_Flash/SD Controller | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 5 of 20 |

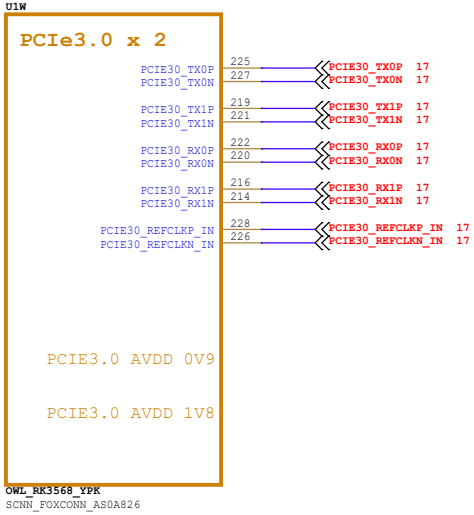
# RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)




# RK3568_V(USB2.0 HOST)




# RK3568_W(PCIe3.0 x2)

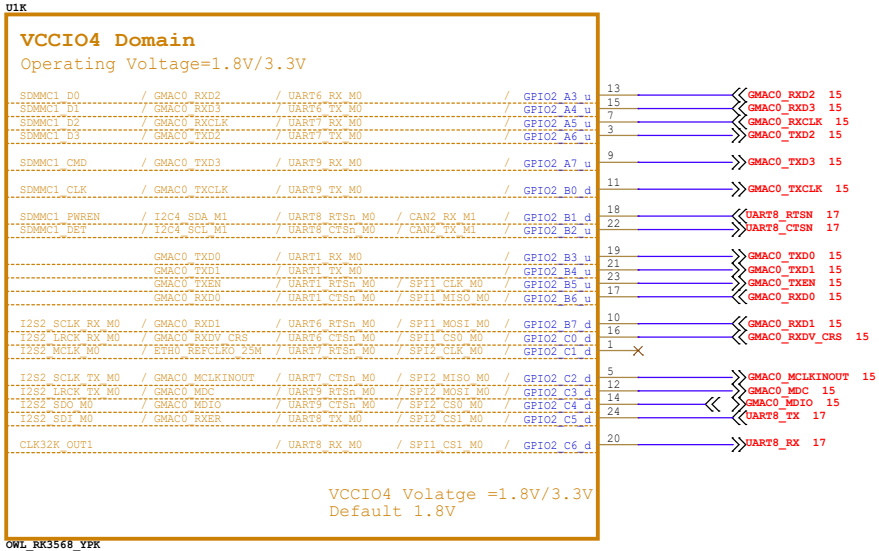



**Note:**
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

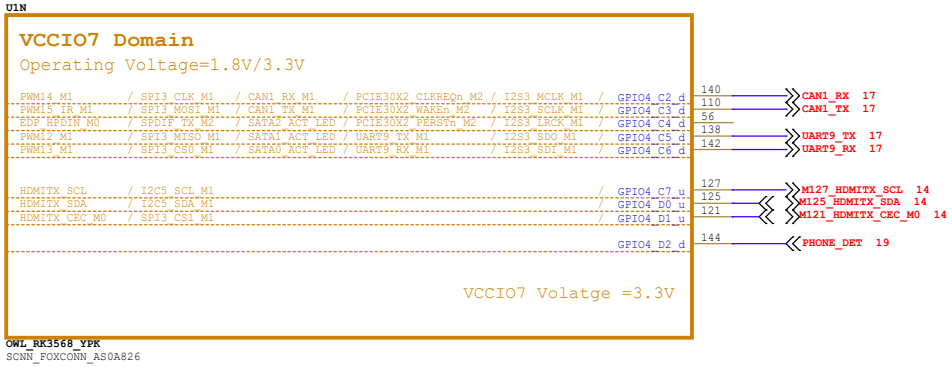


| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | | |
| File: | 06.RK3568_USB/PCIe/SATA PHY | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 6 of 20 |

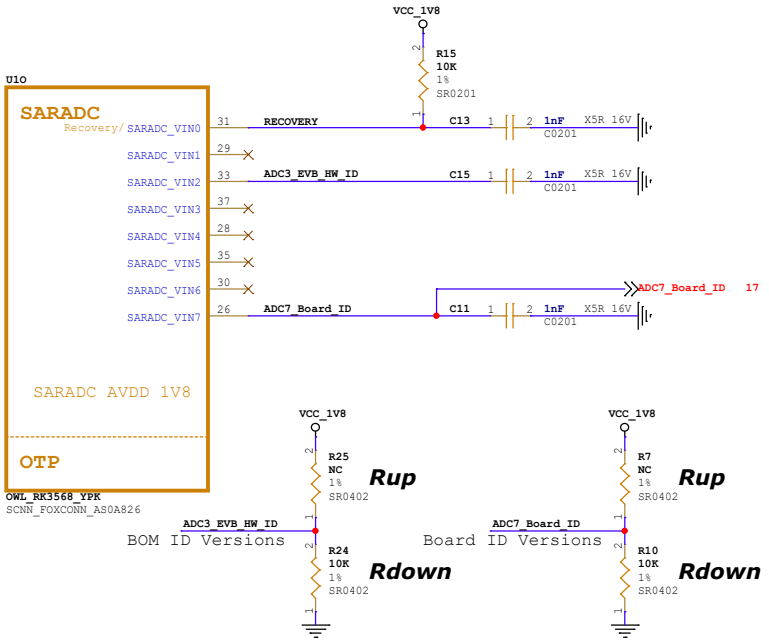
# RK3568_K(VCCIO4 Domain)




# RK3568_N(VCCIO7 Domain)




# RK3568_O(SARADC/OTP)




### BOM ID Versions TABLE 1

| Item | Rup | Rdown | ADC | VOL | VERSION |
|---|---|---|---|---|---|
| LEVEL1 | DNP | 100K | 0 | 0V | V1.0 |
| LEVEL2 | 100K | 20K | 682 | 0.3V | V2.0 |
| LEVEL3 | 100K | 100K | 2047 | 0.9V | V3.0 |
| LEVEL4 | 100K | DNP | 4096 | 1.8V | V4.0 |

### Board ID Versions TABLE 2

| Item | Rup | Rdown | ADC | VOL | VERSION |
|---|---|---|---|---|---|
| LEVEL1 | DNP | 100K | 0 | 0V | WIFI AP6212+SATA |
| LEVEL2 | 100K | 20K | 682 | 0.3V | WIFI AP6256+SATA |
| LEVEL3 | 100K | 100K | 2047 | 0.9V | WIFI WIFI6 |
| LEVEL4 | 100K | 200K | 4096 | 1.2V | WIFI NC+SATA |

**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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| Project: | RK3568_OPC_MINI | | OWLVisionTech |
| File: | 07.RK3568_SARADC/GPIO | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
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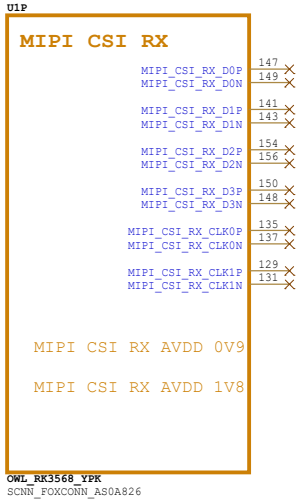
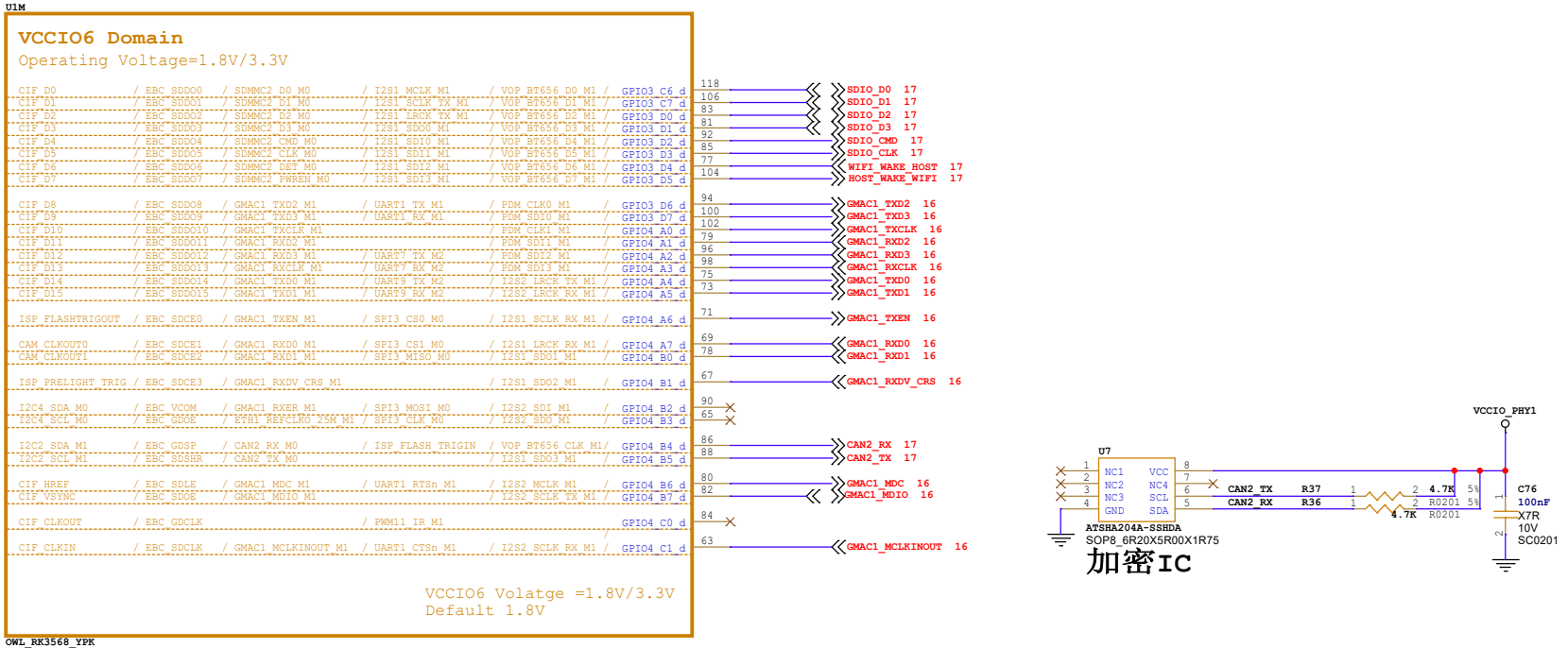
# RK3568_P(MIPI_CSI_RX)




# RK3568_M(VCCIO6 Domain)

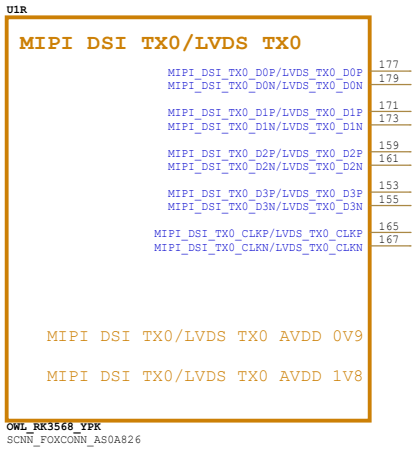




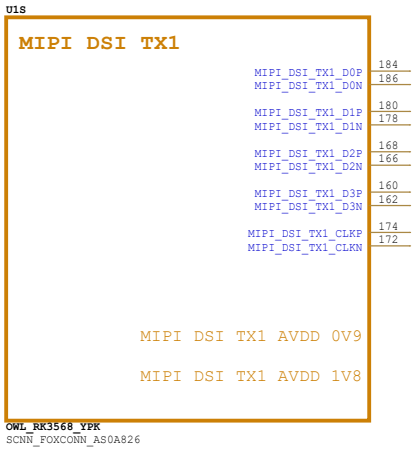


| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | | |
| File: | 08.RK3568_VI Interface | | OWLVisionTech |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 8 of 20 |

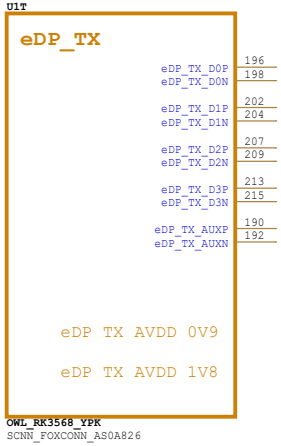
# RK3568_R(MIPI_DSI_TX0/LVDS_TX0)




# RK3568_S(MIPI_DSI_TX1)




# RK3568_T(eDP TX)




**Note:**
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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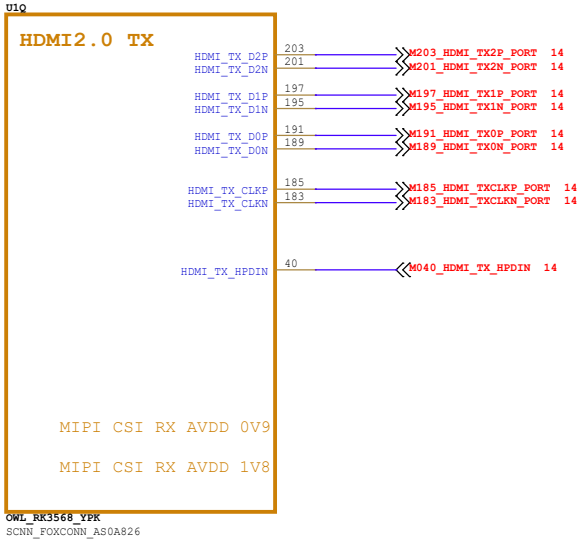
# RK3568_Q(HDMI2.0 TX)

**HDMI TMDS trace**
**100 Ohm ±10%**




| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 09.RK3568_VO Interface_1 | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 9 of 20 |

# RK3568_H(VCCIO1 Domain)

U1H

## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

| | | | | | |
|---|---|---|---|---|---|
| I2C3_SDA_M0 | UART3_RX_M0 | CAN1_RX_M0 | AUDIOPWM_LOUT_P | ACODEC_ADC_DATA | GPIO1_A0_u |
| I2C3_SCL_M0 | UART3_TX_M0 | CAN1_TX_M0 | AUDIOPWM_LOUT_N | ACODEC_ADC_CLK | GPIO1_A1_u |
| I2S1_MCLK_M0 | UART3_RTSn_M0 | SCR_CLK | PCIE30X1_PERSTn_M2 | | |
| I2S1_SCLK_TX_M0 | UART3_CTSn_M0 | SCR_IO | PCIE30X1_WAKEn_M2 | ACODEC_DAC_CLK | |
| I2S1_SCLK_RX_M0 | UART4_RX_M0 | PDM_CLK1_M0 | SPDIF_TX_M0 | | GPIO1_A4_d |
| I2S1_LRCK_TX_M0 | UART4_RTSn_M0 | SCR_RST | PCIE30X1_CLKREQn_M2 | ACODEC_DAC_SYNC | |
| I2S1_LRCK_RX_M0 | UART4_TX_M0 | PDM_CLK0_M0 | AUDIOPWM_ROUT_P | | |
| I2S1_SDO0_M0 | UART4_CTSn_M0 | SCR_DET | AUDIOPWM_ROUT_N | ACODEC_DAC_DATAL | |
| I2S1_SDO1_M0 | I2S1_SDI3_M0 | PDM_SDI3_M0 | PCIE20_CLKREQn_M2 | ACODEC_DAC_DATAR | GPIO1_B0_d |
| I2S1_SDO2_M0 | I2S1_SDI2_M0 | PDM_SDI2_M0 | PCIE20_WAKEn_M2 | ACODEC_ADC_SYNC | GPIO1_B1_d |
| I2S1_SDO3_M0 | I2S1_SDI1_M0 | PDM_SDI1_M0 | PCIE20_PERSTn_M2 | | GPIO1_B2_d |
| | I2S1_SDI0_M0 | PDM_SDI0_M0 | | | |

VCCIO1 Volatge =1.8V/3.3V
Default 3.3V

43
47
39
41
45
255

GMAC1_RSTn 16

FAN_EN 4,19

R72
0R/NC
R0402

OWL_RK3568_YPK
SCNN_FOXCONN_AS0A826

**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 19.RK3568_Audio Interface | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 10 of 20 |

# RK3568_L(VCCIO5 Domain)

U1L

## VCCIO5 Domain

Operating Voltage=1.8V/3.3V

| | | | | | |
|---|---|---|---|---|---|
| LCDC_D0 | VOP_BT656_D0_M0 | SPI0_MISO_M1 | PCIE20_CLKREQn_M1 | I2S1_MCLK_M2 | GPIO2_D0_d |
| LCDC_D1 | VOP_BT656_D1_M0 | SPI0_MOSI_M1 | PCIE20_WAKEn_M1 | I2S1_SCLK_TX_M2 | GPIO2_D1_d |
| LCDC_D2 | VOP_BT656_D2_M0 | SPI0_CS0_M1 | PCIE30X1_CLKREQn_M1 | I2S1_LRCK_TX_M2 | GPIO2_D2_d |
| LCDC_D3 | VOP_BT656_D3_M0 | SPI0_CLK_M1 | PCIE30X1_WAKEn_M1 | I2S1_SDI0_M2 | GPIO2_D3_d |
| LCDC_D4 | VOP_BT656_D4_M0 | SPI2_CS1_M1 | PCIE30X2_CLKREQn_M1 | I2S1_SDI1_M2 | GPIO2_D4_d |
| LCDC_D5 | VOP_BT656_D5_M0 | SPI2_CS0_M1 | PCIE30X2_WAKEn_M1 | I2S1_SDI2_M2 | GPIO2_D5_d |
| LCDC_D6 | VOP_BT656_D6_M0 | SPI2_MOSI_M1 | PCIE30X2_PERSTn_M1 | I2S1_SDI3_M2 | GPIO2_D6_d |
| LCDC_D7 | VOP_BT656_D7_M0 | SPI2_MISO_M1 | UART8_TX_M1 | I2S1_SDO0_M2 | GPIO2_D7_d |
| LCDC_CLK | VOP_BT656_CLK_M0 | SPI2_CLK_M1 | UART8_RX_M1 | I2S1_SDO1_M2 | GPIO3_A0_d |
| LCDC_D8 | VOP_BT1120_D0 | SPI1_CS0_M1 | PCIE30X1_PERSTn_M1 | SDMMC2_D0_M1 | GPIO3_A1_d |
| LCDC_D9 | VOP_BT1120_D1 | GMAC1_TXD2_M0 | I2S3_MCLK_M0 | SDMMC2_D1_M1 | GPIO3_A2_d |
| LCDC_D10 | VOP_BT1120_D2 | GMAC1_TXD3_M0 | I2S3_SCLK_M0 | SDMMC2_D2_M1 | GPIO3_A3_d |
| LCDC_D11 | VOP_BT1120_D3 | GMAC1_RXD2_M0 | I2S3_LRCK_M0 | SDMMC2_D3_M1 | GPIO3_A4_d |
| LCDC_D12 | VOP_BT1120_D4 | GMAC1_RXD3_M0 | I2S3_SDO_M0 | SDMMC2_CMD_M1 | GPIO3_A5_d |
| LCDC_D13 | VOP_BT1120_CLK | GMAC1_TXCLK_M0 | I2S3_SDI_M0 | SDMMC2_CLK_M1 | GPIO3_A6_d |
| LCDC_D14 | VOP_BT1120_D5 | GMAC1_RXCLK_M0 | | SDMMC2_DET_M1 | GPIO3_A7_d |
| LCDC_D15 | VOP_BT1120_D6 | ETH1_REFCLKO_25M_M0 | | SDMMC2_PWREN_M1 | GPIO3_B0_d |
| LCDC_D16 | VOP_BT1120_D7 | GMAC1_RXD0_M0 | UART4_RX_M1 | PWM8_M0 | GPIO3_B1_d |
| LCDC_D17 | VOP_BT1120_D8 | GMAC1_RXD1_M0 | UART4_TX_M1 | PWM9_M0 | GPIO3_B2_d |
| LCDC_D18 | VOP_BT1120_D9 | GMAC1_RXDV_CRS_M0 | I2C5_SCL_M0 | PDM_SDI0_M2 | GPIO3_B3_d |
| LCDC_D19 | VOP_BT1120_D10 | GMAC1_RXER_M0 | I2C5_SDA_M0 | PDM_SDI1_M2 | GPIO3_B4_d |
| LCDC_D20 | VOP_BT1120_D11 | GMAC1_TXD0_M0 | I2C3_SCL_M1 | PWM10_M0 | GPIO3_B5_d |
| LCDC_D21 | VOP_BT1120_D12 | GMAC1_TXD1_M0 | I2C3_SDA_M1 | PWM11_IR_M0 | GPIO3_B6_d |
| LCDC_D22 | PWM12_M0 | GMAC1_TXEN_M0 | UART3_TX_M1 | PDM_SDI2_M2 | GPIO3_B7_d |
| LCDC_D23 | PWM13_M0 | GMAC1_MCLKINOUT_M0 | UART3_RX_M1 | PDM_SDI3_M2 | GPIO3_C0_d |
| LCDC_HSYNC | VOP_BT1120_D13 | SPI1_MOSI_M1 | PCIE20_PERSTn_M1 | I2S1_SDO2_M2 | GPIO3_C1_d |
| LCDC_VSYNC | VOP_BT1120_D14 | SPI1_MISO_M1 | UART5_TX_M1 | I2S1_SDO3_M2 | GPIO3_C2_d |
| LCDC_DEN | VOP_BT1120_D15 | SPI1_CLK_M1 | UART5_RX_M1 | I2S1_SCLK_RX_M2 | GPIO3_C3_d |
| PWM14_M0 | VOP_PWM_M1 | GMAC1_MDC_M0 | UART7_TX_M1 | PDM_CLK1_M2 | GPIO3_C4_d |
| PWM15_IR_M0 | SPDIF_TX_M1 | GMAC1_MDIO_M0 | UART7_RX_M1 | I2S1_LRCK_RX_M2 | GPIO3_C5_d |

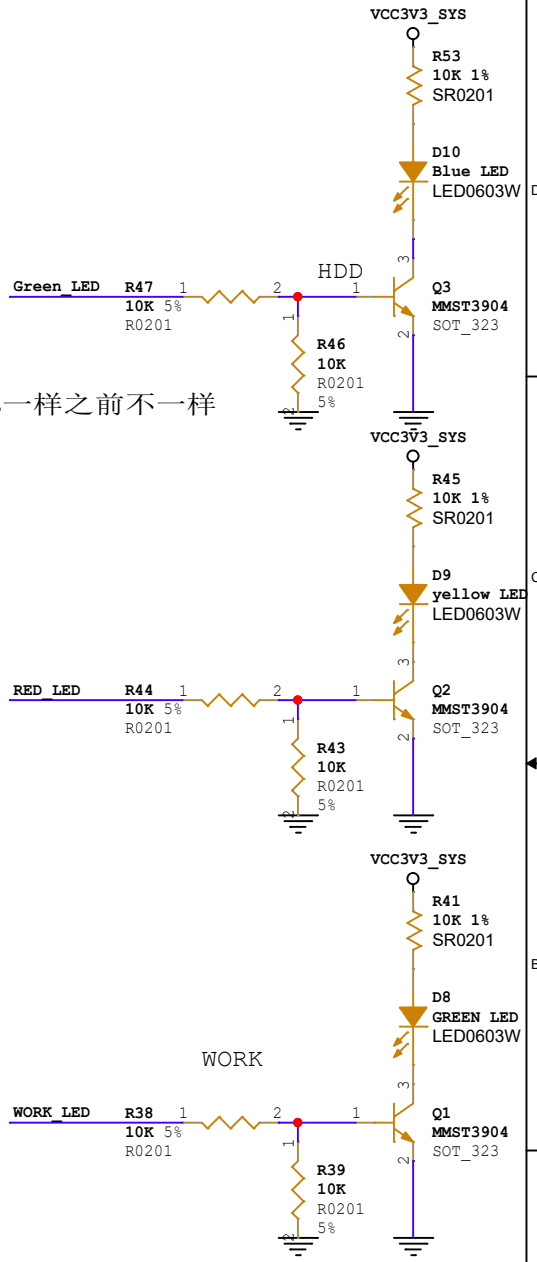
VCCIO5 Volatge =1.8V/3.3V
Default 1.8V

金手指要改为3V3

119 25GLAN_ResetA 17
134 WIFI_POWER_EN 17
136 PCIE_POWER_EN 17
120 GMAC0_RSTn 15
126 PCIE30X2_CLKREQn_M1 17
130 PCIE30X2_WAKEn_M1 17
128 PCIE30X2_PERSTn_M1 17
117 X
115 BT_RST 17
132 BT_WAKE_HOST 17
124 HOST_WAKE_BT 17
113 X
122 25GLAN_ResetB 17
111 Green_LED
109 X
107 RED_LED
105 WORK_LED
101 UART4_RX 17
103 UART4_TX 17
97 X
95 X
48 X
99 X
116 UART3_TX 17
91 UART3_RX 17
89 X
108 UART5_TX 17
114 UART5_RX 17
112 UART7_TX 17
87 UART7_RX 17

OWL_RK3568_YPK
SCNN_FOXCONN_AS0A826

BT与EVB一样之前不一样




**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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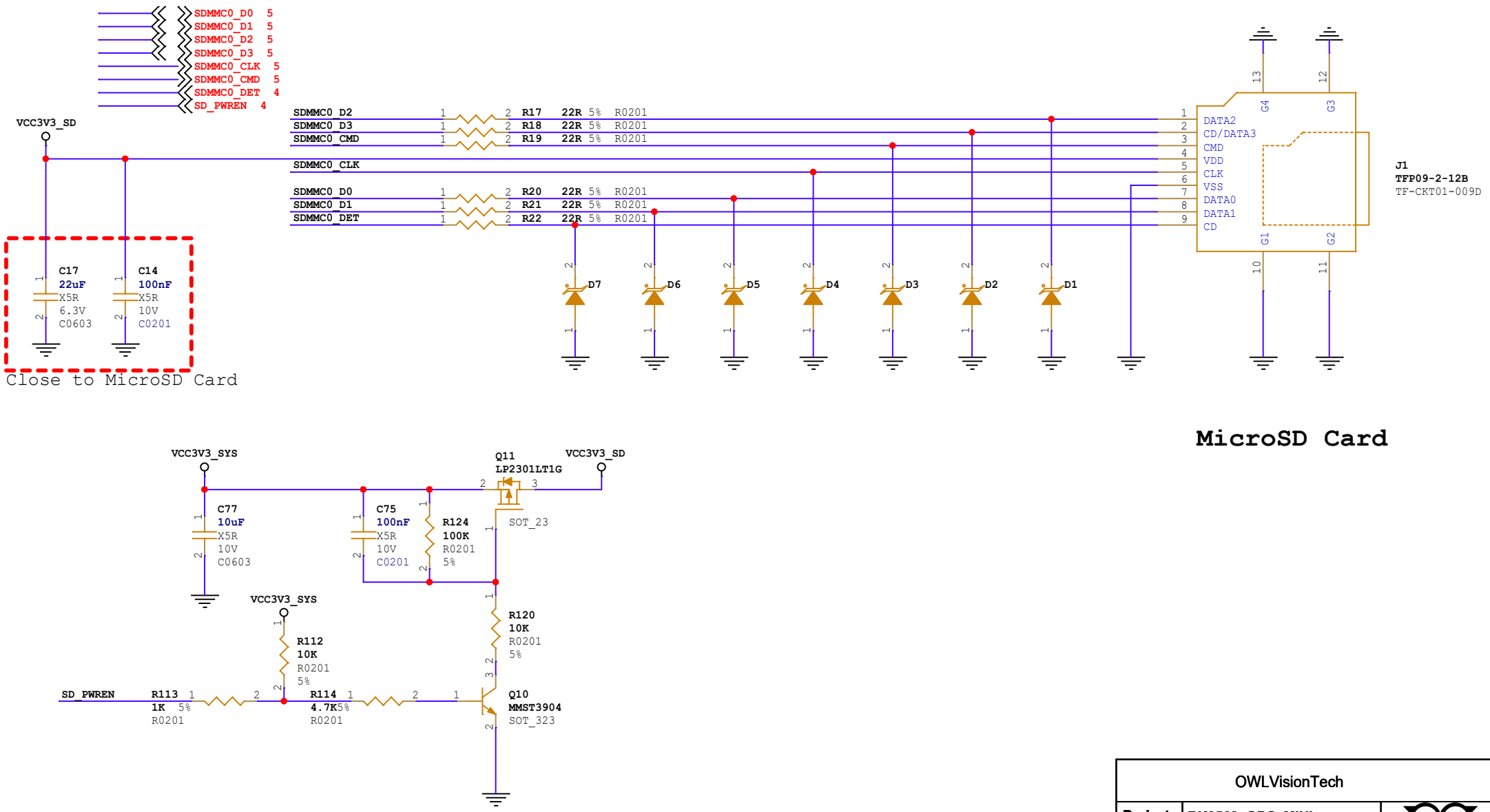
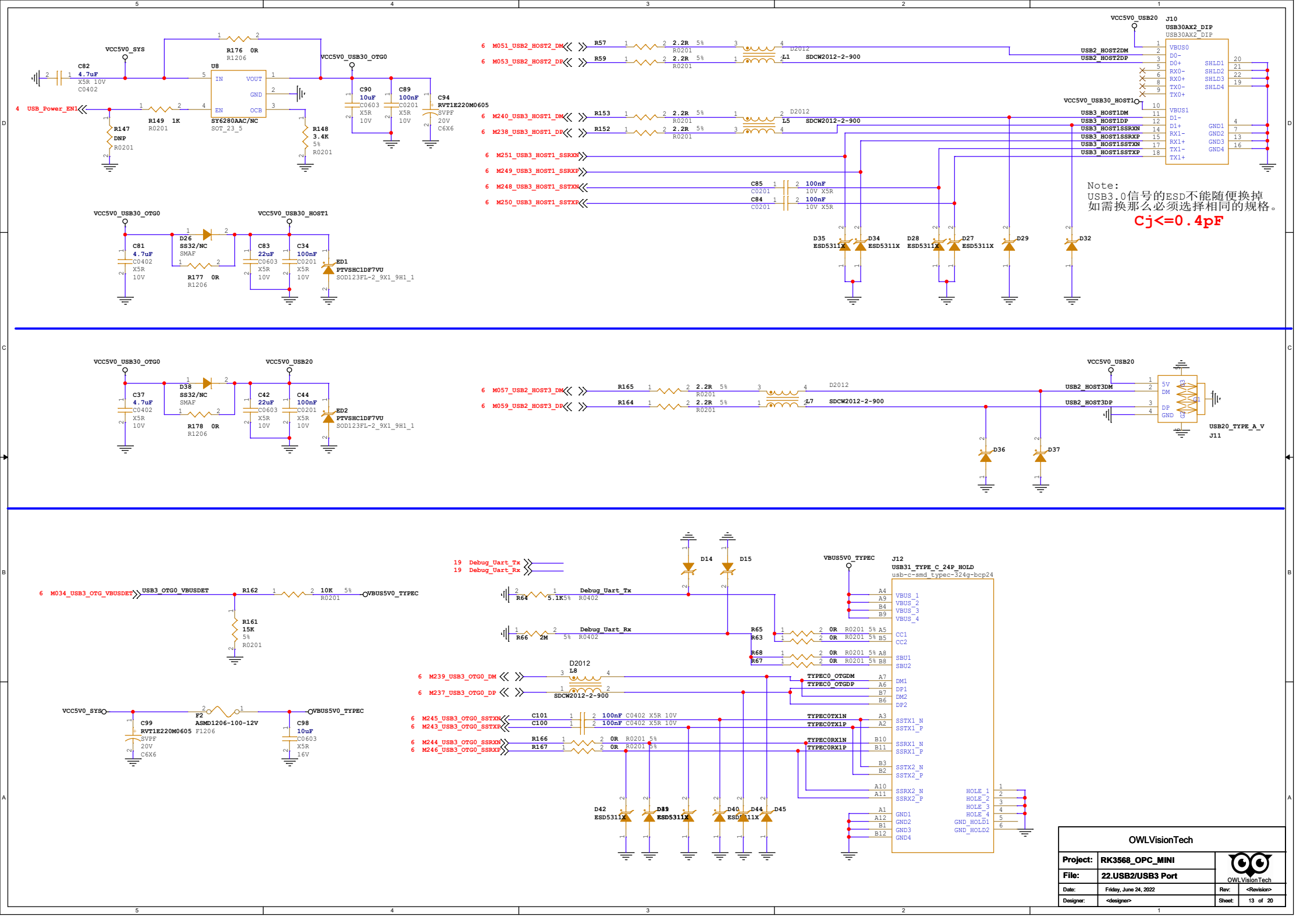
| | | | |
|---|---|---|---|
| OWLVisionTech | | | |
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 20.RK3568_VO Interface_2 | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 11 of 20 |




# MicroSD Card

| | | | |
|---|---|---|---|
| OWLVisionTech | | | |
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 21.Flash-MicroSD Card | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 12 of 20 |


VCC5V0_SYS
R176 0R
R1206
VCC5V0_USB30_OTG0
C82
4.7uF
X5R 10V
C0402
U8
IN
VOUT
GND
EN
OCB
SY6280AAC/NC
SOT_23_5
4 USB_Power_EN1
R147
DNP
R0201
R149 1K
R0201
R148
3.4K
5%
R0201
C90
10uF
C0603
X5R
10V
C89
100nF
C0201
X5R
10V
C94
RVT1E220M0605
SVPF
20V
C6X6
VCC5V0_USB30_OTG0
VCC5V0_USB30_HOST1
C81
4.7uF
C0402
X5R
10V
D26
SS32/NC
SMAF
R177 0R
R1206
C83
22uF
C0603
X5R
10V
C34
100nF
C0201
X5R
10V
ED1
PTVSHC1DF7VU
SOD123FL-2_9X1_9H1_1
6 M051_USB2_HOST2_DM
6 M053_USB2_HOST2_DP
R57
R59
2.2R 5%
R0201
D2012
L1
SDCW2012-2-900
VCC5V0_USB20
J10
USB30AX2_DIP
USB30AX2_DIP
USB2_HOST2DM
USB2_HOST2DP
VCC5V0_USB30_HOST1
6 M240_USB3_HOST1_DM
6 M238_USB3_HOST1_DP
R153
R152
L5
SDCW2012-2-900
USB3_HOST1DM
USB3_HOST1DP
USB3_HOST1SSRXN
USB3_HOST1SSRXP
USB3_HOST1SSTXN
USB3_HOST1SSTXP
6 M251_USB3_HOST1_SSRXN
6 M249_USB3_HOST1_SSRXP
6 M248_USB3_HOST1_SSTXN
6 M250_USB3_HOST1_SSTXP
C85
C84
100nF
10V X5R
C0201
D35
D34
D28
D27
D29
D32
ESD5311X
Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。
Cj<=0.4pF
VCC5V0_USB30_OTG0
VCC5V0_USB20
C37
4.7uF
C0402
X5R
10V
D38
SS32/NC
SMAF
R178 0R
R1206
C42
22uF
C0603
X5R
10V
C44
100nF
C0201
X5R
10V
ED2
PTVSHC1DF7VU
SOD123FL-2_9X1_9H1_1
6 M057_USB2_HOST3_DM
6 M059_USB2_HOST3_DP
R165
R164
L7
SDCW2012-2-900
USB2_HOST3DM
USB2_HOST3DP
USB20_TYPE_A_V
J11
D36
D37
6 M034_USB3_OTG_VBUSDET
USB3_OTG0_VBUSDET
R162 10K 5%
R0201
VBUS5V0_TYPEC
R161
15K
5%
R0201
VCC5V0_SYS
C99
RVT1E220M0605
SVPF
20V
C6X6
F2
ASMD1206-100-12V
F1206
C98
10uF
C0603
X5R
16V
19 Debug_Uart_Tx
19 Debug_Uart_Rx
D14
D15
R64
5.1K
Debug_Uart_Tx
R0402
R66
2M
Debug_Uart_Rx
R0402
R65
R63
R68
R67
0R
R0201 5%
VBUS5V0_TYPEC
J12
USB31_TYPE_C_24P_HOLD
usb-c-smd_typec-324g-bcp24
VBUS_1
VBUS_2
VBUS_3
VBUS_4
CC1
CC2
SBU1
SBU2
DM1
DP1
DM2
DP2
6 M239_USB3_OTG0_DM
6 M237_USB3_OTG0_DP
L8
SDCW2012-2-900
TYPEC0_OTGDM
TYPEC0_OTGDP
6 M245_USB3_OTG0_SSTXN
6 M243_USB3_OTG0_SSTXP
C101
C100
100nF C0402 X5R 10V
TYPEC0TX1N
TYPEC0TX1P
6 M244_USB3_OTG0_SSRXN
6 M246_USB3_OTG0_SSRXP
R166
R167
0R R0201 5%
TYPEC0RX1N
TYPEC0RX1P
SSTX1_N
SSTX1_P
SSRX1_N
SSRX1_P
SSTX2_N
SSTX2_P
SSRX2_N
SSRX2_P
GND1
GND2
GND3
GND4
HOLE_1
HOLE_2
HOLE_3
HOLE_4
GND_HOLD1
GND_HOLD2
D42
D43
D40
D44
D45
ESD5311X
OWLVisionTech
Project: RK3568_OPC_MINI
File: 22.USB2/USB3 Port
Date: Friday, June 24, 2022
Rev: <Revision>
Designer: <designer>
Sheet: 13 of 20

HDMI_TX2P_PORT
HDMI_TX2N_PORT
M203_HDMI_TX2P_PORT 9
M201_HDMI_TX2N_PORT 9

HDMI_TX1P_PORT
HDMI_TX1N_PORT
M197_HDMI_TX1P_PORT 9
M195_HDMI_TX1N_PORT 9

HDMI_TX0P_PORT
HDMI_TX0N_PORT
M191_HDMI_TX0P_PORT 9
M189_HDMI_TX0N_PORT 9

HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
M185_HDMI_TXCLKP_PORT 9
M183_HDMI_TXCLKN_PORT 9

HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN
M127_HDMITX_SCL 7
M125_HDMITX_SDA 7
M121_HDMITX_CEC_M0 7
M040_HDMI_TX_HPDIN 9

VCC5V0_SYS
U2
TMI6263BH
SOT_23_5
IN
OUT
GND
EN
SET
C45
4.7uF
SC0402
X5R
10V
R69
10K
5%
SR0201
D16
B5819W
SOD_123
VCC5V_HDMI_TX
C47
4.7uF
SC0402
X5R
10V

## HDMI TX DDC

VCC5V0_SYS
D17
B5819WS
SOD_323
VCC3V3_SYS
R78
10K
5%
R0201
Q8
2SK3018
SOT_323
R73
1.8K
5%
R0201
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC3V3_SYS
R79
10K
5%
R0201
Q9
2SK3018
SOT_323
R74
1.8K
5%
R0201
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

## HDMI TX CEC

VCC3V3_SYS
VCC5V0_SYS
R77
27K
5%
R0201
Q7
2SK3018
SOT_323
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

## HDMI TX HPD

HDMI_TX_HPDIN
R75
1K
5%
R0201
HDMI_TX_HPD_PORT
R76
100K
5%
R0201

U11
PESDALC10N5VU
ESD2510H0_75
Cj<=0.4pF
U10
PESDALC10N5VU
ESD2510H0_75
IO1
IO2
GND
IO3
IO4
NC_10
NC_9
NC_7
NC_6
HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT
VCC5V_HDMI_TX
ED6
ESD5341N
ESD0402
ED5
ESD5341N
ESD0402
ED4
ESD5341N
ESD0402
ED3
ESD5341N
ESD0402
C46
100nF
X5R
10V
C0201
J13
HDMI_TYPE_A
HDMIA19_HDMI_01A
D2P
D2_G
D2N
D1P
D1_G
D1N
D0P
D0_G
D0N
CLKP
CLK_G
CLKN
CEC
Utility
SCL
SDA
GND
+5V
HPD
Type A

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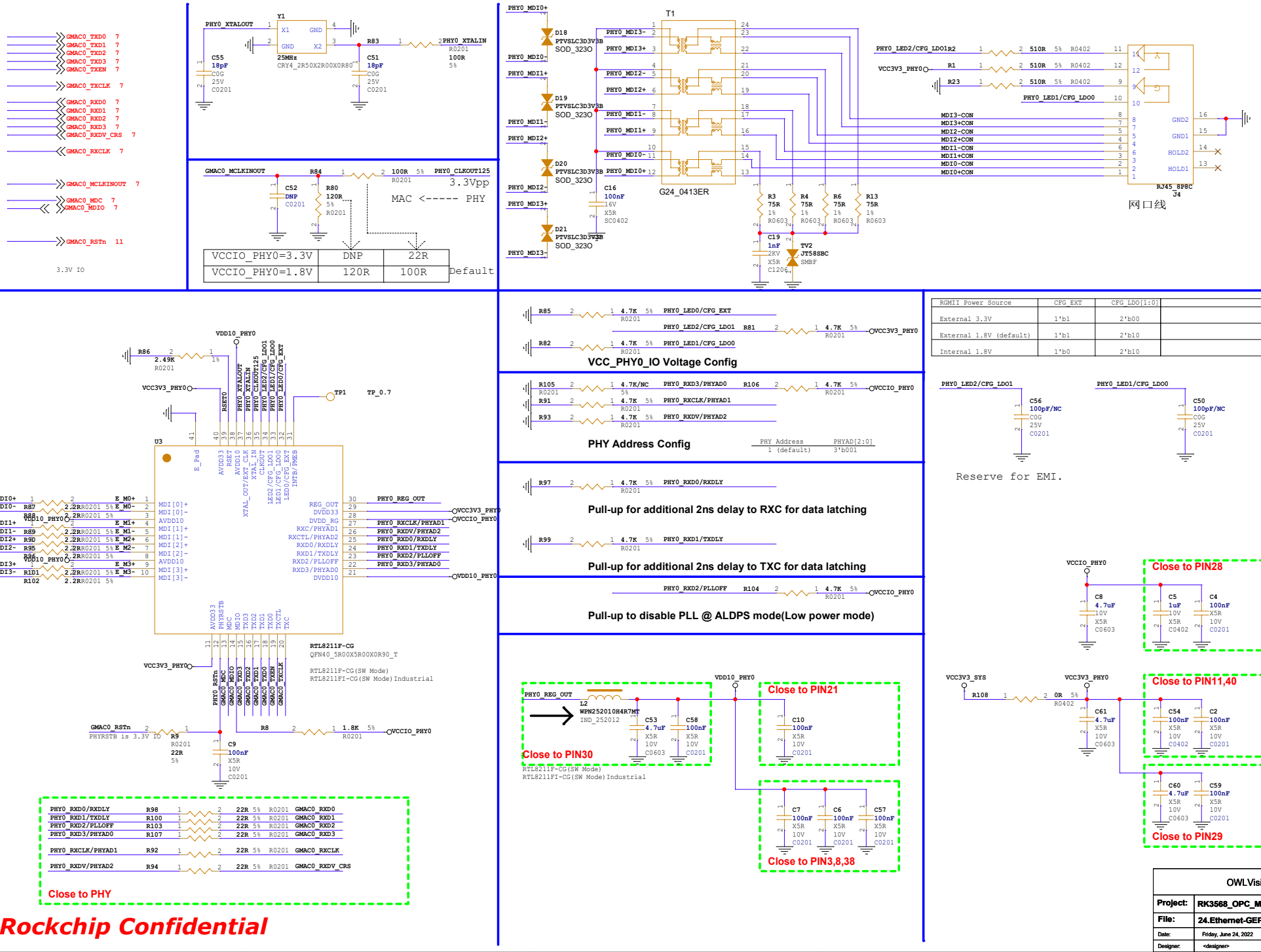
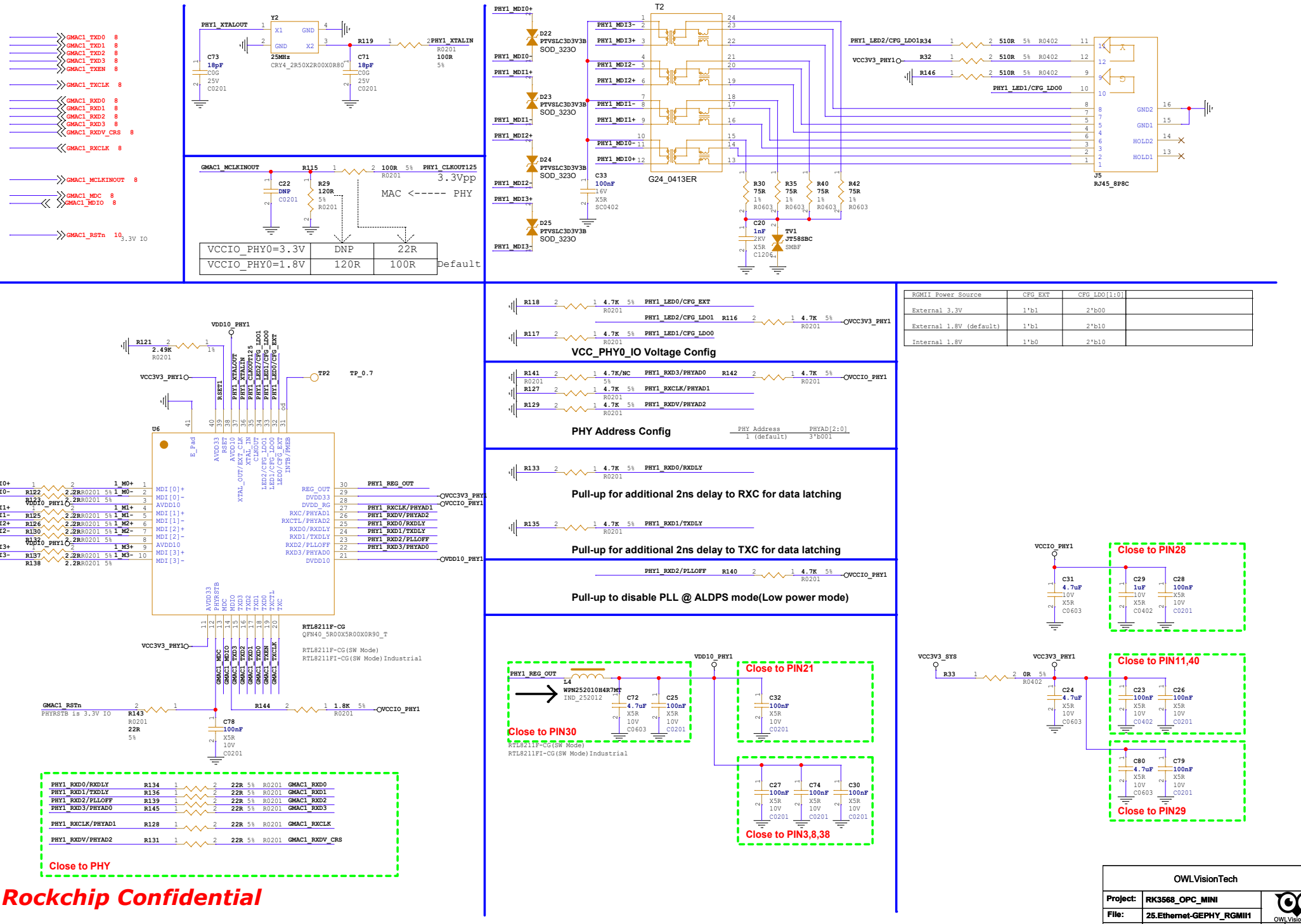
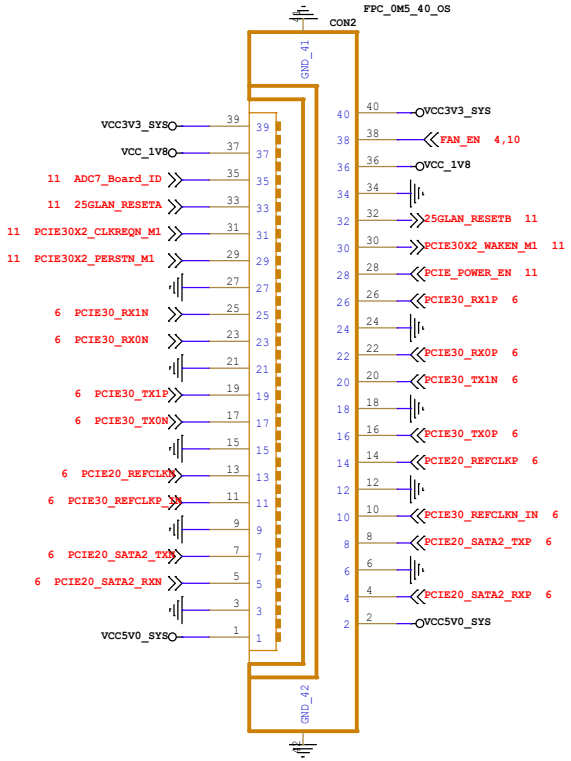
| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 23.VO-HDMI2.0 TX | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 14 of 20 |

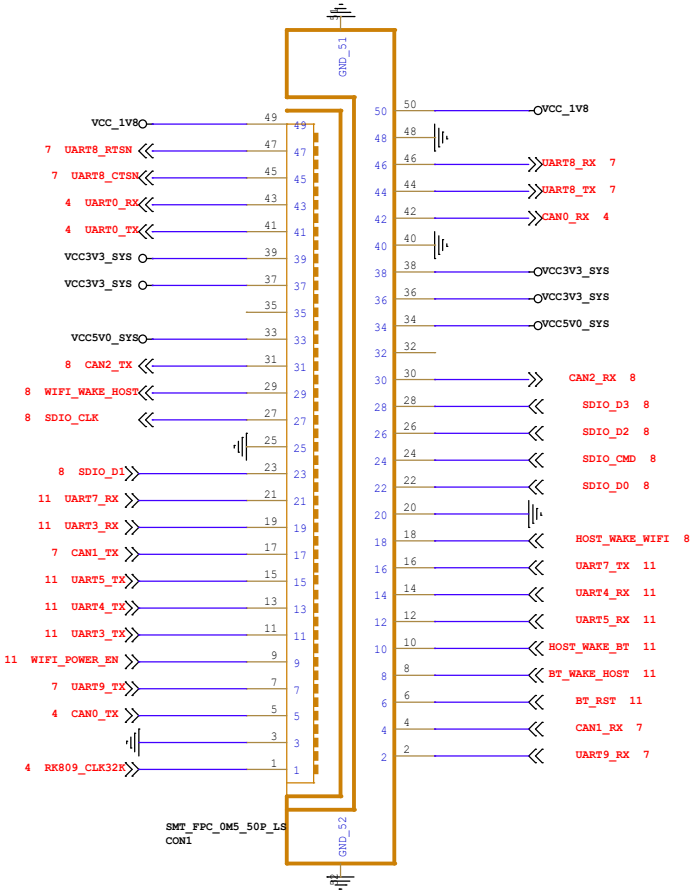

GMAC0_TXD0 7
GMAC0_TXD1 7
GMAC0_TXD2 7
GMAC0_TXD3 7
GMAC0_TXEN 7
GMAC0_TXCLK 7
GMAC0_RXD0 7
GMAC0_RXD1 7
GMAC0_RXD2 7
GMAC0_RXD3 7
GMAC0_RXDV_CRS 7
GMAC0_RXCLK 7
GMAC0_MCLKINOUT 7
GMAC0_MDC 7
GMAC0_MDIO 7
GMAC0_RSTn 11
3.3V IO
PHY0_XTALOUT
Y1
25MHz
CRY4_2R50X2R00X0R80
C55 18pF C0G 25V C0201
C51 18pF C0G 25V C0201
R83 100R 5% R0201
PHY0_XTALIN
GMAC0_MCLKINOUT
R84 100R 5% R0201
PHY0_CLKOUT125
3.3Vpp
MAC <----- PHY
C52 DNP C0201
R80 120R 5% R0201
VCCIO_PHY0=3.3V DNP 22R
VCCIO_PHY0=1.8V 120R 100R Default
PHY0_MDI0+
PHY0_MDI0-
PHY0_MDI1+
PHY0_MDI1-
PHY0_MDI2+
PHY0_MDI2-
PHY0_MDI3+
PHY0_MDI3-
T1
G24_0413ER
D18 PTVSLC3D3V3B SOD_323O
D19 PTVSLC3D3V3B SOD_323O
D20 PTVSLC3D3V3B SOD_323O
D21 PTVSLC3D3V3B SOD_323O
C16 100nF 16V X5R SC0402
R3 75R 1% R0603
R4 75R 1% R0603
R6 75R 1% R0603
R13 75R 1% R0603
C19 1nF 2KV X5R C1206
TV2 JT58SBC SMBF
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
R2 510R 5% R0402
R1 510R 5% R0402
R23 510R 5% R0402
VCC3V3_PHY0
MDI3-CON
MDI3+CON
MDI2-CON
MDI2+CON
MDI1-CON
MDI1+CON
MDI0-CON
MDI0+CON
GND2
GND1
HOLD2
HOLD1
RJ45_8P8C
J4
网口线
VDD10_PHY0
R86 2.49K 1% R0201
VCC3V3_PHY0
TP1 TP_0.7
U3
E_Pad
RSET0
PHY_XTALOUT
PHY_XTALIN
PHY_CLKOUT125
PHY_LED2/CFG_LDO1
PHY_LED1/CFG_LDO0
PHY_LED0/CFG_EXT
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
AVDD10
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode) Industrial
E_M0+ E_M0- E_M1+ E_M1- E_M2+ E_M2- E_M3+ E_M3-
R87 R88 R89 R90 R95 R96 R101 R102 2.2R R0201 5%
VCC3V3_PHY0
VCCIO_PHY0
VDD10_PHY0
GMAC0_RSTn
PHYRSTB is 3.3V IO
R9 22R 5% R0201
R8 1.8K 5% R0201
C9 100nF X5R 10V C0201
R85 4.7K 5% R0201 PHY0_LED0/CFG_EXT
R82 4.7K 5% R0201 PHY0_LED1/CFG_LDO0
R81 4.7K 5% R0201 PHY0_LED2/CFG_LDO1
VCC_PHY0_IO Voltage Config
R105 4.7K/NC 5% R0201 PHY0_RXD3/PHYAD0
R91 4.7K 5% R0201 PHY0_RXCLK/PHYAD1
R93 4.7K 5% R0201 PHY0_RXDV/PHYAD2
R106 4.7K 5% R0201 VCCIO_PHY0
PHY Address Config
PHY Address PHYAD[2:0]
1 (default) 3'b001
R97 4.7K 5% R0201 PHY0_RXD0/RXDLY
Pull-up for additional 2ns delay to RXC for data latching
R99 4.7K 5% R0201 PHY0_RXD1/TXDLY
Pull-up for additional 2ns delay to TXC for data latching
R104 4.7K 5% R0201 PHY0_RXD2/PLLOFF VCCIO_PHY0
Pull-up to disable PLL @ ALDPS mode(Low power mode)
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V (default) | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
C56 100pF/NC C0G 25V C0201
C50 100pF/NC C0G 25V C0201
Reserve for EMI.
PHY0_RXD0/RXDLY R98 22R 5% R0201 GMAC0_RXD0
PHY0_RXD1/TXDLY R100 22R 5% R0201 GMAC0_RXD1
PHY0_RXD2/PLLOFF R103 22R 5% R0201 GMAC0_RXD2
PHY0_RXD3/PHYAD0 R107 22R 5% R0201 GMAC0_RXD3
PHY0_RXCLK/PHYAD1 R92 22R 5% R0201 GMAC0_RXCLK
PHY0_RXDV/PHYAD2 R94 22R 5% R0201 GMAC0_RXDV_CRS
Close to PHY
PHY0_REG_OUT
L2 WPN252010H4R7MT IND_252012
C53 4.7uF X5R 10V C0603
C58 100nF X5R 10V C0201
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode) Industrial
VDD10_PHY0
Close to PIN21
C10 100nF X5R 10V C0201
C7 100nF X5R 10V C0201
C6 100nF X5R 10V C0201
C57 100nF X5R 10V C0201
Close to PIN3,8,38
VCCIO_PHY0
C8 4.7uF X5R 10V C0603
C5 1uF X5R 10V C0402
C4 100nF X5R 10V C0201
Close to PIN28
VCC3V3_SYS
R108 0R 5% R0402
VCC3V3_PHY0
C61 4.7uF X5R 10V C0603
C54 100nF X5R 10V C0402
C2 100nF X5R 10V C0201
C60 4.7uF X5R 10V C0603
C59 100nF X5R 10V C0201
Close to PIN11,40
Close to PIN29
Rockchip Confidential
OWLVisionTech
Project: RK3568_OPC_MINI
File: 24.Ethernet-GEPHY_RGMII0
Date: Friday, June 24, 2022
Rev: <Revision>
Designer: <designer>
Sheet: 15 of 20


GMAC1_TXD0 8
GMAC1_TXD1 8
GMAC1_TXD2 8
GMAC1_TXD3 8
GMAC1_TXEN 8
GMAC1_TXCLK 8
GMAC1_RXD0 8
GMAC1_RXD1 8
GMAC1_RXD2 8
GMAC1_RXD3 8
GMAC1_RXDV_CRS 8
GMAC1_RXCLK 8
GMAC1_MCLKINOUT 8
GMAC1_MDC 8
GMAC1_MDIO 8
GMAC1_RSTn 10
3.3V IO
PHY1_XTALOUT
Y2
25MHz
CRY4_2R50X2R00X0R80
C73 18pF C0G 25V C0201
C71 18pF C0G 25V C0201
R119 R0201 100R 5%
PHY1_XTALIN
GMAC1_MCLKINOUT
R115 100R 5% R0201
PHY1_CLKOUT125
3.3Vpp
MAC <----- PHY
C22 DNP C0201
R29 120R 5% R0201
VCCIO_PHY0=3.3V | DNP | 22R
VCCIO_PHY0=1.8V | 120R | 100R
Default
PHY1_MDI0+
PHY1_MDI0-
PHY1_MDI1+
PHY1_MDI1-
PHY1_MDI2+
PHY1_MDI2-
PHY1_MDI3+
PHY1_MDI3-
D22 PTVSLC3D3V3B SOD_323O
D23 PTVSLC3D3V3B SOD_323O
D24 PTVSLC3D3V3B SOD_323O
D25 PTVSLC3D3V3B SOD_323O
T2
G24_0413ER
C33 100nF 16V X5R SC0402
R30 75R 1% R0603
R35 75R 1% R0603
R40 75R 1% R0603
R42 75R 1% R0603
C20 1nF 2KV X5R C1206
TV1 JT58SBC SMBF
PHY1_LED2/CFG_LDO1
R34 510R 5% R0402
VCC3V3_PHY1
R32 510R 5% R0402
R146 510R 5% R0402
PHY1_LED1/CFG_LDO0
J5 RJ45_8P8C
GND2
GND1
HOLD2
HOLD1
VDD10_PHY1
R121 2.49K 1% R0201
VCC3V3_PHY1
TP2 TP_0.7
U6
E_Pad
RSET1
PHY1_XTALOUT
PHY1_XTALIN
PHY1_CLKOUT125
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
PHY1_LED0/CFG_EXT
INTB/PWEB
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
PHY1_REG_OUT
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
PHY1_MDI0+ R122 2.2R 1% R0201 1_M0+
PHY1_MDI0- R123 2.2R 1% R0201 1_M0-
PHY1_MDI1+ R124 2.2R 1% R0201 1_M1+
PHY1_MDI1- R125 2.2R 1% R0201 1_M1-
PHY1_MDI2+ R126 2.2R 1% R0201 1_M2+
PHY1_MDI2- R130 2.2R 1% R0201 1_M2-
PHY1_MDI3+ R132 2.2R 1% R0201 1_M3+
PHY1_MDI3- R137 2.2R 1% R0201 1_M3-
R138 2.2R 1% R0201
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
GMAC1_RSTn
PHYRSTB is 3.3V IO
R143 22R 5% R0201
R144 1.8K 5% R0201
VCCIO_PHY1
C78 100nF X5R 10V C0201
PHY1_RXD0/RXDLY R134 22R 5% R0201 GMAC1_RXD0
PHY1_RXD1/TXDLY R136 22R 5% R0201 GMAC1_RXD1
PHY1_RXD2/PLLOFF R139 22R 5% R0201 GMAC1_RXD2
PHY1_RXD3/PHYAD0 R145 22R 5% R0201 GMAC1_RXD3
PHY1_RXCLK/PHYAD1 R128 22R 5% R0201 GMAC1_RXCLK
PHY1_RXDV/PHYAD2 R131 22R 5% R0201 GMAC1_RXDV_CRS
Close to PHY
R118 4.7K 5% R0201 PHY1_LED0/CFG_EXT
PHY1_LED2/CFG_LDO1
R116 4.7K 5% R0201 VCC3V3_PHY1
R117 4.7K 5% R0201 PHY1_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config
R141 4.7K/NC 5% R0201 PHY1_RXD3/PHYAD0
R142 4.7K 5% R0201 VCCIO_PHY1
R127 4.7K 5% R0201 PHY1_RXCLK/PHYAD1
R129 4.7K 5% R0201 PHY1_RXDV/PHYAD2
PHY Address Configuration
PHY Address 1 (default) PHYAD[2:0] 3'b001
R133 4.7K 5% R0201 PHY1_RXD0/RXDLY
Pull-up for additional 2ns delay to RXC for data latching
R135 4.7K 5% R0201 PHY1_RXD1/TXDLY
Pull-up for additional 2ns delay to TXC for data latching
PHY1_RXD2/PLLOFF R140 4.7K 5% R0201 VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V (default) | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
PHY1_REG_OUT
L4 WPN252010H4R7MT IND_252012
C72 4.7uF X5R 10V C0603
C25 100nF X5R 10V C0201
Close to PIN30
VDD10_PHY1
Close to PIN21
C32 100nF X5R 10V C0201
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C27 100nF X5R 10V C0201
C74 100nF X5R 10V C0201
C30 100nF X5R 10V C0201
Close to PIN3,8,38
VCCIO_PHY1
C31 4.7uF 10V X5R C0603
C29 1uF 10V X5R C0402
C28 100nF X5R 10V C0201
Close to PIN28
VCC3V3_SYS
R33 0R 5% R0402
VCC3V3_PHY1
C24 4.7uF X5R 10V C0603
C23 100nF X5R 10V C0402
C26 100nF X5R 10V C0201
Close to PIN11,40
C80 4.7uF X5R 10V C0603
C79 100nF X5R 10V C0201
Close to PIN29
Rockchip Confidential
OWLVisionTech
Project: RK3568_OPC_MINI
File: 25.Ethernet-GEPHY_RGMII1
OWLVisionTech
Date: Friday, June 24, 2022
Rev: <Revision>
Designer: <designer>
Sheet: 16 of 20

# WIFI/BT Module

## Module Power




When standby, SDIO of SOC is powered on continuously, r6009 and r6008 are not connected, r6010 is connected, WIFI_WAKEHOST is used to wake up SOC by default.

When standby, SDIO of SOC is powered off, r6009 and r6008 are connected, r6010 is not connected and wake up SOC by WAKEUP_SOC_OPTION

| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 26.WIFI6+PCIE2.5G | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
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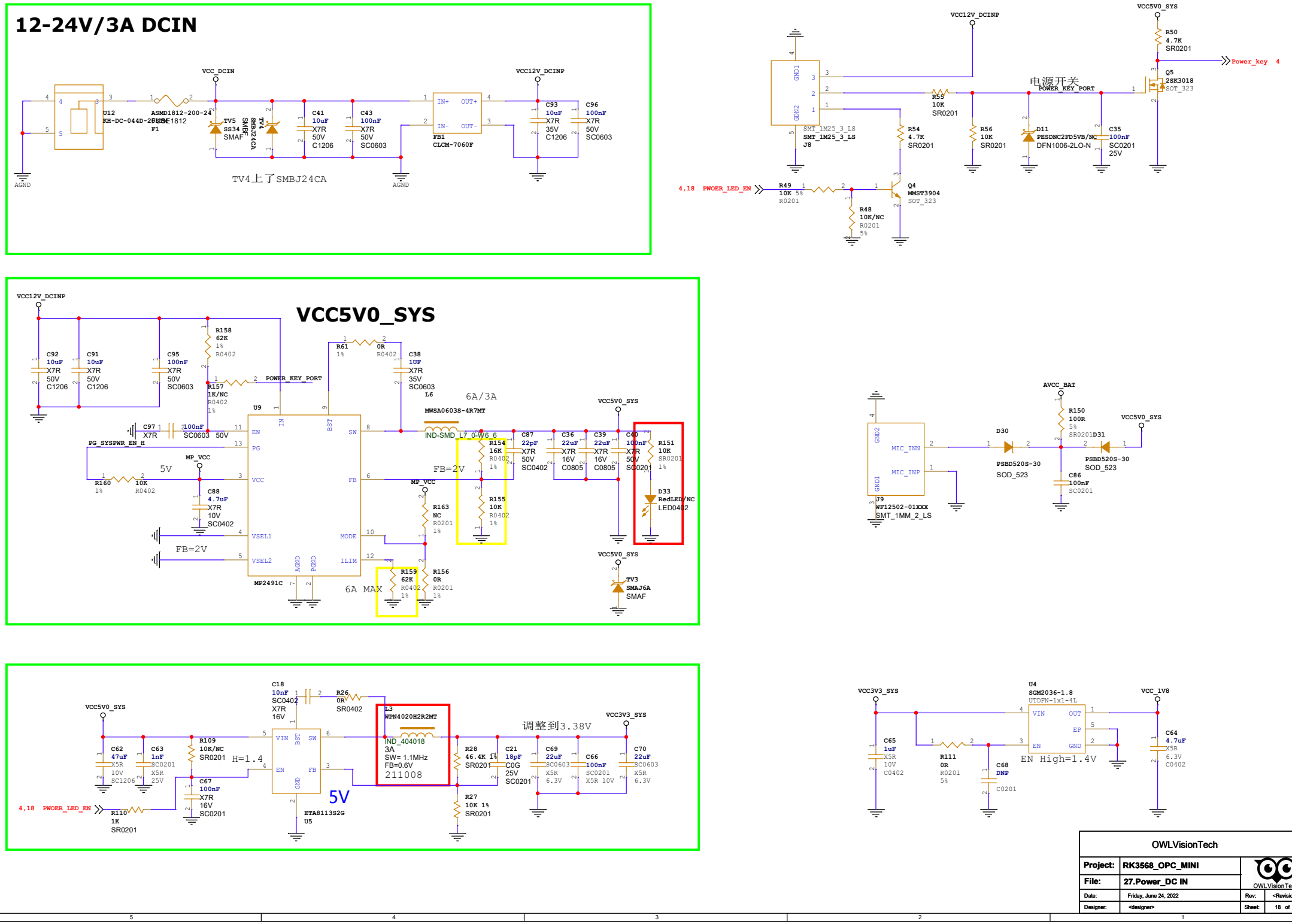
12-24V/3A DCIN
VCC_DCIN
VCC12V_DCINP
U12
KH-DC-044D-2.5/5.5
ASMD1812-200-24
SMD1812
F1
TV5
SS34
SMAF
TV4
SMBJ24CA
SMB
C41
10uF
X7R
50V
C1206
C43
100nF
X7R
50V
SC0603
FB1
CLCM-7060F
C93
10uF
X7R
35V
C1206
C96
100nF
X7R
50V
SC0603
TV4上了SMBJ24CA
AGND
VCC5V0_SYS
VCC12V_DCINP
R50
4.7K
SR0201
Power_key 4
电源开关
POWER_KEY_PORT
Q5
2SK3018
SOT_323
R55
10K
SR0201
R54
4.7K
SR0201
R56
10K
SR0201
D11
PESDNC2FD5VB/NC
DFN1006-2LO-N
C35
100nF
SC0201
25V
SMT_1M25_3_LS
SMT_1M25_3_LS
J8
4,18 PWOER_LED_EN
R49
10K 5%
R0201
Q4
MMST3904
SOT_323
R48
10K/NC
R0201
5%
VCC5V0_SYS
R158
62K
1%
R0402
R61
1%
0R
R0402
C38
1UF
X7R
35V
SC0603
L6
6A/3A
MWSA0603S-4R7MT
POWER_KEY_PORT
R157
1K/NC
R0402
1%
C97
X7R
100nF
SC0603
50V
U9
EN
IN
BST
SW
PG
VCC
FB
VSEL1
VSEL2
MODE
ILIM
AGND
PGND
MP2491C
PG_SYSPWR_EN_H
5V
MP_VCC
R160
10K
R0402
C88
4.7uF
X7R
10V
SC0402
FB=2V
IND-SMD_L7_0-W6_6
R154
16K
R0402
1%
R155
10K
R0402
1%
C87
22pF
X7R
50V
SC0402
C36
22uF
X7R
16V
C0805
C39
22uF
X7R
16V
C0805
C40
100nF
X7R
50V
SC0201
R151
10K
SR0201
1%
D33
RedLED/NC
LED0402
R163
NC
R0201
1%
R159
62K
R0402
1%
R156
0R
R0201
1%
6A MAX
TV3
SMAJ6A
SMAF
AVCC_BAT
R150
100R
5%
SR0201
D31
PSBD520S-30
SOD_523
D30
PSBD520S-30
SOD_523
C86
100nF
SC0201
GND2
GND1
MIC_INN
MIC_INP
J9
WF12502-01XXX
SMT_1MM_2_LS
C18
10nF
SC0402
X7R
16V
R26
0R
SR0402
L3
WPN4020H2R2MT
IND_404018
3A
SW= 1.1MHz
FB=0.6V
211008
VCC5V0_SYS
VCC3V3_SYS
调整到3.38V
C62
47uF
X5R
10V
SC1206
C63
1nF
SC0201
X5R
25V
R109
10K/NC
SR0201
H=1.4
C67
100nF
X7R
16V
SC0201
R110
1K
SR0201
4,18 PWOER_LED_EN
VIN
BST
SW
EN
FB
GND
ETA8113S2G
U5
5V
R28
46.4K 1%
SR0201
C21
18pF
C0G
25V
SC0201
R27
10K 1%
SR0201
C69
22uF
SC0603
X5R
6.3V
C66
100nF
SC0201
X5R 10V
C70
22uF
SC0603
X5R
6.3V
VCC3V3_SYS
U4
SGM2036-1.8
UTDFN-1x1-4L
VIN
OUT
EP
EN
GND
VCC_1V8
C65
1uF
X5R
10V
C0402
R111
0R
R0201
5%
C68
DNP
C0201
EN High=1.4V
C64
4.7uF
X5R
6.3V
C0402
OWLVisionTech
Project: RK3568_OPC_MINI
File: 27.Power_DC IN
Date: Friday, June 24, 2022
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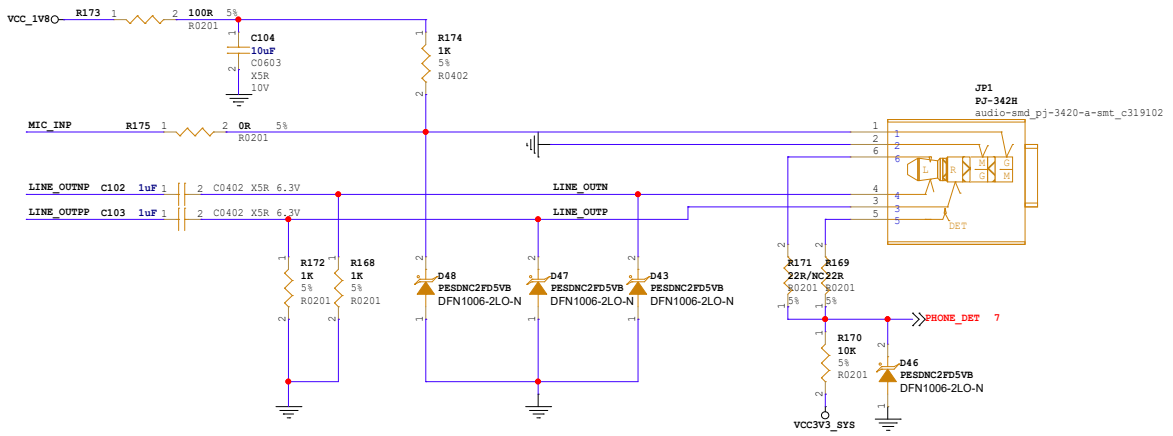
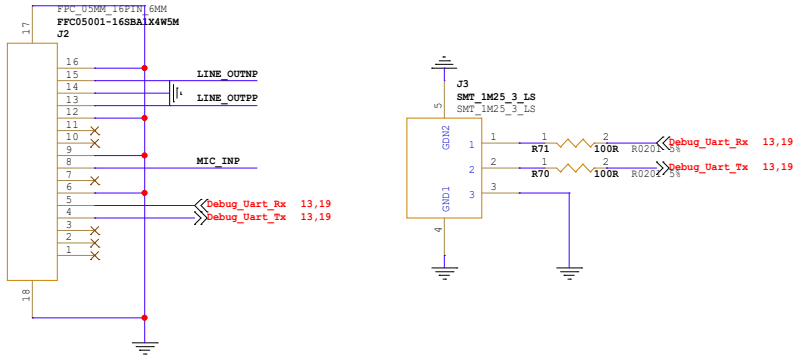
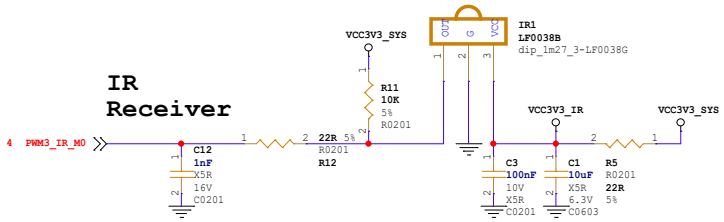
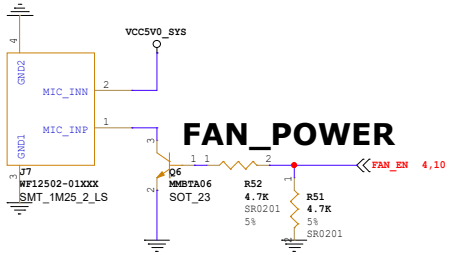
Sheet: 18 of 20



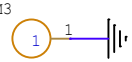

| OWLVisionTech | | | |
|---|---|---|---|
| Project: | RK3568_OPC_MINI | OWLVisionTech | |
| File: | 28.UART IO | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 19 of 20 |

**H2**
**NA**
NP-C1P20

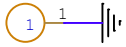

**H4**
**NA**
NP-C1P20


**H3**
**NA**
NP-C1P20


**H1**
**NA**
M3




**H5**
**NA**
M3




**MARK4**
**FID_MARK_PASTE**


**MARK2**
**FID_MARK_PASTE**


**MARK1**
**FID_MARK_PASTE**


**MARK3**
**FID_MARK_PASTE**


| OWLVisionTech | | | |
|---|---|---|---|
| **Project:** | **RK3568_OPC_MINI** | OWLVisionTech | |
| **File:** | **29.Mark/Hole/Heatsink** | | |
| Date: | Friday, June 24, 2022 | Rev: | <Revision> |
| Designer: | <designer> | Sheet: | 20 of 20 |