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RTL8370MB-CG

LAYER 2 MANAGED 8+2-PORT 10/100/1000 SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.0
10 April 2017
Track ID: JATR-8275-15

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2017/04/10	First release.

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1. General Description

The Realtek RTL8370MB-CG is a TQFP176 E-PAD, high-performance 8+2-port Gigabit Ethernet switch. It integrates 8 low-power Giga-PHYs that support 1000Base-T/100Base-T/10Base-T.

For specific applications, the RTL8370MB supports two extra interfaces. Extension GMAC1 supports RGMII(3.3v/2.5v)/MII/TMII/RMII/SGMII/1000Base-X/100Base-FX, Extension GMAC2 supports RGMII(3.3v/2.5v/1.8v)/MII/TMII/RMII/HSGMII/SGMII/1000Base-X/100Base-FX. The RTL8370MB implements all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8370MB features superior memory management technology to efficiently utilize memory space. The RTL8370MB integrates a 4096-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the EEPROM Serial Management Interface (SMI), and each of the entries can be configured as a static entry. The entry aging time is between 200 and 400 seconds. Sixteen Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The Extension GMAC1 and Extension GMAC2 of the RTL8370MB can connect to an external PHY or MAC with different interfaces. These interfaces could be connected to an external CPU or RISC as 8-port Gigabit Router applications. In router applications, the RTL8370MB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

Note: RTL8370MB Extra Interface can be used as:

Reduced Gigabit Media Independent Interface (RGMII)
Media Independent Interface (MII)
Turbo Media Independent Interface (TMII)
Reduced Media Independent Interface (RMII)
High-Serial Gigabit Media Independent Interface (HSGMII)
Serial Gigabit Media Independent Interface (SGMII)
IEEE 1000Base-X
IEEE 100Base-FX

The RTL8370MB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8370MB supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8370MB can forward IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping.

In order to support flexible traffic classification, the RTL8370MB supports 96-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

To meet security and management application requirements, the RTL8370MB supports IEEE 802.1x Port-based/MAC-based Access Control. For those ports that do not pass IEEE 802.1x authentication, the RTL8370MB provides a Port-based/MAC-based Guest VLAN function for them to access limited network resources. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time or multimedia networking applications, the RTL8370MB supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority; (5) CVLAN-based priority; (6) SVLAN-based priority; and (7) SMAC-based/LUTFWD-based priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8370MB provides a 4096-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8370MB supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or EEPROM SMI Slave after reset.

In router applications, the router may want to know the input port of the incoming packet. The RTL8370MB supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8370MB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, the RTL8370MB will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- Single-chip 8+2-port gigabit non-blocking switch architecture;
- Embedded 8-port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Supports Realtek Cable Test (RTCT) function
- Extra Interface (Extension GMAC1 and Extension GMAC2) supports
  - Dual-port Full Duplex Media Independent Interface (MII)
  - Dual-port Full Duplex Turbo Media Independent Interface (TMII)
  - Dual-port Reduced Media Independent Interface (RMII)
  - Dual-port Reduced Gigabit Media Independent Interface (RGMII)
  - Serial Gigabit Media Independent Interface (SGMII)
  - IEEE 1000Base-X/ IEEE 100Base-FX
- Extension GMAC2 supports HSGMII (High -Serial Gigabit Media Independent Interface, 3.125GHz)
- Supports 96-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions support mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment
  - Supports 5 types of user defined ACL rule format for 96 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4096K VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Supports Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Supports per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - Supports 4096-entry MAC address table with 4-way hash algorithm, and 64-entry CAM
  - Up to 4096 L2/L3 Filtering Database
- Supports Spanning Tree port behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances

- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Supports Quality of Service (QoS)
  - Supports per port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ) to provide minimum bandwidth
  - One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (64 shared meters, with 8kpbs granulation)
- Supports RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with 8 Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports 32 L2/IPv4 Multicast mappings to SVLAN
- Supports 4 IEEE 802.3ad Link aggregation port groups
- Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol
- Supports Loop Detection
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Supports 1 interrupt output to external CPU for notification
- Each port supports 3 parallel LEDs when Extension GMAC1&2 not work in RGMII/MII/TMII/RMII mode
- Supports serial mode LED, per port one/two/three LEDs
- Supports Slave EEPROM SMI/I2C-Like/SPI interface to access configuration register
- Integrated 8051 microprocessor
- Supports SPI Flash Interface
- 25MHz crystal
- TQFP 176-pin E-PAD package

3. Block Diagram

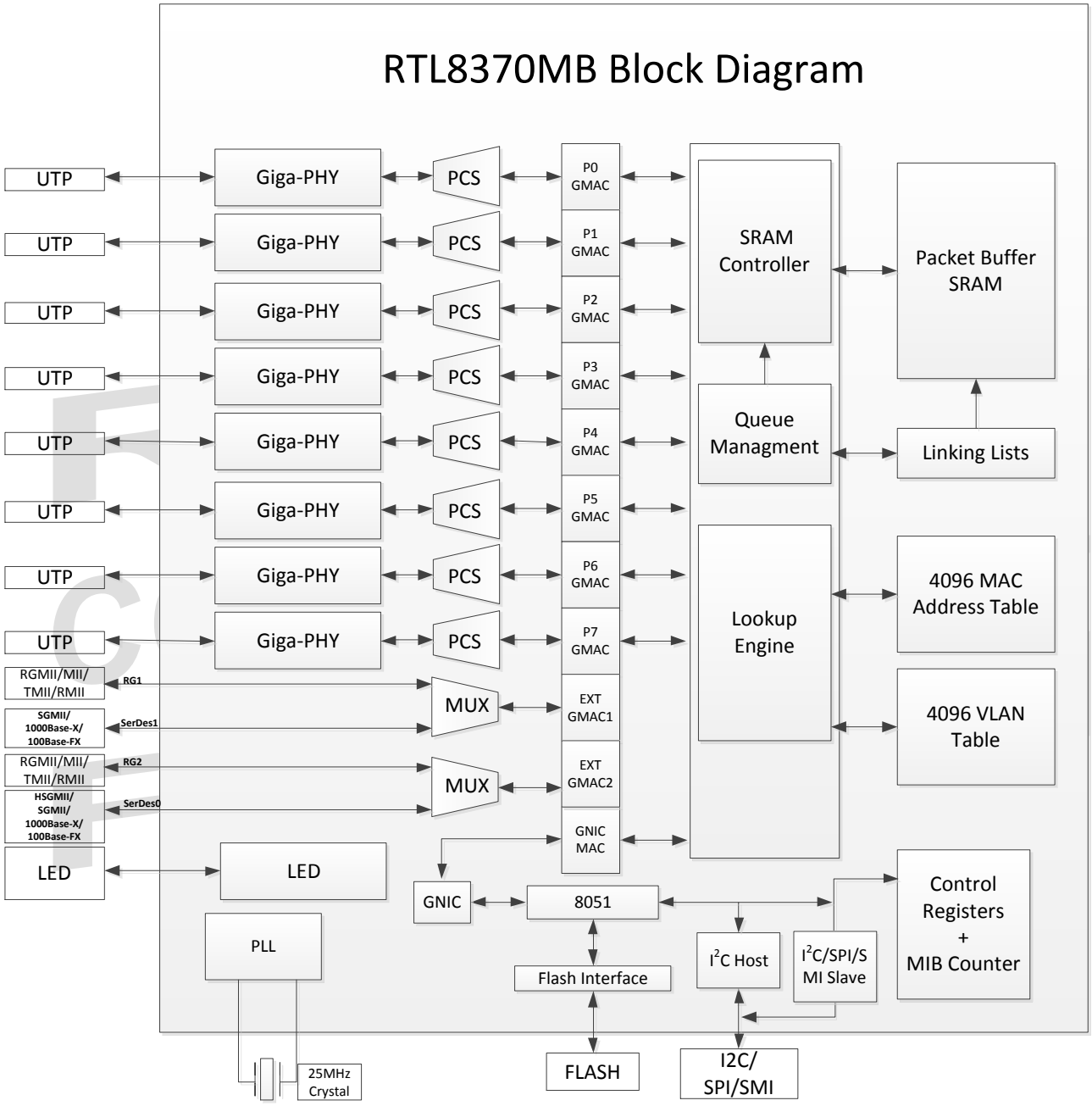


Figure 1. Block Diagram of RTL8370MB

4. System Applications

- 8-Port 1000Base-T+2-Port 1000Base-X/100Base-FX Un-Managed Switch
- 8-Port 1000Base-T Router with Dual MII/RGMII
- 8-Port 1000Base-T Router with Dual SGMII

4.1. 8-Port 1000Base-T+2-Port 1000Base-X/100Base-FX Switch

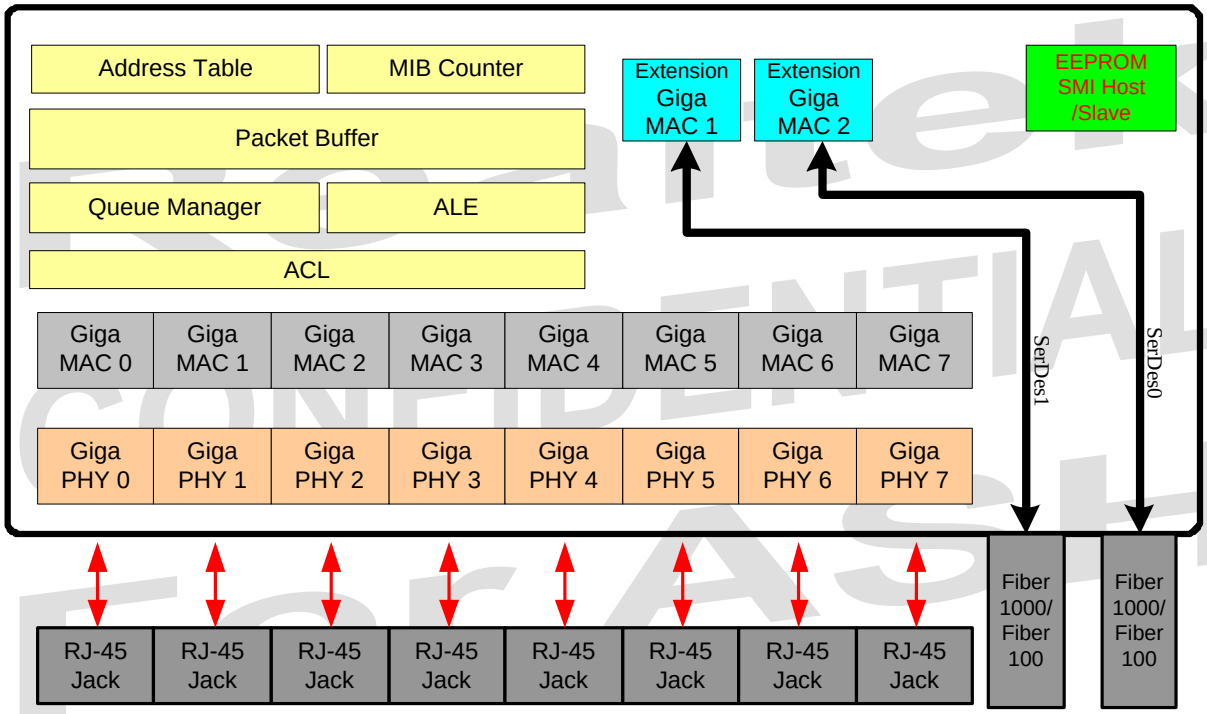


Figure 2. 8-Port 1000Base-T+2-Port 1000Base-X/100Base-FX Switch

Note: In this application, Parallel or Serial LED is recommended.

4.2. 8-Port 1000Base-T Router with Dual MII/RGMII

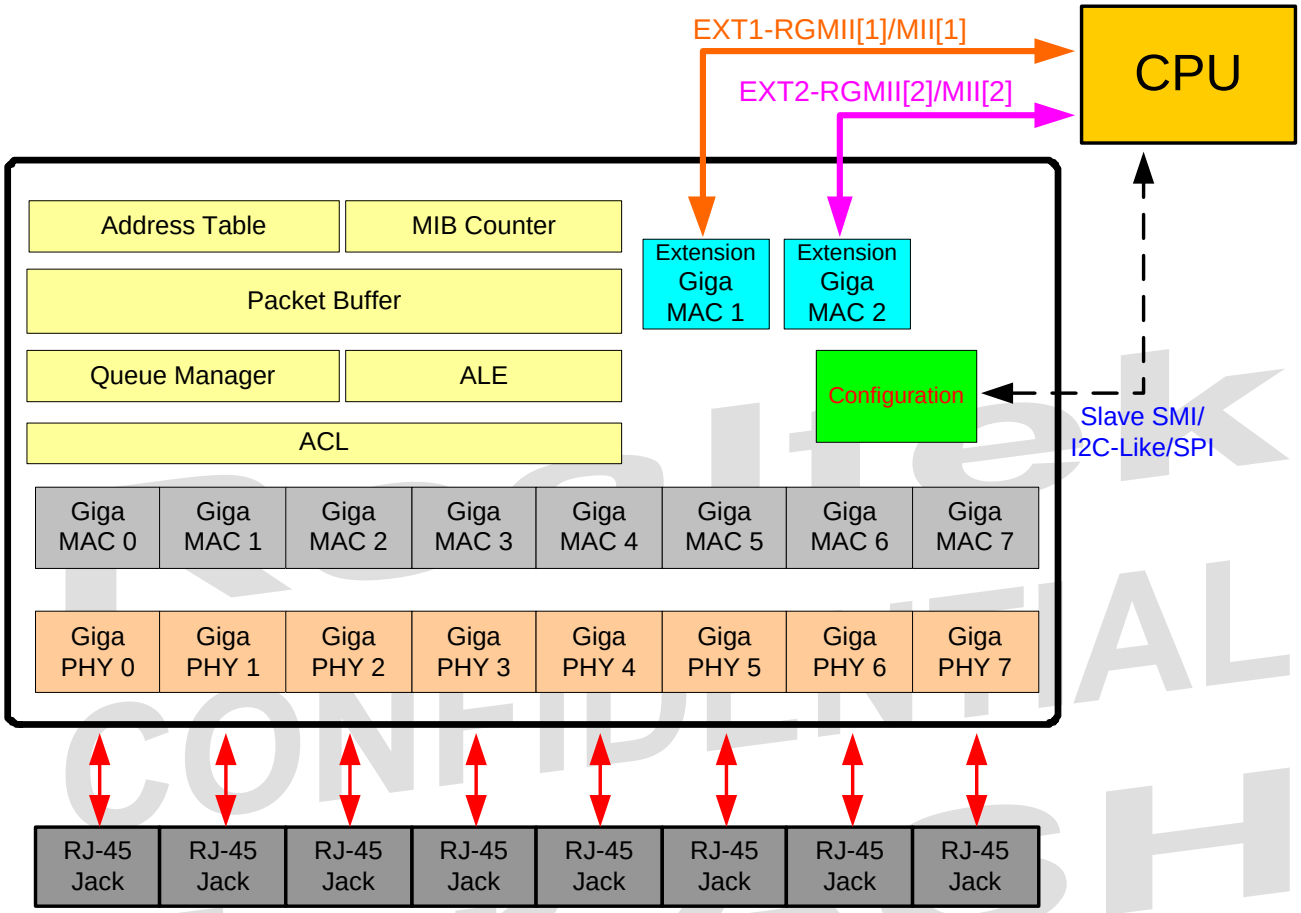


Figure 3. 8-Port 1000Base-T Router with Dual MII/RGMII

Note1: Extra Interface (Extension GMAC1 and Extension GMAC2) in MII/RGMII Mode.
Note2: In this application, Serial LED is recommended.
Note3: EXT1-RGMII support 3.3v/2.5v; EXT2-RGMII support 3.3v/2.5v/1.8v.

4.3. 8-Port 1000Base-T Router with Dual SGMII

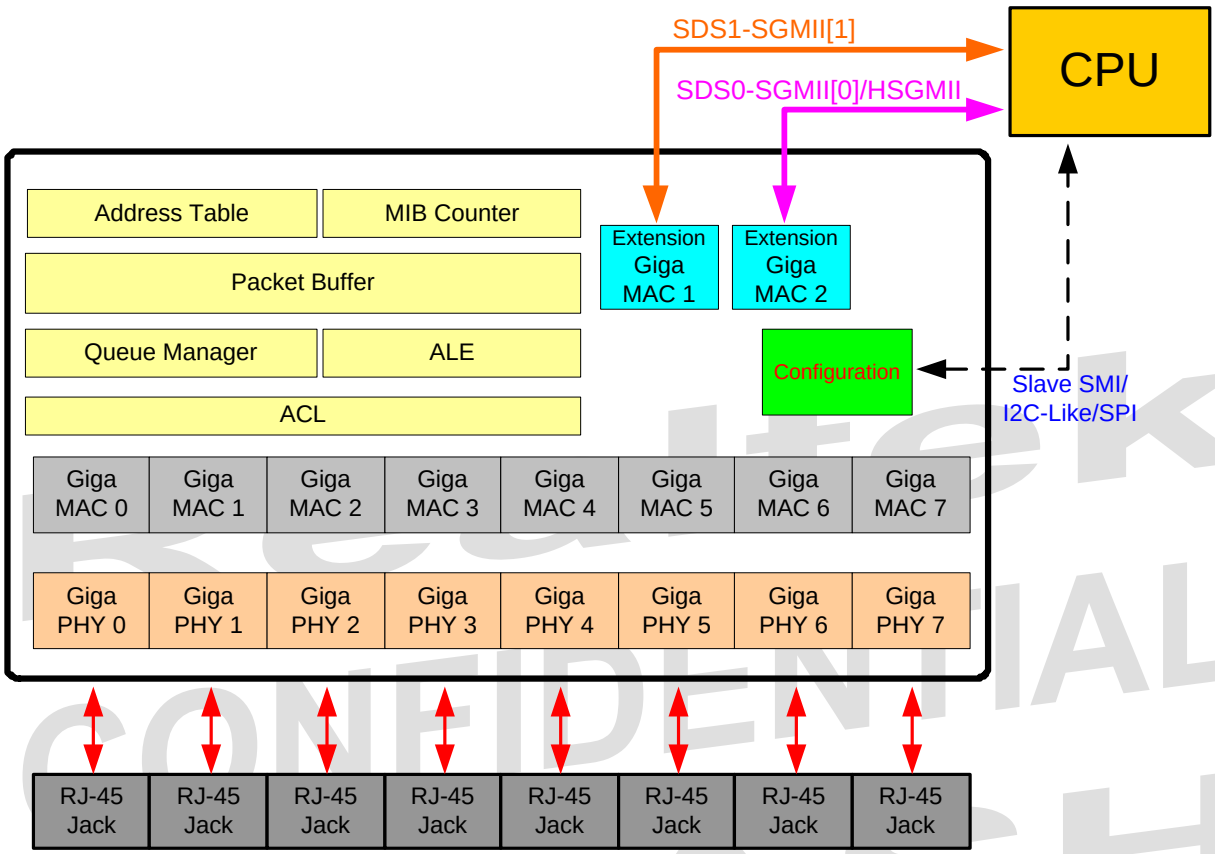


Figure 4. 8-Port 1000Base-T Router with Dual SGMII

Note1: Extension GMAC1 in SGMII Mode and Extension GMAC2 in SGMII/HSGMII Mode.
Note2: In this application, Parallel or Serial LED is recommended.

4.4. 8-Port 1000Base-T Router with RGMII(MII)+SGMII

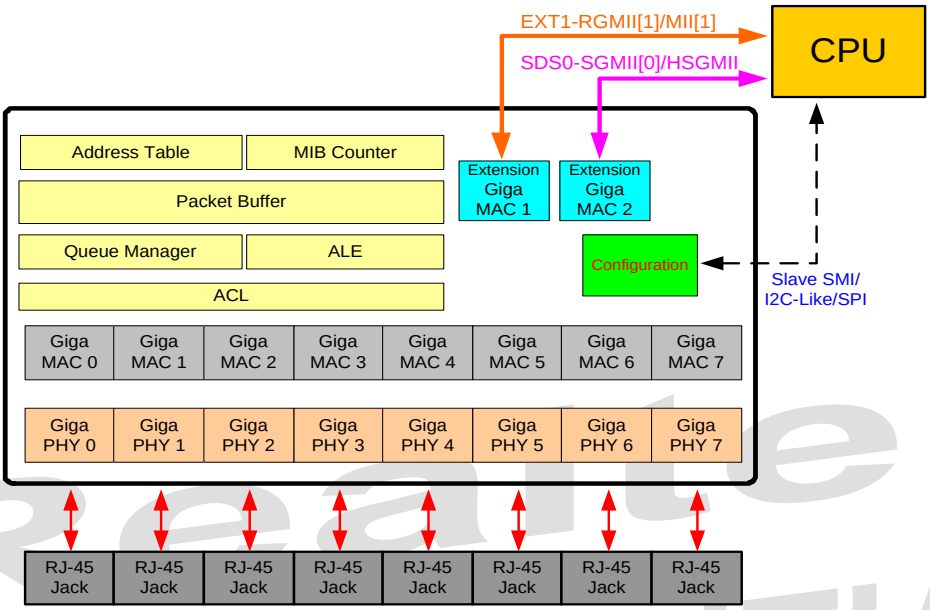


Figure 5. 8-Port 1000Base-T Router with EXT-GMAC1(MII/RGMII) and EXT-GMAC2(SGMII/HSGMII)

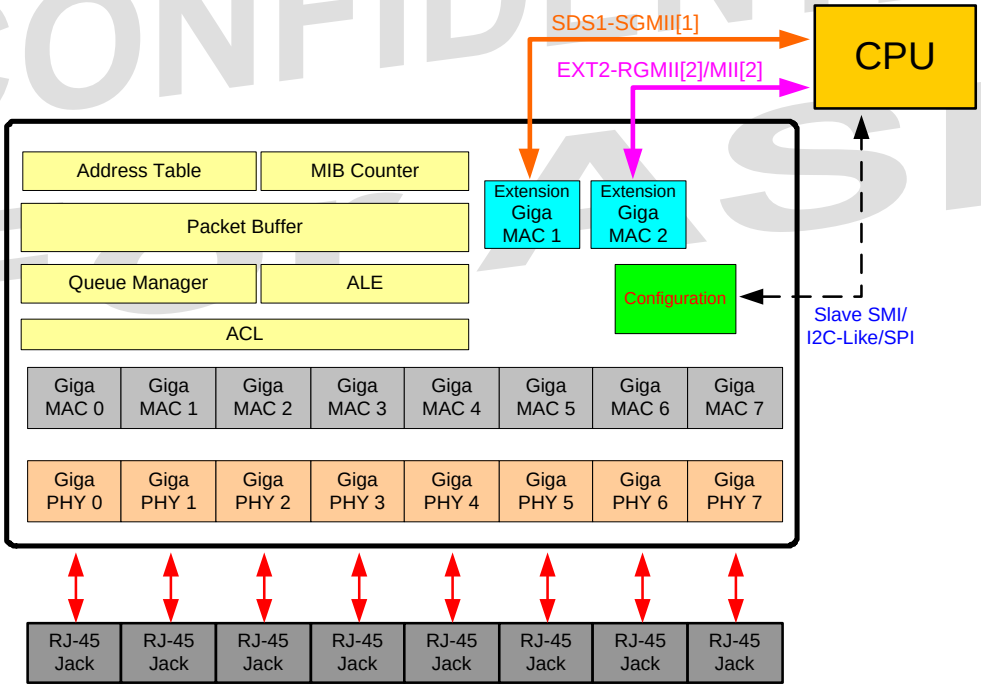


Figure 6. 8-Port 1000Base-T Router with EXT-GMAC1(SGMII) and EXT-GMAC2(MII/RGMII)

Note1: Two extra Interfaces in MII/RGMII and SGMII/HSGMII Mode individually.
Note2: In this application, Parallel or Serial LED is recommended.
Note3: EXT1-RGMII supports 3.3v/2.5v; EXT2-RGMII supports 3.3v/2.5v/1.8v.

5. Pin Assignments

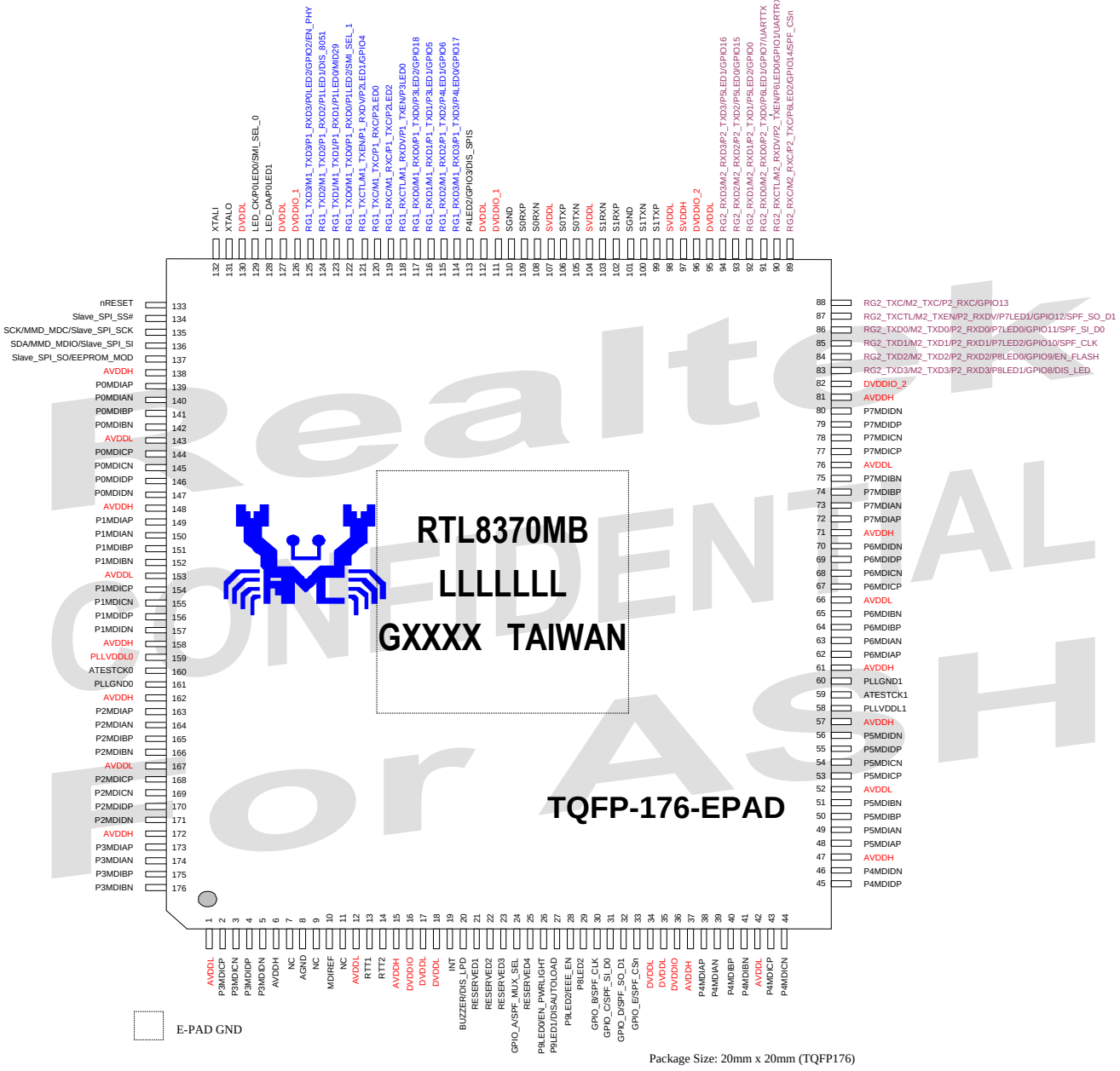


Figure 7. Pin Assignments

5.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 7).

5.2. Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

IPU: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

IS: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

OPU: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type
AVDDL	1	AP
P3MDICP	2	AI/O
P3MDICN	3	AI/O
P3MDIDP	4	AI/O
P3MDIDN	5	AI/O
AVDDH	6	AP
NC	7	-
AGND	8	AG
NC	9	-
MDIREF	10	AO
NC	11	-
AVDDL	12	AP
RTT1	13	AO
RTT2	14	AI
AVDDH	15	AP
DVDDIO	16	P
DVDDL	17	P
DVDDL	18	P
INT	19	O
BUZZER/DIS_LPD	20	I/O_{PU}
RESERVED1	21	I_{PD}
RESERVED2	22	I/O_{PD}
RESERVED3	23	I/O_{PD}
GPIO_A/SPF_MUX_SEL	24	I/O_{PU}

Name	Pin No.	Type
RESERVED4	25	I/O_{PU}
P9LED0/EN_PWRLIGHT	26	I/O_{PU}
P9LED1/DISAUTOLOAD	27	I/O_{PU}
P9LED2/EEE_EN	28	I/O_{PU}
P8LED2	29	I/O_{PU}
GPIO_B/SPF_CLK	30	I/O_{PU}
GPIO_C/SPF_SI_D0	31	I/O_{PU}
GPIO_D/SPF_SO_D1	32	I/O_{PU}
GPIO_E/SPF_CSn	33	I/O_{PU}
DVDDL	34	P
DVDDL	35	P
DVDDIO	36	P
AVDDH	37	AP
P4MDIAP	38	AI/O
P4MDIAN	39	AI/O
P4MDIBP	40	AI/O
P4MDIBN	41	AI/O
AVDDL	42	AP
P4MDICP	43	AI/O
P4MDICN	44	AI/O
P4MDIDP	45	AI/O
P4MDIDN	46	AI/O
AVDDH	47	AP
P5MDIAP	48	AI/O

Name	Pin No.	Type
P5MDIAN	49	AI/O
P5MDIBP	50	AI/O
P5MDIBN	51	AI/O
AVDDL	52	AP
P5MDICP	53	AI/O
P5MDICN	54	AI/O
P5MDIDP	55	AI/O
P5MDIDN	56	AI/O
AVDDH	57	AP
PLLVDDL1	58	AP
ATESTCK1	59	AO
PLLGND1	60	AG
AVDDH	61	AP
P6MDIAP	62	AI/O
P6MDIAN	63	AI/O
P6MDIBP	64	AI/O
P6MDIBN	65	AI/O
AVDDL	66	AP
P6MDICP	67	AI/O
P6MDICN	68	AI/O
P6MDIDP	69	AI/O
P6MDIDN	70	AI/O
AVDDH	71	AP
P7MDIAP	72	AI/O
P7MDIAN	73	AI/O
P7MDIBP	74	AI/O
P7MDIBN	75	AI/O
AVDDL	76	AP
P7MDICP	77	AI/O
P7MDICN	78	AI/O
P7MDIDP	79	AI/O
P7MDIDN	80	AI/O
AVDDH	81	AP
DVDDIO_2	82	P
RG2_TXD3/M2_TXD3/P2_RXD3/ P8LED1/GPIO8/DIS_LED	83	I/O_{PU}
RG2_TXD2/M2_TXD2/P2_RXD2/ P8LED0/GPIO9/EN_FLASH	84	I/O_{PU}
RG2_TXD1/M2_TXD1/P2_RXD1/ P7LED2/GPIO10/SPF_CLK	85	I/O_{PU}
RG2_TXD0/M2_TXD0/P2_RXD0/ P7LED0/GPIO11/SPF_SI_D0	86	I/O_{PU}
RG2_TXCTL/M2_TXEN/P2_RXDV/P7LED1/GPIO12/SPF_SO_D1	87	I/O_{PU}

Name	Pin No.	Type
RG2_TXC/M2_TXC/P2_RXC/ GPIO13	88	I/O_{PU}
RG2_RXC/M2_RXC/P2_TXC/ P6LED2/SPF_CSn/GPIO14	89	I/O_{PU}
RG2_RXCTL/M2_RXDV/P2_ TXEN/P6LED0/GPIO1/UARTRX	90	I/O_{PU}
RG2_RXD0/M2_RXD0/P2_TXD0/ P6LED1/GPIO7/UARTTX	91	I/O_{PU}
RG2_RXD1/M2_RXD1/P2_TXD1/ P5LED2/GPIO0	92	I/O_{PU}
RG2_RXD2/M2_RXD2/P2_TXD2/ P5LED0/GPIO15	93	I/O_{PU}
RG2_RXD3/M2_RXD3/P2_TXD3/ P5LED1/GPIO16	94	I/O_{PU}
DVDDL	95	P
DVDDIO_2	96	P
SVDDH	97	AP
SVDDL	98	AP
S1TXP	99	AO
S1TXN	100	AO
SGND	101	AG
S1RXP	102	AI
S1RXN	103	AI
SVDDL	104	AP
S0TXN	105	AO
S0TXP	106	AO
SVDDL	107	AP
S0RXN	108	AI
S0RXP	109	AI
SGND	110	AG
DVDDIO_1	111	P
DVDDL	112	P
P4LED2/GPIO3/DIS_SPIS	113	I/O_{PU}
RG1_RXD3/M1_RXD3/P1_TXD3/ P4LED0/GPIO17	114	I/O_{PU}
RG1_RXD2/M1_RXD2/P1_TXD2/ P4LED1/GPIO6	115	I/O_{PU}
RG1_RXD1/M1_RXD1/P1_TXD1/ P3LED1/GPIO5	116	I/O_{PU}
RG1_RXD0/M1_RXD0/P1_TXD0/ P3LED2/GPIO18	117	I/O_{PU}
RG1_RXCTL/M1_RXDV/P1_ TXEN/P3LED0	118	I/O_{PU}
RG1_RXC/M1_RXC/P1_TXC/ P2LED2	119	I/O_{PU}
RG1_TXC/M1_TXC/P1_RXC/ P2LED0	120	I/O_{PU}

Name	Pin No.	Type
RG1_TXCTL/M1_TXEN/P1_RXDV/P2LED1/GPIO4	121	I/O_{PU}
RG1_TXD0/M1_TXD0/P1_RXD0/P1LED2/SMI_SEL_1	122	I/O_{PU}
RG1_TXD1/M1_TXD1/P1_RXD1/P1LED0/MID29	123	I/O_{PU}
RG1_TXD2/M1_TXD2/P1_RXD2/P1LED1/DIS_8051	124	I/O_{PU}
RG1_TXD3/M1_TXD3/P1_RXD3/P0LED2/GPIO2/EN_PHY	125	I/O_{PU}
DVDDIO_1	126	P
DVDDL	127	P
LED_DA/P0LED1	128	I/O_{PU}
LED_CK/P0LED0/SMI_SEL_0	129	I/O_{PU}
DVDDL	130	P
XTALO	131	AO
XTALI	132	AI
nRESET	133	I_S
Slave_SPI_SS#	134	I_{PU}
SCK/MMD_MDC/Slave_SPI_SCK	135	I/O_{PU}
SDA/MMD_MDIO/Slave_SPI_SI	136	I/O_{PU}
Slave_SPI_SO/EEPROM_MOD	137	I/O_{PU}
AVDDH	138	AP
P0MDIAP	139	AI/O
P0MDIAN	140	AI/O
P0MDIBP	141	AI/O
P0MDIBN	142	AI/O
AVDDL	143	AP
P0MDICP	144	AI/O
P0MDICN	145	AI/O
P0MDIDP	146	AI/O
P0MDIDN	147	AI/O
AVDDH	148	AP
P1MDIAP	149	AI/O
P1MDIAN	150	AI/O
P1MDIBP	151	AI/O
P1MDIBN	152	AI/O
AVDDL	153	AP
P1MDICP	154	AI/O
P1MDICN	155	AI/O
P1MDIDP	156	AI/O
P1MDIDN	157	AI/O
AVDDH	158	AP
PLLVDDL0	159	AP
ATESTCK0	160	AO

Name	Pin No.	Type
PLLGND0	161	AG
AVDDH	162	AP
P2MDIAP	163	AI/O
P2MDIAN	164	AI/O
P2MDIBP	165	AI/O
P2MDIBN	166	AI/O
AVDDL	167	AP
P2MDICP	168	AI/O
P2MDICN	169	AI/O
P2MDIDP	170	AI/O
P2MDIDN	171	AI/O
AVDDH	172	AP
P3MDIAP	173	AI/O
P3MDIAN	174	AI/O
P3MDIBP	175	AI/O
P3MDIBN	176	AI/O
EPAD_GND	177	G

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	139 140 141 142 144 145 146 147	AI/O	10	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	149 150 151 152 154 155 156 157	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	163 164 165 166 168 169 170 171	AI/O	10	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	173 174 175 176 2 3 4 5	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	38 39 40 41 43 44 45 46	AI/O	10	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

Pin Name	Pin No.	Type	Drive (mA)	Description
P5MDIAP/N P5MDIBP/N P5MDICP/N P5MDIDP/N	48 49 50 51 53 54 55 56	AI/O	10	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P6MDIAP/N P6MDIBP/N P6MDICP/N P6MDIDP/N	62 63 64 65 67 68 69 70	AI/O	10	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P7MDIAP/N P7MDIBP/N P7MDICP/N P7MDIDP/N	72 73 74 75 77 78 79 80	AI/O	10	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

6.2. RGMII Interface Pins

Table 3. RGMII Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG1_RXCTL, RG2_RXCTL	118, 90	I_{PU}	-	RGMII Receive Control. The RG_RXCTL indicates RXDV at rising of RG_RXCLK and the logical derivative of RXER and RXDV at the falling edge of RG_RXCLK.
RG1_RXD[3:0] RG2_RXD[3:0]	114,115,116,117 94,93,92,91	I_{PU}	-	RGMII Receive Data Bus. In RGMII 1000Base-T mode, RXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of the RG_RXCLK and bit[7:4] presented on the falling edge of the RG_RXCLK. RXD[7:4] are ignored in this mode. In RGMII 10/100Base-T modes, the received data nibble is presented on RXD[3:0] on the rising edge of RG_RXCLK and duplicated on the falling edge of RG_RXCLK.

Pin Name	Pin No.	Type	Drive (mA)	Description
RG1_RXC, RG2_RXC	119, 89	I_{PU}	-	RGMII Receive Clock Input. Used for RG_RXD[3:0] and RG_RXCTL synchronization at both RG_RXCLK rising and falling edges. The frequency (with ±50ppm tolerance) depends on the link speed. 1000M: 125MHz 100M: 25MHz 10M: 2.5MHz
RG1_TXC, RG2_TXC	120, 88	O_{PU}	-	RGMII Transmit Clock Output. Used for RG_TXD[3:0] and RG_TXCTL synchronization at both RG_TXCLK rising and falling edges. The frequency (with ±50ppm tolerance) depends on the link speed. 1000M: 125MHz 100M: 25MHz 10M: 2.5MHz
RG1_TXD[3:0] RG2_TXD[3:0]	125,124,123,122 83,84,85,86	O_{PU}	-	RGMII Transmit Data Bus. In RGMII 1000Base-T mode, TXD[3:0] runs at a double data rate with bits[3:0] presented on the rising edge of the RG_TXCLK and bit[7:4] presented on the falling edge of the RG_TXCLK. TXD[7:4] are ignored in this mode. In RGMII 10/100Base-T modes, the transmitted data nibble is presented on TXD[3:0] on the rising edge of RG_TXCLK and duplicated on the falling edge of RG_TXCLK.
RG1_TXCTL, RG2_TXCTL	121, 87	O_{PU}	-	RGMII Transmit Control. The RG_TXCTL indicates TXEN at rising of RG_TXCLK, and the logical derivative of TXER and TXEN at the falling edge of RG_TXCLK.

6.3. MII/TMII Interface Pins

Table 4. MII/TMII Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
M1_RXDV/P1_TXEN, M2_RXDV/P2_TXEN	118,90	I_{PU}	-	1\M_RXDV Pin in TMII/MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD. M_RXDV is synchronous to M_RXC. 2\P_TXEN Pin in TMII/MII PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXC.

Pin Name	Pin No.	Type	Drive (mA)	Description
M1_RXD[3:0]/P1_TXD[3:0], M2_RXD[3:0]/P2_TXD[3:0]	114,115,116,117 94,93,92,91	I_{PU}	-	1\M_RXD[3:0] Pin in TMII/MII MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXC. 2\P_TXD[3:0] Pin in TMII/MII PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXC .
M1_RXC/P1_TXC, M2_RXC/P2_TXC	119, 89	I/O_{PU}	-	1\M_RXC Pin in TMII/MII MAC Mode. MII Receive Clock.(input) Used to synchronize M_RXD[3:0], and M_RXDV. The frequency depends on the link speed. MII:100Base-Tx→25MHz, 10Base-T→2.5MHz TMII:200Mbps→50MHz, 20Mbps→5MHz 2\P_TXC Pin in TMII/MII PHY Mode. MII Transmit Clock. (output) Used to synchronize P_TXD[3:0], and P_TXEN. It provides 25MHz clock reference at 100Base-TX, and 2.5MHz clock reference at 10Base-T. In TMII mode it provides 50MHz clock reference at 200Mbps, and 5MHz clock at 20Mbps.
M1_TXC/P1_RXC, /M2_TXC/P2_RXC	120, 88	I/O_{PU}	-	1\ M_TXC Pin in TMII/MII MAC Mode. MII Transmit Clock. (input) Used to synchronize M_TXD[3:0], and M_TXEN. The frequency depends on the link speed. MII:100Base-Tx→25MHz, 10Base-T→2.5MHz TMII:200Mbps→50MHz, 20Mbps→5MHz 2\P_RXC Pin in TMII/MII PHY Mode. MII Receive Clock. (output) Used to synchronize P_RXD[3:0], and P_RXDV. It provides 25MHz clock reference at 100Base-TX , and 2.5MHz clock reference at 10Base-T. In TMII mode it provides 50MHz clock reference at 200Mbps, and 5MHz clock at 20Mbps.
M1_TXD[3:0]/P1_RXD[3:0], M2_TXD[3:0]/P2_RXD[3:0]	125,124,123,122 83,84,85,86	O_{PU}	-	1\ M_TXD[3:0] Pin in TMII/MII MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXC in 10/100Base-TX mode. 2\ P_RXD[3:0] Pin in TMII/MII PHY Mode. MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXC.

Pin Name	Pin No.	Type	Drive (mA)	Description
M1_TXEN/P1_RXDV, M2_TXEN/P2_RXDV	121, 87	O_{PU}	-	1\M_ TXEN Pin in TMII/MII MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXC in 10/100Base-TX mode. 2\P_ RXDV Pin in TMII/MII PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_ RXDV is synchronous toP_ RXC.

6.4. RMII Interface Pins

Table 5. RMII Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
M1_RXDV/P1_TXEN, M2_RXDV/P2_TXEN	118,90	I_{PU}	-	1\CRSDV Pin in RMII MAC Mode. Carrier Sense/Receive Data Valid. This synchronous input is asserted by the PHY when the receive medium is non-idle. It is synchronous to REFCLK. 2\TXEN Pin in RMII PHY Mode. The synchronous output indicates that valid data is being driven on the P_TXD[1:0] bus. It is synchronous to REFCLK.
M1_RXD[1:0]/P1_TXD[1:0], M2_RXD[1:0]/P2_TXD[1:0]	116,117 92,91	I_{PU}	-	1\RXD[1:0] Pin in RMII MAC Mode. MII Receive Data Bus. M_RXD[1:0] is synchronous to REFCLK. 2\TXD[1:0] Pin in RMII PHY Mode. MII Transmit Data Bus. P_TXD[1:0] is synchronous to REFCLK.
M1_TXC/P1_RXC, M2_TXC/P2_RXC	120, 88	I/O_{PU}	-	REFCLK Pin in RMII Mode. This pin is bi-directional. When MAC mode, REFCLK is an input pin. When PHY mode, REFCLK outputs a 50MHz reference clock. All transmissions must be synchronized to this clock during 10/100M operation.
M1_TXD[1:0]/P1_RXD[1:0], M2_TXD[1:0]/P2_RXD[1:0]	123,122 85,86	O_{PU}	-	1\ TXD[1:0] Pin in RMII MAC Mode. MII Transmit Data Bus. M_TXD[1:0] is synchronous to REFCLK in 10/100Base-TX mode. 2\ RXD[1:0] Pin in RMII PHY Mode. MII Receive Data Bus. P_RXD[1:0] is synchronous to REFCLK.

Pin Name	Pin No.	Type	Drive (mA)	Description
M1_TXEN/P1_RXDV, M2_TXEN/P2_RXDV	121, 87	O_{PU}	-	1\TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD[1:0] bus. M_TXEN is synchronous to REFCLK. 2\CRSDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This synchronous output is asserted by the PHY when the receive medium is non-idle. It is synchronous to REFCLK.

6.5. SerDes Interface Pins

Table 6. SerDes Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
S0RXP, S0RXN	109 108	AI	-	100FX/1000Base-X/SGMII/HSGMII SerDes 0 Interface Receive Data Differential Input Pair. (When ExtMAC2 in SGMII/HSGMII or Fiber mode.)
S0TXP, S0TXN	106 105	AO	-	100FX/1000Base-X/SGMII/HSGMII SerDes 0 Interface Transmit Data Differential Output Pair. (When ExtMAC2 in SGMII/HSGMII or Fiber mode.)
S1RXP, S1RXN	102 103	AI	-	100FX/1000Base-X/SGMII SerDes 1 Interface Receive Data Differential Input Pair. (When ExtMAC1 in SGMII or Fiber mode.)
S1TXP, S1TXN	99 100	AO	-	100FX/1000Base-X/SGMII SerDes 1 Interface Transmit Data Differential Output Pair. (When ExtMAC1 in SGMII or Fiber mode.)

6.6. Parallel LED Pins

Table 7. Parallel LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P9LED2	28	O_{PU}	-	Port 9 Parallel LED LED2 Output Signal. P7LED2 indicates information is defined by register or EEPROM.
P9LED1	27	O_{PU}	-	Port 9 Parallel LED LED1 Output Signal. P7LED1 indicates information is defined by register or EEPROM.
P9LED0	26	O_{PU}	-	Port 9 Parallel LED LED0 Output Signal. P7LED0 indicates information is defined by register or EEPROM.
P8LED2	29	O_{PU}	-	Port 8 Parallel LED LED2 Output Signal. P7LED2 indicates information is defined by register or EEPROM.
P8LED1	83	O_{PU}	-	Port 8 Parallel LED LED1 Output Signal. P7LED1 indicates information is defined by register or EEPROM.

Pin Name	Pin No.	Type	Drive (mA)	Description
P8LED0	84	O_{PU}	-	Port 8 Parallel LED LED0 Output Signal. P7LED0 indicates information is defined by register or EEPROM.
P7LED2	85	O_{PU}	-	Port 7 Parallel LED LED2 Output Signal. P7LED2 indicates information is defined by register or EEPROM.
P7LED1	87	O_{PU}	-	Port 7 Parallel LED LED1 Output Signal. P7LED1 indicates information is defined by register or EEPROM.
P7LED0	86	O_{PU}	-	Port 7 Parallel LED LED0 Output Signal. P7LED0 indicates information is defined by register or EEPROM.
P6LED2	89	O_{PU}	-	Port 6 Parallel LED LED2 Output Signal. P6LED2 indicates information is defined by register or EEPROM.
P6LED1	91	O_{PU}	-	Port 6 Parallel LED LED1 Output Signal. P6LED1 indicates information is defined by register or EEPROM.
P6LED0	90	O_{PU}	-	Port 6 Parallel LED LED0 Output Signal. P6LED0 indicates information is defined by register or EEPROM.
P5LED2	92	O_{PU}	-	Port 5 Parallel LED LED2 Output Signal. P5LED2 indicates information is defined by register or EEPROM.
P5LED1	94	O_{PU}	-	Port 5 Parallel LED LED1 Output Signal. P5LED1 indicates information is defined by register or EEPROM.
P5LED0	93	O_{PU}	-	Port 5 Parallel LED LED0 Output Signal. P5LED0 indicates information is defined by register or EEPROM.
P4LED2	113	O_{PU}	-	Port 4 Parallel LED LED2 Output Signal. P4LED2 indicates information is defined by register or EEPROM.
P4LED1	115	O_{PU}	-	Port 4 Parallel LED LED1 Output Signal. P4LED1 indicates information is defined by register or EEPROM.
P4LED0	114	O_{PU}	-	Port 4 Parallel LED LED0 Output Signal. P4LED0 indicates information is defined by register or EEPROM.
P3LED2	117	O_{PU}	-	Port 3 Parallel LED LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM.
P3LED1	116	O_{PU}	-	Port 3 Parallel LED LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM.
P3LED0	118	O_{PU}	-	Port 3 Parallel LED LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM.
P2LED2	119	O_{PU}	-	Port 2 Parallel LED LED2 Output Signal. P2LED2 indicates information is defined by register or EEPROM.
P2LED1	121	O_{PU}	-	Port 2 Parallel LED LED1 Output Signal. P2LED1 indicates information is defined by register or EEPROM.
P2LED0	120	O_{PU}	-	Port 2 Parallel LED LED0 Output Signal. P2LED0 indicates information is defined by register or EEPROM.
P1LED2	122	O_{PU}	-	Port 1 Parallel LED LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM.
P1LED1	124	O_{PU}	-	Port 1 Parallel LED LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM.
P1LED0	123	O_{PU}	-	Port 1 Parallel LED LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM.

Pin Name	Pin No.	Type	Drive (mA)	Description
P0LED2	125	O_{PU}	-	Port 0 Parallel LED LED2 Output Signal. P0LED2 indicates information is defined by register or EEPROM.
P0LED1	128	O_{PU}	-	Port 0 Parallel LED LED1 Output Signal. P0LED1 indicates information is defined by register or EEPROM.
P0LED0	129	O_{PU}	-	Port 0 Parallel LED LED0 Output Signal. P0LED0 indicates information is defined by register or EEPROM.

6.7. Serial Mode LED Pins

Table 8. Serial Mode LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_CK	129	O_{PU}	-	Serial Mode LED Clock Signal.
LED_DA	128	O_{PU}	-	Serial Mode LED Data Signal.

6.8. SPI FLASH Interface Pins

Table 9. SPI FLASH Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SPF_CSn	89	O_{PU}	-	SPI FLASH chip select signal.
SPF_SO_D1	87	I/O_{PU}	-	In Serial I/O Mode SPI Serial FLASH Serial Data Output (RTL8370 MB input pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is MSB)
SPF_SI_D0	86	I/O_{PU}	-	In Serial I/O Mode SPI Serial FLASH Serial Data Input (RTL8370 MB output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
SPF_CLK	85	O_{PU}	-	SPI FLASH Clock.
GPIO_E/SPF_CSn	33	O_{PU}	-	SPI FLASH chip select signal.
GPIO_D/SPF_SO_D1	32	I/O_{PU}	-	In Serial I/O Mode SPI Serial FLASH Serial Data Output (RTL8370 MB input pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is MSB)
GPIO_C/SPF_SI_D0	31	I/O_{PU}	-	In Serial I/O Mode SPI Serial FLASH Serial Data Input (RTL8370MB output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
GPIO_B/SPF_CLK	30	O_{PU}	-	SPI FLASH Clock.

Note: When strapping SPF_MUX_SEL pulls down SPI FLASH interface position is pin 30\31\32\33, else is pin 89\87\86\85.

6.9. UART Interface Pins

Table 10. UART Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
UARTRX	90	I_{PU}	-	UART Rx Input Signal.
UARTTX	91	O_{PU}	-	UART Tx Output Signal.

6.10. CPU Interface Pins

Table 11. CPU Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
Slave_SPI_SS#	134	I_{PU}	-	SPI slave Mode Chip Select Input.
SCK/MMD_MDC/Slave_SPI_SCK	135	I/O_{PU}	-	1\EEPROM auto load mode serial clock output 2\I2C slave mode serial clock input 3\MDC/MDIO slave mode serial clock input 4\ SPI slave Mode serial clock input
SDA/MMD_MDIO/Slave_SPI_SI	136	I/O_{PU}	-	1\EEPROM auto load mode serial data input 2\I2C slave mode serial data (bidirectional) 3\MDC/MDIO slave mode serial data (bidirectional) 4\ SPI slave Mode serial data input
Slave_SPI_SO	137	O_{PU}	-	SPI slave Mode serial data output

6.11. GPIO Interface Pins

Table 12. GPIO Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
GPIO0	92	I/O_{PU}	-	General Purpose Input/Output Interfaces IO0.
GPIO1	90	I/O_{PU}	-	General Purpose Input/Output Interfaces IO1.
GPIO2	125	I/O_{PU}	-	General Purpose Input/Output Interfaces IO2.
GPIO3	113	I/O_{PU}	-	General Purpose Input/Output Interfaces IO3.
GPIO4	121	I/O_{PU}	-	General Purpose Input/Output Interfaces IO4.
GPIO5	116	I/O_{PU}	-	General Purpose Input/Output Interfaces IO5.
GPIO6	115	I/O_{PU}	-	General Purpose Input/Output Interfaces IO6.
GPIO7	91	I/O_{PU}	-	General Purpose Input/Output Interfaces IO7.
GPIO8	83	I/O_{PU}	-	General Purpose Input/Output Interfaces IO8
GPIO9	84	I/O_{PU}	-	General Purpose Input/Output Interfaces IO9.
GPIO10	85	I/O_{PU}	-	General Purpose Input/Output Interfaces IO10.
GPIO11	86	I/O_{PU}	-	General Purpose Input/Output Interfaces IO11.
GPIO12	87	I/O_{PU}	-	General Purpose Input/Output Interfaces IO12.
GPIO13	88	I/O_{PU}	-	General Purpose Input/Output Interfaces IO13.
GPIO14	89	I/O_{PU}	-	General Purpose Input/Output Interfaces IO14.
GPIO15	93	I/O_{PU}	-	General Purpose Input/Output Interfaces IO15.
GPIO16	94	I/O_{PU}	-	General Purpose Input/Output Interfaces IO16.
GPIO17	114	I/O_{PU}	-	General Purpose Input/Output Interfaces IO17.
GPIO18	117	I/O_{PU}	-	General Purpose Input/Output Interfaces IO18.
GPIO_A	24	I/O_{PU}	-	General Purpose Input/Output Interfaces IO_A.
GPIO_B	30	I/O_{PU}	-	General Purpose Input/Output Interfaces IO_B
GPIO_C	31	I/O_{PU}	-	General Purpose Input/Output Interfaces IO_C.
GPIO_D	32	I/O_{PU}	-	General Purpose Input/Output Interfaces IO_D.
GPIO_E	33	I/O_{PU}	-	General Purpose Input/Output Interfaces IO_E.

6.12. Configuration Strapping Pins

Table 13. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
Slave_SPI_SO/EEPROM_MOD	137	I/O$_{PU}$	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16). *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.*
P9LED0/EN_PWRLIGHT	26	I/O$_{PU}$	Enable Power On Light. Pull Up: Enable Power On Light Pull Down: Disable Power On Light. *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
RG2_TXD2/M2_TXD2/P2_RXD2/P8LED0/GPIO9/EN_FLASH	84	I/O$_{PU}$	Enable SPI FLASH Interface. Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface *Note 1: The strapping pin DISAUTOLOAD, DIS_8051, and EN_SPIF are for power on or* reset initial stage configuration. (Refer to *Table 14. Configuration Strapping Pins Configuration Note.*) *Note 2: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
RG1_TXD2/M1_TXD2/P1_RXD2/P1LED1/DIS_8051	124	I/O$_{PU}$	Disable Embedded 8051. Pull Up: Disable embedded 8051 upon power on or reset Pull Down: Enable embedded 8051 upon power on or reset *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
P9LED1/DISAUTOLOAD	27	I/O$_{PU}$	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset *Note1: When DIS_8051=1 and DISAUTOLOAD=0, the EEPROM data will be treat as register configuration data upon power on or reset initial stage. When DIS_8051 = 0 and DISAUTOLOAD =0, the EEPROM data will be loaded to embedded 8051 instruction memory upon power on or reset.* *Note2: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*

Pin Name	Pin No.	Type	Description
RG1_TXD0/M1_TXD0/P1_RXD0/P1LED2/SMI_SEL_1	122	I/O$_{PU}$	Slave I2C/Slave MII Management Interface Selection 1. Slave I2C/Slave MII Management Interface Selection 0. [SMI_SEL_1, SMI_SEL_0] 00：LSB I2C 01：MSB I2C 10：MDC/MDIO 11：RTK I2C *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
LED_CK/P0LED0/SMI_SEL_0	129	I/O$_{PU}$	
P4LED2/GPIO3/DIS_SPIS	113	I/O$_{PU}$	Disable SPI Slave Interface for External CPU Access RTL8370MB Register Pull Up: Disable SPI Slave Interface and refer [SMI_SEL_1, SMI_SEL_0] Pull Down: Enable SPI Slave Interface *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.*
RG1_TXD1/M1_TXD1/P1_RXD1/P1LED0/MID29	123	I/O$_{PU}$	Slave SMI (MDC/MDIO) Device Address. Pull Up: Slave SMI (MDC/MDIO) Device Address is d’29 Pull Down: Slave SMI (MDC/MDIO) Device Address is 0 *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
RG1_TXD3/M1_TXD3/P1_RXD3/P0LED2/GPIO2/EN_PHY	125	I/O$_{PU}$	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset..* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
P9LED2/EEE_EN	28	I/O$_{PU}$	Enable 802.3az EEE. Pull Up: Enable 802.3az EEE. Pull Down: Disable 802.3az EEE. *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.
GPIO_A/SPF_MUX_SEL	24	I/O$_{PU}$	SPI FLASH Interface Position Select. Pull Up: Select Spi-Flash-1 pin 89\87\86\85. Pull Down: Select Spi-Flash-2 pin 30\31\32\33. *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.*

Pin Name	Pin No.	Type	Description
RG2_TXD3/M2_TXD3/P2_RXD3/P8LED1/GPIO8/DIS_LED	83	I/O$_{PU}$	Disable/Enable LED function When Powered On. Pull Down: Enable LED Pull Up: Disable LED. *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
BUZZER/DIS_LPD	20	I/O$_{PU}$	Realtek Loop Detection Configuration. Pull Up: Disable Loop detection function Pull Down: Enable Loop detection function 2KHz signal out when looping is detected *Note: Pull high or low via an external 4.7k ohm resistor upon power on or reset.*

Table 14. Configuration Strapping Pins Configuration Note

DISAUTOLOAD	DIS_8051	EN_FLASH	Initial Stage (Power On or Reset) Loading Data	
			From	To
0	0	0	EEPROM	Embedded 8051 Instruction Memory
0	0	1	FLASH	Embedded 8051 Instruction Memory
0	1	0	EEPROM	Register
1	Irrelevant	Irrelevant	No Action	No Action

6.13. Miscellaneous Pins

Table 15. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
XTALI	132	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/-50ppm tolerance crystal reference or oscillator input.
XTALO	131	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.
MDIREF	10	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
NC	7,9,11	-	Not connect. Must be left floating in normal operation.
SCK/MMD_MDC/Slave_SPI_SCK	135	I/O	Master I2C Interface Clock for EEPROM auto download Slave I2C Interface Clock for external CPU to access DUT Slave MII Management Interface Clock (selected via hardware strapping SMI_SEL1 & SMI_SEL0).
SDA/MMD_MDIO/Slave_SPI_SI	136	I/O	Master I2C Interface Data for EEPROM auto download Slave I2C Interface Data for external CPU to access DUT Slave MII Management Interface Data (selected via hardware strapping SMI_SEL1 & SMI_SEL0).
nRESET	133	$I_{S/PU}$	System Reset Input Pin. When low active will reset the RTL8370MB.
INT	19	I/O_{PU}	Interrupt Output for External CPU.
RESERVED1	21	I_{PD}	Reserved. This pin must be pulled low via an external 4.7k ohm resistor upon power on.
RESERVED2	22	I/O_{PD}	Reserved. This pin must be pulled low via an external 4.7k ohm resistor upon power on.
RESERVED3	23	I/O_{PD}	Reserved. This pin must be pulled low via an external 4.7k ohm resistor upon power on.
RESERVED4	25	I/O_{PU}	Reserved. This pin must be left floating in normal operation.
GPIO8	83	O_{PU}	Group1 Master I2C - SCK
GPIO9	84	I/O_{PU}	Group1 Master I2C - SDA
GPIO15	93	O_{PU}	Group2 Master I2C - SCK
GPIO16	94	I/O_{PU}	Group2 Master I2C - SDA
P9LED2/EEE_EN	28	O_{PU}	Group3 Master I2C - SCK
P8LED2	29	I/O_{PU}	Group3 Master I2C - SDA

Note 1: Group1/2/3 Master I2C can be used to connect PoE controller and SFP.
Note 2: Time-sharing is applied in the design of three Master I2C Groups. Only one group may be operated at a time.

6.14. Test Pins

Table 16. Test Pins

Pin Name	Pin No.	Type	Description
ATESTCK0	160	AO	Reserved for Internal Use. Must be left floating.
ATESTCK1	59	AO	Reserved for Internal Use. Must be left floating.
RTT1	13	AO	Reserved for Internal Use. Must be left floating.
RTT2	14	AI	Reserved for Internal Use. Must be left floating.

6.15. Power and GND Pins

Table 17. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO	16,36	P	Digital I/O High Voltage Power.
DVDDIO_1	111,126	P	Digital I/O High Voltage Power for Extension Port 1 General Purpose Interfaces.
DVDDIO_2	82,96	P	Digital I/O High Voltage Power for Extension Port 2 General Purpose Interfaces.
DVDDL	17,18,34,35,95,112, 127,130	P	Digital Low Voltage Power.
AVDDH	6,15,37,47,57,61,71, 81,138,148,158,162, 172	AP	Analog High Voltage Power.
AVDDL	1,12,42,52,66,76,14 3,153,167	AP	Analog Low Voltage Power.
SVDDL	98,104,107	AP	SerDes Low Voltage Power.
SVDDH	97	AP	SerDes High Voltage Power.
PLLVDDL0	159	AP	PLL0 Low Voltage Power.
PLLVDDL1	58	AP	PLL1 Low Voltage Power.
GND	EPAD_GND	G	GND.
AGND	8	AG	Analog GND.
SGND	101,110	AG	SerDes GND.
PLLGND0	161	AG	PLL0 GND.
PLLGND1	60	AG	PLL1 GND.

7. Physical Layer Functional Overview

7.1. MDI Interface

The RTL8370MB embeds eight Gigabit Ethernet PHYs. The Gigabit Ethernet PHY uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

7.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

7.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error

rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.8. Auto-Negotiation for UTP

The RTL8370MB obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8370MB advertises full capabilities (1000Full-only Giga PHY, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.9. Crossover Detection and Auto Correction

The RTL8370MB automatically determines whether or not it needs to crossover between pairs (see Table 18) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8370MB automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 18. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

7.10. Polarity Correction

The RTL8370MB automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

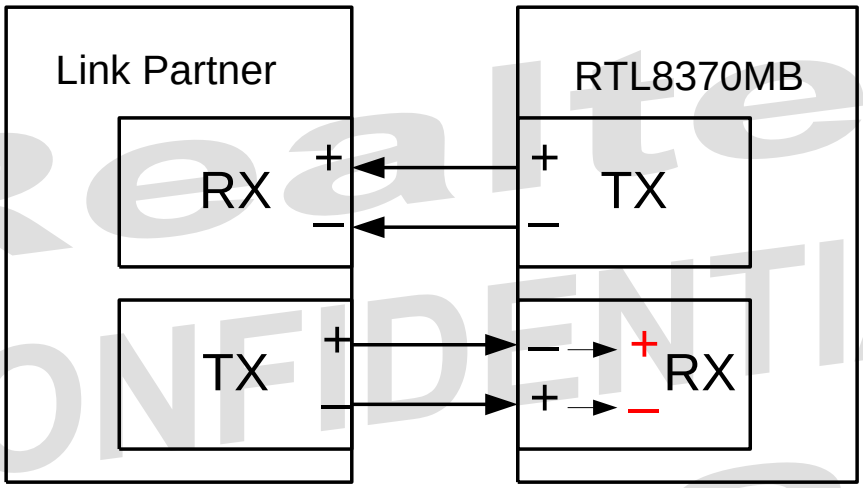


Figure 8. Conceptual Example of Polarity Correction

8. General Function Description

8.1. Reset

8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8370MB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

8.1.2. Software Reset

The RTL8370MB supports two software resets; a chip reset and a soft reset.

8.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

8.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will clear the FIFO and re-start the packet buffer link list.

8.2. IEEE 802.3x Full Duplex Flow Control

The RTL8370MB supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

8.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "truncated binary exponential backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8370MB is 10.

The half duplex back-off algorithm in the RTL8370MB does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

8.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8370MB sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL8370MB supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

8.4. Search and Learning

Search

When a packet is received, the RTL8370MB uses the destination MAC address, Filtering Identifier (FID) and enhanced Filtering Identifier (FID) to search the 4096-entry look-up table. The 48-bit MAC address, 4-bit FID and 3-bit EFID use a hash algorithm to calculate an 12-bit index value. The RTL8370MB uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8370MB uses the source MAC address, FID, and EFID of the incoming packet to hash into a 12-bit index. It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8370MB will update the entry with new information. If

there is no match and the 4096 entries are not all occupied by other MAC addresses, the RTL8370MB will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

The RTL8370MB supports a 64-entry Content Addressable Memory (CAM) to avoid look-up table hash collisions. When all 4096 entries in the look-up table index are occupied, the source MAC address can be learned into the 64-entry CAM. If both the look-up table and the CAM are full, the source MAC address will not be learned in the RTL8370MB.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8370MB is between 200 and 400 seconds (typical is 300 seconds).

8.5. SVL and IVL/SVL

The RTL8370MB supports a 4K-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

8.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8370MB. The maximum packet length may be set to 1522, 1536, 1552, or 16K bytes.

8.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8370MB supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 19 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 19. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
All LANs Bridge Management Group Address	01-80-C2-00-00-10

Assignment	Value
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined 802.1 Bridge Address	01-80-C2-00-00-04 | 01-80-C2-00-00-0F
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F

8.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8370MB enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate, all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

8.9. Port Security Function

The RTL8370MB supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

8.10. MIB Counters

The RTL8370MB supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

8.11. Port Mirroring

The RTL8370MB supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored from a mirror port.

8.12. VLAN Function

The RTL8370MB supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to 'admit all' , 'admit untagged only', and 'admit tagged only'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8370MB will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8370MB also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8370MB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8370MB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

8.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8370MB provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

8.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8370MB supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8370MB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8370MB compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When ‘802.1Q tag aware VLAN’ is enabled, the RTL8370MB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If ‘802.1Q tag aware VLAN’ is disabled, the RTL8370MB performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when ‘802.1Q tag aware VLAN’ is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8370MB. One is the ‘VLAN tag admit control’. The other is ‘VLAN member set ingress filtering’, which will drop frames if the ingress port is not in the member set.

8.12.3. Protocol-Based VLAN

The RTL8370MB supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 9. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be ‘Ethernet’ and value to be ‘0x0800’. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

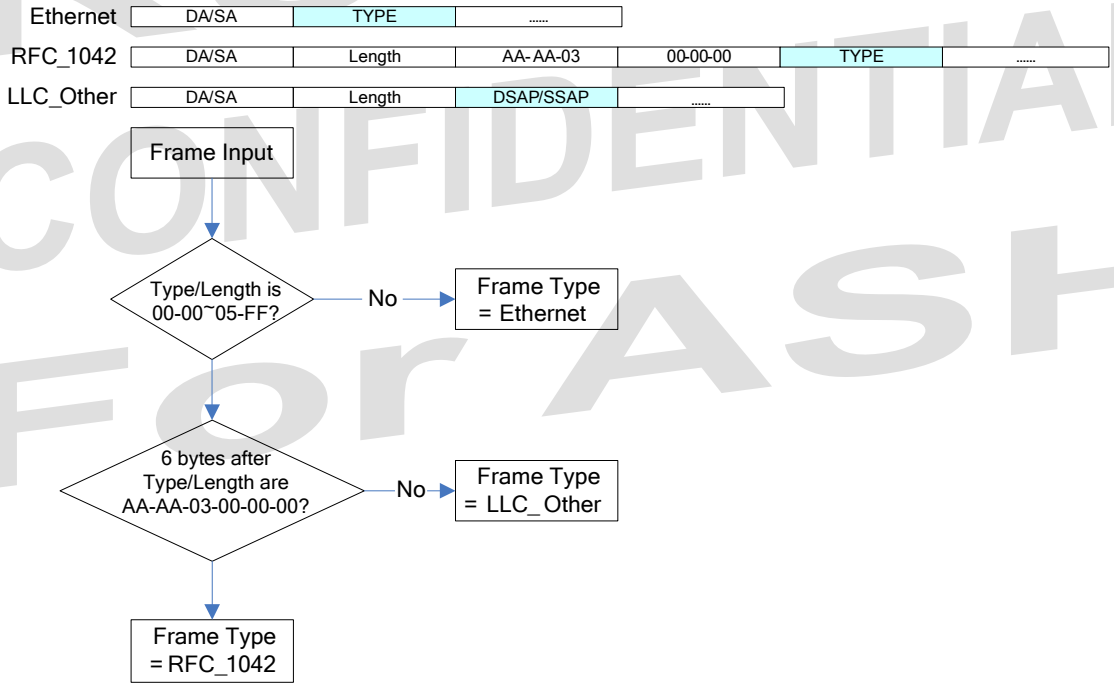


Figure 9. Protocol-Based VLAN Frame Format and Flow Chart

8.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8370MB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8370MB will drop non-tagged packets and packets with an incorrect PVID.

8.13. QoS Function

The RTL8370MB supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8370MB, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

8.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

8.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8370MB can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8370MB identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

8.13.3. Priority Queue Scheduling

The RTL8370MB supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- APR leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 10 shows the RTL8370MB packet-scheduling diagram.

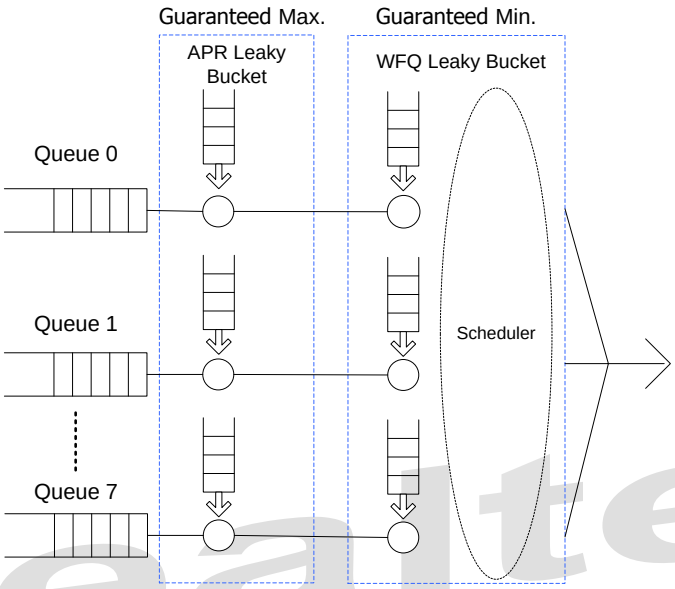


Figure 10. RTL8370MB MAX-MIN Scheduling Diagram

8.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8370MB supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. Each output queue has a 3-bit 802.1p/Q, and a 6-bit IP DSCP value configuration register.

8.13.5. ACL-Based Priority

The RTL8370MB supports 96-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

8.14. IGMP & MLD Snooping Function

The RTL8370MB supports IGMP v1/v2/v3 and MLD v1/v2 snooping. The RTL8370MB can trap all IGMP and MLD packets to the CPU port. The CPU processes these packets, gets the IP multicast group information of all ports, and writes the correct multicast entry to the lookup table via EEPROM SMI.

8.15. IEEE 802.1x Function

The RTL8370MB supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior
- Guest VLAN

8.15.1. Port-Based Access Control

Each port of the RTL8370MB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

8.15.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

8.15.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

8.15.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

8.15.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction must be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

8.15.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

8.15.7. Guest VLAN

When the RTL8370MB enables the Port-based or MAC-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, the RTL8370MB will drop all packets from this port.

The RTL8370MB also supports one Guest VLAN to allow unauthorized ports or packets to be forwarded to a limited VLAN domain. The user can configure one VLAN ID and member set for these unauthorized packets.

8.16. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8370MB supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8370MB also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

8.17. Embedded 8051

An 8051 MCU is embedded in the RTL8370MB to support management functions. The 8051 MCU can access all of the registers in the RTL8370MB through the internal bus. With the Network Interface Circuit (NIC) acting as the data path, the 8051 MCU connects to the switch core and can transmit frames to or receive frames from the Ether network. The features of the 8051 MCU are listed below:

- 256 Bytes fast internal RAM
- On-chip 48K data memory
- On-chip 16K code memory
- Supports code-banking

- 12KBytes NIC buffer
- EEPROM read/write ability

8.18. Realtek Cable Test (RTCT)

The RTL8370MB physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair. The RTL8370MB also provides LED support to indicate test status and results.

8.19. LED Indicator

The RTL8370MB supports parallel and serial mode LEDs for each port. Each pin may have different indicator information (defined in Table 20). Upon reset, the RTL8370MB supports chip diagnostics and LED operation test by blinking all LEDs once. LED0 group default indicate Link/Act, LED1 group default indicate Spd1000, LED2 group default indicate Spd100.

Table 20. LED Definitions

LED Statuses	Description
LED_Off	LED pin Output disable.
Dup/Col	Duplex/Collision, Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

8.19.1. Parallel LED Mode

The RTL8370MB supports parallel LED mode. Each port has three LED indicator pins. The parallel LED pin also supports pin strapping configuration functions. The PnLED0, PnLED1, and PnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is pulled high upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. For details refer to Figure 11 and Figure 12. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The PnLED1 can be combined with PnLED0 or PnLED2 as a Bi-color LED.

LED_PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

- P0LED1 should pull up upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- P0LED1 should be pulled down upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

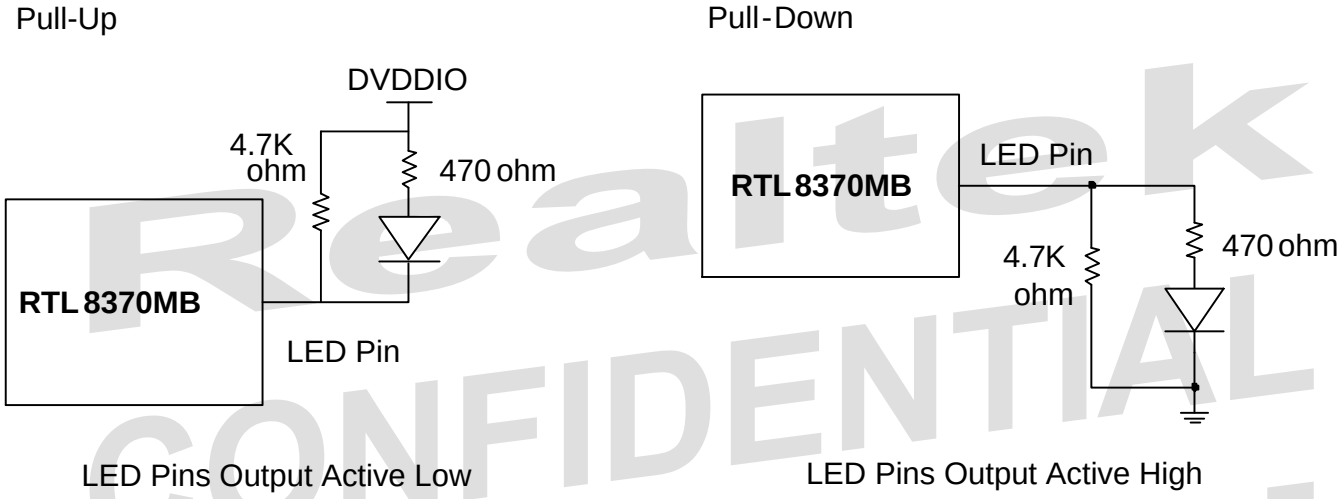


Figure 11. Pull-Up and Pull-Down of LED Pins for Single-Color LED

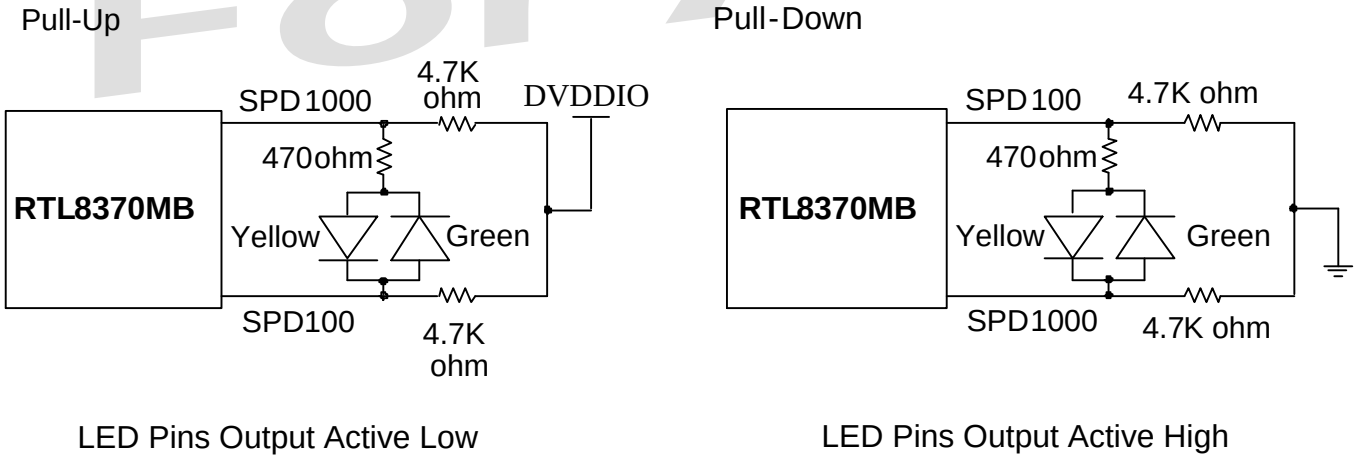


Figure 12. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

8.19.2. Serial LED Mode

The RTL8370MB supports serial shift LED mode to show the speed, link status and other information of the port status. The parallel LED pins are shared with EXT1 RGMII/GPIO and so on, if work in these modes, the serial LED mode can be used to show port status. In serial mode each port supports up to three LED indicator pins, LED0, LED1, and LED2.

8.19.2.1 Serial Shift LED Default Mode; Per-Port Three Single-Color LED

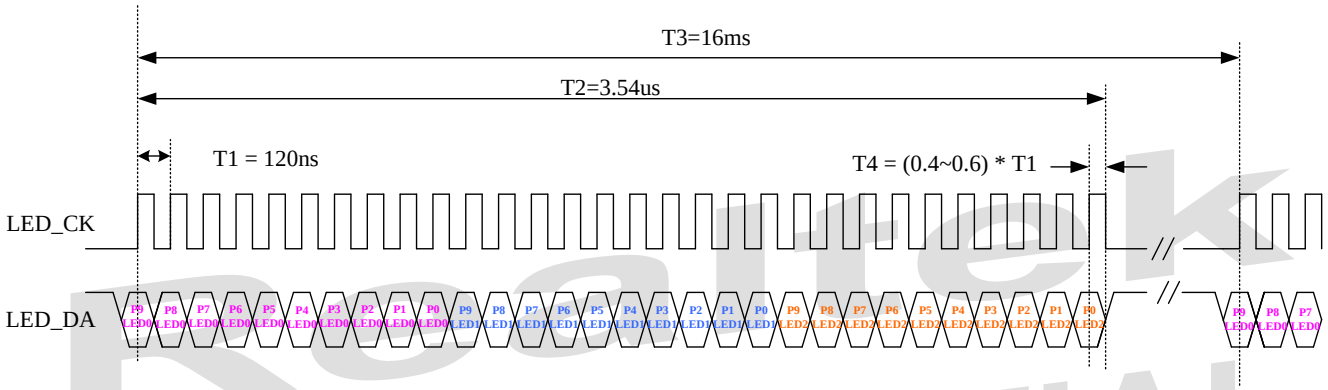


Figure 13. Serial Shift LED Default Mode; Per-Port Three Single-Color LED

A 74HC164 8-Bit Serial-In, Parallel-Out Shift Register captures the per-port link status and diagnostic information. The related circuit design is shown in the following diagram.

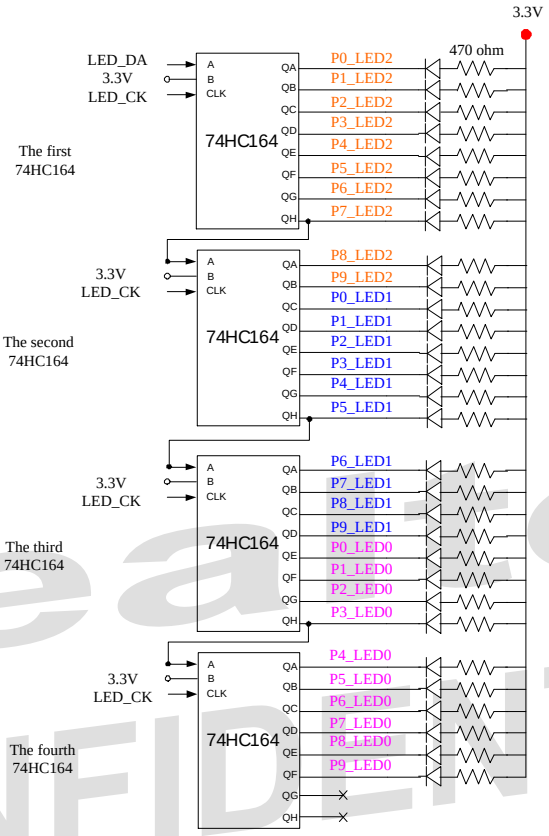


Figure 14. RTL8370MB+74HC164 Serial LED Connection Diagram (Per-Port Three Single-Color LED)

The RTL8231 shift register mode could reserve the serial data, and output parallel data in order. There are 36 shift registers in the RTL8231. The output data sequence is shown below:

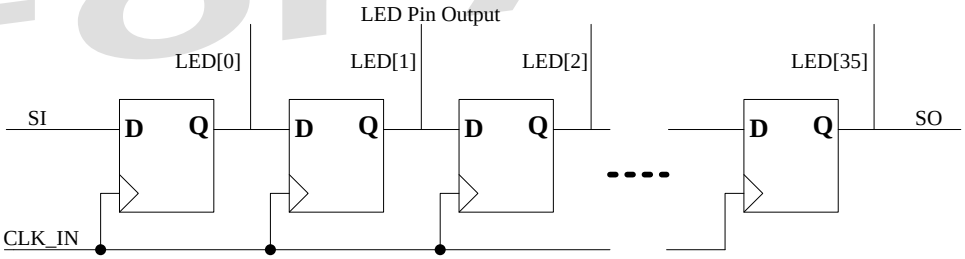


Figure 15. RTL8231 Output Data Sequence

Current serial data is received at the SI pin and shifts the preceding data to the next stage at each rising edge of the serial clock. The first serial data input to the RTL8231 is output from the pin 15 LED[0]. At the last shift register, the serial data is output to the LED[35] pin and the SO pin at the same time.

The strapping pins configuration of RTL8231 in Shift Register Mode is shown in Table 21.

Table 21. RTL8231 Shift Register Mode Strapping Pins Configuration

Pin Name	Pin Num	Type	Description	Configuration for serial LED mode
LED[0]/ Dis_SMI	15	I/O_{PD}	Select RTL8231 in the SMI mode or Shift Register mode. 0: SMI mode.(default) 1: Shift register mode.	Pull high
SO/MOD[1]	16	I/O	MOD[1:0] defines the parallel output initial value after finish reset. 2b'00: LED[15] initial high, others parallel output initial low. 2b'01: all parallel output initial high. 2b'10: LED[0] initial high, others parallel output initial low. 2b'11: LED[15] initial low, others parallel output initial high.	Pull low
LED[15]/ MOD[0]	42	I/ O_{PU}		Pull high

The related circuit design is shown in the following figure.

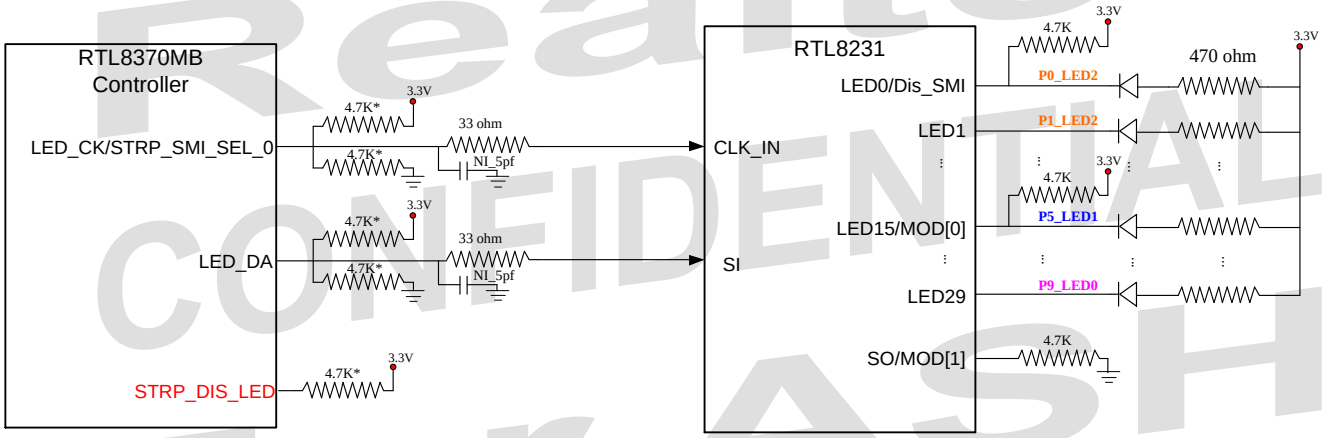


Figure 16. RTL8370MB+RTL8231 Serial LED Connection Diagram (Per-Port Three Single-Color LED)

Note: A 4.7K ohm pull up or pull down resistor maybe used for proper strapping configuration.

8.19.2.2 RTL8370MB Serial Shift LED; Per-Port Two Single-Color LED

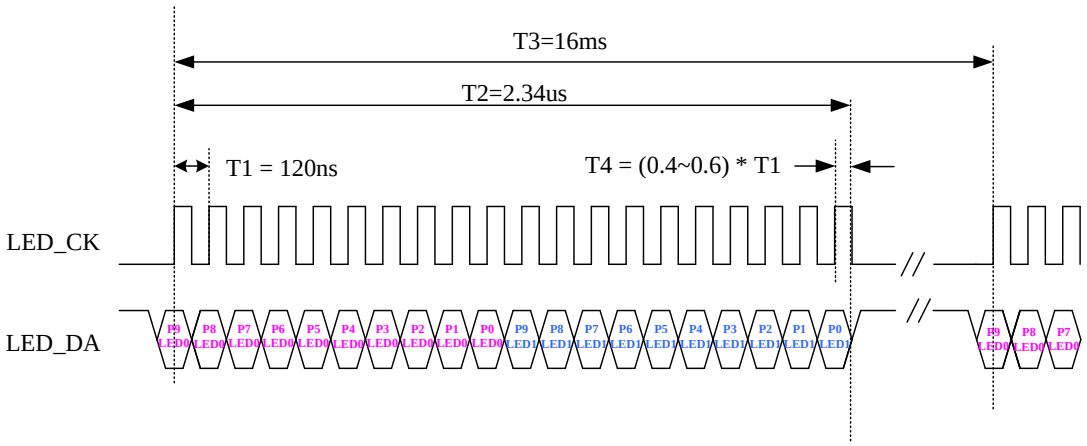


Figure 17. RTL8370MB Serial Shift LED; Per-Port Two Single-Color LED

8.19.2.3 RTL8370MB Serial Shift LED; Per-Port One Single-Color LED

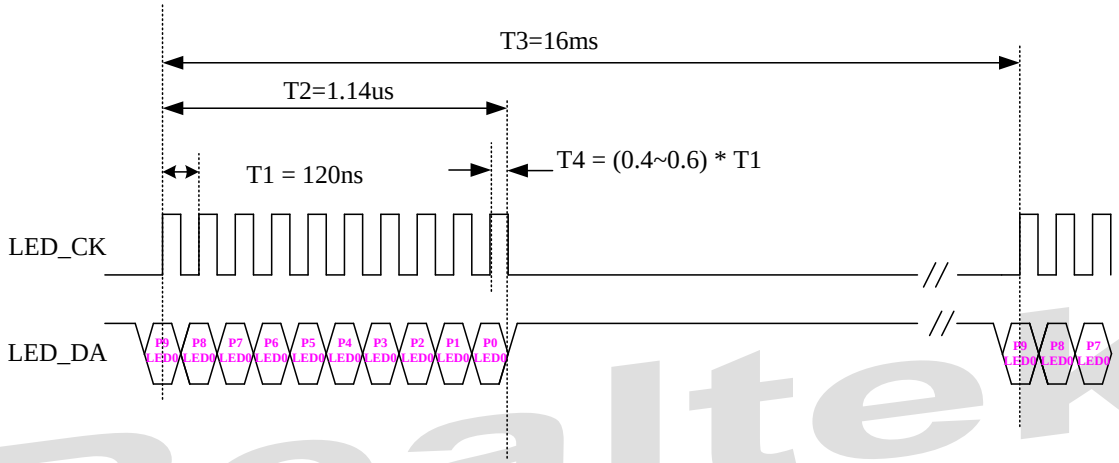


Figure 18. RTL8370MB Serial Shift LED; Per-Port One Single-Color LED

8.20. Green Ethernet

8.20.1. Link-On and Cable Length Power Saving

The RTL8370MB provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

8.20.2. Link-Down Power Saving

The RTL8370MB implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

8.21. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8370MB support IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation, and 10Base-T in full/half duplex mode.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access

Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 10Base-T, EEE defines a 10Mbps PHY (10Base-Te) with reduced transmit amplitude requirements. 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of class-D (Cat-5) cable

The RTL8370MB MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

8.22. Interrupt Pin for External CPU

The RTL8370MB provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the RTL8370MB will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

9. Interface Descriptions

9.1. I2C Master for EEPROM Auto-load

The EEPROM interface of the RTL8370MB uses the serial bus I2C to read the Serial EEPROM. When the RTL8370MB is powered up, it drives SCK and SDA to read the configuration/code data from the EEPROM by strapping configuration.

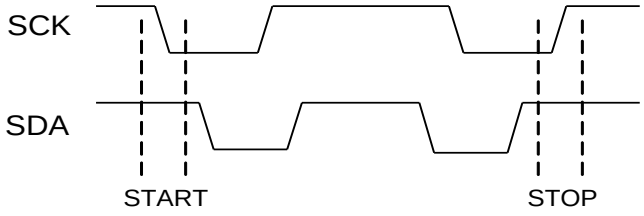


Figure 19. I2C Start and Stop Command

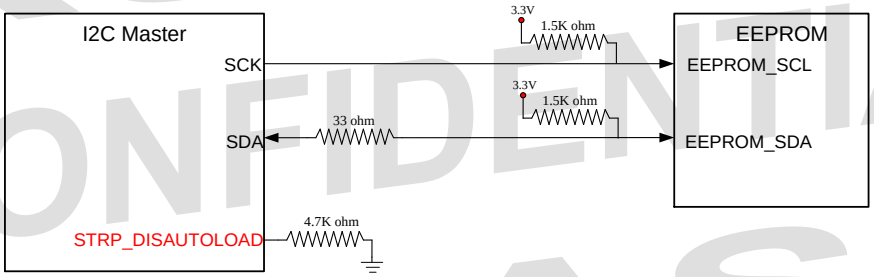


Figure 20. I2C Master for EEPROM Auto-load Interface Connection Example

The EEPROM can be divided into two sizes: 2Kb~8Kb and 32Kb~512Kb. The address of the small size EEPROM is 8-bits, however the larger EEPROM has word-high addressing and word-low addressing, and it is 16-bits (two bytes). The RTL8370MB supports these two types of EEPROM.

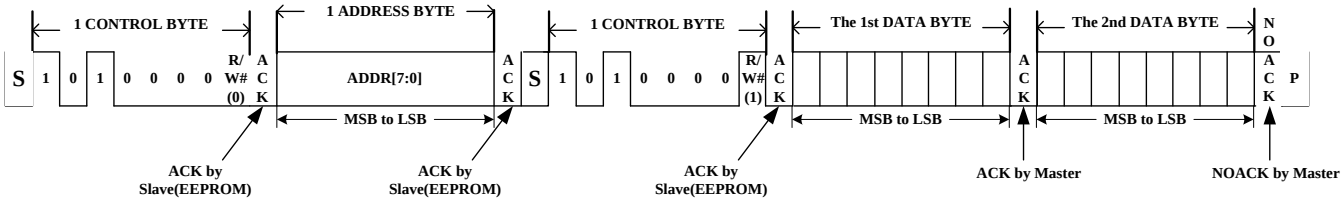


Figure 21. 8-Bit EEPROM Sequential Read

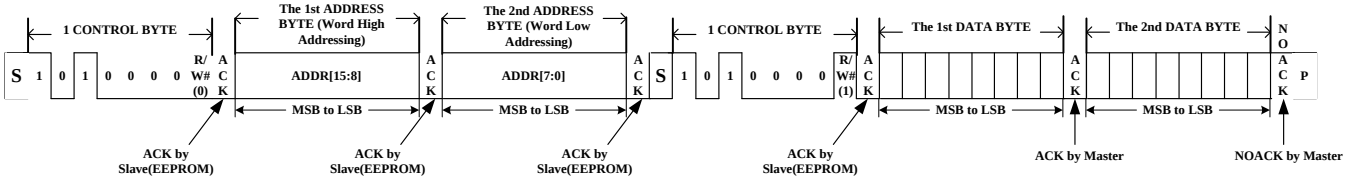


Figure 22. 16-Bit EEPROM Sequential Read

9.2. I2C-Like Slave Interface for External CPU to Access the RTL8370MB

When EEPROM auto-load is complete, the RTL8370MB registers can be accessed via SCK and SDA (I2C-Like) via an external CPU (Decided by Strapping Configuration).

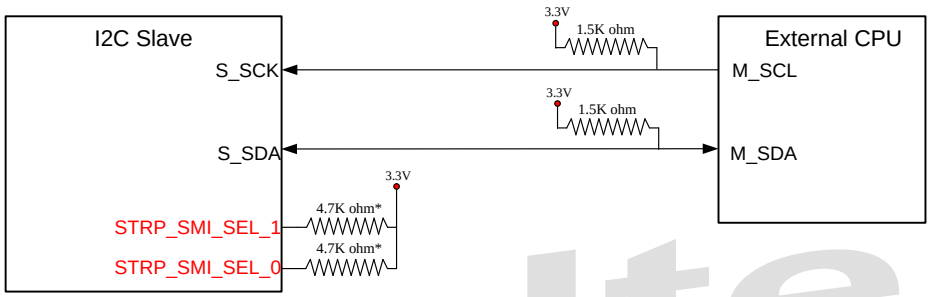


Figure 23. I2C-Like Slave for External CPU Access Interface Connection Example

Note: For the RTL8370MB, the Strapping STRP_DIS_SPIS should be kept floating or pulled up by a 4.7K ohm Resistor.

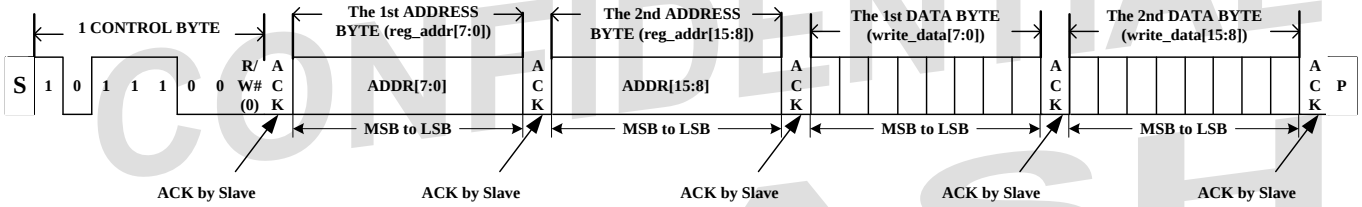


Figure 24. I2C-Like Slave Interface Write Command

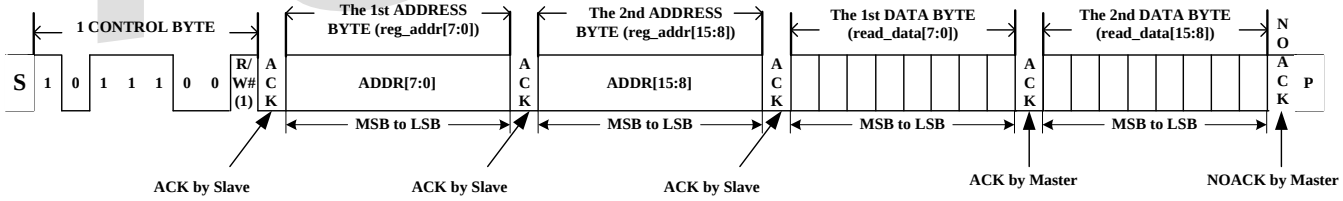


Figure 25. I2C-Like Slave Interface Read Command

9.3. Slave MII Management SMI Interface for External CPU to Access RTL8370MB

The RTL8370MB registers can be accessed via Slave MDC and MDIO via an external CPU (Decided by Strapping Configuration).

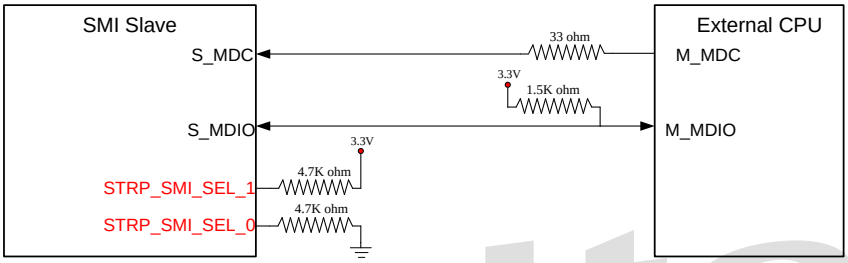


Figure 26. Slave MII Management SMI Interface Connection Example

Note: For the RTL8370MB, the Strapping STRP_DIS_SPIS should be kept floating or pulled up by a 4.7K ohm Resistor.

Table 22. Slave MII Management SMI Access Format

	Management Frame Fields							
	PRE	**ST**	**OP**	**DEVAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note: By default, a Slave needs no less than 32bit Preambles (PRE) for accessing a slave via the Slave SMI interface. An External CPU can configure the Slave to enable preamble suppression function. In that case the Slave does not need preamble befor accessing a slave.

9.4. Slave SPI Interface for External CPU to Access RTL8370MB

The RTL8370MB registers can be accessed via a Slave SPI Interface using an external CPU (Decided by Strapping Configuration).

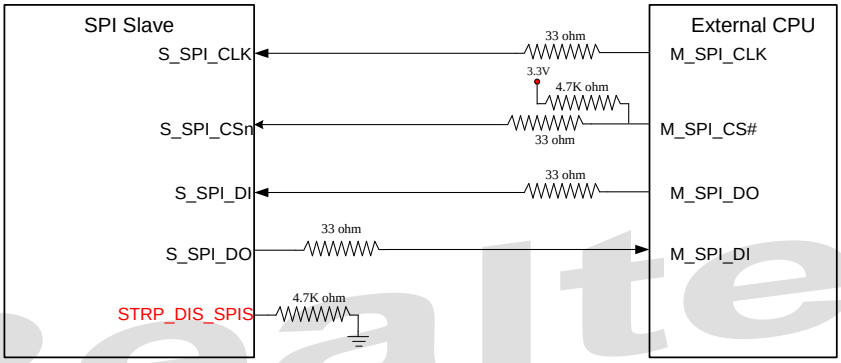


Figure 27. Slave SPI for External CPU Access Interface Connection Example

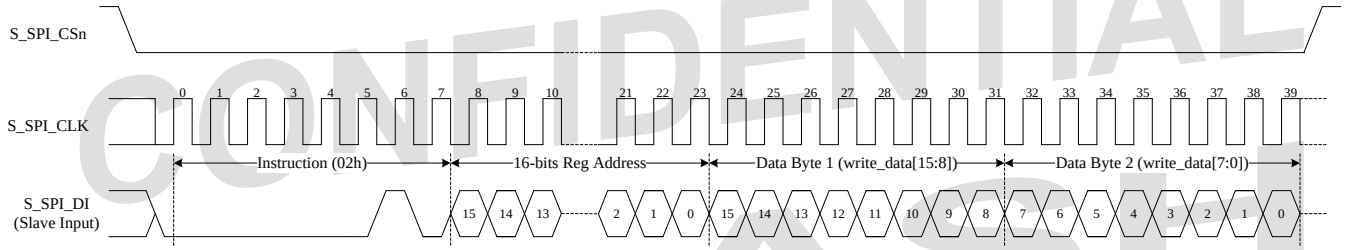


Figure 28. Slave SPI for External CPU Access Write Command

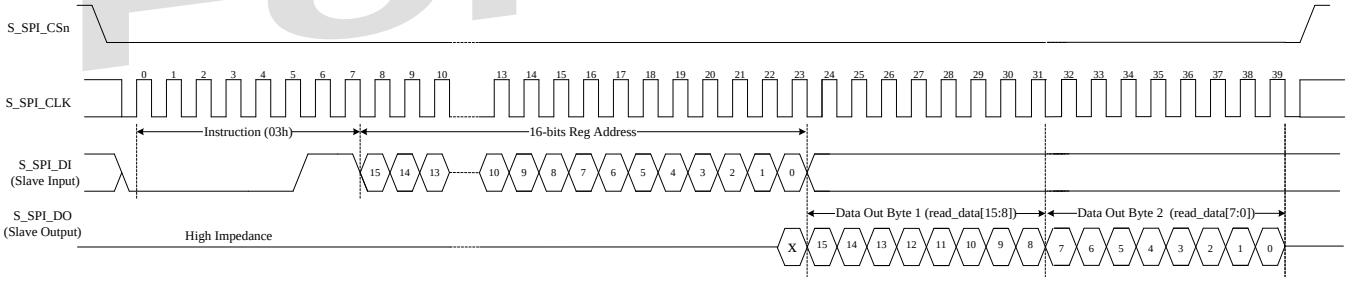


Figure 29. Slave SPI for External CPU Access Read Command

9.5. SPI FLASH Interface

The RTL8370MB supports Serial IO and Dual IO mode SPI Interface to Connect SPI FLASH. The RTL8370MB only supports 3-byte address mode access. No more than 4Mbyte capacity of SPI FLASH is better for RTL8370MB application.

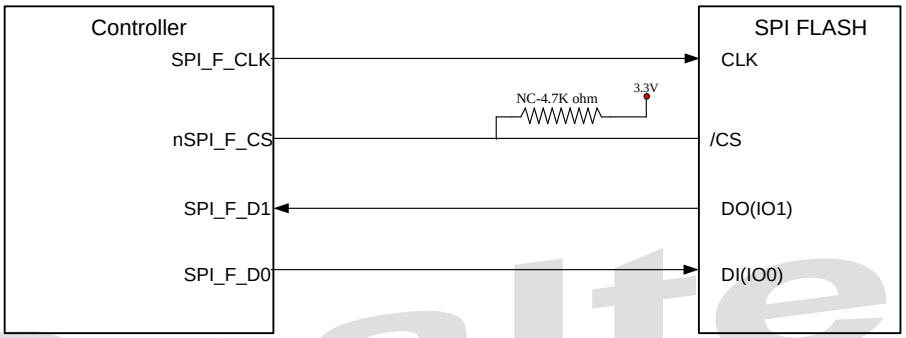


Figure 30. SPI FLASH Interface Connection Example

9.6. Extension GMAC1 & GMAC2 RGMII/MII/TMII/RMII Interface

The RTL8370MB shares two extension interfaces and an LED interface with the General Purpose Interface. When the extension interfaces are configured as dual RGMII/MII/TMII/RMII mode, the LED interface only supports LED_DA and LED_CK pins in serial LED mode.

Table 23. RTL8370MB General Purpose Interface Pin Definitions

RGMII	MAC MII	PHY MII	MAC TMII	PHY TMII	MAC RMII	PHY RMII
RG1_RXD3	M1_MRXD3	M1_PTXD3	TM1_MRXD3	TM1_PTXD3	-	-
RG1_RXD2	M1_MRXD2	M1_PTXD2	TM1_MRXD2	TM1_PTXD2	-	-
RG1_RXD1	M1_MRXD1	M1_PTXD1	TM1_MRXD1	TM1_PTXD1	RM1_MRXD1	RM1_PTXD1
RG1_RXD0	M1_MRXD0	M1_PTXD0	TM1_MRXD0	TM1_PTXD0	RM1_MRXD0	RM1_PTXD0
RG1_RXCTL	M1_MRXDV	M1_PTXEN	TM1_MRXDV	TM1_PTXEN	RM1_MCRSDV	RM1_PTXEN
RG1_RXC	M1_MRXC	M1_PTXC	TM1_MRXC	TM1_PTXC		
RG1_TXC	M1_MTXC	M1_PRXC	TM1_MTXC	TM1_PRXC	RM1_MREFCK	RM1_PREFCK
RG1_TXCTL	M1_MTXEN	M1_PRXDV	TM1_MTXEN	TM1_PRXDV	RM1_MTXEN	RM1_PCRSDV
RG1_TXD0	M1_MTXD0	M1_PRXD0	TM1_MTXD0	TM1_PRXD0	RM1_MTXD0	RM1_RXD0
RG1_TXD1	M1_MTXD1	M1_PRXD1	TM1_MTXD1	TM1_PRXD1	RM1_MTXD1	RM1_RXD0
RG1_TXD2	M1_MTXD2	M1_PRXD2	TM1_MTXD2	TM1_PRXD2	-	-
RG1_TXD3	M1_MTXD3	M1_PRXD3	TM1_MTXD3	TM1_PRXD3	-	-
RG2_TXD3	M2_MTXD3	M2_PRXD3	TM2_MTXD3	TM2_PRXD3	-	-
RG2_TXD2	M2_MTXD2	M2_PRXD2	TM2_MTXD2	TM2_PRXD2	-	-
RG2_TXD1	M2_MTXD1	M2_PRXD1	TM2_MTXD1	TM2_PRXD1	RM2_MTXD1	RM2_RXD1
RG2_TXD0	M2_MTXD0	M2_PRXD0	TM2_MTXD0	TM2_PRXD0	RM2_MTXD0	RM2_RXD0
RG2_TXCTL	M2_MTXEN	M2_PRXDV	TM2_MTXEN	TM2_PRXDV	RM2_MTXEN	RM2_PCRSDV
RG2_TXC	M2_MTXC	M2_PRXC	TM2_MTXC	TM2_PRXC	-	-
RG2_RXC	M2_MRXC	M2_PTXC	TM2_MRXC	TM2_PTXC	-	-
RG2_RXCTL	M2_MRXDV	M2_PTXEN	TM2_MRXDV	TM2_PTXEN	RM2_MCRSDV	RM2_PTXEN
RG2_RXD0	M2_MRXD0	M2_PTXD0	TM2_MRXD0	TM2_PTXD0	RM2_MRXD0	RM2_PTXD0
RG2_RXD1	M2_MRXD1	M2_PTXD1	TM2_MRXD1	TM2_PTXD1	RM2_MRXD1	RM2_PTXD1
RG2_RXD2	M2_MRXD2	M2_PTXD2	TM2_MRXD2	TM2_PTXD2	-	-
RG2_RXD3	M2_MRXD3	M2_PTXD3	TM2_MRXD3	TM2_PTXD3	-	-

9.6.1. Extension GMAC1 and GMAC2 RGMII Mode

The Extension GMAC1 and Extension GMAC2 of the RTL8370MB support RGMII interfaces to an external CPU.

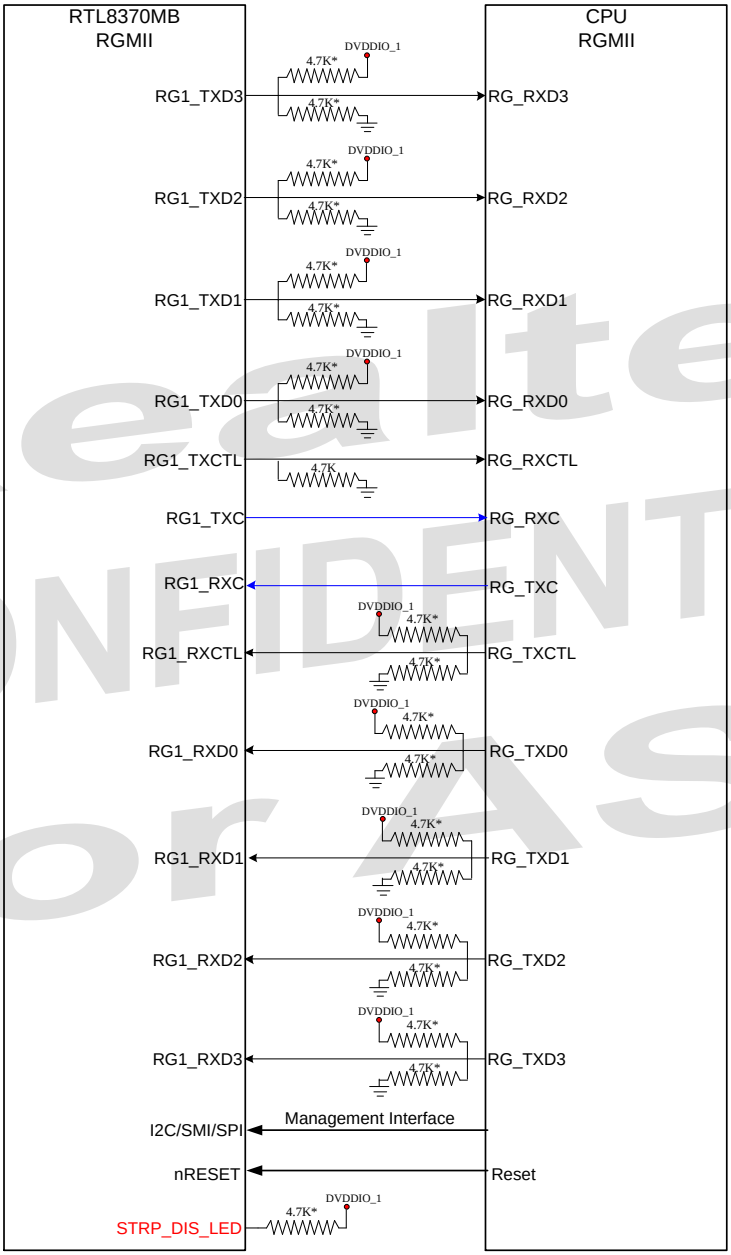


Figure 31. Signal Diagram of RGMII Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

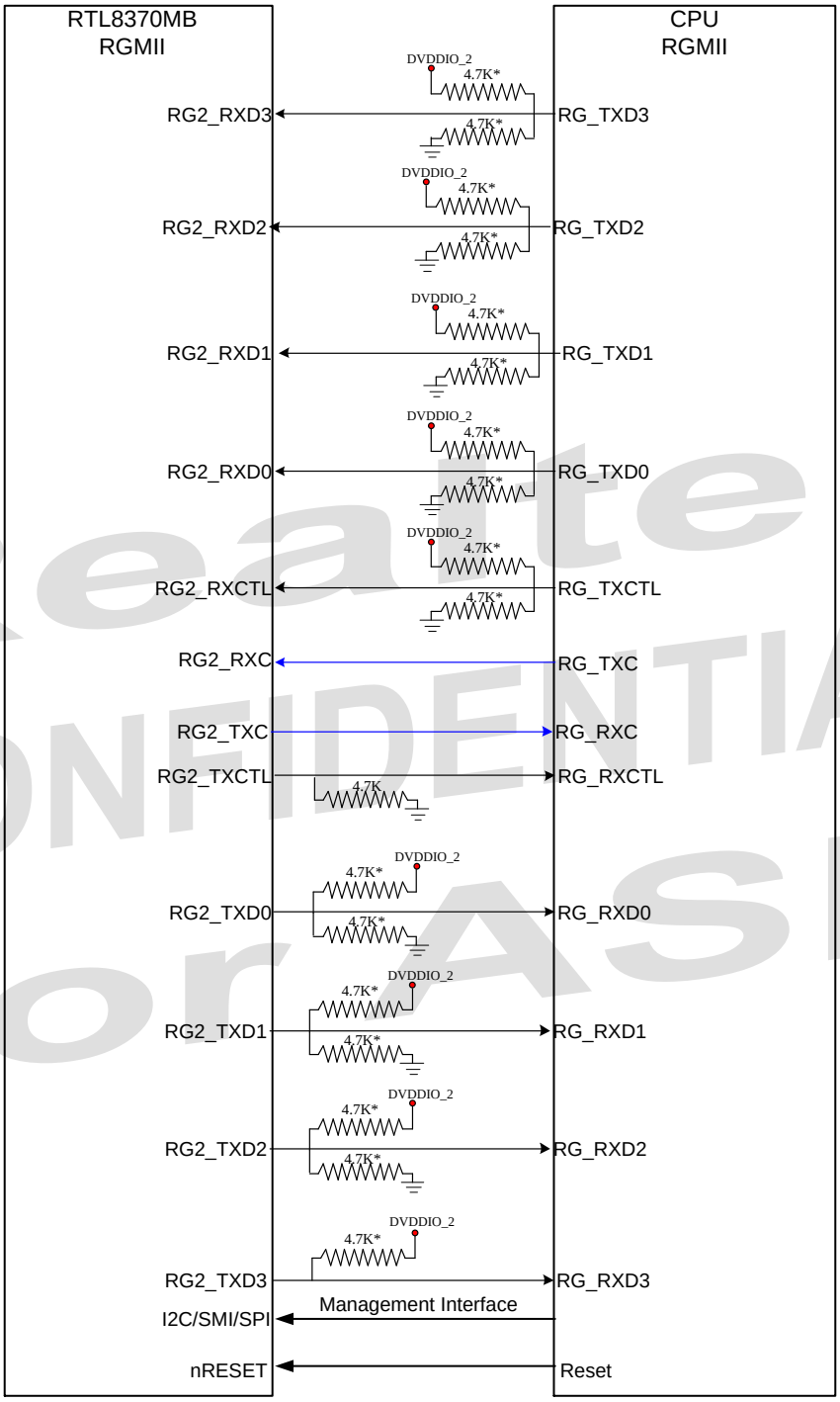


Figure 32. Signal Diagram of RGMII Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

9.6.2. Extension GMAC1 and GMAC2 Full Duplex MII MAC/PHY Mode Interface

Both the Extension GMAC1 and Extension GMAC2 of the RTL8370MB support full duplex MII MAC/PHY mode interfaces to an external CPU.

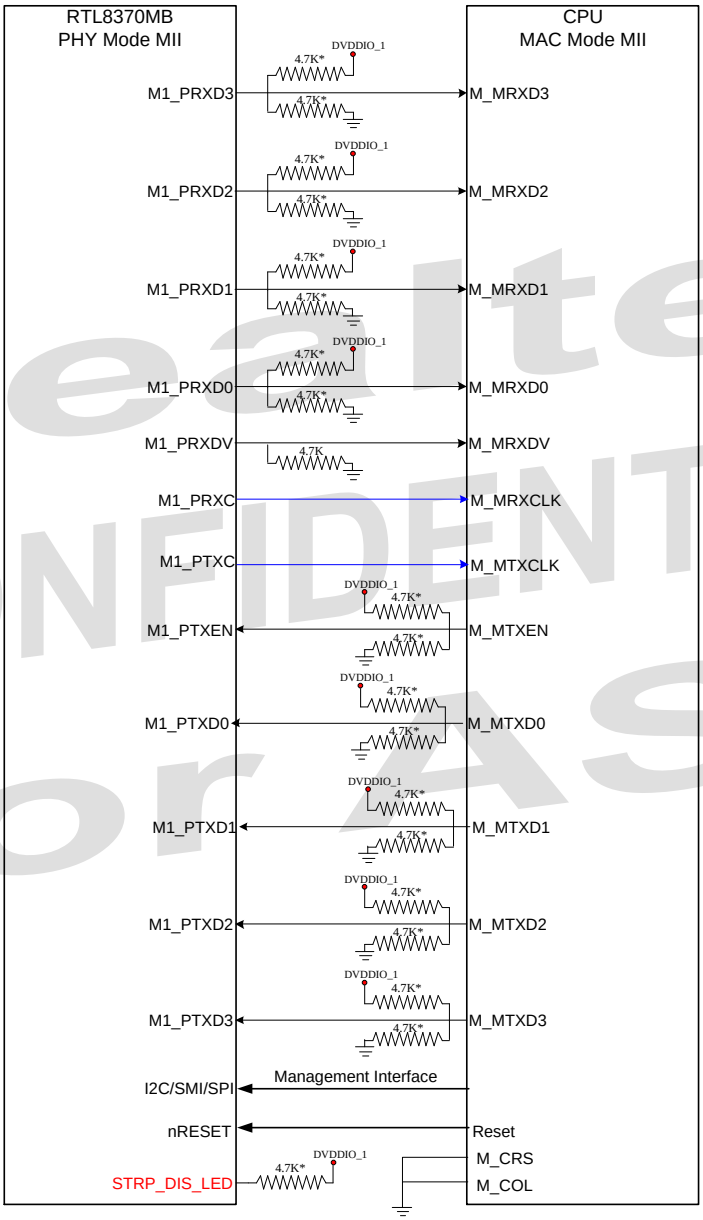


Figure 33. Signal Diagram of MII PHY Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

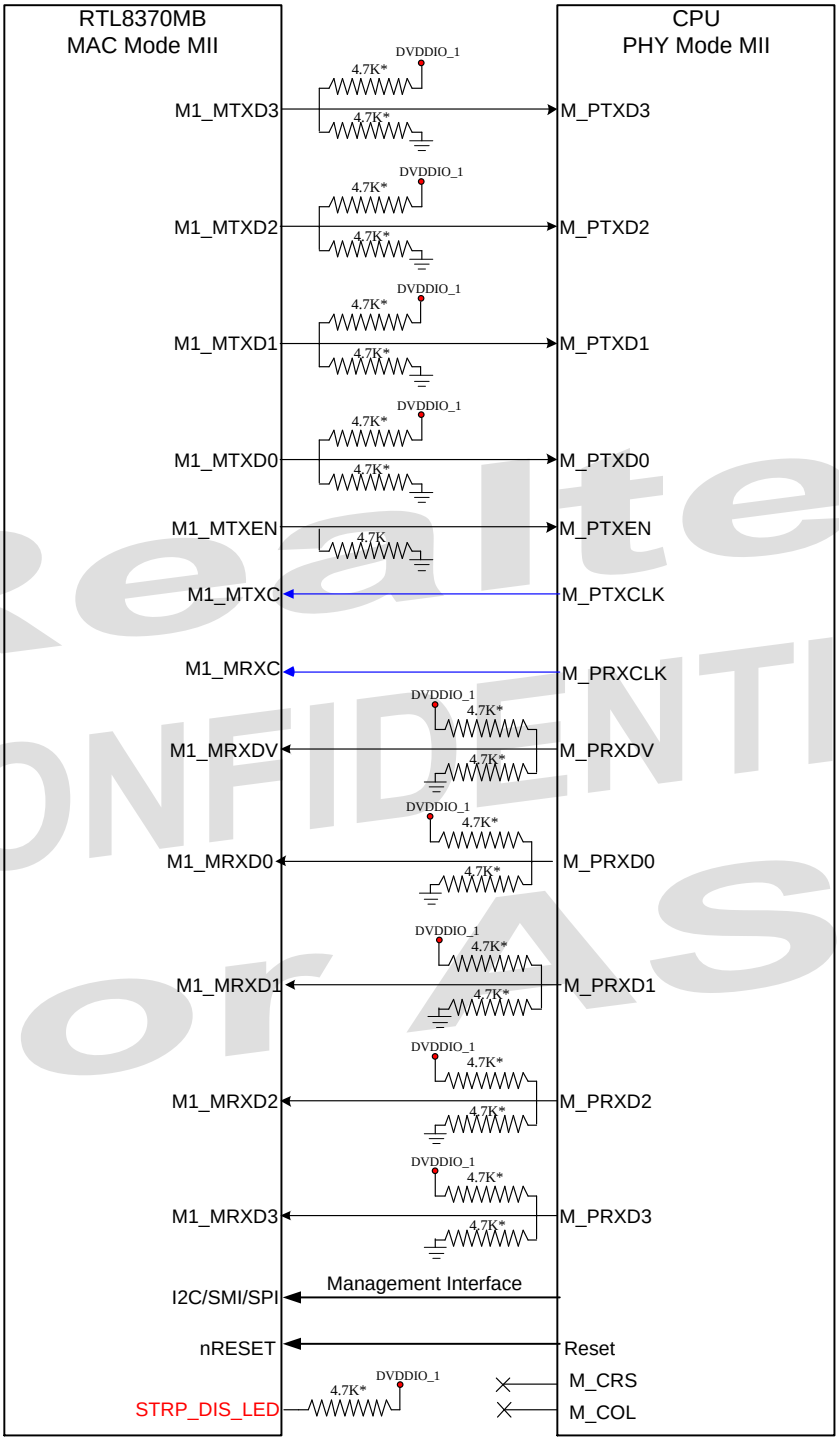


Figure 34. Signal Diagram of MII MAC Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

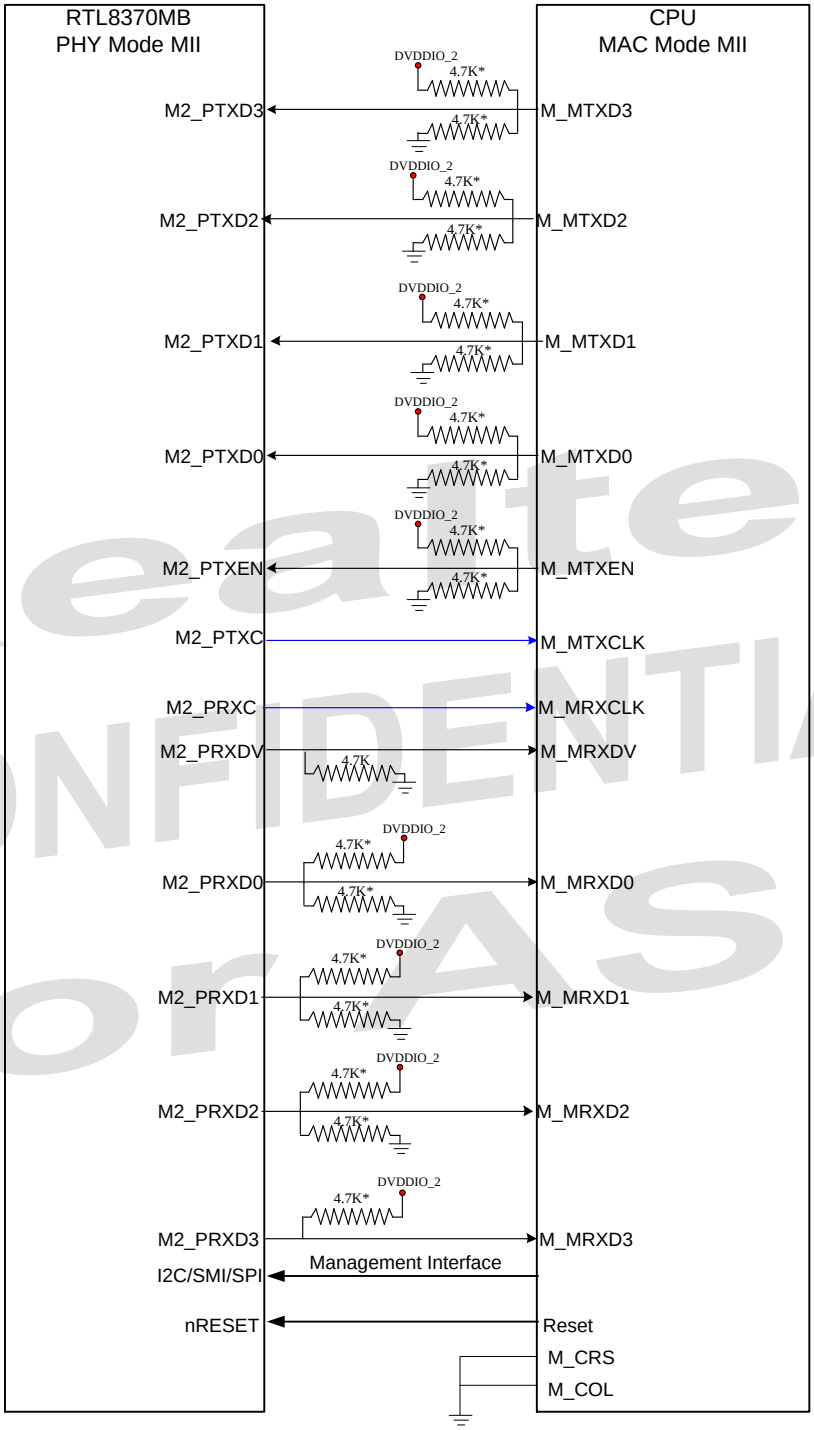


Figure 35. Signal Diagram of MII PHY Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

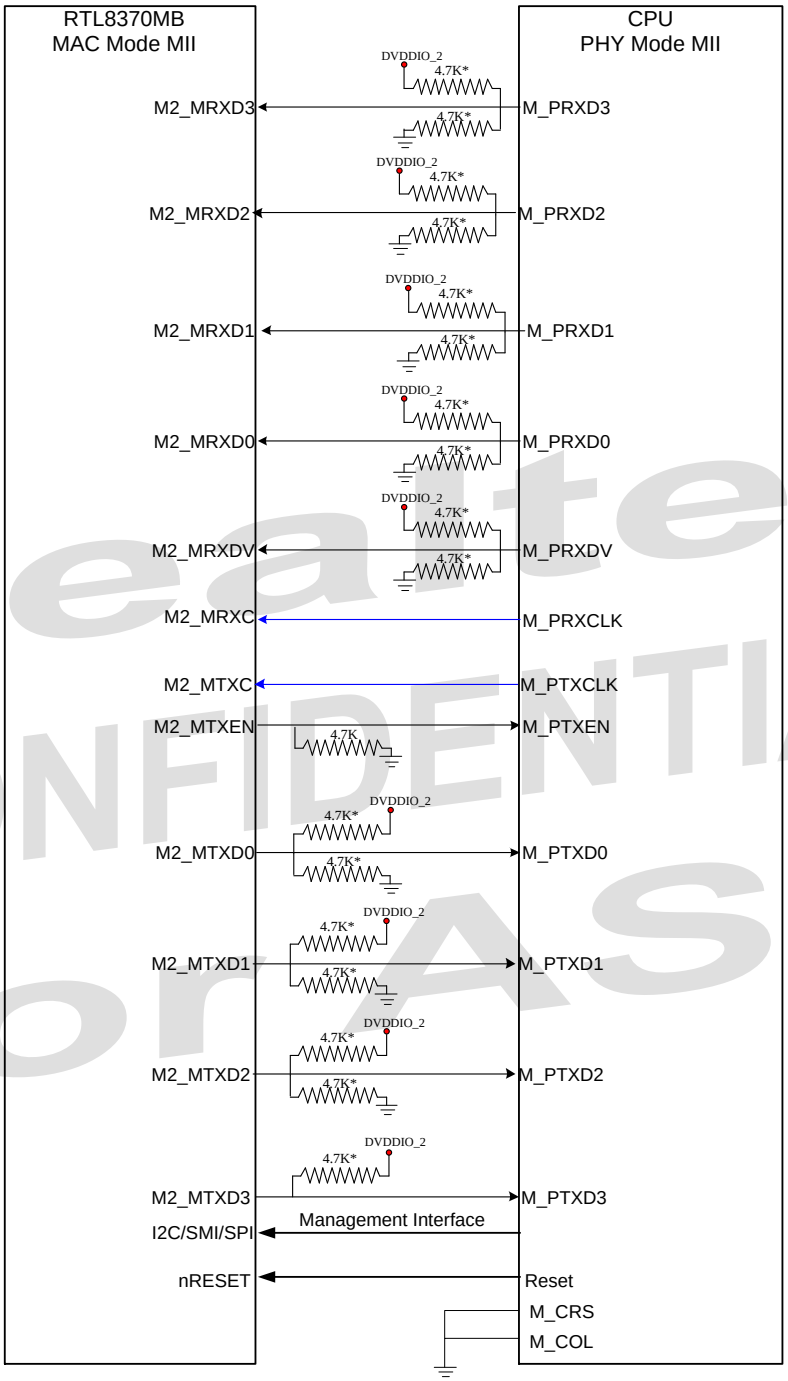


Figure 36. Signal Diagram of MII MAC Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

9.6.3. Extension GMAC1 and GMAC2 Full Duplex TMII MAC/PHY Mode Interface

Both the Extension GMAC1 and Extension GMAC2 of the RTL8370MB support full duplex TMII (Turbo MII) MAC/PHY mode interfaces to an external CPU.

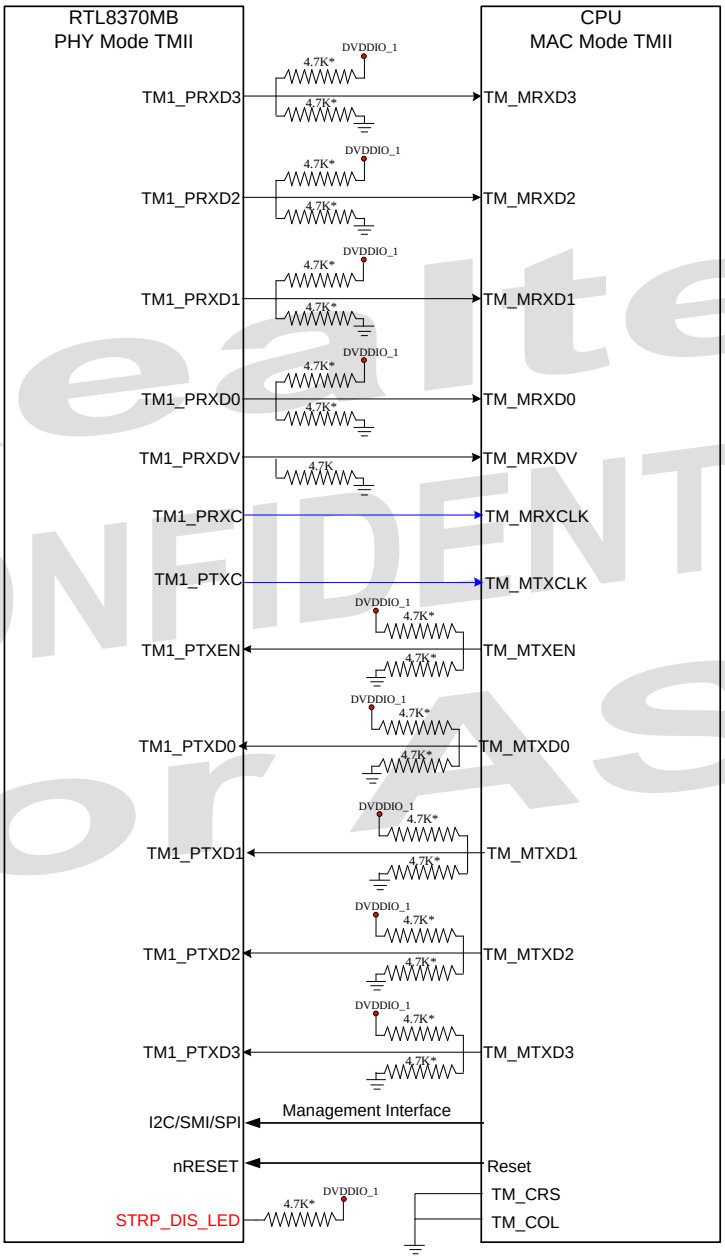


Figure 37. Signal Diagram of TMII PHY Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

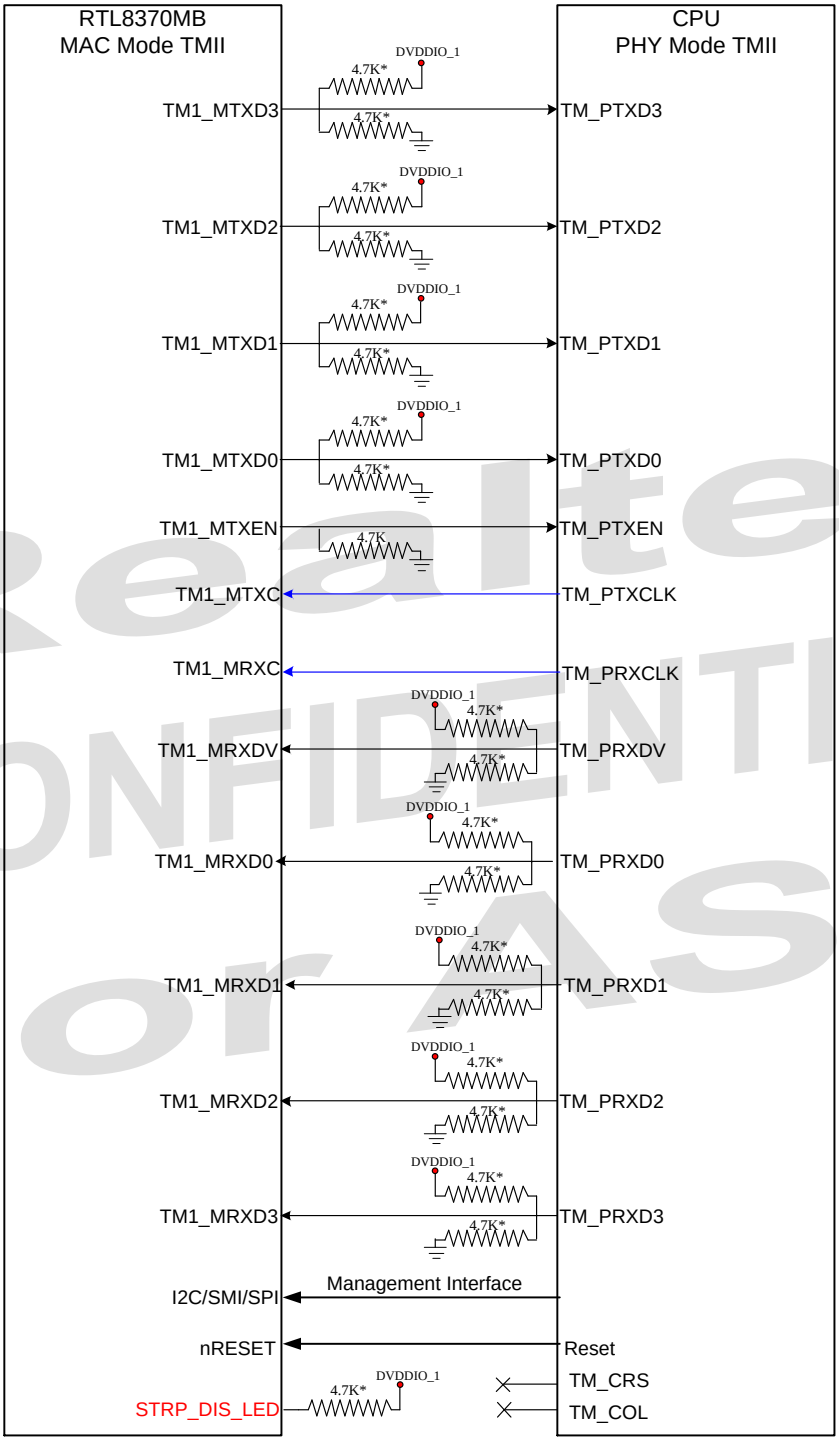


Figure 38. Signal Diagram of TMII MAC Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

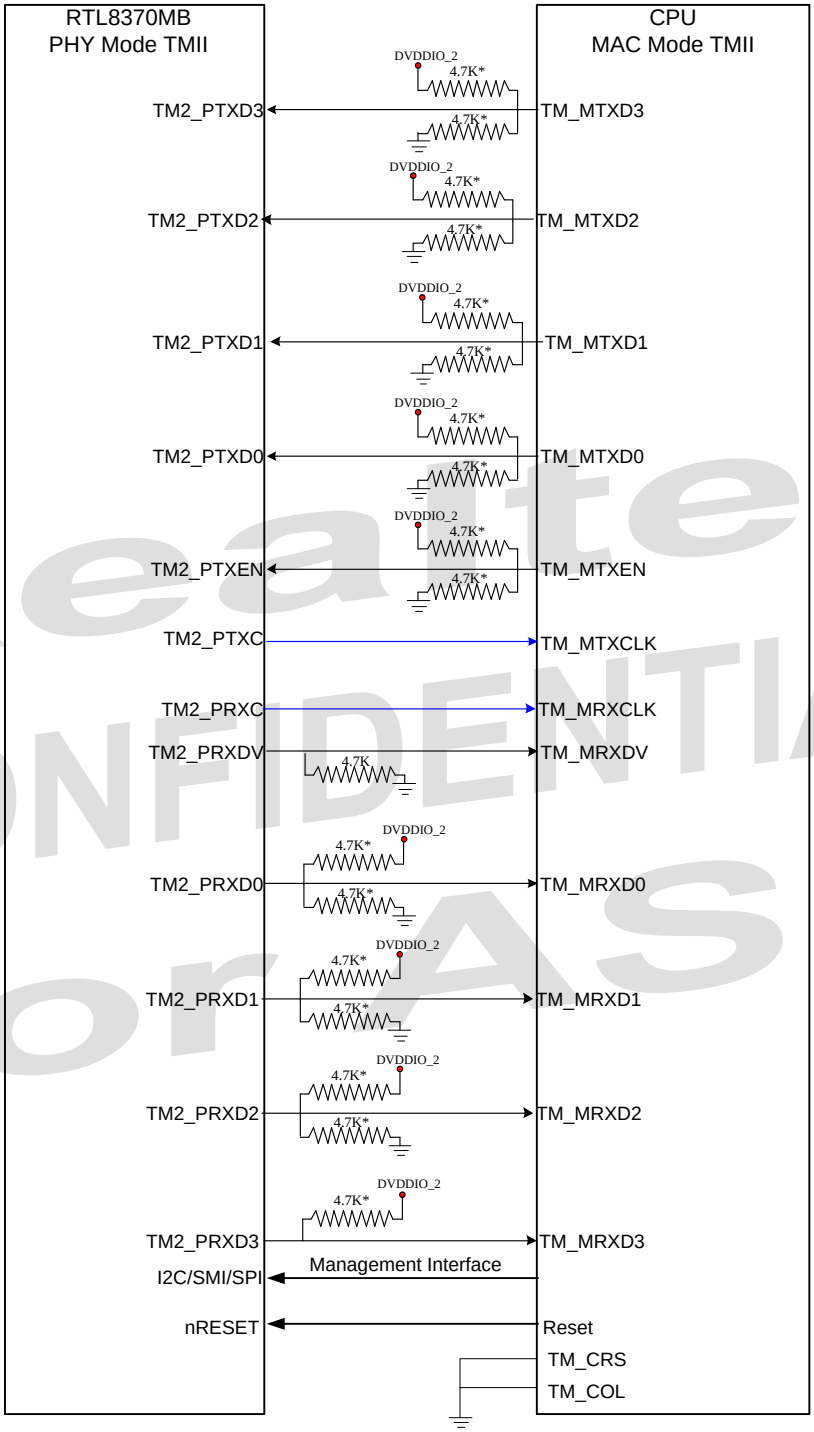


Figure 39. Signal Diagram of TMII PHY Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

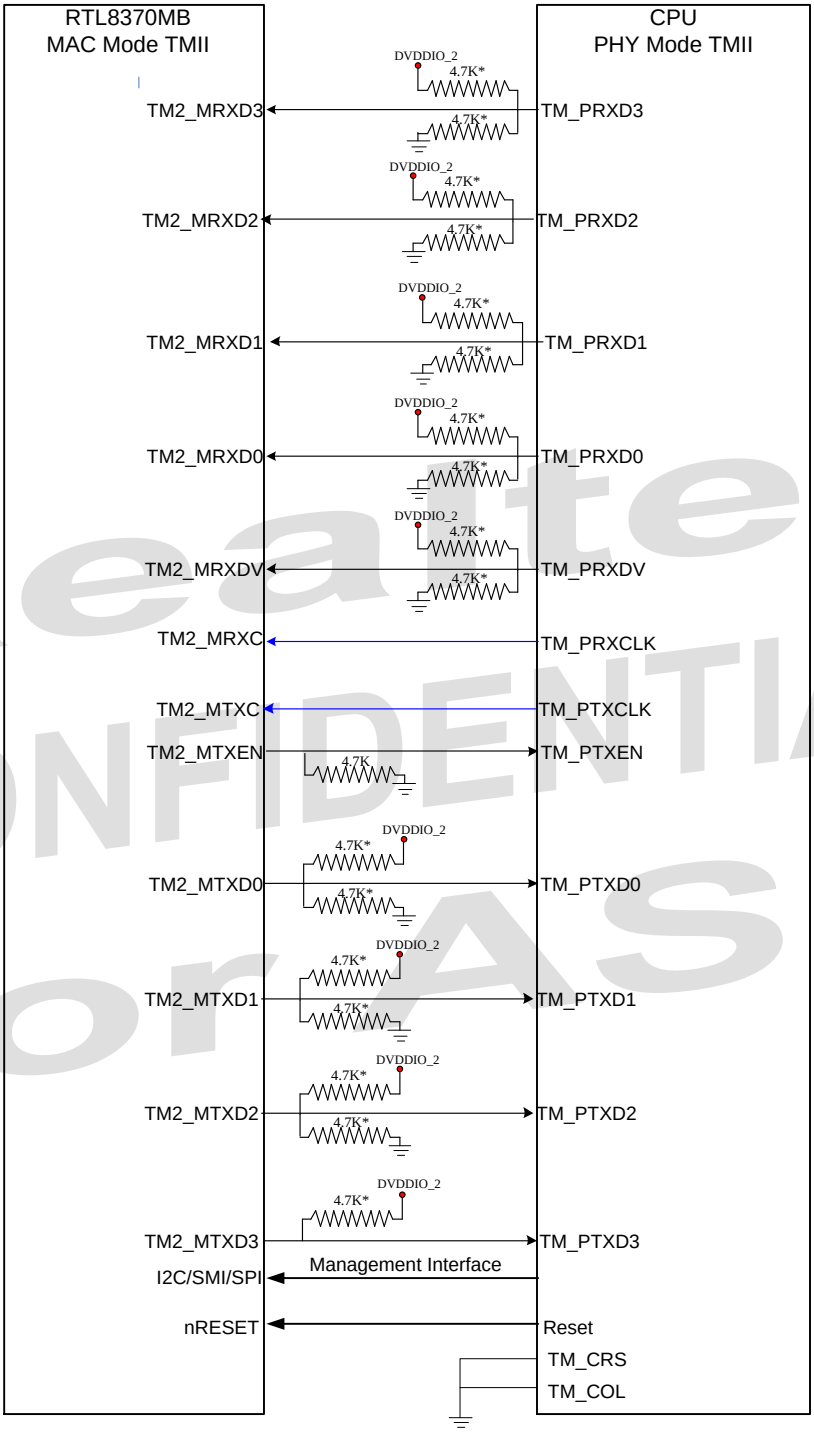


Figure 40. Signal Diagram of TMII MAC Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

9.6.4. Extension GMAC1 and GMAC2 RMII MAC/PHY Mode Interface

Both the Extension GMAC1 and Extension GMAC2 of the RTL8370MB support RMII MAC/PHY mode interfaces to an external CPU.

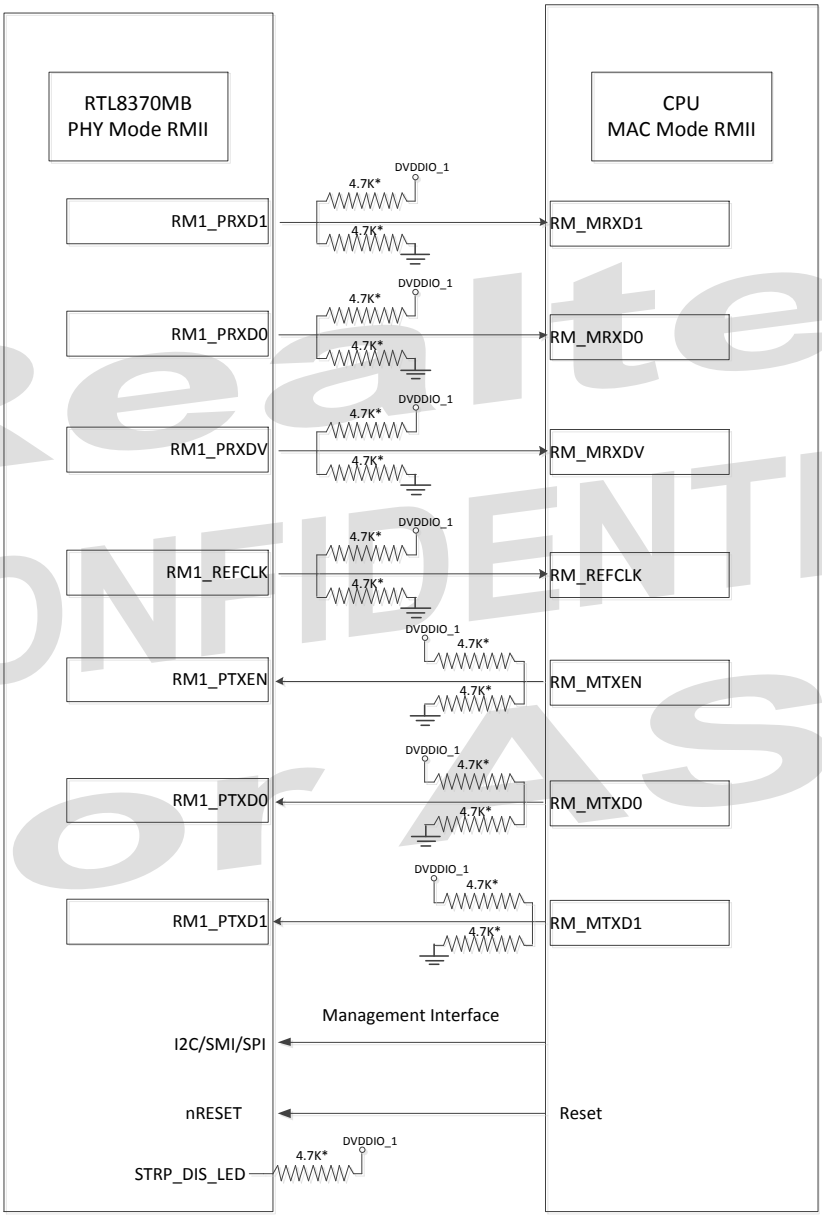


Figure 41. Signal Diagram of RMII PHY Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

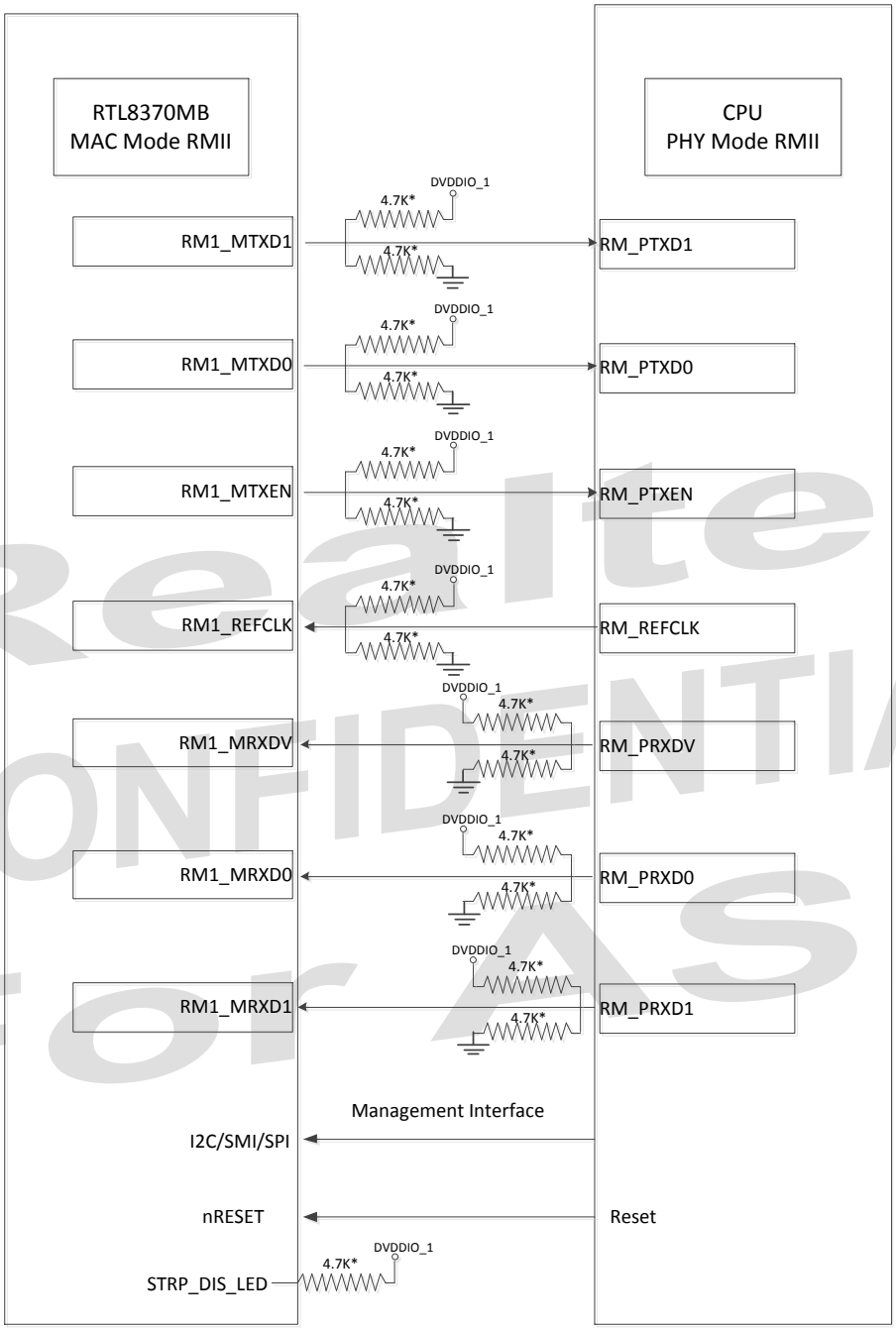


Figure 42. Signal Diagram of RMII MAC Mode of the Extension GMAC1

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

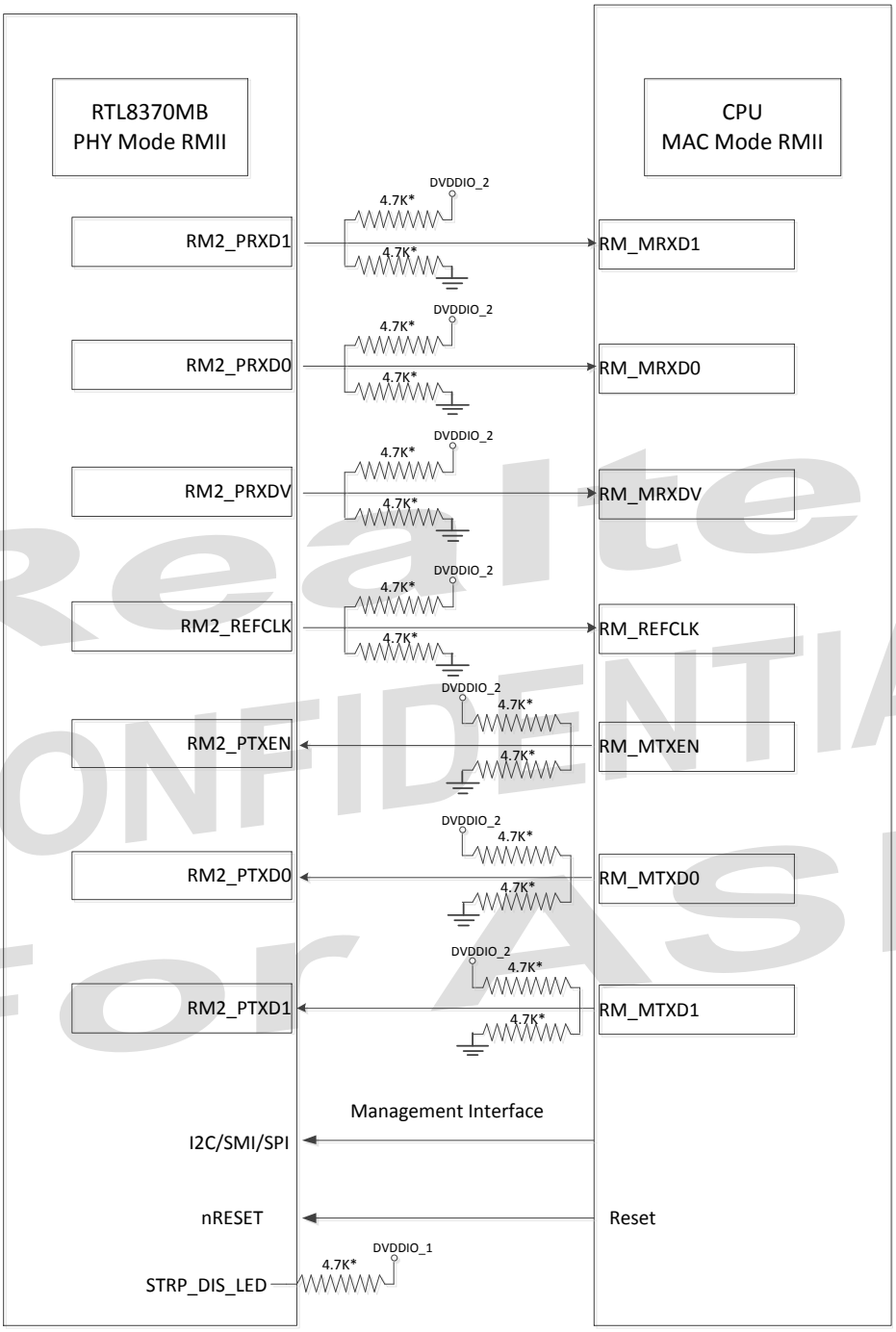


Figure 43. Signal Diagram of RMII PHY Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

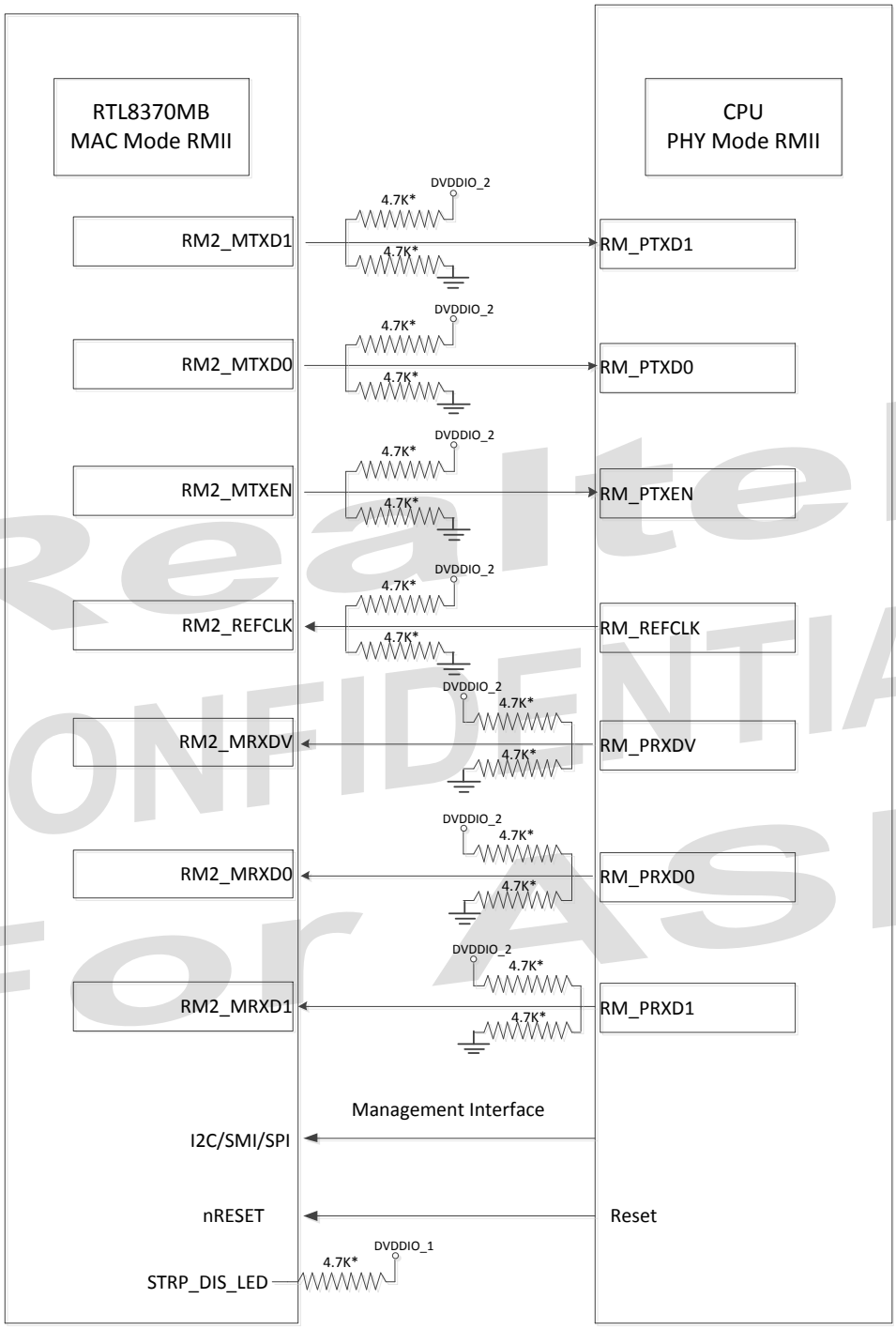


Figure 44. Signal Diagram of RMII MAC Mode of the Extension GMAC2

Note: A 4.7K pull up or pull down resistor may be used for strapping configuration. The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

9.7. Extension GMAC1 & GMAC2 HSGMII/SGMII/1000Base-X/100Base-FX Interface

The RTL8370MB supports SGMII/1000Base-X/100Base-FX interface for Extension GMAC1 & GMAC2 to connect an external CPU or SFP transceiver. Only Extension GMAC2 supports HSGMII.

9.7.1. Extension GMAC1 and GMAC2 SGMII Interface

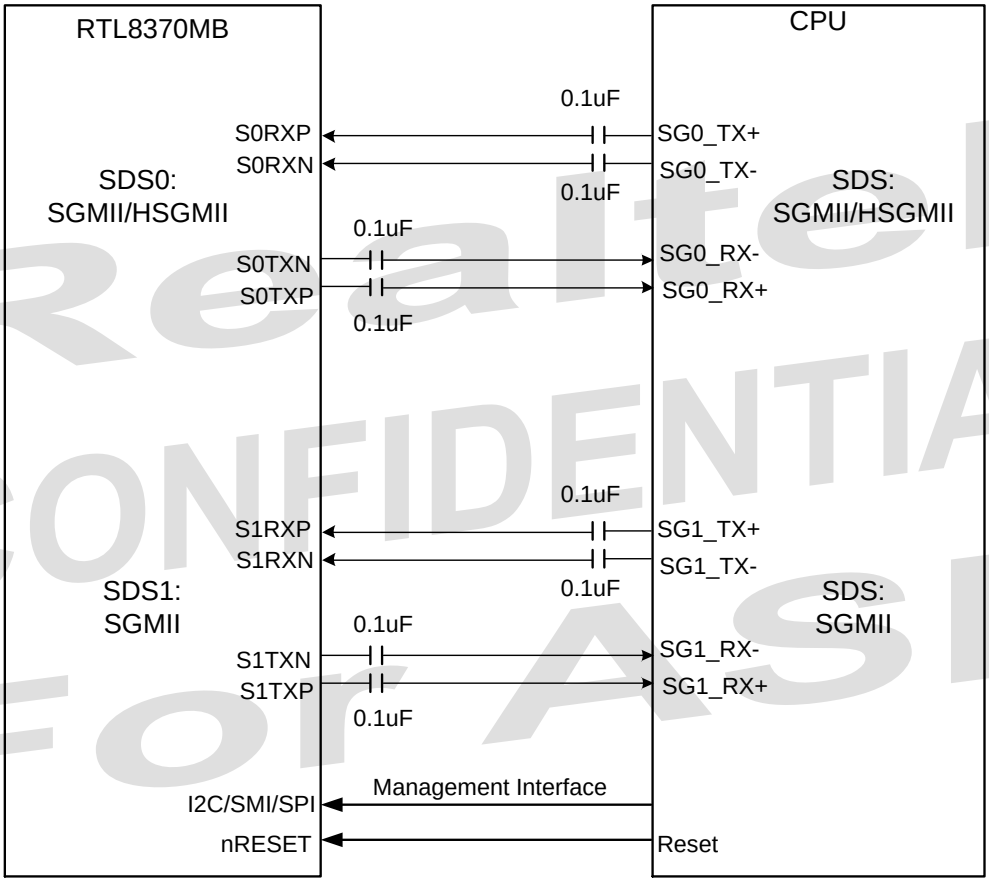


Figure 45. Signal Diagram of SGMII Mode of the Extension GMAC1 & GMAC2

9.7.2. Extension GMAC1 and GMAC2 1000Base-X/100Base-FX Interface

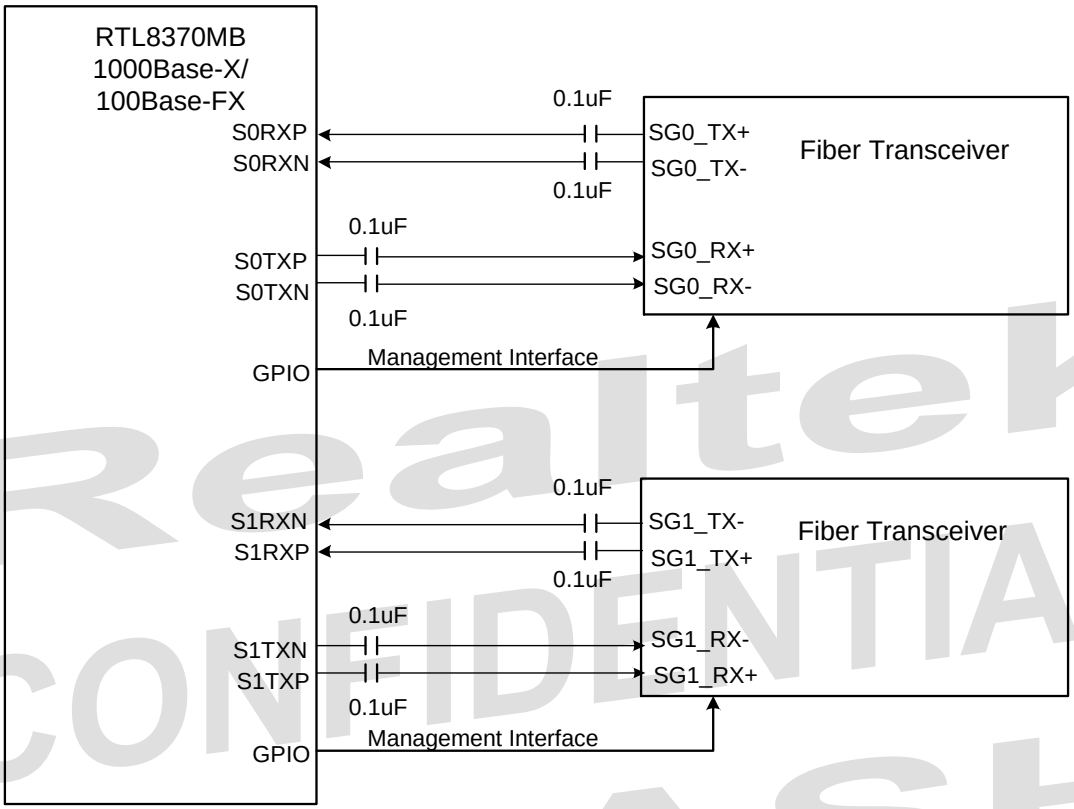


Figure 46. Signal Diagram of 1000Base-X/100Base-FX Mode of the Extension GMAC1/GMAC2

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 24. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO_2, DVDDIO, DVDDIO_1, AVDDH, SVDDH Supply Referenced to GND and AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1,SVDDL Supply Referenced to GND, AGND, PLLGND0, and PLLGND1	GND-0.3	+1.21	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

10.2. Recommended Operating Range

Table 25. Recommended Operating Range

Parameter		Min	Typical	Max	Units
Ambient Operating Temperature TA (RTL8370MB)		0	-	70	°C
DVDDIO, AVDDH, SVDDH Supply Voltage Range		3.135	3.3	3.465	V
DVDDIO_1 Supply Voltage Range	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
DVDDIO_2 Supply Voltage Range	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
	1.8V	1.7	1.8	1.9	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1, SVDDL Supply Voltage Range		1.045	1.1	1.155	V

10.3. Thermal Characteristics

10.3.1. TQFP-176-EPAD

10.3.1.1 Assembly Description

Table 26. Assembly Description

Package	Type	TQFP-176-EPAD
	Dimension (L x W)	20 x 20mm
	Thickness	1.0mm
PCB	PCB Dimension (L x W)	130 x 75mm
	PCB Thickness	1.6mm
	Number of Cu Layer-PCB	2-Layer: - Top layer (1oz): 20% coverage of Cu - Bottom layer (1oz): 75% coverage of Cu 4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

10.3.1.2 Material Properties

Table 27. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.9
PCB		Cu	400
		FR4	0.2

10.3.1.3 Simulation Conditions

Table 28. Simulation Conditions

Input Power	2.8W
Test Board (PCB)	2L (2S)/4L (2S2P)
Control Condition	Air Flow = 0, 1, 2 m/s

10.3.1.4 Thermal Performance of E-Pad TQFP-176 on PCB Under Still Air Convection

Table 29. Thermal Performance of E-Pad TQFP-176 on PCB Under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JB}
4L PCB	25.3	18.2	6.2	15.7
2L PCB	38.2	24.5	6.9	18.8

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB}: Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

10.3.1.5 Thermal Performance of E-Pad TQFP-176 on PCB Under Forced Convection

Table 30. Thermal Performance of E-Pad TQFP-176 on PCB Under Forced Convection

	Air Flow (m/s)	0	1	2
4L PCB	θ_{JA}	25.3	22.8	21.8
	Ψ_{JB}	15.7	15.6	15.4
2L PCB	θ_{JA}	38.2	34.9	33
	Ψ_{JB}	18.8	18.7	18.4

10.4. DC Characteristics

Table 31. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
8UTP+2*1000Base-X System Idle (All Port Link Down)					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	41	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	354	-	mA
Total Power Consumption for All Ports	PS	-	524.7	-	mW
8UTP*1000M+2*1000Base-X Active					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	503	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	1054	-	mA
Total Power Consumption for All Ports	PS	-	2819.3	-	mW
8UTP*100M+2*1000Base-X Active					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	132	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	487	-	mA
Total Power Consumption for All Ports	PS	-	971.3	-	mW

Parameter	SYM	Min	Typical	Max	Units
8UTP*10M+2*1000Base-X Active					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	233	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	403	-	mA
Total Power Consumption for All Ports	PS	-	1212.2	-	mW
8UTP+2*RGMII System Idle (All Port Link Down)					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	26	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	208	-	mA
Total Power Consumption for All Ports	PS	-	314.6	-	mW
8UTP*1000M+2*RGMII 1000M Active					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	486	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	919	-	mA
Total Power Consumption for All Ports	PS	-	2614.7	-	mW
8UTP*100M+2*RGMII 100M Active					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	117	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	323	-	mA
Total Power Consumption for All Ports	PS	-	741.4	-	mW
8UTP*10M+2*RGMII 10M Active					
Power Supply Current for VDDH	IDVDDIO, IAVDDH,ISVDDH	-	220	-	mA
Power Supply Current for VDDL	IDVDDL, IAVDDL, IPLLVDDL,ISVDDL	-	241	-	mA
Total Power Consumption for All Ports	PS	-	991.1	-	mW
2*RGMII Link Down					
Power Supply Current for DVDDIO_1(3.3v)	I DVDDIO_1	-	0	-	mA
Power Supply Current for DVDDIO_2(3.3v)	I DVDDIO_2	-	2	-	mA
Power Supply Current for DVDDIO_1(2.5v)	I DVDDIO_1	-	0	-	mA
Power Supply Current for DVDDIO_2(2.5v)	I DVDDIO_2	-	3	-	mA
Power Supply Current for DVDDIO_2(1.8v)	I DVDDIO_2	-	3	-	mA
2*RGMII 1000M Active					
Power Supply Current for DVDDIO_1(3.3v)	I DVDDIO_1	-	30	-	mA
Power Supply Current for DVDDIO_2(3.3v)	I DVDDIO_2	-	42	-	mA
Power Supply Current for DVDDIO_1(2.5v)	I DVDDIO_1	-	22	-	mA
Power Supply Current for DVDDIO_2(2.5v)	I DVDDIO_2	-	31	-	mA
Power Supply Current for DVDDIO_2(1.8v)	I DVDDIO_2	-	20	-	mA

Parameter	SYM	Min	Typical	Max	Units
2*RGMII 100M Active					
Power Supply Current for DVDDIO_1(3.3v)	I DVDDIO_1	-	4	-	mA
Power Supply Current for DVDDIO_2(3.3v)	I DVDDIO_2	-	6	-	mA
Power Supply Current for DVDDIO_1(2.5v)	I DVDDIO_1	-	3	-	mA
Power Supply Current for DVDDIO_2(2.5v)	I DVDDIO_2	-	6	-	mA
Power Supply Current for DVDDIO_2(1.8v)	I DVDDIO_2	-	5	-	mA
2*RGMII 10M Active					
Power Supply Current for DVDDIO_1(3.3v)	I DVDDIO_1	-	1	-	mA
Power Supply Current for DVDDIO_2(3.3v)	I DVDDIO_2	-	2	-	mA
Power Supply Current for DVDDIO_1(2.5v)	I DVDDIO_1	-	1	-	mA
Power Supply Current for DVDDIO_2(2.5v)	I DVDDIO_2	-	3	-	mA
Power Supply Current for DVDDIO_2(1.8v)	I DVDDIO_2	-	3	-	mA
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	1.9	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V
VDDIO=2.5V					
TTL Input High Voltage	V_{ih}	1.7	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.25	-	-	V
Output Low Voltage	V_{ol}	-	-	0.4	V
VDDIO=1.8V					
TTL Input High Voltage	V_{ih}	1.1	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.6	V
Output High Voltage	V_{oh}	1.25	-	-	V
Output Low Voltage	V_{ol}	-	-	0.45	V

Note 1: DVDDIO=3.3V, AVDDH=3.3V, DVDDIO_1=3.3V/2.5V, DVDDIO_2=3.3V/2.5V/1.8V, DVDDL=1.1V, AVDDL=1.1V PLLVDDL=1.1V.

Note 2: power DVDDIO_1 is for RGMII/MII/TMII/RMII interface of Extension GMAC1, DVDDIO_2 is for RGMII/MII/TMII/RMII interface of Extension GMAC2.

Note 3: Both I_{DVDDIO_1} & I_{DVDDIO_2} should be added to the total current consumption when the dual extension ports of the RTL8370MB are enabled.

10.5. AC Characteristics

10.5.1. I2C Master for EEPROM Auto-Load Interface Timing Characteristics

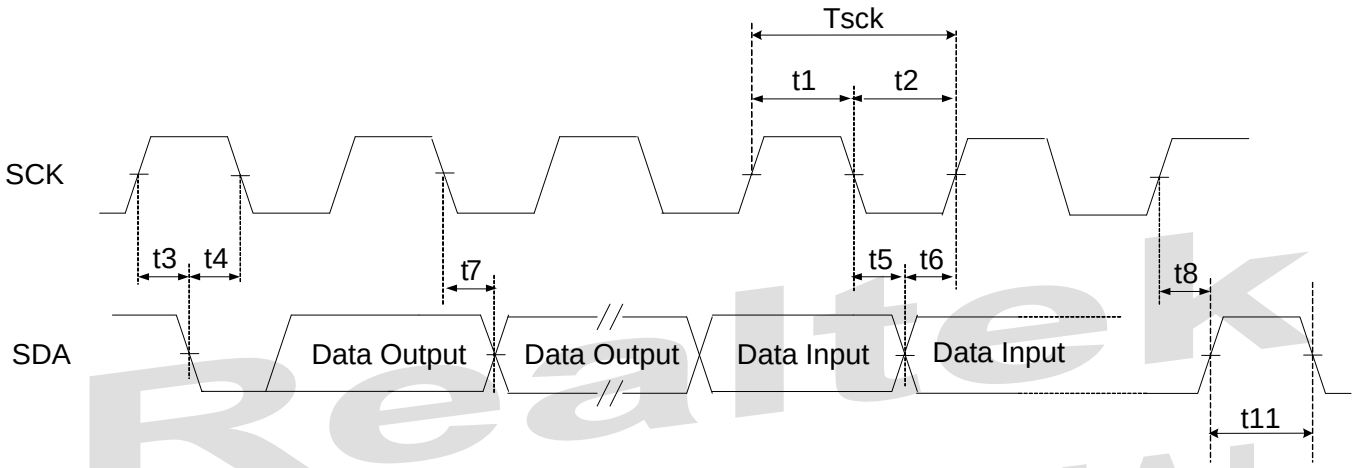


Figure 47. I2C Master for EEPROM Auto-Load Timing Characteristics

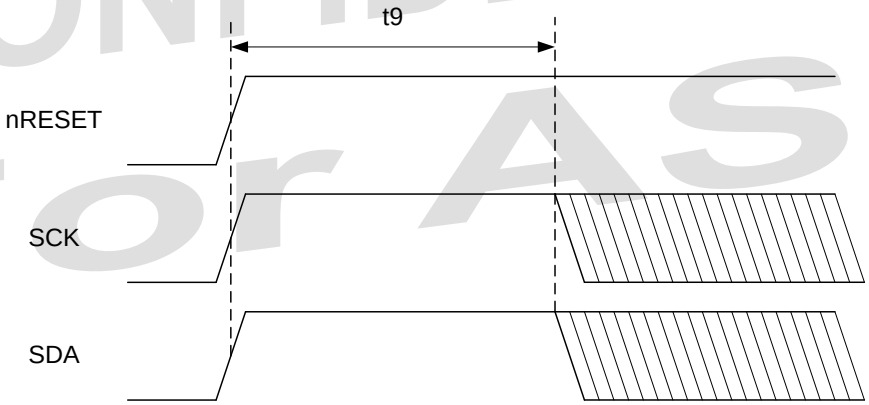


Figure 48. I2C Master for EEPROM Auto-Load Power on Timing

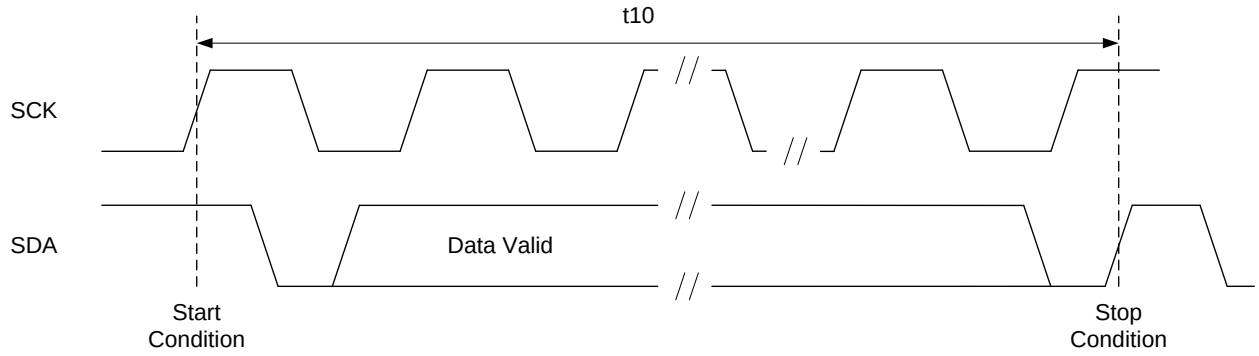


Figure 49. I2C Master for EEPROM Auto-Load Timing

Table 32. Master I2C for EEPROM Auto-Load Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
Tsck	SCK Clock Period	O	-	6	-	µs
t1	SCK High Time	O	2.7	3	-	µs
t2	SCK Low Time	O	2.7	3	-	µs
t3	START Condition Setup Time	O	1.35	1.5	-	µs
t4	START Condition Hold Time	O	1.35	1.5	-	µs
t5	Data Input Hold Time	I	0	-	-	ns
t6	Data Input Setup Time	I	10	-	-	ns
t7	Data output delay	O	1.4	1.5	1.6	µs
t8	STOP Condition Setup Time	O	1.35	1.5	-	µs
t9	SCK/SDA Active from Reset Ready	O	-	-	-	ms
t10	8K-bits EEPROM Auto-Load Time	O	-	-	-	ms
t11	Time the bus free before new START	O	11.25	13.5	-	µs
-	SCK Rise Time (10% to 90%)	O	-	-	100	ns
-	SCK Fall Time (90% to 10%)	O	-	-	100	ns
-	Duty Cycle	O	40	50	60	%

Note: t9 and t10 are measured with the ATMEL AT24C08 EEPROM.

10.5.2. SPI FLASH Interface Timing Characteristics

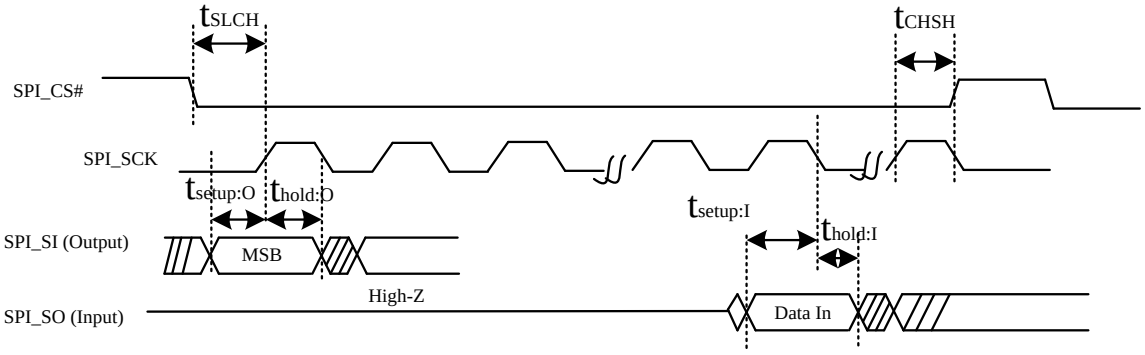


Figure 50. SPI FLASH Timing Characteristics

Table 33. SPI FLASH AC Timing

Symbol	Description	Type	Min	Typical	Max	Units
f_{SPI_SCK}	Clock Frequency of the SPI_SCK	O	-	62.5		MHz
Duty	Duty Cycle of the SPI_SCK	O	45	50	55	%
t_{SLCH}	CS# Active Setup Time	O	6	-	-	ns
t_{CHSH}	CS# Active Hold Time	O	6	-	-	ns
$t_{setup:O}$	Data Output Setup Time	O	2.5	-	-	ns
$t_{hold:O}$	Data Output Hold Time	O	3.5	-	-	ns
$t_{setup:I}$	Data Input Setup Time	I	2	-	-	ns
$t_{hold:I}$	Data Input Hold Time	I	0	-	-	ns
Test Condition: F_{SPI_SCK}=62.5MHz						

10.5.3. I2C-Like Slave Mode for External CPU Access Interface Timing Characteristics

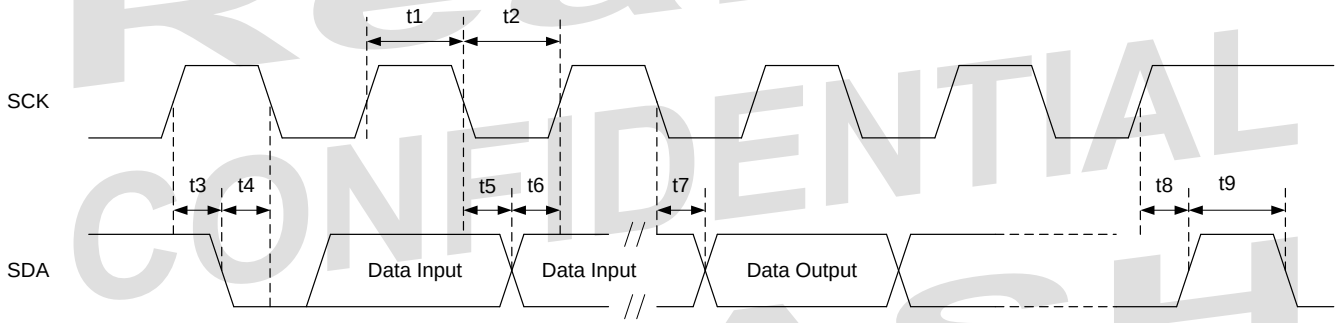


Figure 51. I2C-Like Slave Mode for External CPU Access Interface Timing Characteristics

Table 34. I2C-Like Slave Mode for External CPU Access Interface Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	4.0	-	-	µs
t2	SCK Low Time	I	4.0	-	-	µs
t3	START Condition Setup Time	I	0.25	-	-	µs
t4	START Condition Hold Time	I	0.25	-	-	µs
t5	Data Input Hold Time	I	0	-	-	µs
t6	Data Input Setup Time	I	100	-	-	ns
t7	Clock to Data Output Delay	O	10	-	100	ns
t8	STOP Condition Setup Time	I	0.25	-	-	µs
t9	Time the bus is free before new START	I	0.5	-	-	µs

10.5.4. Slave MII Management SMI for External CPU Access Interface Timing Characteristics

The RTL8370MB supports MDIO slave mode. The Master (the RTL8370MB link partner CPU) can access the Slave (RTL8370MB) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the Master sources the MDIO signal. In a read command, the Slave sources the MDIO signal.

- The timing characteristics (t1, t2, and t3 in Table 35) of the Master (the RTL8370MB link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics (t4 in Table 35) of the Slave (RTL8370MB) are provided by the RTL8370MB when the RTL8370MB sources the MDIO signal (Read command)

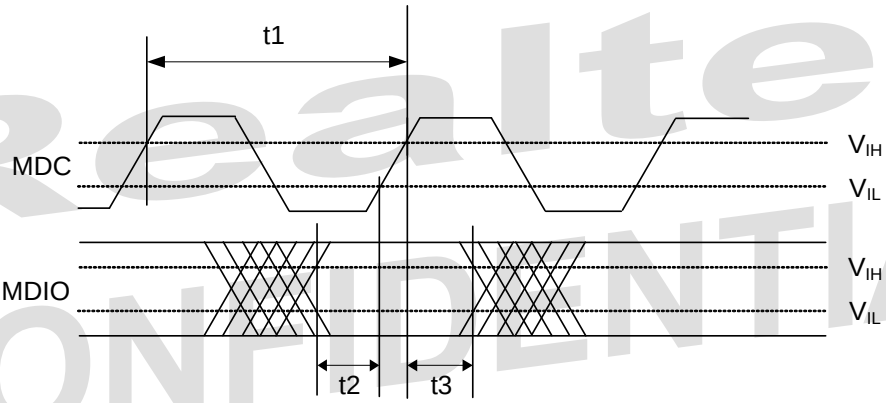


Figure 52. MDIO Sourced by Master (External CPU)

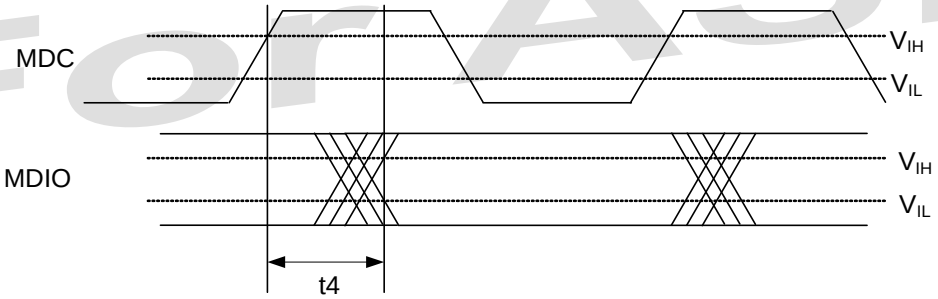


Figure 53. MDIO Sourced by Slave (RTL8370MB)

Table 35. Slave SMI (MDC/MDIO) Timing Characteristics and Requirements

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	8	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	8	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Rising Edge) to Data Delay Time	O	0	-	25	ns

10.5.5. Slave SPI for External CPU Access Interface Timing Characteristics

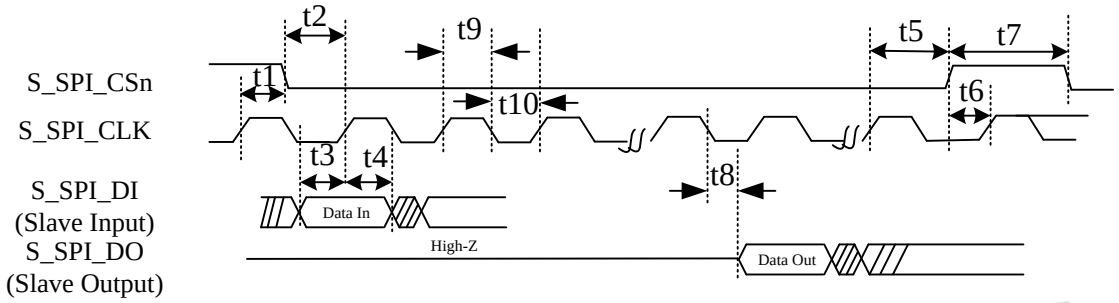


Figure 54. Slave SPI for External CPU Access Interface Timing Characteristics

Table 36. Slave SPI for External CPU Access Interface Timing Characteristics and Requirements

Symbol	Description	Type	Min	Typical	Max	Units
Fs_spi_sck	S_SPI_CLK	I	-	-	5	MHz
t1	S_SPI_CSn Not Active Hold time relative to S_SPI_CLK	I	22	-	-	ns
t2	S_SPI_CSn Active Setup time relative to S_SPI_CLK	I	22	-	-	ns
t3	S_SPI_DI to S_SPI_CLK Setup Time	I	22	-	-	ns
t4	S_SPI_DI to S_SPI_CLK Hold Time	I	22	-	-	ns
t5	S_SPI_CSn Not Active Setup time relative to S_SPI_CLK	I	22	-	-	ns
t6	S_SPI_CSn Active Hold time relative to S_SPI_CLK	I	22	-	-	ns
t7	S_SPI_CSn Deselect Time	I	44	-	-	ns
t8	S_SPI_CLK Falling Edge to S_SPI_DO Output Delay Time	O	12	-	35	ns
t9	S_SPI_CLK Clock High Time	I	50	-	-	ns
t10	S_SPI_CLK Clock Low Time	I	80	-	-	ns

10.5.6. RGMII Timing Characteristics

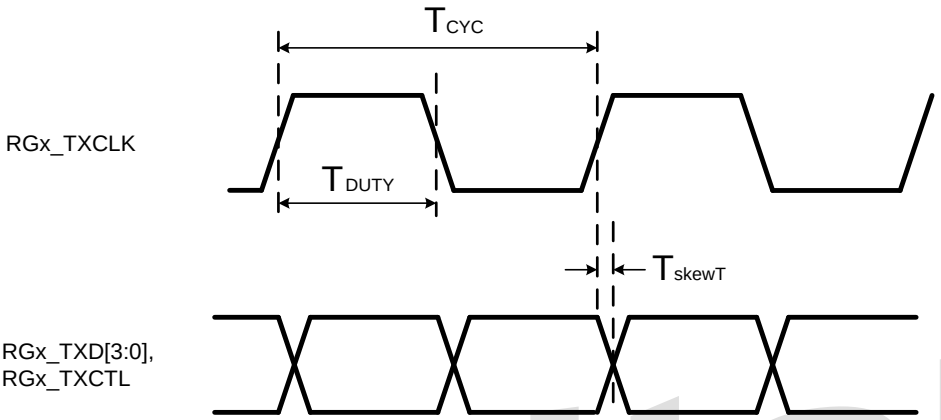


Figure 55. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=0)

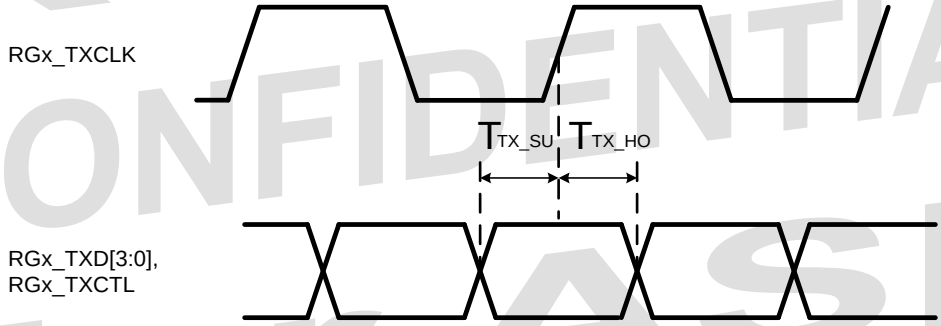


Figure 56. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=2ns)

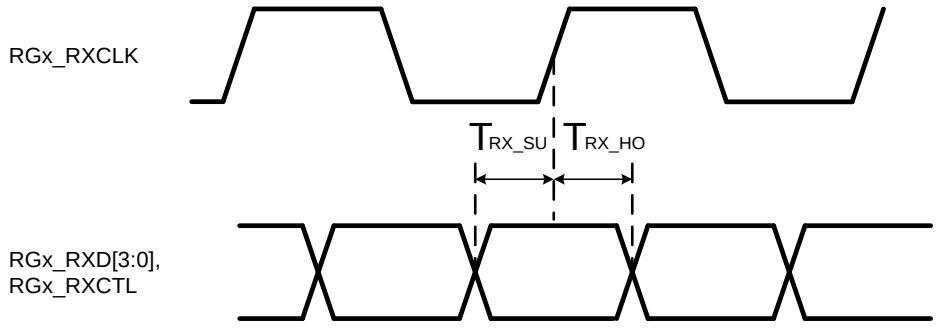


Figure 57. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=0)

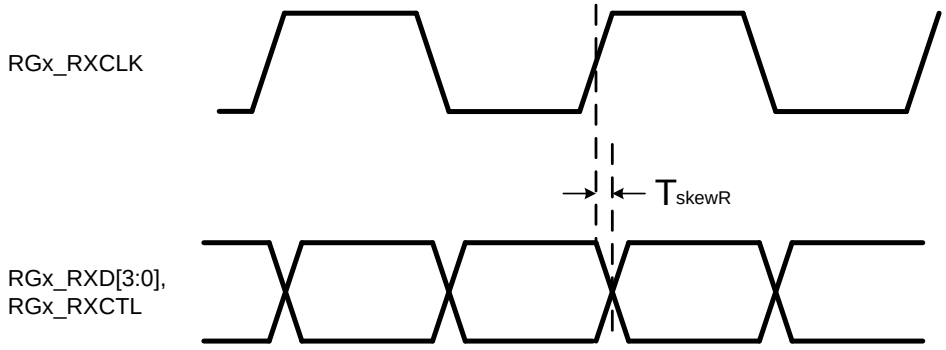


Figure 58. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=2ns)

Table 37. RGMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000M RGx_TXCLKc Output Cycle Time	T_{TX_CYC}	125MHz Clock Output.	O	7.7	8	8.3	ns
100M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	25MHz Clock Output.	O	38	40	42	ns
10M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	2.5MHz Clock Output.	O	380	400	420	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Skew	T_{skewT}	Disable Output Clock Delay. (RGx_TXCLK_DELAY=0).	O	-500	-140	500	ps
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Setup Time	T_{TX_SU}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1).	O	1.2	2.0	-	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Hold Time	T_{TX_HO}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1).	O	1.2	1.8	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Setup Time	T_{RX_SU}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0).	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Hold Time	T_{RX_HO}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0).	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Skew	T_{skewR}	Enable Input Clock Delay. (RGx_RXCLK_DELAY=1).	I	-600	-	600	ps

10.5.7. MII MAC Mode Timing

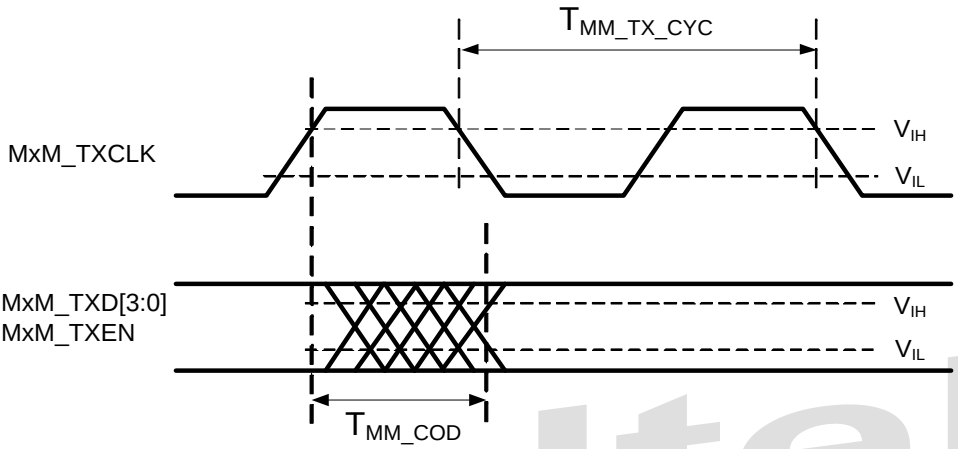


Figure 59. MII MAC Mode Clock to Data Output Delay Timing

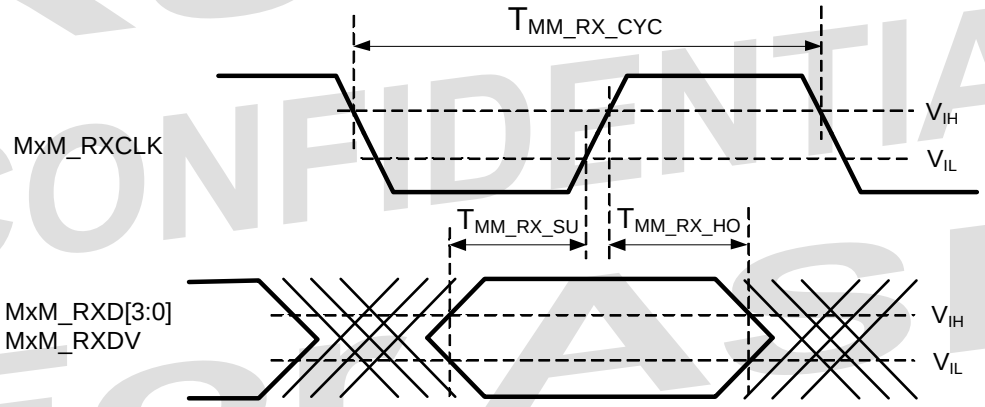


Figure 60. MII MAC Mode Input Timing

Table 38. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-T MxM_TXC and MxM_RXC Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	25MHz Clock Input.	I	-	40	-	ns
10Base-T MxM_TXC and MxM_RXC Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz Clock Input.	I	-	400	-	ns
MxM_TXC to MxM_TXD[3:0], MxM_TXEN Output Delay Time	T_{MM_COD}	-	O	5	-	15	ns
MxM_RXD[3:0], MxM_RXDV Input Setup Time	$T_{MM\_RX\_SU}$	-	I	5	-	-	ns
MxM_RXD[3:0], MxM_RXDV Input Hold Time	$T_{MM\_RX\_HO}$	-	I	5	-	-	ns

10.5.8. MII PHY Mode Timing

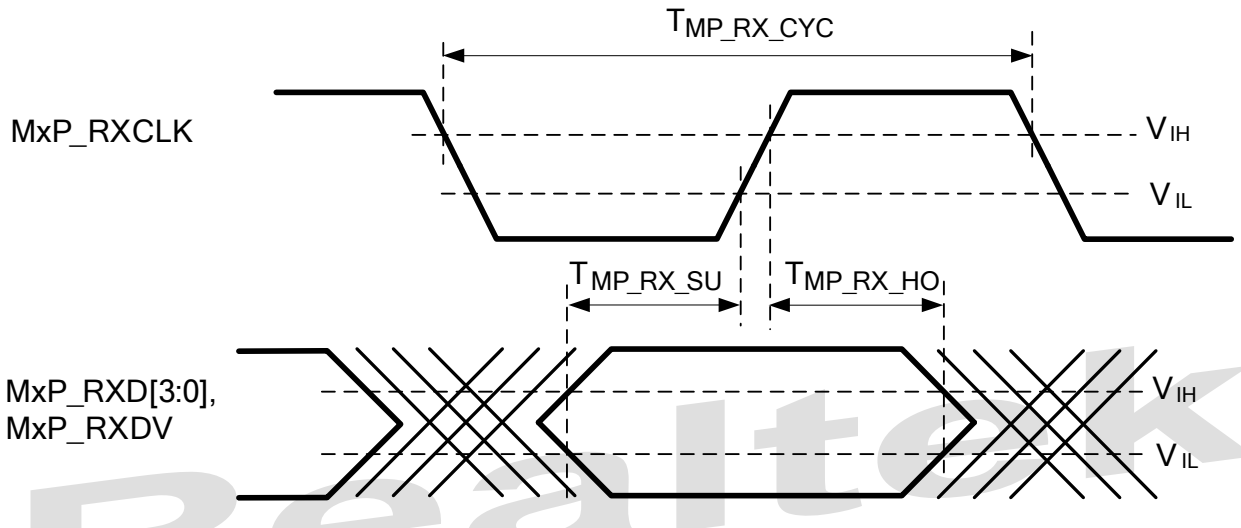


Figure 61. MII PHY Mode Output Timing

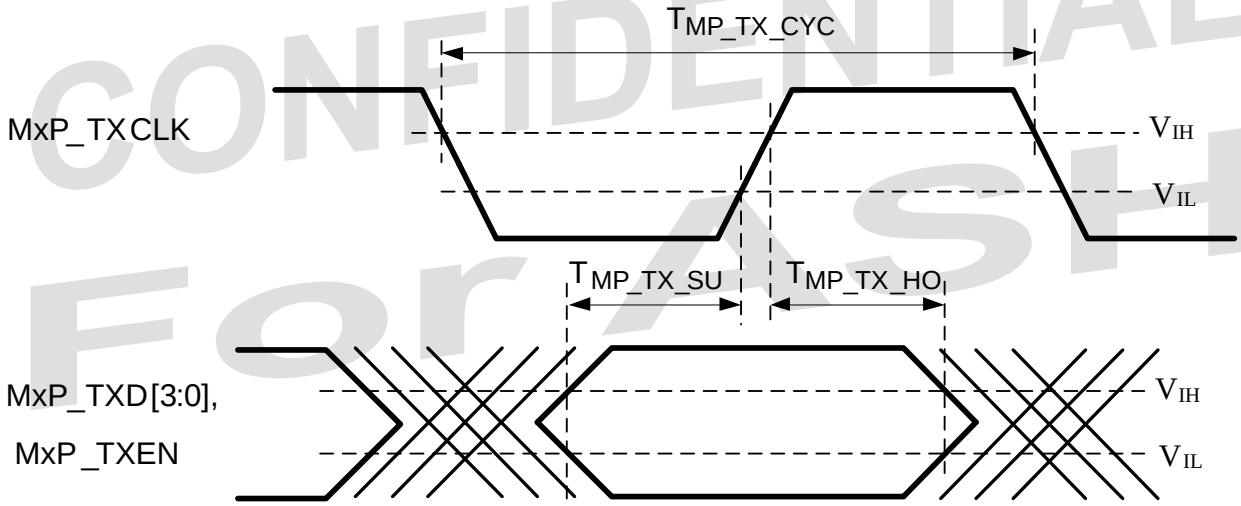


Figure 62. MII PHY Mode Input Timing

Table 39. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100 Base-T MxP_RXC and MxP_TXC Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10 Base-T MxP_RXC and MxP_TXC Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns
MxP_RXD[3:0], MxP_RXDV to MxP_RXC Output Setup Time	$T_{MP\_RX\_SU}$	-	O	15	-	-	ns
MxP_RXD[3:0], MxP_RXDV to MxP_RXC Output Hold Time	$T_{MP\_RX\_HO}$	-	O	15	-	-	ns
MxP_TXD[3:0], MxP_TXEN to MxP_TXC Input Setup Time	$T_{MP\_TX\_SU}$	-	I	2.5	-	-	ns
MxP_TXD[3:0], MxP_TXEN to MxP_TXC Input Hold Time	$T_{MP\_TX\_HO}$	-	I	0	-	-	ns

10.5.9. TMII MAC Mode Timing

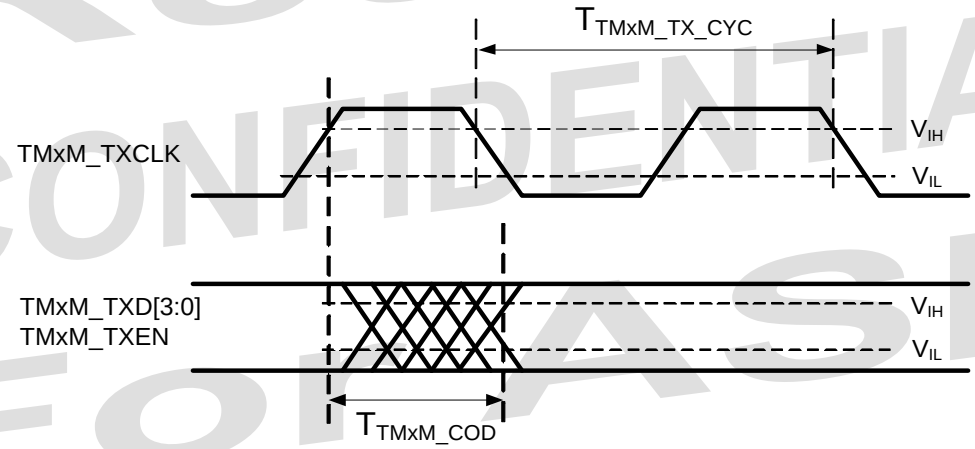


Figure 63. TMII MAC Mode Clock to Data Output Delay Timing

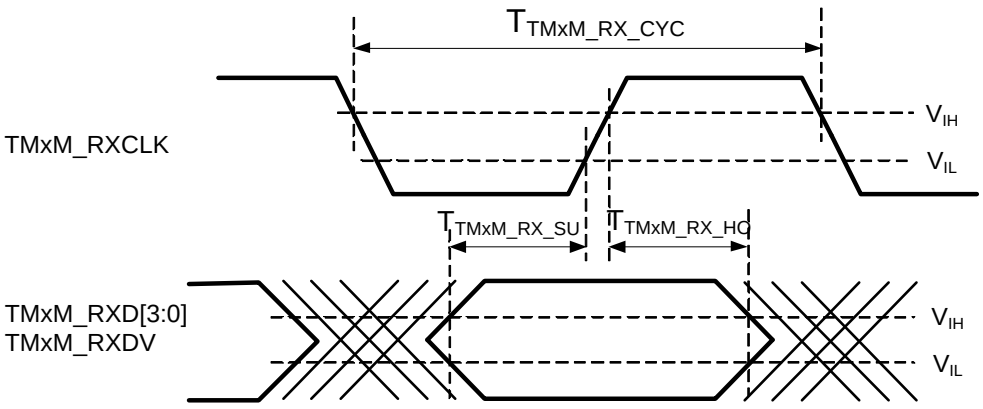


Figure 64. TMII MAC Mode Input Timing

Table 40. TMII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
200Base-T TMxM_TXC and TMxM_RXC Input Cycle Time	$T_{TMxM\_TX\_CYC}$ $T_{TMxM\_RX\_CYC}$	50MHz Clock Input.	I	-	20	-	ns
20Base-T TMxM_TXC and TMxM_RXC Input Cycle Time	$T_{TMxM\_TX\_CYC}$ $T_{TMxM\_RX\_CYC}$	5MHz Clock Input.	I	-	200	-	ns
TMxM_TXC to TMxM_TXD[3:0], TMxM_TXEN Output Delay Time	T_{TMxM_COD}	-	O	0	-	12.5	ns
TMxM_RXD[3:0], TMxM_RXDV Input Setup Time	$T_{TMxM\_RX\_SU}$	-	I	2.5	-	-	ns
TMxM_RXD[3:0], TMxM_RXDV Input Hold Time	$T_{TMxM\_RX\_HO}$	-	I	2.5	-	-	ns

10.5.10. TMII PHY Mode Timing

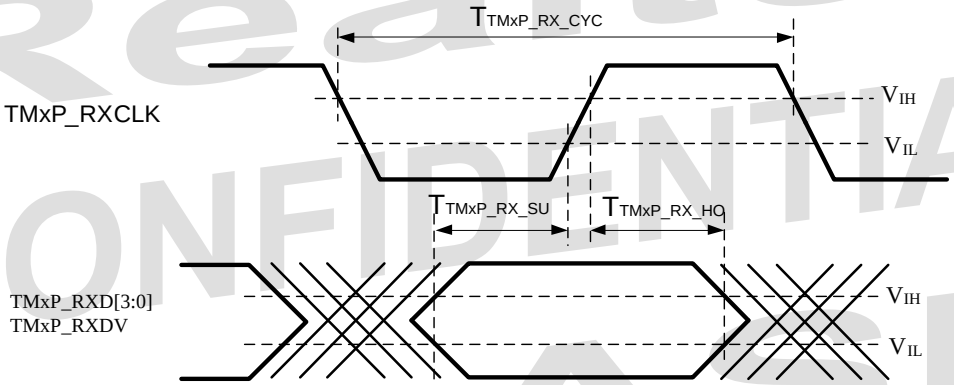


Figure 65. TMII PHY Mode Output Timing

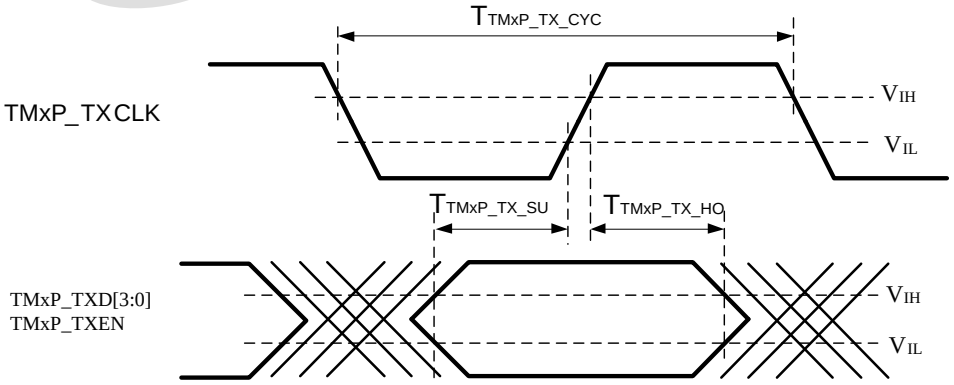


Figure 66. TMII PHY Mode Input Timing

Table 41. TMII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
200Base-T TMxP_RXC and TMxP_TXC Output Cycle Time	$T_{TMxP\_RX\_CYC}$ $T_{TMxP\_TX\_CYC}$	50MHz Clock Output.	O	-	20	-	ns
20Base-T TMxP_RXC and TMxP_TXC Output Cycle Time	$T_{TMxP\_RX\_CYC}$ $T_{TMxP\_TX\_CYC}$	5MHz Clock Output.	O	-	200	-	ns
TMxP_RXD[3:0], TMxP_RXDV to TMxP_RXC Output Setup Time	$T_{TMxP\_RX\_SU}$	-	O	7.5	-	-	ns
TMxP_RXD[3:0], TMxP_RXDV to TMxP_RXC Output Hold Time	$T_{TMxP\_RX\_HO}$	-	O	7.5	-	-	ns
TMxP_TXD[3:0], TMxP_TXEN to TMxP_TXC Input Setup Time	$T_{TMxP\_TX\_SU}$	-	I	2.5	-	-	ns
TMxP_TXD[3:0], TMxP_TXEN to TMxP_TXC Input Hold Time	$T_{TMxP\_TX\_HO}$	-	I	0	-	-	ns

10.5.11. RMII MAC Mode Timing

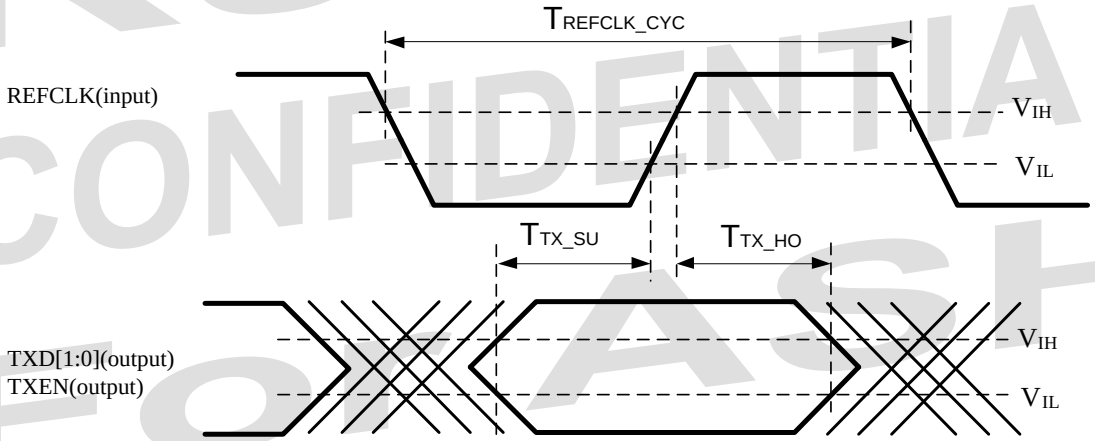


Figure 67. RMII MAC Mode Output Timing

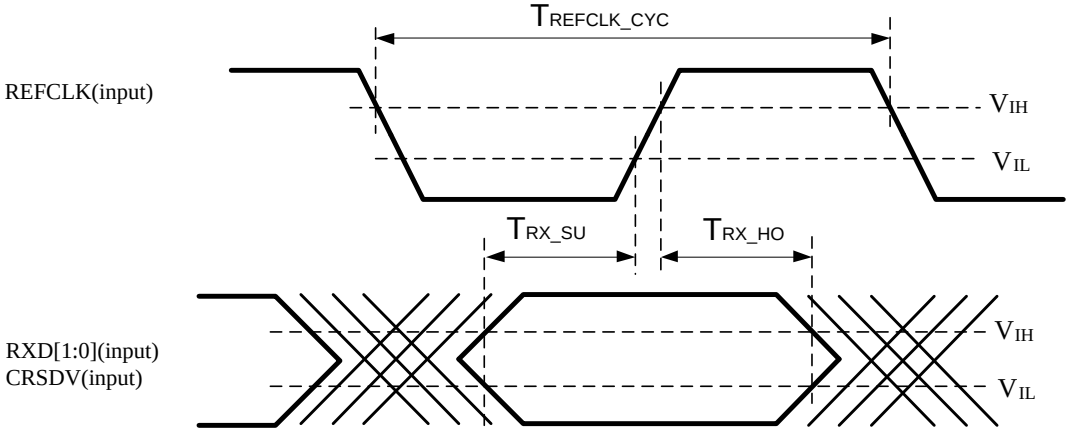


Figure 68. RMII MAC Mode Input Timing

Table 42. RMII MAC Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
REFCLK Cycle Time	T_{REFCLK}	50MHz Clock Input.	I	-	20	-	ns
TXD[1:0], TXEN to REFCLK Output Setup Time	T_{TX_SU}	-	O	6	-	-	ns
TXD[1:0], TXEN to REFCLK Output Hold Time	T_{TX_HO}	-	O	4	-	-	ns
RXD[1:0], CRSDV to REFCLK Input Setup Time	T_{RX_SU}	-	I	2	-	-	ns
RXD[1:0], CRSDV to REFCLK Input Hold Time	T_{RX_HO}	-	I	0	-	-	ns

10.5.12. RMII PHY Mode Timing

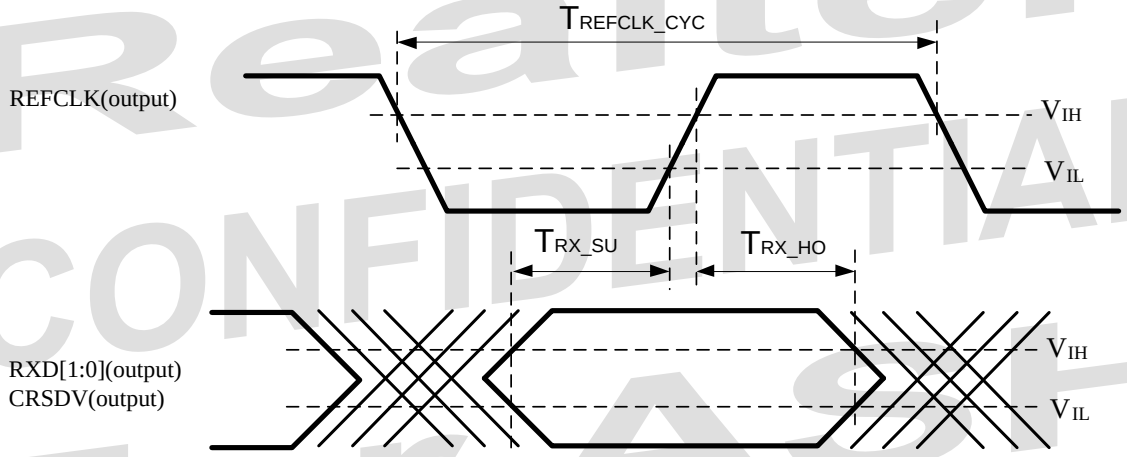


Figure 69. RMII PHY Mode Output Timing

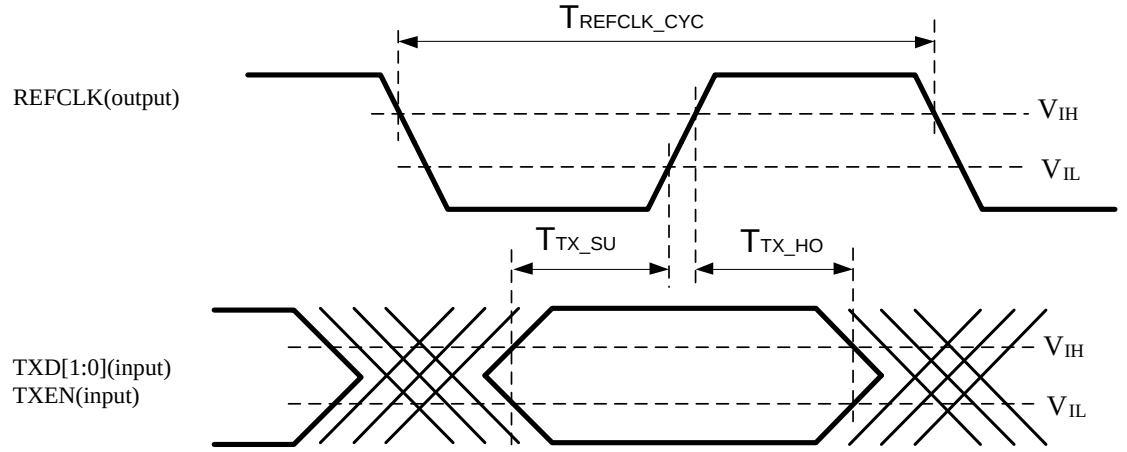


Figure 70. RMII PHY Mode Input Timing

Table 43. RMII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
REFCLK Cycle Time	T_{REFCLK}	50MHz Clock Input.	O	-	20	-	ns
TXD[1:0], TXEN to REFCLK Input Setup Time	T_{TX_SU}	-	I	2	-	-	ns
TXD[1:0], TXEN to REFCLK Input Hold Time	T_{TX_HO}	-	I	0	-	-	ns
RXD[1:0], CRSDV to REFCLK Output Setup Time	T_{RX_SU}	-	O	6	-	-	ns
RXD[1:0], CRSDV to REFCLK Output Hold Time	T_{RX_HO}	-	O	4	-	-	ns

10.5.13. HSGMII Differential Transmitter Characteristics

Table 44. HSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	319.968	320	320.032	ps	320ps±100ppm
T_X1	Eye Mask	-	-	0.175	UI	-
T_X2	Eye Mask	-	-	0.39	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	500	700	1000	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.65	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.35	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

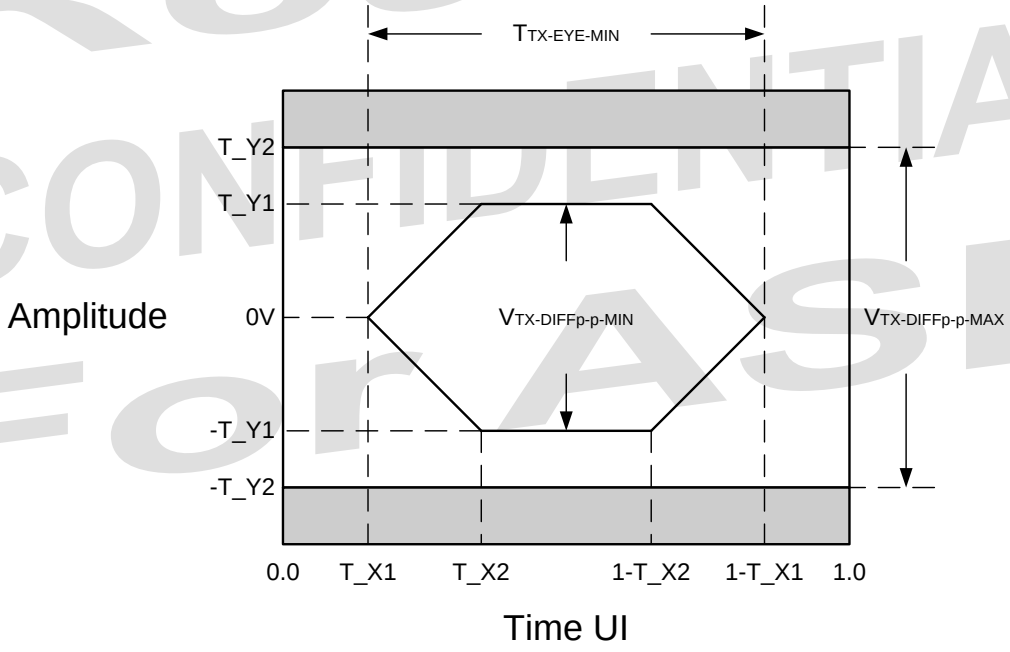


Figure 71. HSGMII Differential Transmitter Eye Diagram

10.5.14. HSGMII Differential Receiver Characteristics

Table 45. HSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	319.968	320	320.032	ps	320ps±100ppm
R_X1	Eye Mask	-	-	0.25	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.5	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.5	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

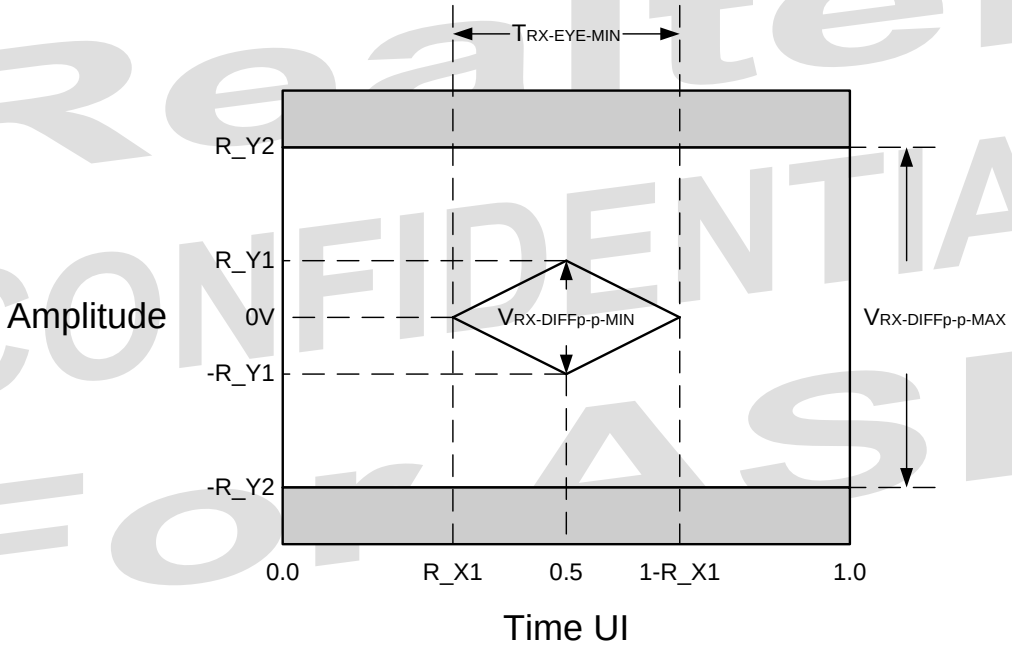


Figure 72. HSGMII Differential Receiver Eye Diagram

10.5.15. SGMII Differential Transmitter Characteristics

Table 46. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps±300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

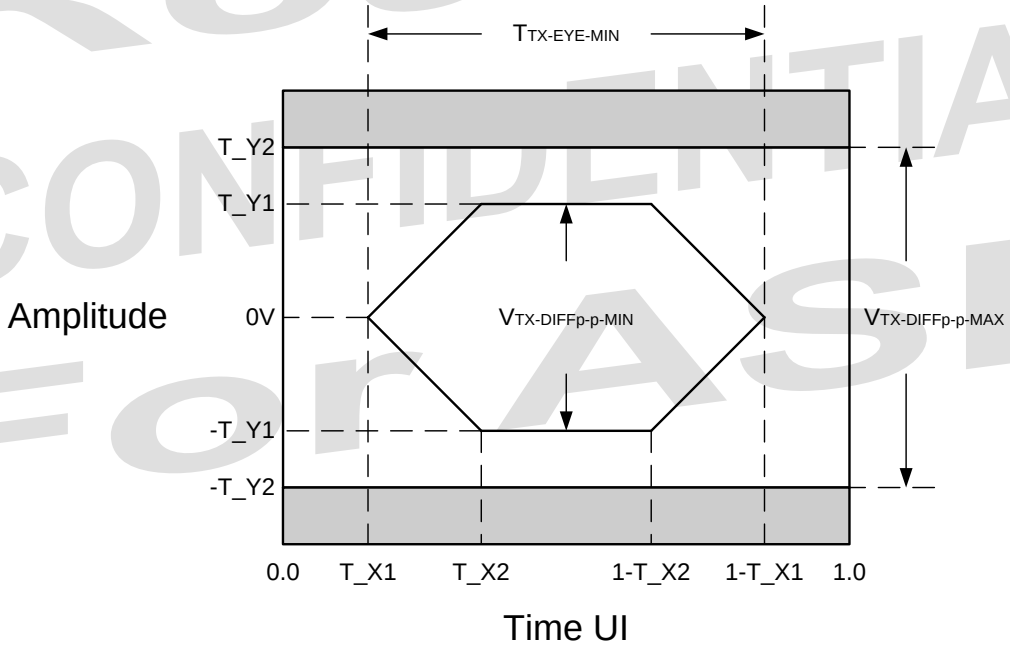


Figure 73. SGMII Differential Transmitter Eye Diagram

10.5.16. SGMII Differential Receiver Characteristics

Table 47. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps±300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

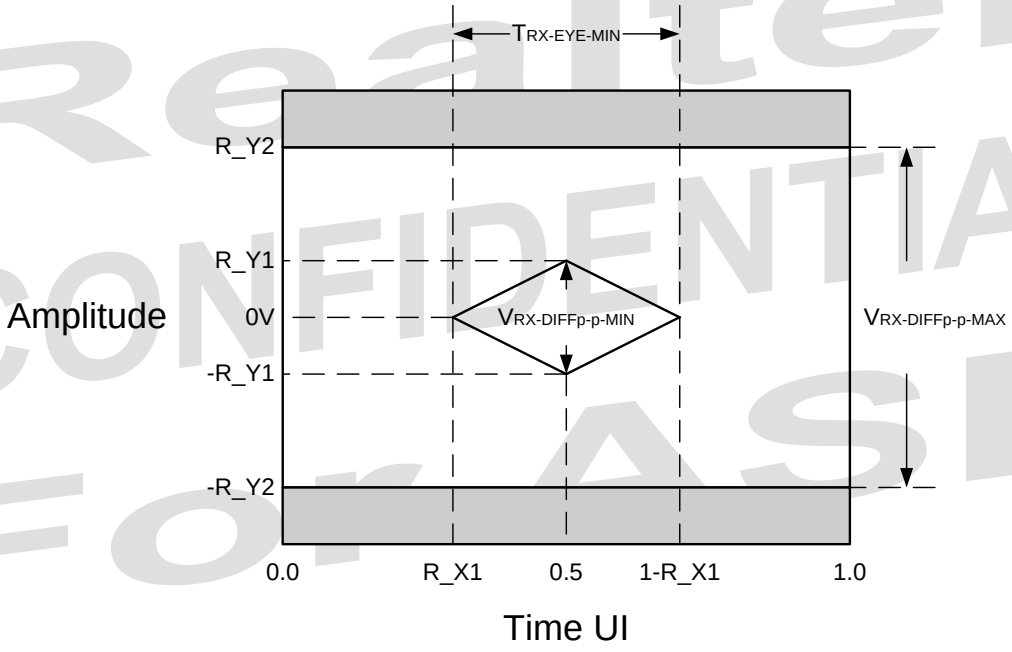


Figure 74. SGMII Differential Receiver Eye Diagram

10.5.17. 1000Base-X/100Base-FX Differential Transmitter Characteristics

Table 48. 1000Base-X/100Base-FX Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval (1000Base-X)	799.76	800	800.24	ps	800ps±300ppm
	Unit Interval (100Base-FX)	7.9976	8.0	8.0024	ns	8ns±300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	650	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	800	1300	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

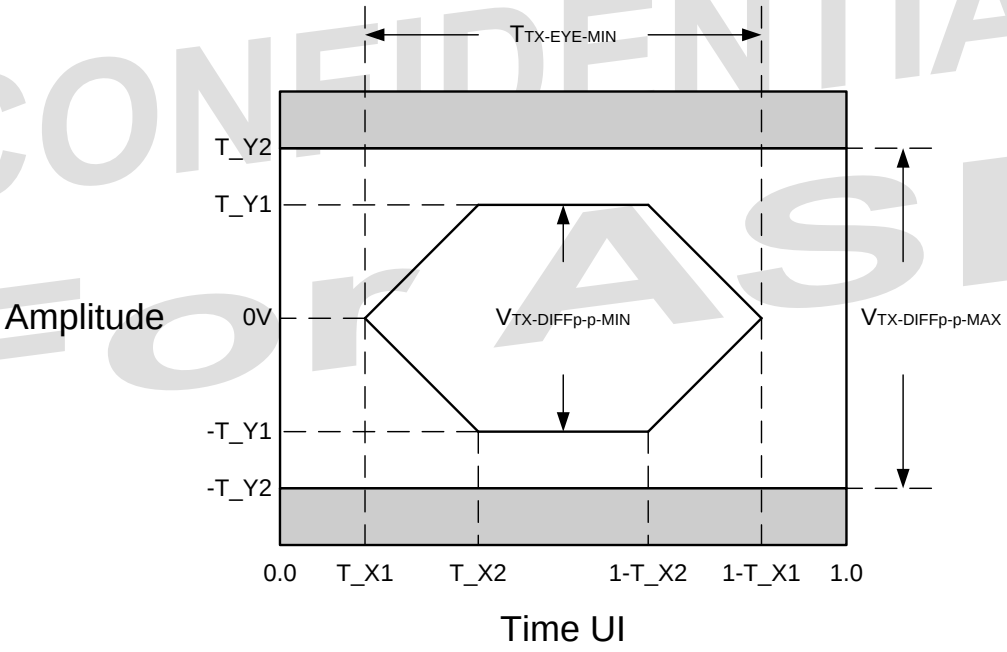


Figure 75. 1000Base-X/100Base-FX Differential Transmitter Eye Diagram

10.5.18. 1000Base-X/100Base-FX Differential Receiver Characteristics

Table 49. 1000Base-X/100Base-FX Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval (1000Base-X)	799.76	800	800.24	ps	800ps±300ppm
	Unit Interval (100Base-FX)	7.9976	8.0	8.0024	ns	8ns±300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

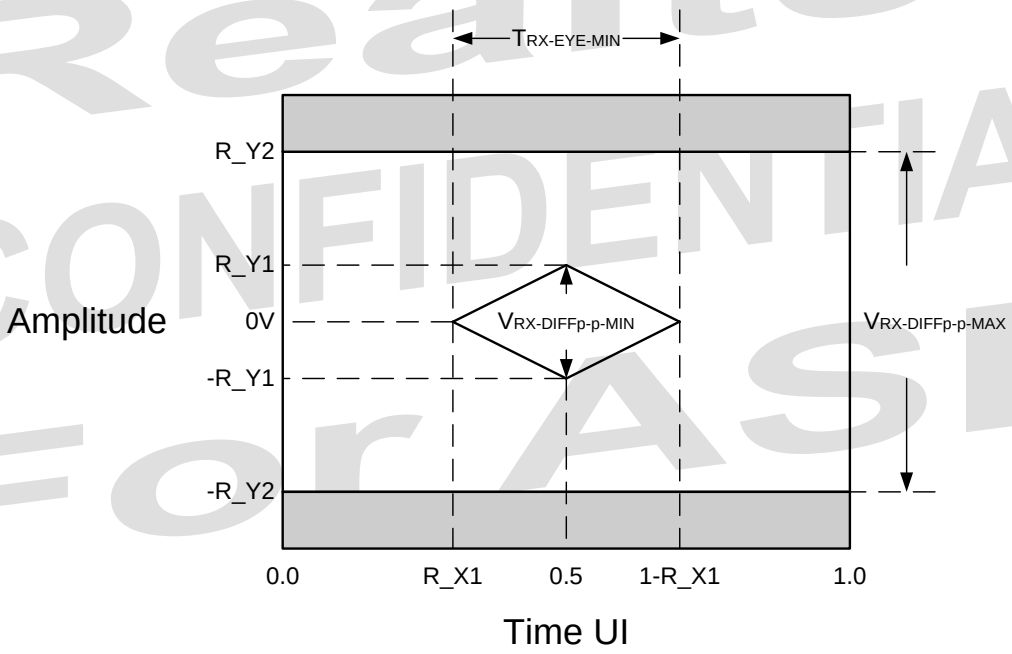


Figure 76. 1000Base-X/100Base-FX Differential Receiver Eye Diagram

10.6. Power and Reset Characteristics

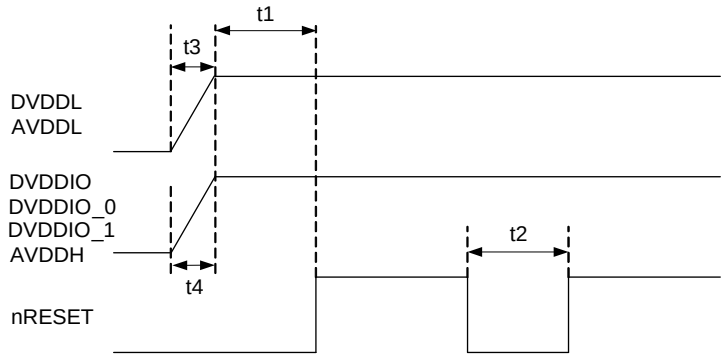


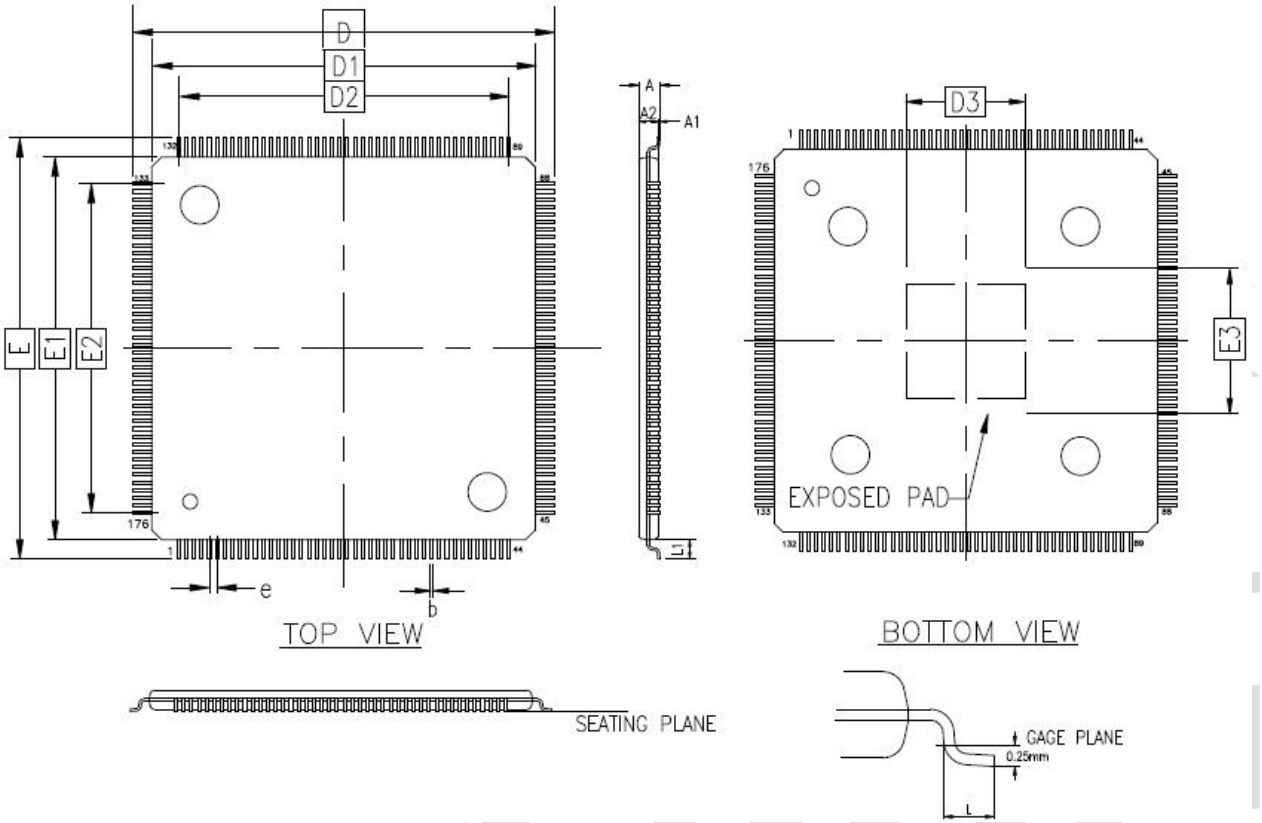
Figure 77. Power and Reset Characteristics

Table 50. Power and Reset Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Reset Delay Time	t1	The duration from all powers steady to the reset signal released to high.	I	10	-	-	ms
Reset Low Time	t2	The duration of reset signal remain low time for issuing a reset to RTL8370MB.	I	10	-	-	ms
VDDL Power Rising Settling Time	t3	DVDDL and AVDDL power rising settling time.	I	0.5	-	-	ms
VDDH Power Rising Settling Time	t4	DVDDIO, DVDDIO_0, DVDDIO_1, and AVDDH power rising settling time.	I	0.5	-	-	ms

11. Mechanical Dimensions

Thermally Enhanced Thin Quad Flat Pack (TQFP) 176 Leads 20x20mm Outline.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
D/ E		22.00BSC			0.866BSC	
D_1/ E_1		20.00BSC			0.787BSC	
D_2/ E_2		17.20BSC			0.677BSC	
D_3/ E_3	5.75	6.00	6.25	0.226	0.236	0.246
e		0.40BSC			0.016BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

12. Ordering Information

Table 51. Ordering Information

Part Number	Package	Status
RTL8370MB-CG	TQFP 176-Pin E-PAD ‘Green’ Package	-

Note: See page 10 for package identification information.

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