RTL8370N-VB
LAYER 2 MANAGED 8-PORT 10/100/1000 SWITCH CONTROLLER

RTL8370MB
LAYER 2 MANAGED 8+2-PORT 10/100/1000 SWITCH CONTROLLER

Layout guide
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8370N-VB/RTL8370MB chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2015-2-05	First Release

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1. General Description

The RTL8370N-VB is an LQFP128 E-PAD, high-performance 8-port Gigabit Ethernet switch.

The RTL8370N-VB feature low-power integrated 8-port Giga-PHYs that support 1000Base-T, 100Base-T, and 10Base-T.

The RTL8370MB is a TQFP176 E-PAD, high-performance 8+2-port Gigabit Ethernet switch. It integrates 8 low-power Giga-PHYs that support 1000Base-T/100Base-T/10Base-T, and provides two extra RGMII/MII/SGMII/1000Base-X/100Base-FX ports for specific applications. The RTL8370MB implements all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

Note: The RTL8370MB Extra Interface (Extension GMAC1 and Extension GMAC2) supports:
Reduced Gigabit Media Independent Interface (RGMII)
Media Independent Interface (MII)
Serial Gigabit Media Independent Interface (SGMII)
IEEE 1000Base-X
IEEE 100Base-FX

2. Application Diagram

2.1. RTL8370N-VB Application Diagram (Demo)

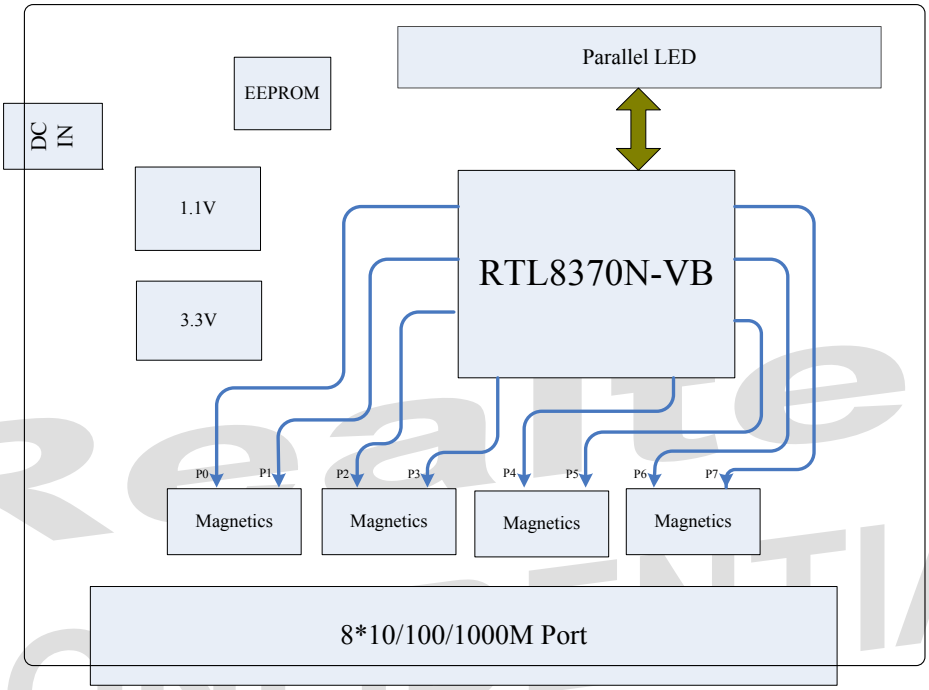

Figure1: 8-Port 1000Base-T Switch Application

2.2. RTL8370MB Application Diagram (Demo)

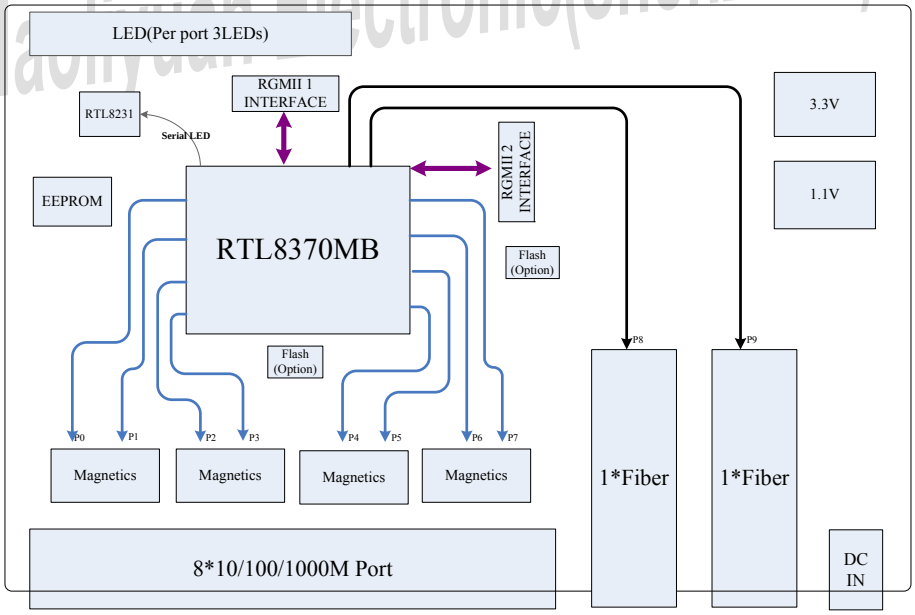

Figure2: 8-Port 1000Base-T+2-Port 1000Base-X/100Base-FX Switch Application

3. General Design and Layout

In order to achieve maximum performance with the RTL8370N-VB/RTL8370MB good design attention is required throughout the design and layout process. The following recommendations will help implement a high performance system.

3.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits. The following criteria are recommended; power noise of VDDH/DVDDIO should be under 100mV and power noise of VDDL should be under 50mV.
- Verify the critical components, such as clock source and transformer, to meet the application requirements.
- Keep ground noise levels below 50mV.
- Use bulk capacitors (4.7uF~10uF) between each power and ground plane.
- Use decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep 0.1uF decoupling capacitors as close as possible to the RTL8370N-VB/RTL8370MB.
- Fill in unused areas of top side and bottom side with solid copper and attach them with via to the ground plane.
- The transformer should be placed as close as possible to the RTL8370N-VB/RTL8370MB.
- The RJ-45 phone jack should be placed as close as possible to the transformer.
- Avoid right angles on all traces.
- Keep trace in the top layer and avoid layer change if possible.
- The MDIREF pin 17 of RTL8370N-VB must connect to GND via 2.49K±1% Ohm resister. This resister must be put as close as possible to RTL8370N-VB.
- The MDIREF pin 10 of the RTL8370MB must connect to GND via a 2.49K±1%Ohm resister. This resister must be put as close as possible to RTL8370MB.

4. Clock Circuit

- Place the crystal as close to the RTL8370N-VB/RTL8370MB as possible.
- Keep the trace between the crystal PIN and RTL8370N-VB/RTL8370MB clock PIN less than 800mil, and the spacing of XI and XO greater than 8mil.
- Surround the clock with ground trace to minimize high-frequency emissions if possible.
- Keep clearance area under the crystal or OSC component.
- Ensure clock traces have an unbroken reference ground plane.
- Don't let the clock trace pass over a gap in the ground plane.
- Use only one 1.5K pull up external resistance to 3.3V for SDA.
- Keep the SCK trace away from the other signals, to avoid unnecessary interference.

5. Power Planes

- When designing a 4-Layer PCB layout, divide the power plane into AVDDL, DVDDL, AVDDH and DVDDIO.
- Use 0.1μF decoupling capacitors and bulk capacitors between each power and ground.
- Keep the power trace in the top layer with might and main into the 2-Layer PCB.

6. Ground Planes

- Keep the ground region under the RTL8370N-VB/RTL8370MB.Avoid too many branches to achieve good heat conductive ability and a good signal return path.
- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground at least 80-mil.

7. E-PAD Layout Note

- Use multi-vias (drill size=20~24mil) in the RTL8370N-VB/RTL8370MB footprint and fill in large areas of component side and solder side with solid copper. Then attach them with vias to the ground plane in order to reduce the temperature of the chip.

8. RMII/SGMII/MII Signal Layout Guidelines

- Ninety-degree trace turns should be avoided. We recommend that the traces turn at 45 angles as shown in Figure 3. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

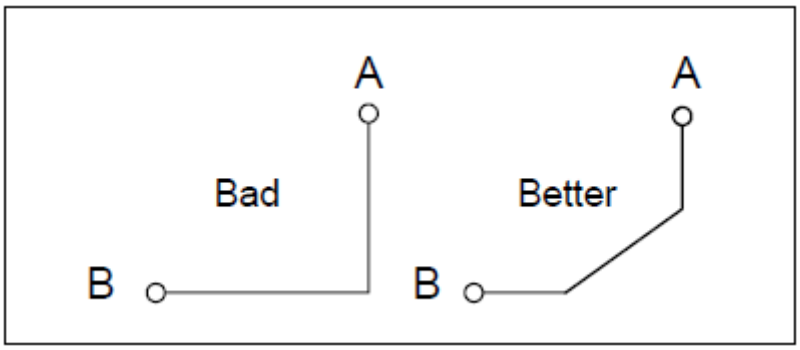

Figure3: Signal Trace Angles

- The trace length and the ratio of trace width or trace height above the ground planes should be carefully considered. Clock and other high speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a GND plane to surround them.
- For traces longer than 5 inches, guard traces should be placed between signal traces. The guard traces should have many GND vias.
- Place source termination resisters near output pins.

- Route the RGMII traces at 50ohm impedance. Match each RGMII TX and RX group to within 25mils.
- Avoid vias and layer change in RGMII interface if possible.

9. Ethernet MDI Differential Signals

- Keep differential-pair impedance at 100ohm±10%.
- All micro strip traces of a differential pair should be 5-mil wide with a 7-mil wide air gap spacing between the trace of the pair for 4-Layer PCB layout.
- All micro strip traces of a differential pair should be 7-mil wide with a 5-mil wide air gap spacing between the trace of the pair for 2-Layer PCB layout.
- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location.
- Avoid vias and layer change if possible.

10. Serdes Differential Signals

- Keep differential-pair impedance at 100ohm±10%.
- All micro strip traces of a differential pair should be 5-mil wide with a 7-mil wide air gap spacing between the trace of the pair for 4-Layer PCB layout.
- All micro strip traces of a differential pair should be 7-mil wide with a 5-mil wide air gap spacing between the trace of the pair for 2-Layer PCB layout.
- Both sides of the TX pair and RX pair should have a ground trace, and the ground trace should be attached with multiple vias to the ground plane in the 2-layer PCB.
- Match the length of both sets of the differential pairs, allowing no more than a 50-mil delta between the lengths of the two signals.
- Differential pairs should have a continuous reference plane, and avoid vias.
- Size 0402 AC coupling capacitors are strongly encouraged as the smaller the package size, the less ESL.
- Locate capacitors for coupled traces at the same location along the differential traces and near output pins of differential pairs.

11. ESD/EMI Protection

- Maintain an 80 mil minimum gap between two differential pairs or signal at the transformer second side to improve ESD protection.
- Maintain an 80 mil minimum gap between signal trace and chassis GND to improve ESD protection.
- Recommend to reserve the complete Bob-smith (75ohm/1% + 68pf/2KV) and Varistor of per 1*Port or 2*Ports. See Figure 4.

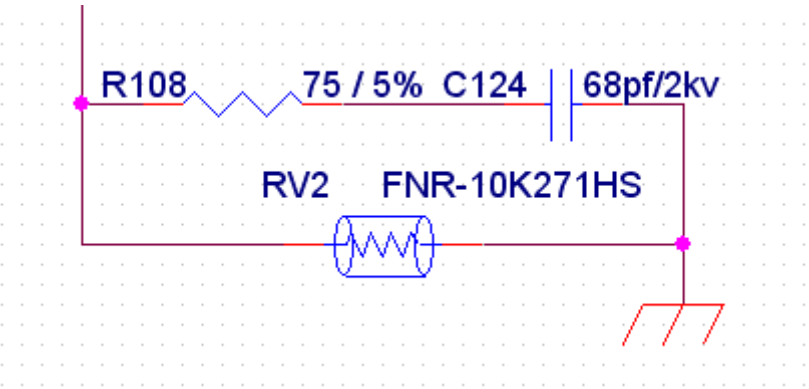

Figure4 Bob-smith and Varistor schematic

- Recommend to reserve the less than 15pF Capacitances at the MDI Bus and Place those capacitances near the transformers as close as possible for the good performance of system ESD/EMI. See Figure 5.

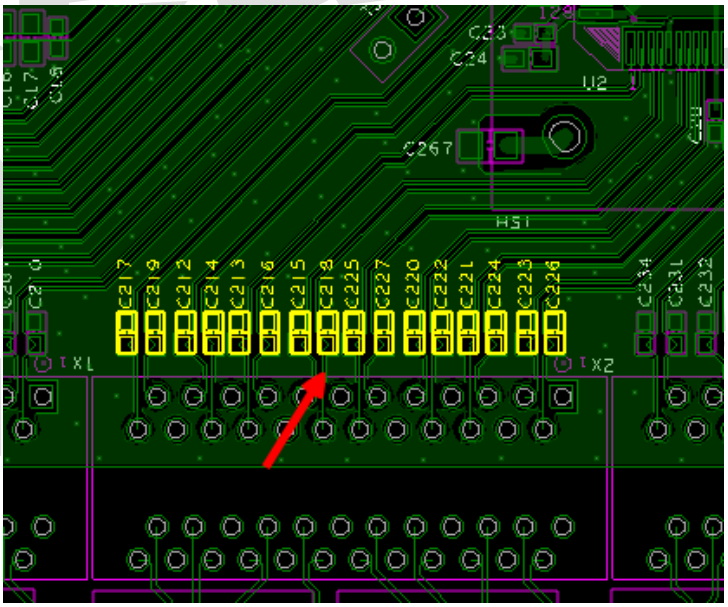

Figure5: Primary side transformer schematics

- Recommend to use the primary side transformers those schematics as Figure 6 for good performance of system EMI/ESD.

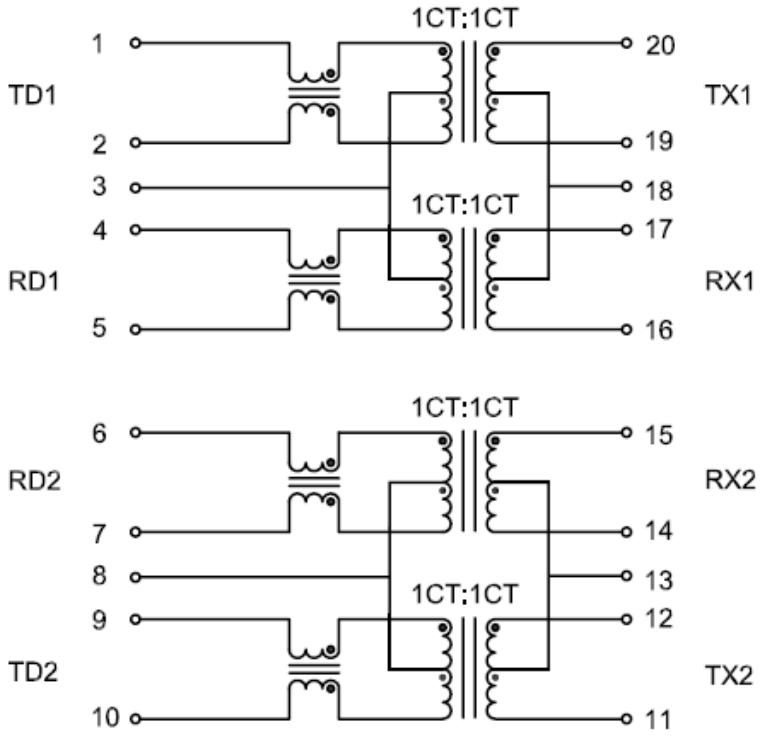

Figure6: Primary side transformer schematics

12. Transformer Options

- The RTL8370N-VB/RTL8370MB uses a transformer with a 1:1 turn ratio. There are many venders offering transformer designs that meet the RTL8370N-VB/RTL8370MB requirement. Examples are U-TRON GSA-4802-R, GTA-4801B-R, GSA-2401B-R, GTA-2401B-R; Pulse H511NL, H5007ANL; Bothhand G2PM109N LF and MNC G4801DG, G4802DG etc.

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