Link Street® 88E6172/88E6176 Datasheet

Low Power 7 Port Gigabit Switch with Energy Efficient Ethernet (EEE)

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Low Power 7 Port Gigabit Switch with Energy Efficient Ethernet (EEE)

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OVERVIEW

The Marvell® 88E6172/88E6176 devices are single-chip integrations of a 7-port Gigabit Ethernet switches with five integrated Gigabit Ethernet transceivers. This device supports “Best in Class” Quality of Service (QoS) and the highest “real world” performance. This device is uniquely suited for Small Office Home Office (SOHO) and Small-to-Medium Business (SMB) applications.

The device contains five 10/100/1000 triple speed Ethernet transceivers (PHYs), one Gigabit SERDES (88E6176 device only), and two digital interfaces that support a combination of GMII, RGMII, MII, and RMII interfaces in a 128-pin QFP package.

The device has a high-speed, non-blocking four traffic class QoS switch fabric that uses the unique Marvell Dynamic Queue Limit architecture. The QoS architecture switches packets into one of four traffic class queues based upon Port, IEEE 802.1p, IPv4 Type of Service (TOS) or Differentiated Services (Diff-Serv), IPv6 Traffic Class, 802.1Q VLAN ID, DA MAC address or SA MAC address. The device also contains a high-performance address lookup engine with support for up to 8K active nodes, and a 1 Mbit frame buffer memory. Back-pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The MAC units in the devices comply fully with the applicable sections of IEEE 802.3 and support frame sizes up to 10KBytes.

The sixth and seventh ports’ interfaces support a direct connection to Management or Router CPUs with integrated MACs. These interfaces, along with BPDU handling for IEEE 802.1D Spanning Tree Protocol, 802.1w Rapid Spanning Tree, 802.1s Multiple VLAN Spanning Tree, programmable per-port VLAN configurations, 802.1Q and Port States, support fully managed switches and truly isolated WAN vs. LAN firewall applications. The device supports 4,096 802.1Q VLAN IDs which can be enabled on a per port basis. Three levels of 802.1Q security is supported with error frame trapping and logging.

The device supports multiple address databases (up to 4096), which allows packet routing without modification of the MAC address. This allows the same MAC address to exist multiple times in the MAC Address database with multiple port mappings, to completely isolate the WAN from the LAN database.

The 88E6176 device’s Gigabit SERDES interface supports SGMII, 1000BASE-X and 100BASE-FX. It can be configured to act as the fifth or sixth port on the device.

The PHY units in the device support the latest 802.3az Energy Efficient Ethernet (EEE) standard. They are designed with Marvell® cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. The device also integrates MDI interface termination resistors into the PHYs. This resistor integration facilitates board layout and reduces board cost by reducing the number of external components. Both the PHY and MAC units in the devices comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

The PHYs also include an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

The 88E6172/88E6176 also supports Wake-on-LAN and Wake on Frame event detection allowing an attached CPU to enter sleep mode and enabling even greater system power savings.

Up to 12 LEDs can be directly driven by the device, which supports both single and dual color LEDs. The combining of multiple ports Link/Activity LED into a single LED is also supported.

The devices many operating modes can be configured using SMI (serial management interface - MDC/MDIO). The devices also support a standalone QoS mode or configuration via a low cost serial EEPROM.

The devices are designed for cost-sensitive Gigabit Ethernet switch systems that require Quality of Service, Trunking, Stacking, and/or Spanning Tree.

Highlighted Features

- Supports 802.3az Energy Efficient Ethernet
- Wire speed performance with Maximum Frame size up to 10K Bytes
- 'Best-in-Class' per port TCP/IP Ingress Rate Limiting along with independent Storm Prevention
  - 5 Ingress Rate Limiting buckets per port, supporting Rate-based and Priority-based rate limiting
  - Non-Rate Limited frames based on SA or DA
- Per port, programmable MAC hardware address learn limiting
- Wake-on-LAN and Wake of Frame Event Detection
- Layer 2 Policy Control List (PCL) enables drop, trap, or mirroring based on SA, DA, VID, Ethertype, VBAS, PPPoE, UDP, and DHCP Option 82
- Remote Management capabilities allow device configuration and readback via Ethernet frames
- Per port, programmable MAC hardware address learn limiting
- Quality of Service support with four traffic classes
- QoS determined by Port, IEEE 802.1p tagged frames, IPv4's Type of Service (TOS) & Differentiated Services (DS), IPv6's Traffic Class 802.1Q VID, Destination MAC address, or Source MAC address
- DSCP (layer 3) to frame priority (layer 2) marking
- Frame priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Queue priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Strict, Weighted, or mixed mode QoS selectable per port
- Globally Programmable QoS weighting via a 128-entry table
- 802.1Q VLAN support for the full 4,096 VLAN IDs
- Supports multiple provider ports within a single chip via a programmable Ethertype per port
- Enhanced 802.1s Per VLAN Spanning Tree supporting up to 64 spanning tree instances
- Single Link/Activity LED programmable across multiple ports
  - Single and Dual color LED support for Link, Speed, Duplex Mode, Collision, and Tx/Rx Activities

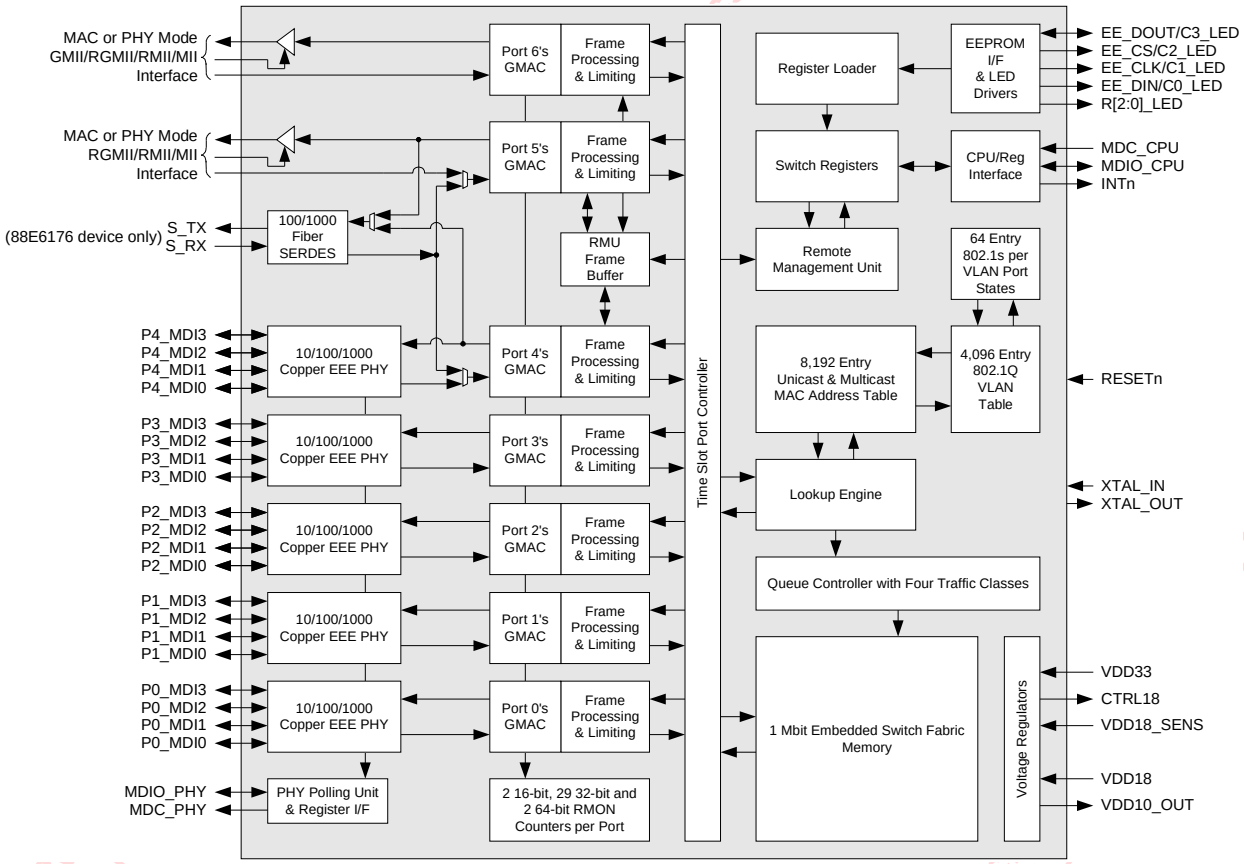
Features

- Single 3.3V supply
- Marvell® Header for increased Routing performance
- Shared 1 Mbit on-chip memory-based switch fabric with true non-blocking switching performance
- High performance lookup engine with support for up to 8K unicast or multicast MAC address entries with automatic learning and aging
- MAC SA based 802.1X authentication
- Port Trunking and Port Monitoring/Mirroring
- Egress tagging/untagging selectable per port or by 802.1Q VLAN ID
- Port based VLANs supported in any combination across multiple chips
- Port States & BPDU handling for Spanning Tree
- 28 32-bit and 2 64-bit RMON Counters per port
- Egress Rate shaping on all ports
- Integrated Gigabit SERDES supporting SGMII, 1000BASE-X, and 100BASE-FX (8E6176 device only)
- Supports Media Detect mode for copper and fiber support when paired with Port 4's PHY (88E6176 device only)
- Ports 5 and 6 support RGMII/MII/RMII interfaces. Additionally, Port 6 also supports a GMII interface
- Integrated with five independent Auto-Crossover Ethernet transceivers fully compliant with the applicable sections of IEEE802.3 and IEEE802.3u
  - Integrated MDI interface termination resistors
  - Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- Requires a low-cost 25 MHz XTAL clock source
- Supports 4-Wire 93C56/93C66 or 2-Wire 24C01/24C02/24C04 EEPROMs
  - Able to program attached EEPROMs and save configurations
- 14 x 14mm 128-pin TQFP package
- Low power dissipation P_{AVE} = less than 2W
- Available in Commercial grade temperature specification
- 88E6176 device is available in Industrial grade temperature specification

Applications

- Gigabit Ethernet broadband router with four 1000BASE-TX LAN ports and one 1000BASE-TX or 1000BASE-X WAN port
- 5 port Gigabit Ethernet Switch

Figure 1: 88E6172/88E6176 Top Level Block Diagram



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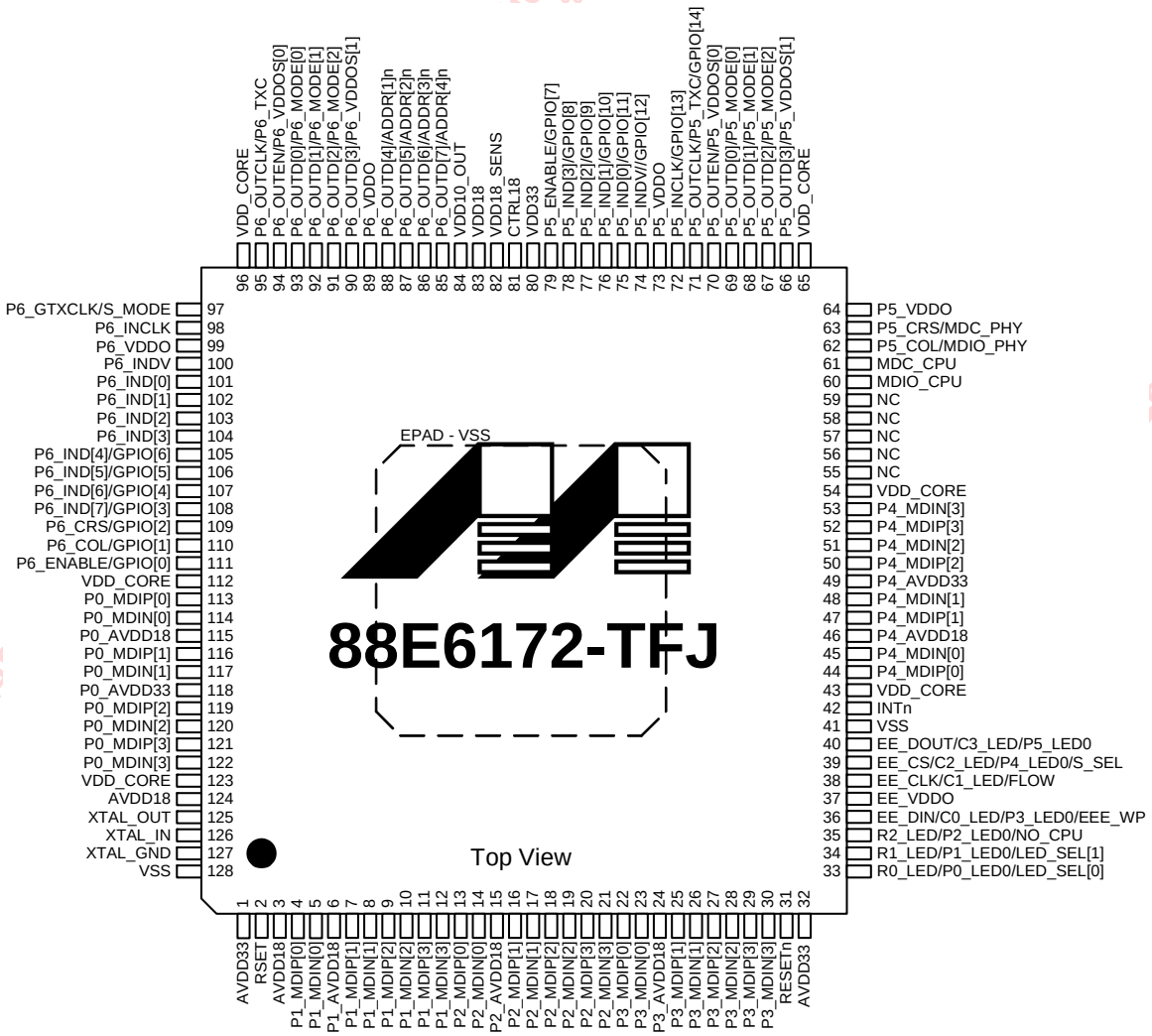
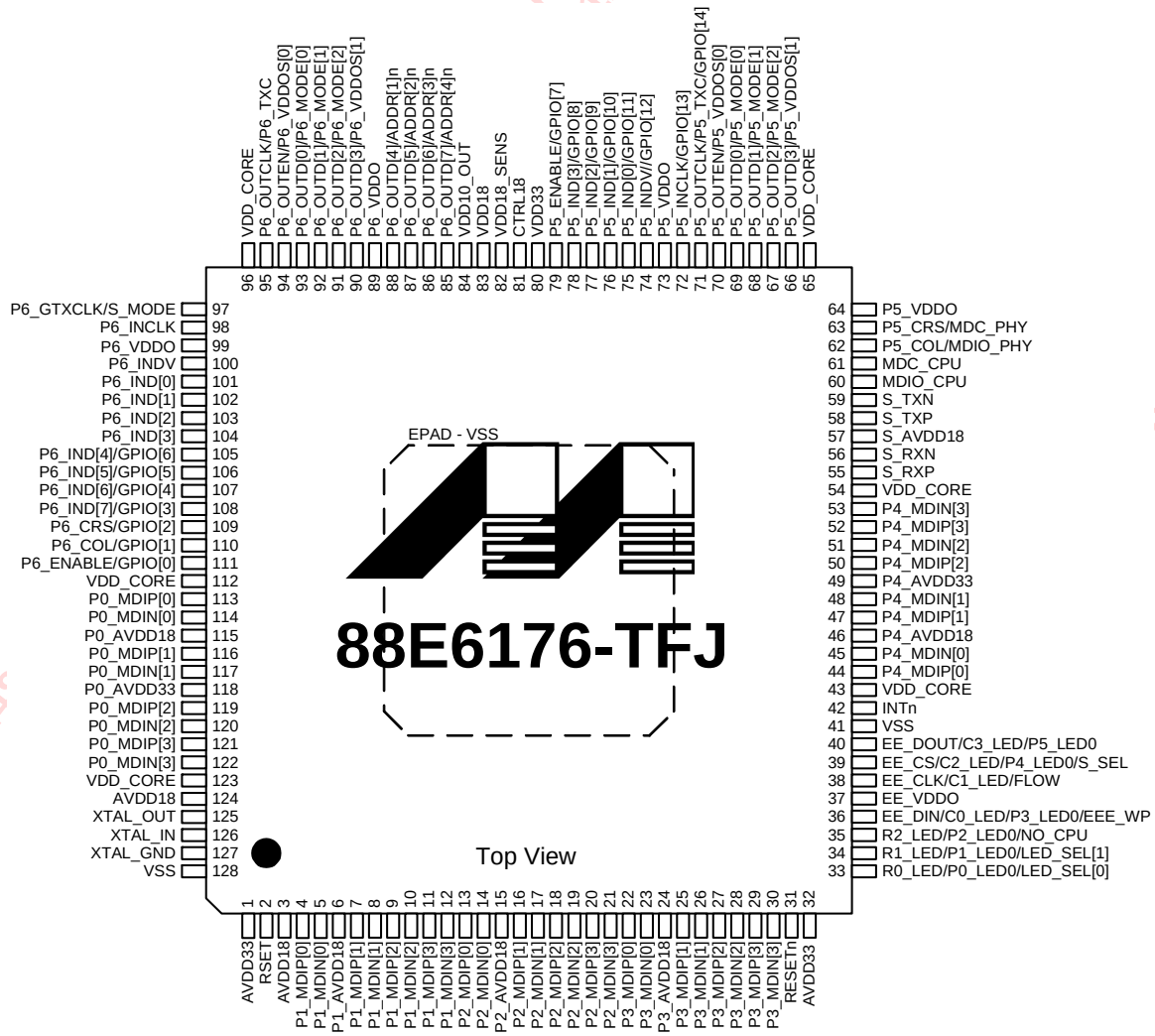


Figure 3: 88E6176 Device Pinout



1.1 Pin Description

Table 1: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability
Analog	Analog pin

Note The MDI pins are internally terminated and do not need external termination resistors.

Table 2: Network 10/100/1000 PHY Interface (Ports 0 to 4)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
44 22 13 4 113 45 23 14 5 114	44 22 13 4 113 45 23 14 5 114	P4_MDIP[0] P3_MDIP[0] P2_MDIP[0] P1_MDIP[0] P0_MDIP[0] P4_MDIN[0] P3_MDIN[0] P2_MDIN[0] P1_MDIN[0] P0_MDIN[0]	I/O	Media Dependent Interface [0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] corresponds to BI_DA±. In MDIX configuration, MDIP/N[0] corresponds to BI_DB±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. **NOTE:** Unused MDI pins must be left floating.
47 25 16 7 116 48 26 17 8 117	47 25 16 7 116 48 26 17 8 117	P4_MDIP[1] P3_MDIP[1] P2_MDIP[1] P1_MDIP[1] P0_MDIP[1] P4_MDIN[1] P3_MDIN[1] P2_MDIN[1] P1_MDIN[1] P0_MDIN[1]	I/O	Media Dependent Interface [1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] corresponds to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. **NOTE:** Unused MDI pins must be left floating.
50 27 18 9 119 51 28 19 10 120	50 27 18 9 119 51 28 19 10 120	P4_MDIP[2] P3_MDIP[2] P2_MDIP[2] P1_MDIP[2] P0_MDIP[2] P4_MDIN[2] P3_MDIN[2] P2_MDIN[2] P1_MDIN[2] P0_MDIN[2]	I/O	Media Dependent Interface [2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] corresponds to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. **NOTE:** Unused MDI pins must be left floating.
52 29 20 11 121 53 30 21 12 122	52 29 20 11 121 53 30 21 12 122	P4_MDIP[3] P3_MDIP[3] P2_MDIP[3] P1_MDIP[3] P0_MDIP[3] P4_MDIN[3] P3_MDIN[3] P2_MDIN[3] P1_MDIN[3] P0_MDIN[3]	I/O	Media Dependent Interface [3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] corresponds to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. **NOTE:** Unused MDI pins must be left floating.

Table 3: SGMII/100BASE-FX/1000BASE-X Interface

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
--	55	S_RXP	Input	Receiver input – Positive. S_RXP connects directly to the fiber-optic receiver's positive output or to another device's TXP (Transmitter output – Positive) pins.
--	56	S_RXN	Input	Receiver input – Negative. S_RXN connects directly to the fiber-optic receiver's negative output or to another device's TXN (Transmitter output – Negative) pins.
--	58	S_TXP	Output	Transmitter output – Positive. S_TXP connects directly to the fiber-optic transmitter's positive input or to another device's RXP (Receiver input – Positive) pins.
--	59	S_TXN	Output	Transmitter output – Negative. S_TXN connects directly to the fiber-optic transmitter's negative input or to another device's RXN (Receiver input – Negative) pins.

Note The SERDES interface supports an SDET signal input on any GPIO pin.

Table 4: Reference, Clock, and Reset

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
2	2	RSET	Analog	Resistor Current reference. A 4.99 kohm 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.
126	126	XTAL_IN	Input	25 MHz system reference clock input provided from the board. The clock source can come from an external crystal or an external 1.8V oscillator. This is the only clock required. Refer to Section 3.6.2, Clock Timing for timing requirements.
125	125	XTAL_OUT	Output	System reference clock output provided to the board. This output can only be used to drive an external crystal. It cannot be used to drive external logic. If an external oscillator is used this pin should be left unconnected.
127	127	XTAL_GND	Input	Analog Ground for the XTAL. The external crystal circuit requires capacitors to be connected to the XTAL_IN and XTAL_OUT pins. The other side of these capacitors must be connected to this pin instead of being directly connected to the ground plane. Use as short of a trace as possible.
31	31	RESETn	I/O	Hardware reset. Active low input and output. As an output, RESETn is driven low when power is first applied to the device. It will stay low for 8 to 14 mSec (10 mSec typical). In this mode RESETn can be used to reset other devices on a board while at the same time resetting this device itself. After this time, RESETn becomes an input. As an input, when RESETn is driven low by an external device, this device will then drive RESETn low as an output for 8 to 14 mSec (10 mSec typical). In this mode RESETn can be used to debounce a hardware reset switch. This pin requires an external resistor and capacitor. When RESETn is low all configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or some time after. Refer to Section 3.6.1, Reset and Configuration Timing for details.

Table 5: Port Status LEDs (Ports 0 to 6)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
35	35	R2_LED /P2_LED0 /NO_CPU	Typically Output, PU	Parallel multiplexed LED outputs. These active low LED pins directly drive the port's LEDs supporting a range from 1 to 12 LEDs in a multiplexed fashion. In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to one of the Cx_LED pins below (see Section 2.4, LED Interface for details). These same pins can be used to directly drive from 1 to 6 LEDs in a non-multiplexed fashion (3 from this set of pins – P[2:0]_LED0). In this In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to a power source. The LEDs can be configured to display many options. The LEDs are turned on whenever RESETn is low so their functionally can be visually verified during PCB manufacturing testing. R[2:0]_LED are multifunction pins which are used to configure the device after a hardware reset. After reset is asserted, the Px_LED pins become inputs and the configuration information below is latched 1 mSec after the rising edge of RESETn as follows: R[1:0]_LED: LED_SEL[1:0] 0 = Link/Activity with Speed by Blink Rate 1 = Link/Activity with Speed by 3 Colors 2 = Separate Link/Activity by Speed 3 = Link/Activity with Separate Speed **NOTE:** See Section 2.4, LED Interface for a complete description of each of these LED Selections P2_LED: NO_CPU 0 = CPU is attached 1 = No CPU is attached When the 'CPU is attached' mode is selected, all the ports will be initialized in the Disabled Port State and the PHYs will be powered down. This allows software time to boot and fully configure the switch before it allows packets to flow through it. R[2:0]_LED are internally pulled high via a resistor so the pins can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration low.
34	34	R1_LED /P1_LED0 /LED_SEL[0]		
33	33	R0_LED /P0_LED0 /LED_SEL[0]		

Table 5: Port Status LEDs (Ports 0 to 6) (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
40	40	EE_DOUT /C3_LED /P5_LED0	I/O, PU	Serial EEPROM data out from a 4-wire EEPROM device or Serial EEPROM data I/O to/from a 2-wire EEPROM device and Column 3 for the LEDs. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive (and send if 2-wire EEPROM) the EEPROM (address[1]/) data (to/) from the external serial EEPROM (if present). 2-wire EEPROMs require that this pin is connected to EE_VDDO through a 4.7 kohm pull-up resistor. EE_DOUT is a multi-function pin which is also used to connect to the anode of LED column 3 for each row, if used in the multiplexed LED mode (see R[2:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P5_LED0). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. EE_DOUT is internally pulled high via a resistor so the pin can be left floating when unused.
39	39	EE_CS /C2_LED /P4_LED0 /S_SEL	Typically Output, PD	Serial EEPROM chip select and Column 2 for the LEDs. EE_CS is the 4-wire serial EEPROM chip select referenced to EE_CLK. It is used to enable the external 4-wire serial EEPROM (if present), and to delineate each data transfer. The pin is not used for 2-wire serial EEPROMs. EE_CS is a multi-function pin which is also used to connect to the anode of LED column 2 for each row, if used in the multiplexed LED mode (see R[2:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P4_LED0). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. It is also used to configure the device after a hardware reset. After reset is asserted, EE_CS becomes an input and the S_SEL SERDES configuration information below is latched 1mSec after the rising edge of RESETn as follows: 0 = Connect the SERDES to Port 4's MAC 1 = Connect the SERDES to Port 5's MAC only if P5_MODE = 0x6 (else the SERDES is disabled and powered down) EE_CS is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to EE_VDDO for a configuration high.

Table 5: Port Status LEDs (Ports 0 to 6) (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
38	38	EE_CLK /C1_LED /FLOW	Typically Output, PD	Serial EEPROM clock and Column 1 for the LEDs. EE_CLK is the serial EEPROM clock reference output by the devices. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin which is also used to connect to the anode of LED column 1 for each row, if used in the multiplexed LED mode (see R[2:0]_LED above). This pin is not used when the LEDs are in a non-multiplexed mode. It is also used to configure the device after a hardware reset. After reset is asserted, EE_CLK becomes an input and the configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0 = Disable flow control on all ports 1 = Enable advertisement of full-duplex flow control on all PHYs and enable “forced collision” flow control on all half duplex ports Full-duplex flow control requires support from the end station. It is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (i.e., FLOW = 0x1 at reset), and sees that the end station also supports Pause (from data returned during Auto-Negotiation). Half-duplex flow control is active on all half-duplex ports when enabled. EE_CLK is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to EE_VDDO for a configuration high.

Table 5: Port Status LEDs (Ports 0 to 6) (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
36	36	EE_DIN /C0_LED /P3_LED0 /EEE_WP	Typically Output, PD	Serial EEPROM data into the 4-wire EEPROM devices and Column 0 for the LEDs. EE_DIN is serial EEPROM data referenced to EE_CLK used to transmit the EEPROM command and address to the external 4-wire serial EEPROM (if present). The pin is not used for 2-wire serial EEPROMs. EE_DIN is a multi-function pin which is also used to connect to the anode of LED column 0 for each row, if used in the multiplexed LED mode (see R[2:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P3_LED0). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. It is also used to configure the device after a hardware reset. After reset is asserted, EE_DIN becomes an input and the configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0 = Enable Energy Efficient Ethernet (EEE) in the PHYs and the EEPROM is write enabled 1 = Disable Energy Efficient Ethernet (EEE) in the PHYs and the EEPROM is write protected EE_DIN is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to EE_VDDO for a configuration high.

1. The address is sent out the EE_IO pin only for 2-wire EEPROMs.

Table 6: Port 5 xMII Receive Interface Enable

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
79	79	P5_ENABLE /GPIO[7]	Input, PU	Port 5's RGMII/MII interface enable (generically referred to as xMII5) or GPIO[7]. When this pin is P5_ENABLE, setting this pin high will enable the output drivers on the xMII5 interface pins, brings link up on Port 5 and enables the interface to transmit and receive data if the port's PortState bits allow it. When this pin is low, xMII5's output pins will be disabled (i.e., they are tri-stated). P5_ENABLE acts as Link status and is reflected in the registers (Port Offset 0x0). This pin becomes GPIO[7] if P5_MODE is 0x6 (xMII disabled) or the pin is configured to become GPIO[7] (Global 2 offset 0x1A). P5_ENABLE is internally pulled high so the pin can be left floating to enable Port 5's interface.

Table 7: Port 5 xMII Receive Interface

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
72	72	P5_INCLK /GPIO[13]	I/O, PU	Input Clock. INCLK is a reference for INDV and IND. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. INCLK is an output when the xMII is configured in MII PHY mode. When Port 5 is configured by P5_MODE to be RMII PHY mode or RMII MAC mode, or disabled, this pin becomes GPIO[13]. INCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left floating when unused.
78 77 76 75	78 77 76 75	P5_IND[3] /GPIO[8] P5_IND[2] /GPIO[9] P5_IND[1] /GPIO[10] P5_IND[0] /GPIO[11]	Input, PU	Input Data. IND[3:0] (or IND[1:0] where appropriate) receives the data to be sent into the switch. In RGMII mode IND[3:0] are used as RXD[3:0]. When Port 5 is disabled (by P5_MODE = 0x6) these pins become GPIO[8:11]. When Port 5 is configured by P5_MODE to be RMII PHY mode or RMII MAC mode, then P5_IND[5:2] become GPIO[9:8]. The IND pins are internally pulled high via resistor so the pins can be left floating when unused.

Table 7: Port 5 xMII Receive Interface (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
74	74	P5_INDV /GPIO[12]	Input, PD	Input Data Valid. Input Data Valid is used to indicate when IND[3:0] contains frame information. INDV must be synchronous to INCLK. In RGMII mode INDV is used as RX_CTL. When Port 5 is disabled (by P5_MODE = 0x6) this pin becomes GPIO[12]. INDV is internally pulled low via resistor so the pin can be left floating when unused.
63	63	P5_CRS /MDC_PHY	Input/Output, PU	Carrier Sense or Management Data Clock, Master. Carrier sense is used to indicate carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. In MII MAC mode, P5_CRS is an input. In MII PHY mode, this pin is an output. This pin is only used when port is operating in half-duplex mode. In all other modes this pin is MDC_PHY and is used to manage external PHY devices connected to Ports 4, 5, and 6. Management Data Clock, Master mode, is the reference clock output for the serial management interface (SMI) that connects to an external SMI slave device, typically external PHYs. This pin is MDC_PHY when the port's Px_MODE <> 0x1 or 0x2. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P5_ ENABLE.

Table 7: Port 5 xMII Receive Interface (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
62	62	P5_COL /MDIO_PHY	Input/Output, PU	Collision or Management Data I/O, Master. Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. COL is not synchronous to INCLK. COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's Px_MODE = 0x1 or 0x2. COL is an output for Px_MODE = 0x1 and its an input for Px_MODE = 0x2. Management Data I/O, Master is used to transfer management data in and out of the device synchronously to MDC_PHY. This pin requires an external pull-up resistor in the range of 4.7K to 10kohm. This pin is MDIO_PHY when the port's Px_MODE <> 0x1 or 0x2. This device uses Device Addresses 0x05 to 0x06 to access the external PHYs for ports 5 to 6 respectively. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P5_ENABLE.

Table 8: Port 5 xMII Transmit Interface

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
70	70	P5_OUTEN /P5_VDDOS[0]	Typically Output, PD	P5 Output Enable. Output Enable is used to indicate when OUTD[3:0] contains frame information. OUTEN is synchronous to OUTCLK in all modes. In RGMII mode OUTEN is used as TX_CTL. P5_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin becomes an input and the configuration information below is latched at the rising edge of RESETn: If P5_VDDOS[1], below on the P5_OUTD[3] pin, is high at the rising edge of RESETn: 0 = The P5_VDDO pins are powered by 3.3 volts 1 = The P5_VDDO pins are powered by 2.5 volts If P5_VDDOS[1], below on the P5_OUTD[3] pin, is low at the rising edge of RESETn: X = The P5_VDDO pins are powered by 1.8 volts See P5_VDDO for the list of pins that are powered by this rail. P5_OUTEN is tri-stated during RESETn or when P5_ENABLE is low. OUTEN is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration high.
71	71	P5_OUTCLK /P5_TXC /GPIO[14]	Input/Output, PU	Output Clock. OUTCLK is a clock reference for OUTEN and OUTD[3:0] when the port is in MII mode. The speed of OUTCLK is 50 MHz, 25 MHz or 2.5 MHz depending the speed of the Port. The direction of OUTCLK is a function of the port's Px_MODE and the port's PHY Detect bit (Port offset 0x00). See the C_Mode bits in Port offset 0x00. In RGMII mode OUTCLK is used as TXC. When Port 5 is disabled (by P5_MODE = 0x6) this pin becomes GPIO[14]. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 8: Port 5 xMII Transmit Interface (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
66	66	P5_OUTD[3] / P5_VDDOS[1]	Typically Output, PU	Output Data. OUTD[3:0] outputs the data to be transmitted from the switch. OUTD is synchronous to OUTCLK in all modes. In RGMII mode OUTD[3:0] are used as TXD[3:0]. P5_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: OUTD[2:0] = P5_MODE[2:0] OUTD[3] = P5_VDDOS[1] P5_MODE[2:0] sets Port 5's Mode of operation as follows: 0x0 = Reserved for future use 0x1 = MII PHY mode w/output P5 MII CLKs[1] at 2.5, 25, or 50 MHz[2] 0x2 = MII MAC mode w/input P5 MII CLKs 0x3 = Reserved for future use 0x4 = RMII PHY Mode w/output Px_OUTCLK at 50 MHz 0x5 = RMII MAC Mode w/input Px_OUTCLK at 50 MHz 0x6 = Port 5 disabled (with its pins tri-stated)[3] 0x7 = RGMII mode P5_VDDOS[1] selects the P5 voltage setting as follows: 0x0 = P5_VDDO pins are powered by 1.8 volts 0x1 = P5_VDDO pins are powered by 2.5 or 3.3 volts. (P5_VDDOS[0], above on the P5_OUTEN pin, is used to select between 2.5 and 3.3 volts. See P5_VDDO for the list of pins that are powered by this rail. P5_OUTD pins are tri-stated during RESETn or when P5_ENABLE is low. OUTD pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7kohm resistor to VSS for a configuration low.
67	67	P5_OUTD[2] /P5_MODE[2]		
68	68	P5_OUTD[1] / P5_MODE[1]		
69	69	P5_OUTD[0] /P5_MODE[0]		

1. P5's MII CLKs refer to both P5_OUTCLK and P5_INCLK.
2. P5_OUTCLK's frequency is determined by the port's ForceSpd and 200BASE bits (Port offset 0x01).
3. In this mode many of P5's pins become the GPIO[13:7] pins.

Table 9: Port 6 xMII Receive Interface Enable

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
111	111	P6_ENABLE /GPIO[0]	Input, PU	Port 6's GMII/RGMII/MII interface enable (generically referred to as xMII6) or GPIO[6]. When this pin is P6_ENABLE, setting this pin high will enable the output drivers on the XMII6 interface pins, brings link up on Port 6 and enables the interface to transmit and receive data if the port's PortState bits allow it. When this pin is low, xMII6's output pins will be disabled (i.e., they are tri-stated). P6_ENABLE acts as Link status and is reflected in the registers (Port, Offset 0x0) if no PHY is detected connected to the port. This pin becomes GPIO[0] if P6_MODE is 0x6 (xMII disabled) or the pin is configured to become GPIO[0] (Global 2 offset 0x1A). As a GPIO this pin can become an output. P6_RGMII_EN is internally pulled high so the pin can be left floating to enable Port 6's interface.

Table 10: Port 6 xMII Receive Interface

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
98	98	P6_INCLK	I/O, PU	Input Clock. INCLK is a reference for INDV and IND. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. INCLK is an output when the xMII is configured in a PHY mode (when the port's Px_MODE = 0x1). INCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left floating when unused.
108 107 106 105 104 103 102 101	108 107 106 105 104 103 102 101	P6_IND[7] /GPIO[3] P6_IND[6] /GPIO[4] P6_IND[5] /GPIO[5] P6_IND[4] /GPIO[6] P6_IND[3] P6_IND[2] P6_IND[1] P6_IND[0]	Input, PU	Input Data. IND[7:0] (or IND[3:0] where appropriate) receives the data to be sent into the switch. IND must be synchronous to INCLK. In 1000BASE GMII mode IND[7:0] is used. In 1000 BASE RGMII, 200BASE, 100BASE and 10BASE modes IND[3:0] is used and IND[7:4] become GPIO[3:6]. In RGMII mode IND[3:0] are used as RXD[3:0]. These pins become GPIO[3:6] if the port's Px_MODE is 0x6 (disabled). The IND pins are internally pulled high via resistor so the pins can be left floating when unused.
100	100	P6_INDV	Input, PD	Input Data Valid. Input Data Valid is used to indicate when IND[7:0] (or IND[3:0] where appropriate) contains frame information. INDV must be synchronous to INCLK. In RGMII mode INDV is used as RX_CTL. INDV is internally pulled low via resistor so the pin can be left floating when unused.

Table 10: Port 6 xMII Receive Interface (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
109	109	P6_CRS /GPIO[2]	I/O, PU	Carrier Sense or GPIO[2]. Carrier sense is used to indicate carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex MII modes only and is ignored when the port is in full-duplex. This pin is CRS when the port's Px_MODE = 0x1 or 0x2 or 0x3. GPIO[2] is a general purpose input/output pin whose direction and data is controllable via switch registers. This pin is GPIO[2] when the port's Px_MODE does not cause this pin to be CRS (as defined above). CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P6_ENABLE.
110	110	P6_COL /GPIO[1]	Input/Output, PU	Collision or GPIO[1]. Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. COL is not synchronous to INCLK. COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's Px_MODE = 0x1 or 0x2 or 0x3. GPIO[1] is a general purpose input/output pin whose direction and data is controllable via switch registers. This pin is GPIO[1] when the port's Px_MODE does not cause this pin to be COL (as defined above). COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P6_ENABLE.

Table 11: Port 6 xMII Transmit Interface

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
97	97	P6_GTXCLK /S_MODE	Typically Output, PU	Transmit Clock. GTXCLK is a reference for OUTEN and OUTD[7:0] when the port is in GMII. The speed of GTXCLK is 125 MHz and is normally only driven when the speed of the port is 1000 Mbps. GTXCLK is enabled only when P6_MODE = 0x3. In all other P6_MODEs it is tri-stated. GTXCLK is tri-stated during RESETn and when P6_ENABLE is low. It is internally pulled high so the pin can be left unconnected if not used. P6_GTXCLK is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the S_MODE configuration information for the SERDES below is latched at the rising edge of RESETn: 0 = SERDES configured to 100BASE-FX 1 = SERDES configured to 1000BASE-X or SGMII Refer to C_MODE in the Port Status Register for complete details. P6_GTXCLK is tri-stated during RESETn or when P6_ENABLE is low. GTXCLK is internally pulled high via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration low.

Table 11: Port 6 xMII Transmit Interface (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
94	94	P6_OUTEN /P6_VDDOS[0]	Typically Output, PD	Output Enable. Output enable is used to indicate when OUTD[7:0] (or OUTD[3:0] where appropriate) contains frame information. OUTEN is synchronous to GTXCLK in 1000BASE GMII. It is synchronous to OUTCLK in RGMII, 200BASE, 100BASE and 10BASE modes. In RGMII mode OUTEN is used as TX_CTL. P6_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: If P6_VDDOS[1], below on the P6_OUTD[3] pin, is high at the rising edge of RESETn: 0 = The P6_VDDO pins are powered by 3.3 volts 1 = The P6_VDDO pins are powered by 2.5 volts If P6_VDDOS[1], below on the P6_OUTD[3] pin, is low at the rising edge of RESETn: X = The P6_VDDO pins are powered by 1.8 volts See P6_VDDO for the list of pins that are powered by this rail. P6_OUTEN is tri-stated during RESETn or when P6_ENABLE is low. OUTEN is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to VDDO for a configuration high.
95	95	P6_OUTCLK /P6_TXC	I/O, PU	Output Clock. OUTCLK is a clock reference for OUTEN and OUTD[3:0]. The speed of OUTCLK is 50 MHz, 25 MHz or 2.5 MHz depending the speed of the Port. The direction of OUTCLK is a function of the port's Px_MODE and the port's PHY Detect bit (Port offset 0x00). See the C_Mode bits in Port offset 0x00. In RGMII mode, OUTCLK is used as TXC. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 11: Port 6 xMII Transmit Interface (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
85	85	P6_OUTD[7] /ADDR[4]n	Typically Output, PU	Output Data. OUTD[7:0] (or OUTD[3:0] where appropriate) outputs the data to be transmitted from the switch. OUTD is synchronous to GTXCLK in 1000BASE GMII. In RGMII, 200BASE, 100BASE and 10BASE modes OUTD[3:0] is synchronous to OUTCLK and the other OUTD pins are ignored. In RGMII mode OUTD[3:0] are used as TXD[3:0]. P6_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: OUTD[2:0] = P6_MODE[2:0] OUTD[3] = P6_VDDOS[1] OUTD[7:0] = ADDR[4:1]n P6_MODE[2:0] sets Port 6's Mode of operation as follows: 0x0 = Reserved for future use 0x1 = MII PHY mode w/output P6 MII CLKs at 2.5, 25, or 50 MHz[1] 0x2 = MII MAC mode w/input P6 MII CLKs 0x3 = GMII mode 0x4 = RMII PHY Mode w/output Px_OUTCLK at 50 MHz 0x5 = RMII MAC Mode w/output Px_INCLK at 50 MHz 0x6 = Port 6 disabled (with its pins tri-stated)[2] 0x7 = RGMII mode P6_VDDOS[1] selects the P6 voltage setting as follows: 0 = The P6_VDDO pins are powered by 1.8V 1 = The P6_VDDO pins are powered by 2.5 or 3.3V (P6_VDDOS[0], above on the P6_OUTEN pin, is used to select between 2.5 and 3.3 volts) See P6_VDDO for the list of pins that are powered by this rail. ADDR[4:1]n sets the device's SMI address. (ADDR[0] is always zero.) When ADDR[4:1]n = 0x15, the device is in single-chip addressing mode. In this mode, the internal addresses can be accessed directly by the device address and offset. When ADDR[4:1]n ≠ 0x15, the device is set to multi-chip addressing mode. Refer to the Functional Specification for details on multi-chip addressing mode. **NOTE:** The SMI address is based on the inverted values of ADDR[4:1]n. The default configuration is based on the pull-up resistors on these signals (which sets the ADDR[4:1]n pins at 0x15), which in turn sets the actual SMI address to 0x0 (meaning that the device is in single-chip addressing mode). Alternatively, if ADDR[4:1]n = 0x0, then the SMI address would be set to 0x1E. P6_OUTD pins are tri-stated during RESETn or when P6_ENABLE is low. OUTD pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7kohm resistor to VSS for a configuration low.
86	86	P6_OUTD[6] /ADDR[3]n		
87	87	P6_OUTD[5] /ADDR[2]n		
88	88	P6_OUTD[4] /ADDR[1]n		
90	90	P6_OUTD[3] /P6_VDDOS[1]		
91	91	P6_OUTD[2] /P6_MODE[2]		
92	92	P6_OUTD[1] /P6_MODE[1]		
93	93	P6_OUTD[0] /P6_MODE[0]		

1. P6_OUTCLK's frequency is determined by the port's ForceSpd bits (Port offset 0x01).
2. In this mode many of P6's pins become the GPIO[6:0] pins.

Table 12: System and Register Access

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
61	61	MDC_CPU	Input	Management Data Clock, Slave. MDC_CPU is the reference clock input for the serial management interface (SMI) that connects to an external SMI master, typically a CPU. A continuous clock stream is not expected. The CPU's SMI interface is used to access the device's registers but it cannot be used until the device's INTn pin becomes active low (indicating the Register Loader is done processing the EEPROM or that no EEPROM was present). MDC_CPU is internally pulled high via a resistor so it can be left floating when unused. Note: MDC_CPU is powered by the P5_VDDO pins and this pin is 3.3V tolerant if P5_VDDO is powered at 2.5V.
60	60	MDIO_CPU	I/O	Management Data I/O, Slave. MDIO_CPU is used to transfer management data in and out of the device synchronously to MDC_CPU. This pin requires an external pull-up resistor in the range of 4.7 kohm to 10 kohm, depending on board design requirements. The device uses one or all of the 32 possible SMI port addresses (two modes are supported). The address(es) that are used are selectable using the P5_OUTD/ADDR configuration pins. MDIO_CPU is internally pulled high via a resistor so it can be left floating when unused. Note: MDIO_CPU is powered by the P5_VDDO pins and this pin is 3.3V tolerant if P5_VDDO is powered at 2.5V.
42	42	INTn	Open Drain Output	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required somewhere on this interrupt net for it to go high when it is inactive. The INTn pin will go active low which indicates the MDC_CPU/ MDIO_CPU interface is available for use. The CPU SMI interface cannot be used while the Register Loader is processing an EEPROM, if one is present.

Table 13: Power and Ground

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
80	80	VDD33	Power	3.3V power input to on-chip voltage regulator. Connect this pin to 3.3V if the internal 1.0V regulator is used. If the internal regulator is not used this pin can be left unconnected.
81	81	CTRL18	Power	Voltage control to external regulator. This signal controls an external PNP transistor's base to regulate the 1.8V power supply needed for this device. If the internal regulator is not used this pin can be left unconnected.
82	82	VDD18_SENS	Power	Sensing feedback input for the 1.8V regulator. Connect this directly to the collector of the external PNP transistor used to regulate the 1.8V supply. When using an external 1.8V regulator (but using the internal 1.0V regulator), this pin must be connected to a 1.8V power supply. If the internal regulator is not used this pin can be left unconnected.
83	83	VDD18	Power	1.8V power input to the internal 1.0V on-chip regulator. If the internal regulator is not used this pin can be left unconnected.
84	84	VDD10_OUT	Power Output	1.0V power output from the on-chip voltage regulator. If the on-chip regulator is used, connect this output to all the VDD_CORE pins. If the internal regulator is not used this pin can be left unconnected.
64 73	64 73	P5_VDDO	Power	Power to Port 5's interface as well as the CPU interface pins (pin numbers 60 to 79). P5_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P5_VDDOS[1:0] must be configured accordingly – see P5_OUTD[3] & P5_OUTEN).
89 99	89 99	P6_VDDO	Power	Power to Port 6's interface (pin numbers 85to 111). P6_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P6_VDDOS[1:0] must be configured accordingly – see P6_OUTD[3] & P6_OUTEN).
37	37	EE_VDDO	Power	Power to LED, EEPROM interface, INTn and RESETn pins (pin numbers 32 to 42). EE_VDDO must be connected to 3.3V for 3.3V I/O
1 32	1 32	AVDD33	Power	3.3V power to the analog core used to power PHYs on Ports 1-3
118	118	P0_AVDD33	Power	3.3V power to analog core used to power Port 0's PHY
49	49	P4_AVDD33	Power	3.3V power to analog core used to power Port 4's PHY

Table 13: Power and Ground (Continued)

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
46 24 15 6 115	46 24 15 6 115	P[4:0]_AVDD18	Power	1.8V power to analog core used to power each PHY interface.
3 124	3 124	AVDD18	Power	1.8V power to analog core used to power the on-chip PLL.
--	57	S_AVDD18	Power	1.8V power to analog core used to power the SERDES interface. The S_AVDD18 pin can be left unconnected if the SERDES interface is not used.
43 54 65 96 112 123	43 54 65 96 112 123	VDD_CORE	Power	1.0 volt Power to digital core.
41 128 E-PAD	41 128 E-PAD	VSS	Ground	Ground to the device. The device is packaged in the 128-pin TQFP package with an E-PAD (exposed die pad) on the bottom of the package. This E-PAD must be soldered to VSS as it is the main VSS connection on the device.

Table 14: No Connect

88E6172 Pin #	88E6176 Pin #	Pin Name	Pin Type	Description
55 56 57 58 59	--	NC	No Connect	No connect. Do not connect these pins to anything.

1.2 Pin Assignment Lists

1.2.1 88E6172 Device Pin Assignment List

Table 15: 88E6172 Device Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
3	AVDD18
124	AVDD18
1	AVDD33
32	AVDD33
81	CTRL18
38	EE_CLK/C1_LED /FLOW
39	EE_CS/C2_LED/P4_LED0/S_SEL
36	EE_DIN/C0_LED/P3_LED0/EEE_WP
40	EE_DOUT/C3_LED/P5_LED0
37	EE_VDDO
42	INTn
61	MDC_CPU
60	MDIO_CPU
57	NC
56	NC
55	NC
59	NC
58	NC
115	P[0]_AVDD18
6	P[1]_AVDD18
15	P[2]_AVDD18
24	P[3]_AVDD18
46	P[4]_AVDD18
118	P0_AVDD33
114	P0_MDIN[0]
117	P0_MDIN[1]
120	P0_MDIN[2]
122	P0_MDIN[3]
113	P0_MDIP[0]
116	P0_MDIP[1]
119	P0_MDIP[2]
121	P0_MDIP[3]
5	P1_MDIN[0]
8	P1_MDIN[1]
10	P1_MDIN[2]
12	P1_MDIN[3]
4	P1_MDIP[0]
7	P1_MDIP[1]
9	P1_MDIP[2]
11	P1_MDIP[3]
14	P2_MDIN[0]
17	P2_MDIN[1]
19	P2_MDIN[2]
21	P2_MDIN[3]
13	P2_MDIP[0]
16	P2_MDIP[1]
18	P2_MDIP[2]
20	P2_MDIP[3]
23	P3_MDIN[0]

Pin Number	Pin Name
26	P3_MDIN[1]
28	P3_MDIN[2]
30	P3_MDIN[3]
22	P3_MDIP[0]
25	P3_MDIP[1]
27	P3_MDIP[2]
29	P3_MDIP[3]
49	P4_AVDD33
45	P4_MDIN[0]
48	P4_MDIN[1]
51	P4_MDIN[2]
53	P4_MDIN[3]
44	P4_MDIP[0]
47	P4_MDIP[1]
50	P4_MDIP[2]
52	P4_MDIP[3]
62	P5_COL/MDIO_PHY
63	P5_CRS/MDC_PHY
79	P5_ENABLE/GPIO[7]
72	P5_INCLK/GPIO[13]
75	P5_IND[0]/GPIO[11]
76	P5_IND[1]/GPIO[10]
77	P5_IND[2]/GPIO[9]
78	P5_IND[3]/GPIO[8]
74	P5_INDV/GPIO[12]
71	P5_OUTCLK/P5_TXC/GPIO[14]
69	P5_OUTD[0]/P5_MODE[0]
68	P5_OUTD[1]/ P5_MODE[1]

Pin Number	Pin Name
67	P5_OUTD[2]/P5_MODE[2]
66	P5_OUTD[3]/ P5_VDDOS[1]
70	P5_OUTEN/P5_VDDOS[0]
64	P5_VDDO
73	P5_VDDO
110	P6_COL/GPIO[1]
109	P6_CRS/GPIO[2]
111	P6_ENABLE/GPIO[0]
97	P6_GTXCLK/S_MODE
98	P6_INCLK
101	P6_IND[0]
102	P6_IND[1]
103	P6_IND[2]
104	P6_IND[3]
105	P6_IND[4]/GPIO[6]
106	P6_IND[5]/GPIO[5]
107	P6_IND[6]/GPIO[4]
108	P6_IND[7]/GPIO[3]
100	P6_INDV
95	P6_OUTCLK/P6_TXC
93	P6_OUTD[0]/P6_MODE[0]
92	P6_OUTD[1]/P6_MODE[1]
91	P6_OUTD[2]/P6_MODE[2]
90	P6_OUTD[3]/P6_VDDOS[1]
88	P6_OUTD[4]/ADDR[1]n
87	P6_OUTD[5]/ADDR[2]n
86	P6_OUTD[6]/ADDR[3]n
85	P6_OUTD[7]/ADDR[4]n

Pin Number	Pin Name
94	P6_OUTEN/P6_VDDOS[0]
89	P6_VDDO
99	P6_VDDO
33	R0_LED/P0_LED0/LED_SEL[0]
34	R1_LED/P1_LED0/LED_SEL[0]
35	R2_LED/P2_LED0/NO_CPU
31	RESETn
2	RSET
43	VDD_CORE
54	VDD_CORE
65	VDD_CORE
96	VDD_CORE
112	VDD_CORE
123	VDD_CORE
84	VDD10_OUT
83	VDD18
82	VDD18_SENS
80	VDD33
41	VSS
128	VSS
EPAD	VSS
127	XTAL_GND
126	XTAL_IN
125	XTAL_OUT

1.2.2 88E6176 Device Pin Assignment List

Table 16: 88E6176 Device Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
3	AVDD18
124	AVDD18
1	AVDD33
32	AVDD33
81	CTRL18
38	EE_CLK/C1_LED /FLOW
39	EE_CS/C2_LED/P4_LED0/S_SEL
36	EE_DIN/C0_LED/P3_LED0/EEE_WP
40	EE_DOUT/C3_LED/P5_LED0
37	EE_VDDO
42	INTn
61	MDC_CPU
60	MDIO_CPU
115	P[0]_AVDD18
6	P[1]_AVDD18
15	P[2]_AVDD18
24	P[3]_AVDD18
46	P[4]_AVDD18
118	P0_AVDD33
114	P0_MDIN[0]
117	P0_MDIN[1]
120	P0_MDIN[2]
122	P0_MDIN[3]
113	P0_MDIP[0]
116	P0_MDIP[1]
119	P0_MDIP[2]
121	P0_MDIP[3]
5	P1_MDIN[0]
8	P1_MDIN[1]
10	P1_MDIN[2]
12	P1_MDIN[3]
4	P1_MDIP[0]
7	P1_MDIP[1]
9	P1_MDIP[2]
11	P1_MDIP[3]
14	P2_MDIN[0]
17	P2_MDIN[1]
19	P2_MDIN[2]
21	P2_MDIN[3]
13	P2_MDIP[0]
16	P2_MDIP[1]
18	P2_MDIP[2]
20	P2_MDIP[3]
23	P3_MDIN[0]
26	P3_MDIN[1]
28	P3_MDIN[2]
30	P3_MDIN[3]
22	P3_MDIP[0]
25	P3_MDIP[1]
27	P3_MDIP[2]
29	P3_MDIP[3]
49	P4_AVDD33

Pin Number	Pin Name
45	P4_MDIN[0]
48	P4_MDIN[1]
51	P4_MDIN[2]
53	P4_MDIN[3]
44	P4_MDIP[0]
47	P4_MDIP[1]
50	P4_MDIP[2]
52	P4_MDIP[3]
62	P5_COL/MDIO_PHY
63	P5_CRS/MDC_PHY
79	P5_ENABLE/GPIO[7]
72	P5_INCLK/GPIO[13]
75	P5_IND[0]/GPIO[11]
76	P5_IND[1]/GPIO[10]
77	P5_IND[2]/GPIO[9]
78	P5_IND[3]/GPIO[8]
74	P5_INDV/GPIO[12]
71	P5_OUTCLK/P5_TXC/GPIO[14]
69	P5_OUTD[0]/P5_MODE[0]
68	P5_OUTD[1]/ P5_MODE[1]
67	P5_OUTD[2]/P5_MODE[2]
66	P5_OUTD[3]/ P5_VDDOS[1]
70	P5_OUTEN/P5_VDDOS[0]
64	P5_VDDO
73	P5_VDDO
110	P6_COL/GPIO[1]
109	P6_CRS/GPIO[2]
111	P6_ENABLE/GPIO[0]

Pin Number	Pin Name
97	P6_GTXCLK/S_MODE
98	P6_INCLK
101	P6_IND[0]
102	P6_IND[1]
103	P6_IND[2]
104	P6_IND[3]
105	P6_IND[4]/GPIO[6]
106	P6_IND[5]/GPIO[5]
107	P6_IND[6]/GPIO[4]
108	P6_IND[7]/GPIO[3]
100	P6_INDV
95	P6_OUTCLK/P6_TXC
93	P6_OUTD[0]/P6_MODE[0]
92	P6_OUTD[1]/P6_MODE[1]
91	P6_OUTD[2]/P6_MODE[2]
90	P6_OUTD[3]/P6_VDDOS[1]
88	P6_OUTD[4]/ADDR[1]n
87	P6_OUTD[5]/ADDR[2]n
86	P6_OUTD[6]/ADDR[3]n
85	P6_OUTD[7]/ADDR[4]n
94	P6_OUTEN/P6_VDDOS[0]
89	P6_VDDO
99	P6_VDDO
33	R0_LED/P0_LED0/LED_SEL[0]
34	R1_LED/P1_LED0/LED_SEL[0]
35	R2_LED/P2_LED0/NO_CPU
31	RESETn
2	RSET

Pin Number	Pin Name
57	S_AVDD18
56	S_RXN
55	S_RXP
59	S_TXN
58	S_TXP
43	VDD_CORE
54	VDD_CORE
65	VDD_CORE
96	VDD_CORE
112	VDD_CORE
123	VDD_CORE
84	VDD10_OUT
83	VDD18
82	VDD18_SENS
80	VDD33
41	VSS
128	VSS
EPAD	VSS
127	XTAL_GND
126	XTAL_IN
125	XTAL_OUT

2 Application Examples

2.1 Examples using the 88E6172/88E6176 Device

Figure 4: AVB Gigabit Firewall Router with four LAN Ports and one WAN Port using Copper or Fiber and Two Ports for a CPU

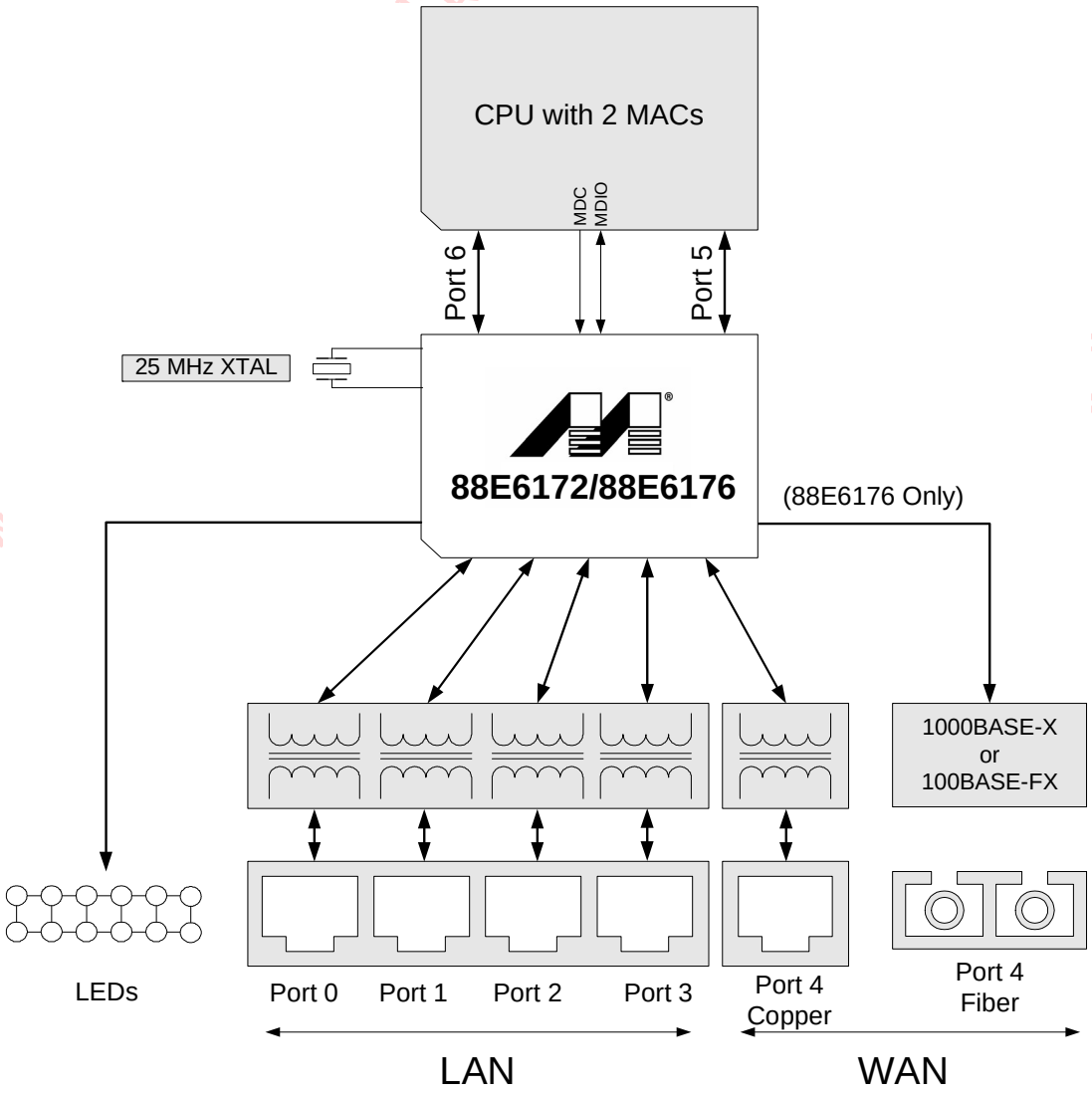
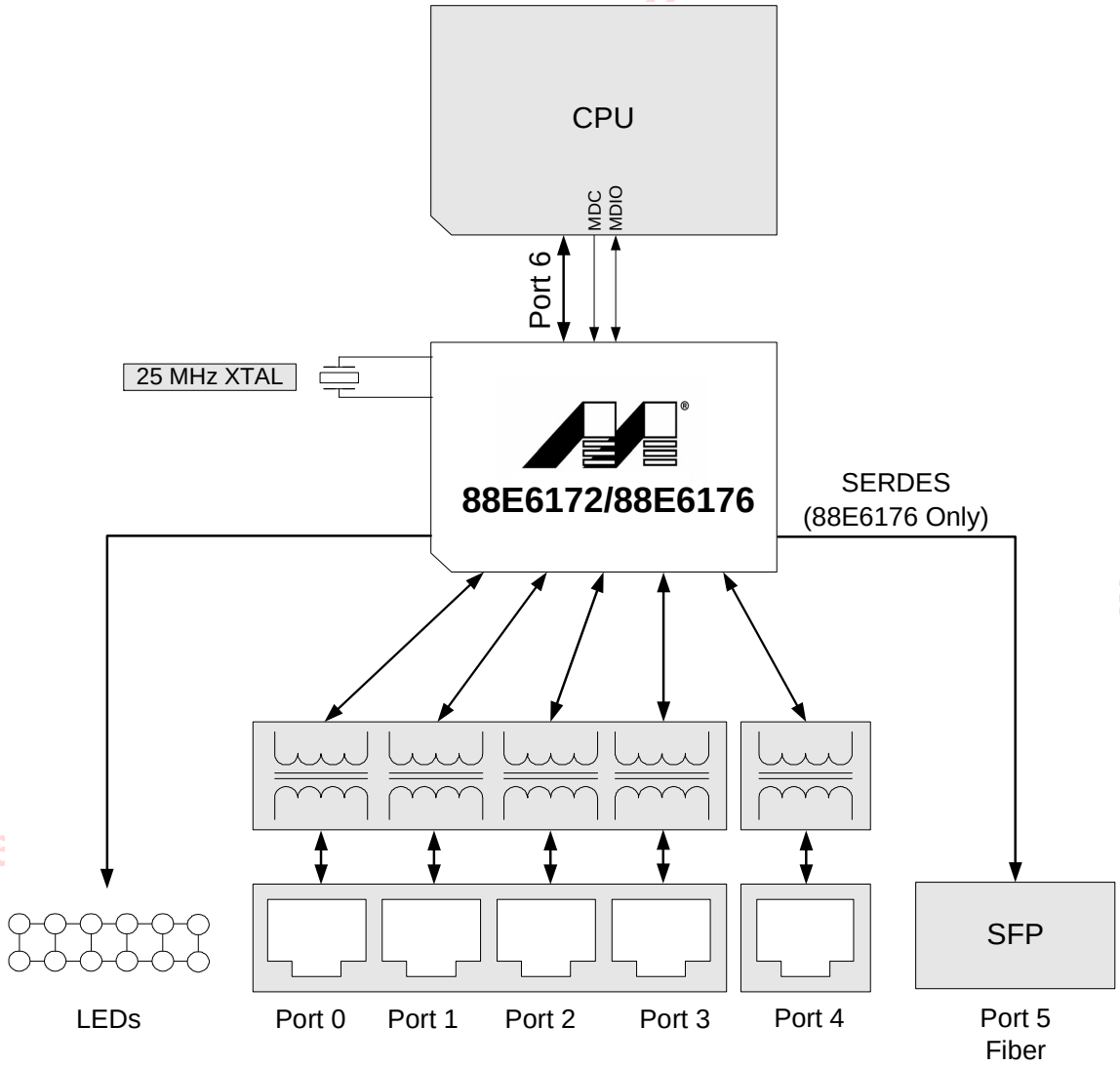


Figure 5: 6 Port AVB Gigabit Ethernet with Fiber Link



2.2 Device Physical Interfaces

The device contains a number of interfaces that support copper media. Table 17 lists the interfaces supported on each port of the 88E6172/88E6176 device. Refer to the diagrams further in this section for connection details.

Table 17: 88E6172/88E6176 Device Interfaces

Port	10BASE-T 100BASE-T	1000BASE-T	GMII	RGMII	RMII	MII/ 200 Mbps MII	1000BASE-X 100BASE-FX SERDES SGMII[1, 2]
0-3	x	x					
4	x	x					x
5				x	x	x	x
6			x	x	x	x	

1. The SERDES/SGMII interface can be configured as Port 4 or Port 5.
2. 1000BASE-X, 100BASE-FX, SERDES and SGMII are available on the 88E6176 device only.

2.2.1 10/100/1000 PHY Interface

Ports 0 to 3 on the device support a 10/100/1000 PHY interface. In the device, this interface supports 10BASE-T, 100BASE-TX, and 1000BASE-T copper IEEE standards. The MAC inside the switch works the same way regardless of the external interface being used. Each PHY's Link, Speed, Duplex and Flow Control information is directly communicated to the MAC it is attached to so the MAC tracks, or follows, the mode the PHY links up in. A detailed description of the PHY functional and register description is covered in the functional specification of the device.

2.2.2 MII 200 Mbps Mode

Port 5 and Port 6 of the device's GMII/MII interfaces can run at a data rate of 200 Mbps, full-duplex. Do not select this mode unless the MAC on the other end of the MII interface can also run at double speed rate. Both PHY (reverse MII) and MAC (forward MII) 200 Mbps modes are supported. To use 200 Mbps mode, P5_MODE or P6_MODE must be set to MII MAC or MII PHY mode. After reset, the CPU or an EEPROM must set the speed to 200 Mbps by setting register 1 bit 12 = 1 and bits 1:0 = 01. Refer to the functional spec for a description of these register bits. There is no change in the format of the data, it just runs faster. When the 200 Mbps MAC mode is selected, an external 50 MHz ±50 ppm clock source must be supplied to both INCLK and OUTCLK. Again, the format of the data is not changed.

2.2.3 SERDES Interface (88E6176 Only)

The SERDES interface can be used for these options:

- Connection to Marvell® triple speed 10/100/1000 copper PHYs
- Connection to 1000BASE-X fiber modules
- SGMII interface
- Cross-chip connection to other Marvell switch devices - i.e., cross-chip connection

The S_SEL pin is used to select which port the SERDES will be connected to.

- S_SEL = 0 - SERDES connected to Port 4's MAC (see Section 2.2.4 for Auto-Media Detect details)
- S_SEL = 1 - SERDES connected to Port 5's MAC

Once the SERDES port designation is determined, the S_MODE pin is used to select the SERDES configuration.

- S_MODE = 0 - SERDES configured to 100BASE-FX
- S_MODE = 1 - SERDES configured to 1000BASE-X or SGMII

2.2.3.1 Triple Speed PHY SERDES Interface Option (88E6176 Only)

The SERDES can be configured to use a triple speed PHY interface to an external PHY. In this mode, the SERDES use the SGMII protocol. The in-band Link, Speed and Duplex signals in the SGMII protocol are ignored. The external PHY's Link, Speed, Duplex and Flow Control information must be transferred to the port's MAC so the MAC is in the correct mode. This can be done in software (if the port's PHYDetect bit is zero - Port offset 0x00) or it is done automatically by the PHY Polling Unit (PPU - Section 2.2.6)

The triple speed PHY interface can support Marvell PHYs with Auto-Media Detect™ for auto switching between copper and fiber. This can be supported in software or automatically in hardware by the PHY Polling Unit (PPU) and by setting the port's MGMII bit to a one (in the port's Port Status Register - offset 0x00). If the port's MGMII bit is not set to a one, the PPU will support copper only and will not support Auto-Media Detect.

The SERDES is connected to Port 4's MAC when the EE_CS/C2_LED/P4_LED0/S_SEL is set to 0 1 mSec after the rising edge of RESETn and if the port's PHYDetect bit is a 1 (in the port's Port Status Register - offset 0x00). PHYDetect will be set to a 1 on Port 4if the PPU finds a PHY at SMI address 0x08.

The SERDES is connected to Port 5's MAC if the EE_CS/CS_LED/P4_LED0/S_SEL pin is set to 1 1 mSec after the rising edge or RESETn.

2.2.4 Port 4 Fiber/Copper Auto-Selection (88E6176 Only)

The device has a patented feature to automatically detect and switch between the Port 4 fiber and copper cable connections. The auto-selection operates in one of three modes: Copper /1000BASE-X, Copper/100BASE-FX, and Copper/SGMII Media Interface.

The device monitors the signals of the S_RXP/N and the P4_MDI[3:0] lines. If a fiber optic cable is plugged in, the device will adjust itself to be in fiber mode. If an RJ-45 cable is plugged in, the device will adjust itself to be in copper mode. If both cables are connected then the first media to establish link, or the preferred media will be enabled. The media which is not enabled will turn off to save power. If the link on the first media is lost, then the inactive media will be powered up, and both media will once again start searching for link.

Figure 6: Port 4 Auto-Media Detect

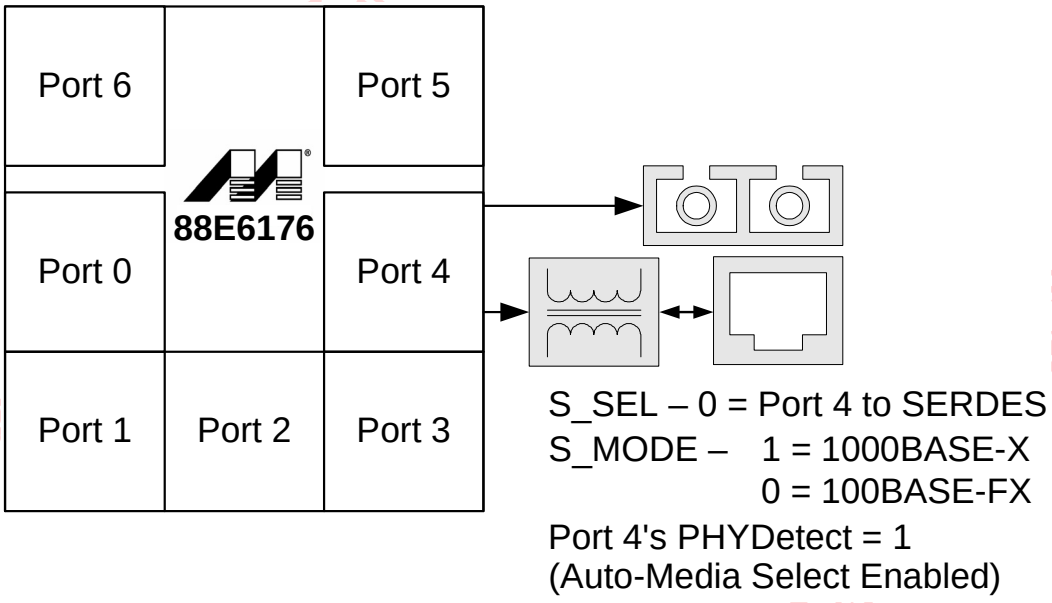


Figure 7: Port 4 Fiber Application

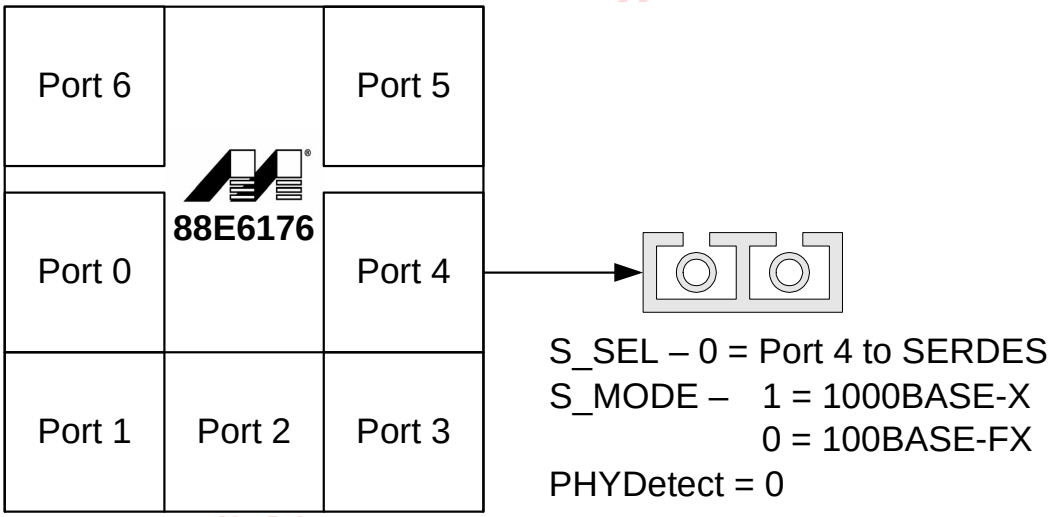


Figure 8: Port 5 Fiber Application

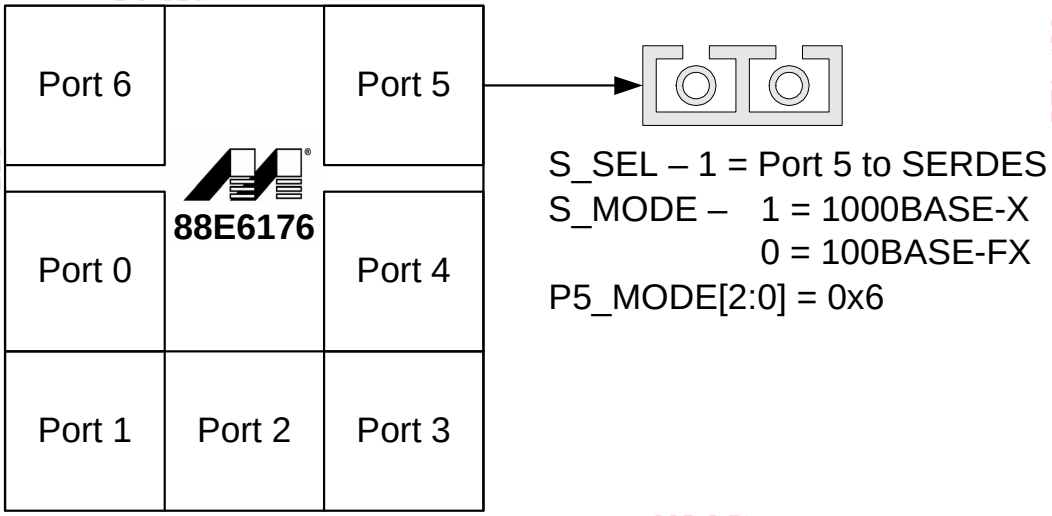


Figure 9: Port 5 MDI Application

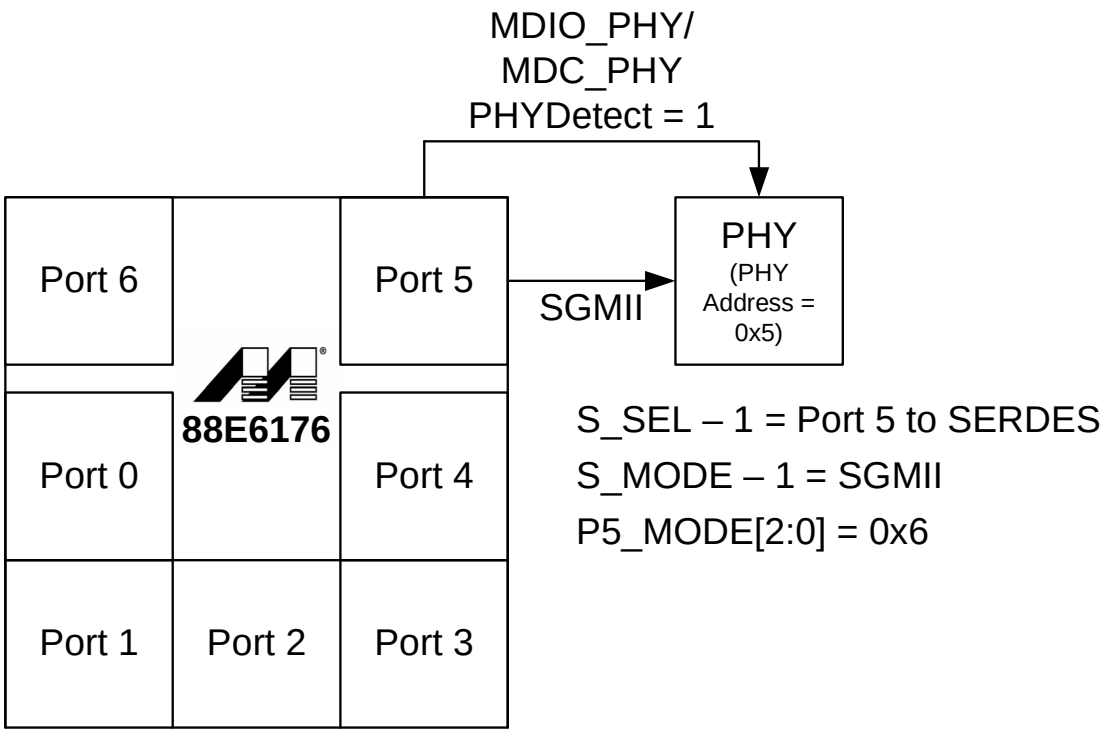
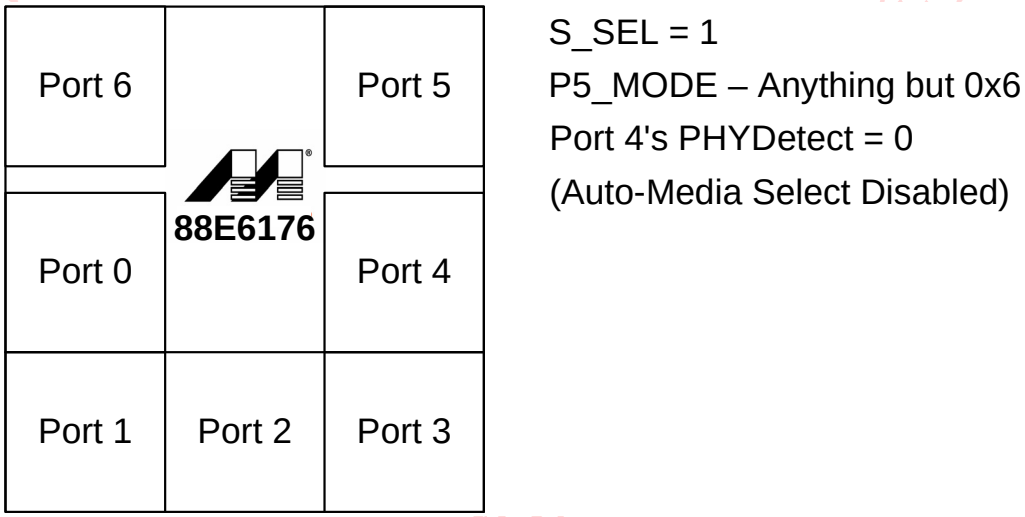


Figure 10: SERDES Disabled



2.2.4.1 IEEE 1000BASE-X SERDES Interface Option (88E6176 Only)

The SERDES can be configured for 100BASE-FX or 1000BASE-X/SGMII modes.

As described in Section 2.2.3.1, the EE_CS/C2_LED/P4_LED0/S_SEL pin determines if Port 4 or Port 5 will be connected to the SERDES interface. Once the port has been determined, the P6_GTCLK/S_MODE pin is used to determine if the SERDES interface is configured for 100BASE-FX or 1000BASE-X/SGMII modes.

The port enters 1000BASE-X mode, if configured, even if an external PHY is detected at the port's SMI address.

1000BASE-X mode uses a PCS to auto-negotiate with a link partner to determine if Flow Control should be supported or not (auto-negotiation can be disabled). Link will be automatically established if the port's SDET[1] is detected high and the port's PCS determines Sync is OK (sets the port's SyncOK to a 1). Link will automatically go down if either SDET or SyncOK go to zero. Speed is always 1000 Mbps and Duplex is always full-duplex on 1000BASE-X ports. An interrupt can be generated on the ports when link changes state (see Global 2, offset 0x00 and 0x01).

2.2.4.2 Port Status Registers

Each switch port of the devices has a status register that reports information about that port's MAC, SERDES or (G)MII interface. These registers can be used to check the current port configuration. See the Functional Specification for details.

1. The P5_ENABLE/GPIO[7] pin is used as the SDET pin.

2.2.5 Digital Interface Options

The (R)(G)MII digital interface supports many different modes defined in the following sections. The (R)(G)MII mode is configured once at reset by external pull-down resistors connected to the P5_MODE[2:0] and P6_MODE[2:0] pins. See Table 8 and Table 11 for more information. If Port 5 or Port 6 is not connected to any device, the port should be disabled. After reset, P5_MODE and P6_MODE are outputs. It is important to consider some devices put internal pull downs on their outputs; therefore, it is recommended not to rely on internal resistors for configuration.

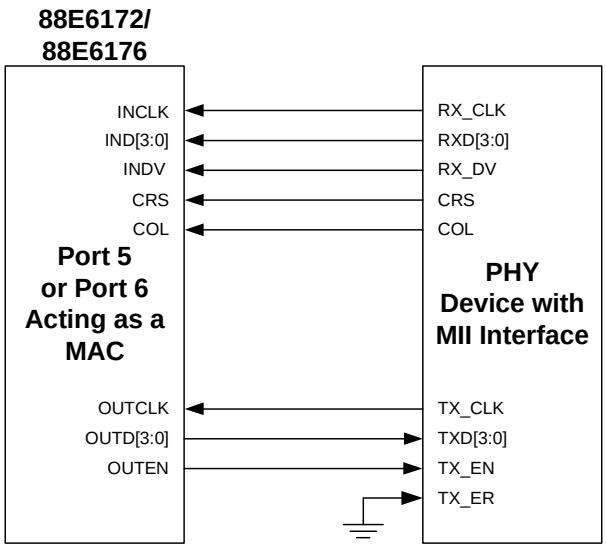
Note

(G)MII PHY mode and (G)MII MAC mode are discussed in the following sections. Electrically, there is no difference since the GMII Interface uses source synchronous clocks. Each concept is discussed separately since the port supports being connected to an external PHY (GMII MAC mode - where the port looks like a MAC supporting 10/100/1000 Mbps) or to an external MAC (GMII PHY mode where the port looks like a PHY supporting 1000 Mbps only).

2.2.5.1 MII MAC Mode

The MII MAC Mode, sometimes called 'Forward MII', configures Port 5 or Port 6's GMAC inside the devices to act as a MAC so it can be directly connected to an external MII-based PHY. In this mode, the devices receive the interface clocks (Px_OUTCLK and Px_INCLK) from the PHY and will work at any frequency from DC to 50 MHz. The two clocks can be asynchronous with each other. Both full- and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII MAC mode is compliant with IEEE 802.3 clause 22. (**Note:** The MII requires only four data bits in each direction so only the lower four data bits are used). P5_MODE or P6_MODE should be set correctly at reset (see Table 8 and Table 11) to select this configuration and the PHY's SMI address must be set to 0x05 for Port 5 or 0x06 for Port 6 for auto-negotiation to operate correctly.

Figure 11: MII MAC Interface Pins

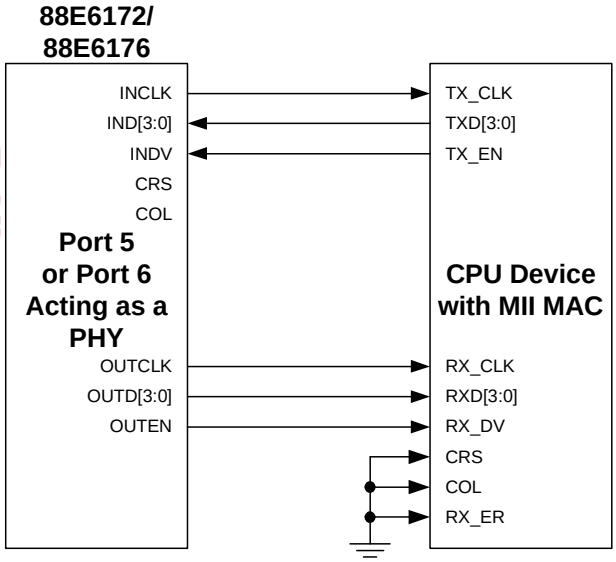


2.2.5.2 MII PHY Mode

The MII PHY Mode, sometimes called 'Reverse MII', configures Port 5 or Port 6's GMAC inside the device to act as a PHY so that it can be directly connected to an external MAC. Only full-duplex modes are supported (since CRS and COL are not driven by the devices outputs) and must match the mode of the link partner's MAC.

The MII PHY mode is compliant with IEEE 802.3 clause 22 in full-duplex mode (**Note**: The MII requires only four data bits in each direction so only the lower four data bits on the devices are used). At reset, P5_MODE and P6_MODE should be set for the appropriate speed — see Table 8 and Table 11. In this mode, there is no external PHY for Port 5 or Port 6, and so Port 5 or Port 6 is skipped by the PPU. In Reverse MII mode, initially the link status is down requiring the system software to force the port's link up to enable the port.

Figure 12: MII PHY Interface Pins

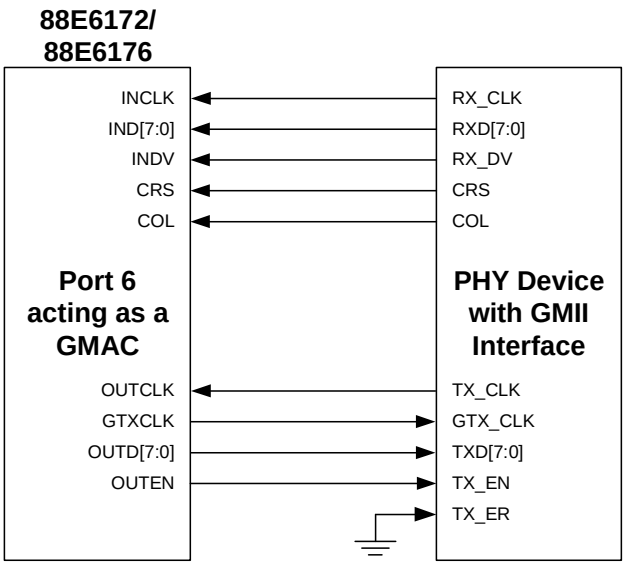


2.2.5.3 GMII MAC Mode

The GMII MAC Mode, sometimes called 'Forward GMII', configures Port 6's GMAC inside the device to act as a gigabit MAC (GMAC) so that it can be directly connected to an external GMII-based Gigabit PHY. In this mode, the devices receive the interface clocks (OUTCLK and INCLK) from the PHY but generate GTXCLK for the PHY. 10 Mbps, 100 Mbps or 1000 Mbps is supported in this configuration. Full- and half-duplex modes are supported at 10 Mbps or 100 Mbps. Full-duplex is supported at 1000 Mbps. The speed and mode in the external PHY's auto-negotiation must be restricted from advertising the 1000BASE, half-duplex case as the GMAC inside the devices do not support that mode. This is done automatically by the PHY Polling Unit (PPU) inside the devices. GMII MAC mode is compliant with IEEE 802.3 clause 28. P6_MODE should be set to GMII mode at reset (see Table 11) for this configuration and the PHY's SMI address must be set to 0x06 for Port 6 for auto-negotiation to operate correctly.

A triple speed interface is supported in GMII MAC mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's settings. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The interface pins will track the speed that the MAC is set to.

Figure 13: GMII MAC Interface Pins

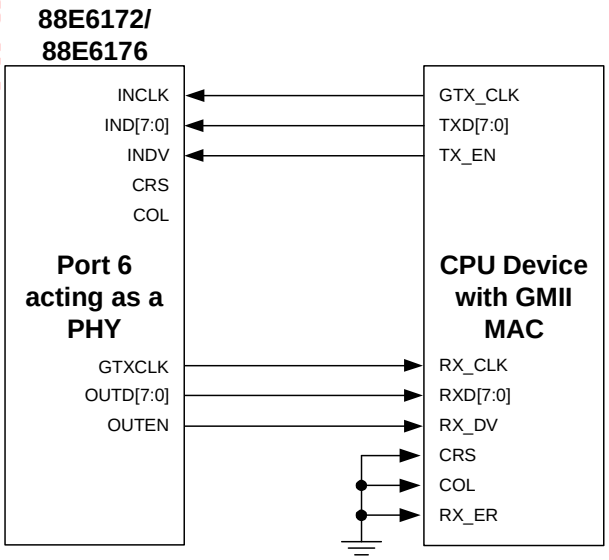


2.2.5.4 GMII PHY Mode

The GMII PHY Mode, sometimes called 'Reverse GMII', configures Port 5's or Port 6's GMAC inside the device to act as a gigabit PHY so that it can be directly connected to an external GMAC. In this mode, the devices drive the transmit interface clock (GTXCLK) and accept the receive interface clock (INCLK). Only gigabit full-duplex mode is supported and must match the mode of the link partner's GMAC. The GMII PHY mode is compliant with IEEE 802.3 clause 28 in gigabit full-duplex. P5_MODE and P6_MODE must be set to GMII mode at reset (see Table 8 and Table 11). In this mode, there is no external PHY for Port 5 or Port 6, so Port 5 or Port 6 are skipped by the PHY Polling Unit (PPU). Initially, the link status is configured down requiring the system software to force the port's link up to enable the port (in the PCS Control Register).

This configuration is identical to the GMII MAC Mode described above except that a CPU is connected instead of a PHY. The lack of an external PHY device restricts the interface to a gigabit speed only with the link initially being down. This allows the CPU time to initialize itself before it enables the switch port connected to it by forcing link up in the switch port's MAC (in the port's Physical Control Register - offset 0x01).

Figure 14: GMII PHY Interface Pins

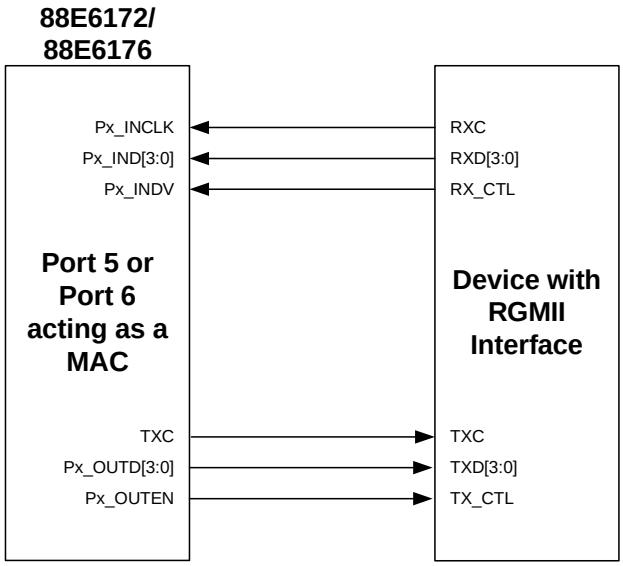


2.2.5.5 RGMII Mode

The RGMII Mode configures Port 5's or Port 6's GMAC to act as a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit PHY or CPU. When the RGMII mode is selected, transmit control (P5_OUTEN or P6_OUTEN) is presented on both clock edges of P5_TXC or P6_TXC. Receive control (P5_INDV or P6_INDV) is presented on both clock edges of P5_INCLK or P6_INCLK.

A triple speed interface is supported in RGMII mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's settings. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The interface pins will track the speed that the MAC is set to.

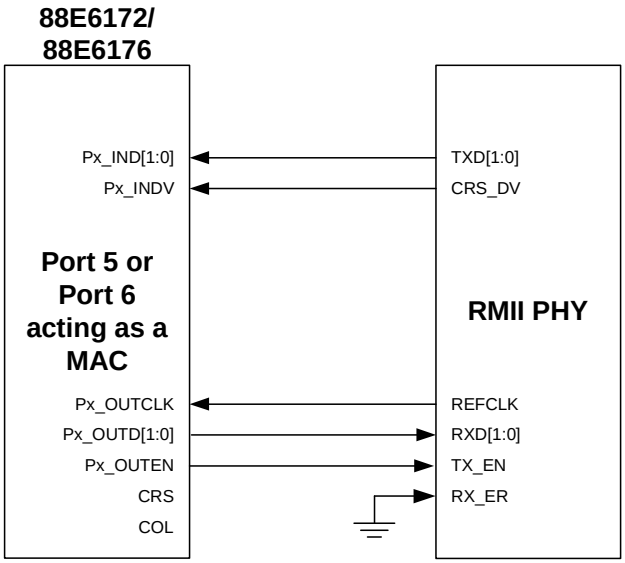
Figure 15: RGMII Interface Pins



2.2.5.6 RMII MAC Mode

RMII MAC Mode (Reduced MII) configures the desired MAC inside the device to act as a 10 or 100 Mbps MAC, enabling it to be directly connected to an external PHY supporting an RMII interface.

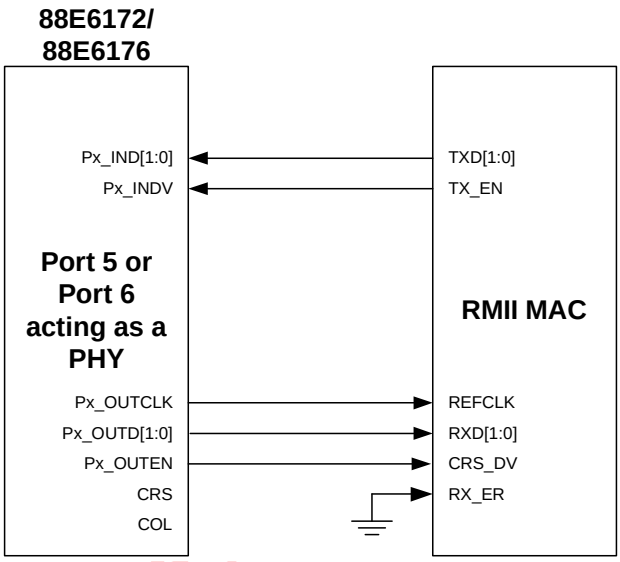
Figure 16: RMII MAC Interface Pins



2.2.5.7 RMII PHY Mode

RMII PHY Mode (Reduced MII) configures the desired MAC inside the device to act as a 10 or 100 Mbps PHY, enabling it to be directly connected to an external CPU supporting an RMII interface.

Figure 17: RMII PHY Interface Pins



2.2.6 PHY Polling Unit (PPU)

The devices contain a PHY Polling Unit (PPU) to transfer Link, Speed, Duplex and Pause information from an external PHY to its associated MAC (the internal PHYs use a direct approach such that this information is transferred even if PHY polling is disabled on the port by its PHYDetect bit being zero - Port offset 0x00). The PPU can perform this job only if the SMI address of the external PHY matches the physical port number it is connected to in the switch (i.e., the PHY connected to Port 5 uses SMI address 0x05, the PHY connected to Port 6 uses SMI address 0x06, etc.).

If PHY polling is disabled on a port (i.e., the port's PHYDetect bit is zero), software must perform the job of setting the switch MAC's mode to the mode of the PHY (for the external PHYs) by forcing the MAC's link, speed, duplex and pause settings (in the port's PCS Control Register - offset 0x01) based upon what it sees in the PHY's registers. Link up must be the last mode register set and link down must be the first mode register cleared (i.e., the port's speed, duplex and pause modes must only be changed while the port's link is down).

Even though the PPU has full access to the external and internal PHY's registers, software can access all of the PHY registers at any time by using the SMI Command and Data registers (Global 2, offsets 0x18 and 0x19).

2.3 General Purpose I/O (GPIO) Configuration

The xMII interfaces on the device include the ability to configure some of the pins as General Purpose I/O (GPIO). The xMII interfaces are configured based on the setting of the Px_MODE pins at reset (as described in Section 1.1, Pin Description, on page 14. Table 18 and Table 19 summarize the GPIO pins that are available in each mode.

Table 18: Port 5 GPIO Summary

P5_MODE	xMII Setting	GPIO Available	Note
011	MII PHY	GPIO[7]	In this mode GPIO[7] is automatically configured to be P5_ENABLE, but can be reprogrammed to be GPIO[7] through the Scratch and Misc Register at Switch Global 2, Offset 0x1A, Index 0x60.
010	MII MAC	GPIO[7]	
100	RMII PHY	GPIO[13], GPIO[9:8], GPIO[7]	
101	RMII MAC	GPIO[13], GPIO[9:8], GPIO[7]	
110	Disabled	GPIO[14:7]	
111	RGMII	GPIO[7]	In this mode GPIO[7] is automatically configured to be P5_ENABLE, but can be reprogrammed to be GPIO[7] through the Scratch and Misc Register at Switch Global 2, Offset 0x1A, Index 0x60.

Table 19: Port 6 GPIO Summary

P6_MODE	xMII Setting	GPIO Available	Note
011	MII PHY	GPIO[6:3], GPIO[0]	In this mode GPIO[0] is automatically configured to be P6_ENABLE, but can be reprogrammed to be GPIO[0] through the Scratch and Misc Register at Switch Global 2, Offset 0x1A, Index 0x60.
010	MII MAC	GPIO[6:3], GPIO[0]	
010	GMII	GPIO[0]	
100	RMII PHY	GPIO[6:1], GIO[0]	
101	RMII MAC	GPIO[6:1], GIO[0]	
110	Disabled	GPIO[6:0]	
111	RGMII	GPIO[6:1], GIO[0]	In this mode GPIO[0] is automatically configured to be P6_ENABLE, but can be reprogrammed to be GPIO[0] through the Scratch and Misc Register at Switch Global 2, Offset 0x1A, Index 0x60.

Once configured as a GPIO, the pin can be programmed to the following functions:

- General Purpose Input
- General Purpose Output
- 125MHz Clock output
- GPIO Port Stall – can be used to stall the transmission of a specific port (or ports) as needed

These functions can be programmed through the Scratch and Misc Register at Switch Global 2, Offset 0x1A (see 88E6352/88E6240/88E6176/88E6172 Functional Specification).

2.4 LED Interface

The device uses a matrixed LED interface allowing each port to have up to two LEDs. The cathode of each LED is connected to a single row signal (Rx_LED). The anode of each LED is connected to a single column signal (Cx_LED). The physical LEDs on the device pins are organized as 3 rows with 4 columns. Table 20 shows the port to physical mapping.

Table 20: LED Mapping

	C0_LE	C1_LED	C2_LED	C3_LED
R0_LED	Port 0, LED 0	Port 1, LED 0	Port 0, LED 1	Port 1, LED 1
R1_LED	Port 2, LED 0	Port 3, LED 0	Port 2, LED 1	Port 3, LED 1
R2_LED	Port 4, LED 0	Port 5, LED 0	Port 4, LED 1	Port 5, LED 1

The column signals (Cx_LED) are also shared with the EEPROM interface, and the architecture allows for the LEDs and EEPROM to operate at the same by time multiplexing the bus into 5 time cycles (C0_LED, C1_LED, C2_LED, C3_LED, and EEPROM). This prevents EEPROM access from interfering with LED operation and vice versa.

Although an EEPROM is not required for most applications, the 88E6172/88E6176 device supports either 2 or 4 wire EEPROMs. Figure 18 and Figure 19 illustrate typical LED connections with 2 or 4 wire EEPROM connections.

Figure 18: Four LEDs plus a 4 wire EEPROM

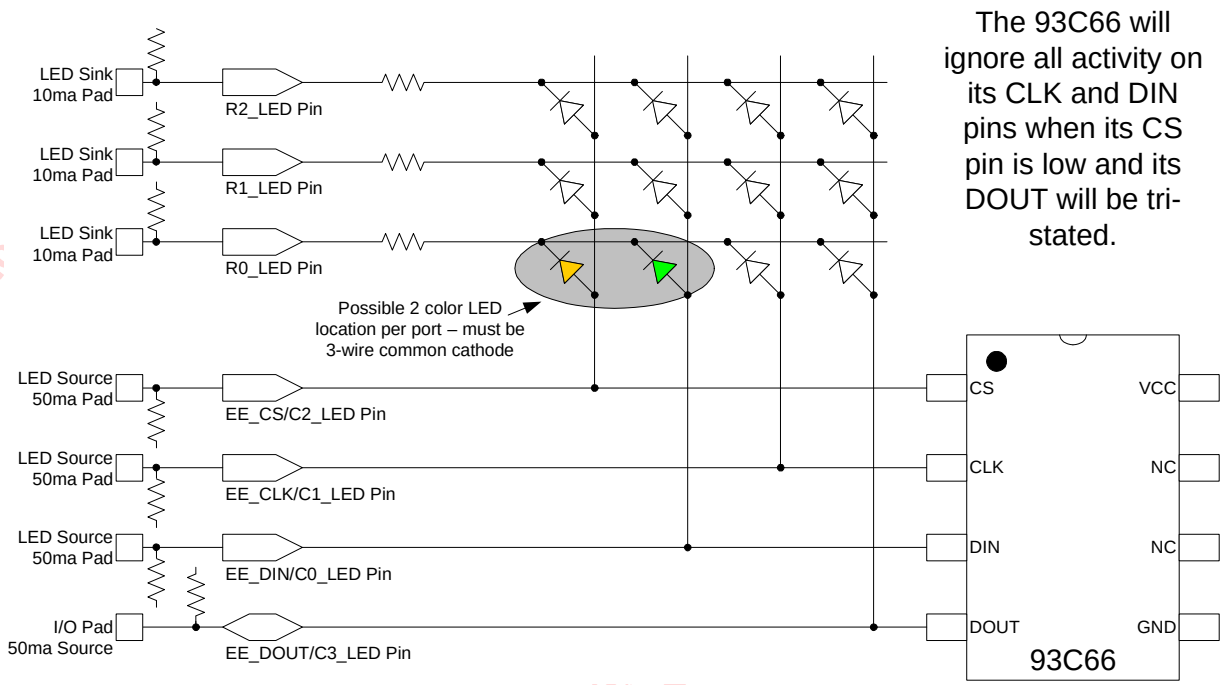
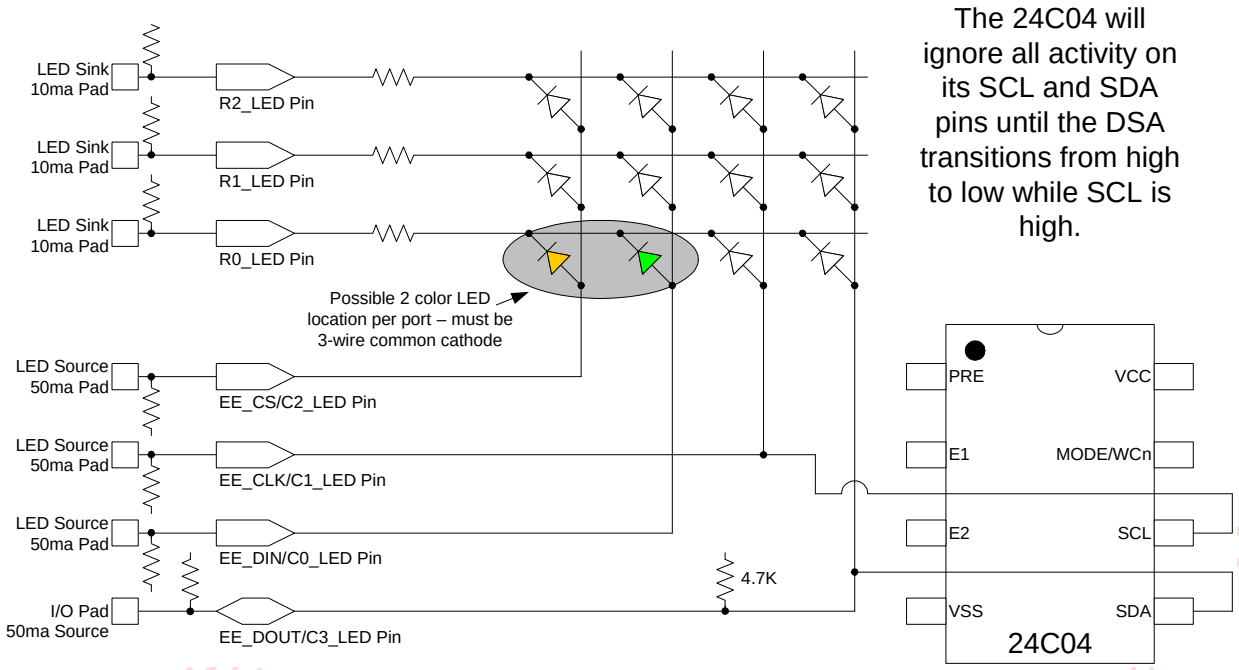


Figure 19: Two LEDs plus 2 wire EEPROM



2.4.1 LED Options

Each port supports up to two LEDs that can be configured individually to show many different options.

These options include:

- Link (off = no link, on = link)
- Activity (off = no activity, on = blink)
- Link/Activity (off = no link, on = link, blink = activity)
- 10 Mbps Link (off = no link, on = 10 Mbps link)
- 10 Mbps Link/Activity (off = no activity, on = 10 Mbps link, blink = activity)
- 100 Mbps Link (off = no link, on = 100 Mbps link)
- 100 Mbps Link/Activity (off = no activity, on = 10 Mbps link, blink = activity)
- 10/100 Mbps Link (off = no link, on = 10/100 Mbps link)
- 10/100 Mbps Link/Activity (off = no activity, on = 10/100 Mbps link, blink = activity)
- Gig Link (off = no link, on = Gig link)
- Gig Link/Activity (off = no activity, on = Gig link, blink = activity)
- 10 Mbps/Gig Link (off = no link, on = 10 Mbps or Gig link)
- 10 Mbps/Gig Link/Activity (off = no activity, on = 10 Mbps or Gig link, blink = activity)
- 100 Mbps/Gig Link (off = no link, on = 100 Mbps or Gig link)
- 100 Mbps/Gig Link/Activity (off = no activity, on = 100 Mbps or Gig link, blink = activity)
- Link/Activity/Speed by blink rate (off = no link, on = link, blink = activity, blink speed = link speed)
- Duplex/Collision (off = half-duplex, on = full-duplex, blink = collision)
- Force Blink
- Force On
- Force Off
- Special (see Section 2.4.2)

Each port's LED options can be configured in the switch port registers (port offset 0x16). Please refer to 88E6172/88E6176 Datasheet Part 2: Switch Core for more information.

2.4.2 Special LEDs

In some applications, two sets of LEDs are desired. One set on the rear panel which would indicate Link/Speed/Activity per port and a second set on the front panel where a common LED can indicate the LAN and/or WAN Activity on a combination of ports. The special LEDs available on the 88E6172/88E6176 device can be used for these types of applications.

Special LEDs are available on Ports 0-1 and can be configured for any of the LEDs available on that port. The special functions are as follows:

Port 0 Special LED – LAN Link/Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Ports 0-4.

Port 1 Special LED – WAN Link Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Port 0.

2.4.3 Power up LED Configurations

The power up LED configuration can be set by the LED_SEL[1:0] pins. These pins are internally pulled high, setting a default configuration of 0x3, but can be configured at Reset using 4.7 kohm pull-down resistors.

The functions of each LED for the standard configuration options are given in the following tables:

Table 21: LED_SEL[1:0] = 0x3 (Default)

	C0_LED	C1_LED	C2_LED	C3_LED
R0_LED	Port 0 Link/Activity	Port 1 Link/Activity	Port 0 Gig Link	Port 1 Gig Link
R1_LED	Port 2 Link/Activity	Port 3 Link/Activity	Port 2 Gig Link	Port 3 Gig Link
R2_LED	Port 4 Link/Activity	LAN Link/Activity (Default Ports 0-4)	Port 4 Gig Link	Fiber Link from SERDES

This configuration is designed for systems with one or two LEDs where the first LED can be used to show Link and Activity while the second LED can be used to show a higher speed link has been established (either Gig only or 100/Gig). The special LAN and WAN LEDs can be used on the front panel of the switch to show LAN/WAN activity (see Figure 20).

Figure 20: LED_SEL[1:0] = 0x3 Example Implementation

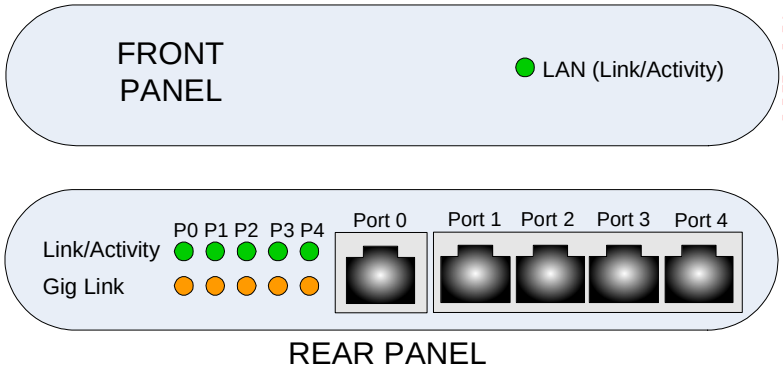


Table 22: LED_SEL[1:0] = 0x2

	C0_LED	C1_LED	C2_LED	C3_LED
R0_LED	Port 0 Gig Link/Activity	Port 1 Gig Link/Activity	Port 0 10/100 Link/Activity	Port 1 10/100 Link/Activity
R1_LED	Port 2 Gig Link/Activity	Port 3 Gig Link/Activity	Port 2 10/100 Link/Activity	Port 3 10/100 Link/Activity
R2_LED	Port 4 Gig Link/Activity	Fiber Gig Link/Activity	Port 4 10/100 Link/Activity	Fiber 100 Mbps Link/Activity

This configuration is designed for systems with two LEDs where one LED is used to show Gig Link and Activity and the second LED is used to show 10/100 Link and Activity. Port 5's LEDs can be used to show Gigabit and 10/100Mbps Link and Activity on the SERDES port (see Figure 21).

Figure 21: LED_SEL[1:0] = 0x2 Example Implementation

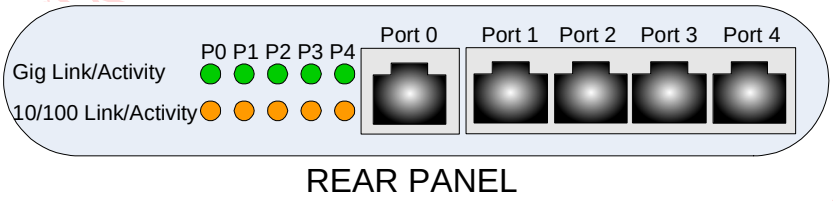


Table 23: LED_SEL[1:0] = 0x1

	C0_LED	C1_LED	C2_LED	C3_LED
R0_LED	Port 0 100/Gig Link/Activity	Port 1 100/Gig Link/Activity	Port 0 10/100 Link/Activity	Port 1 10/100 Link/Activity
R1_LED	Port 2 100/Gig Link/Activity	Port 3 100/Gig Link/Activity	Port 2 10/100 Link/Activity	Port 3 10/100 Link/Activity
R2_LED	Port 4 100/Gig Link/Activity	Fiber 100 Mbps Link/Activity	Port 4 10/100 Link/Activity	Fiber Gig Link/Activity

This configuration is designed to work with bi-color or tri-color LEDs where one color can be used to show link/activity at one speed, the second color can be used to show link/activity at a second speed, and the third color (or mix of the first two) can be used to show link/activity at the third speed. By using a combination of LED 0 and LED 1 the user has the option of using the mixed color to identify any of the three speeds.

With this configuration, only LED 0 will light if there is Gig Link/Activity and only LED 1 will light if there is 10Mb Link/Activity. If there is 100Mb Link/Activity then both LED 0 and LED 1 will light causing a mixed color. This example is shown in Figure 22.

Figure 22: LED_SEL[1:0] = 0x1 Example Implementation

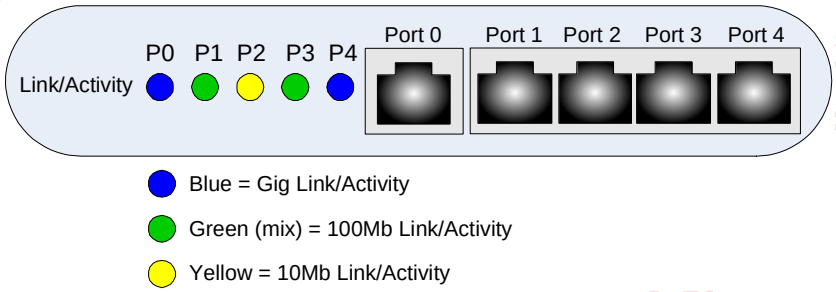
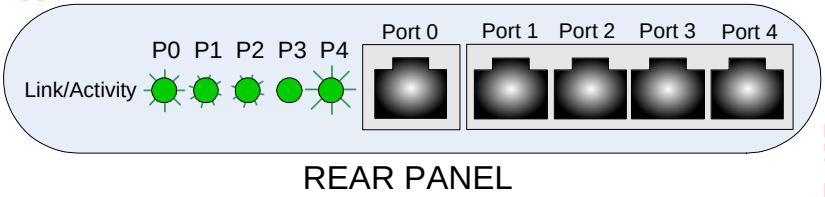


Table 24: LED_SEL[1:0] = 0x1

	C0_LED	C1_LED	C2_LED	C3_LED
R0_LED	Port 0 Link/Activity/Speed (by blink rate)	Port 1 Link/Activity/Speed (by blink rate)	Reserved	Reserved
R1_LED	Port 2 Link/Activity/Speed (by blink rate)	Port 3 Link/Activity/Speed (by blink rate)	Reserved	Reserved
R2_LED	Port 4 Link/Activity/Speed (by blink rate)	Port 5 Link/Activity	Reserved	Port 6 Link/Activity

This configuration is designed for a system with a single LED, where the speed of the link can be observed by the blink rate of the LED (the faster the link, the faster the blink rate). The default blink rates are 84ms for 1Gbps, 170ms for 100 Mbps, and 340ms for 10 Mbps (see Figure 23).

Figure 23: LED_SEL[1:0] = 0x0 Example Implementation

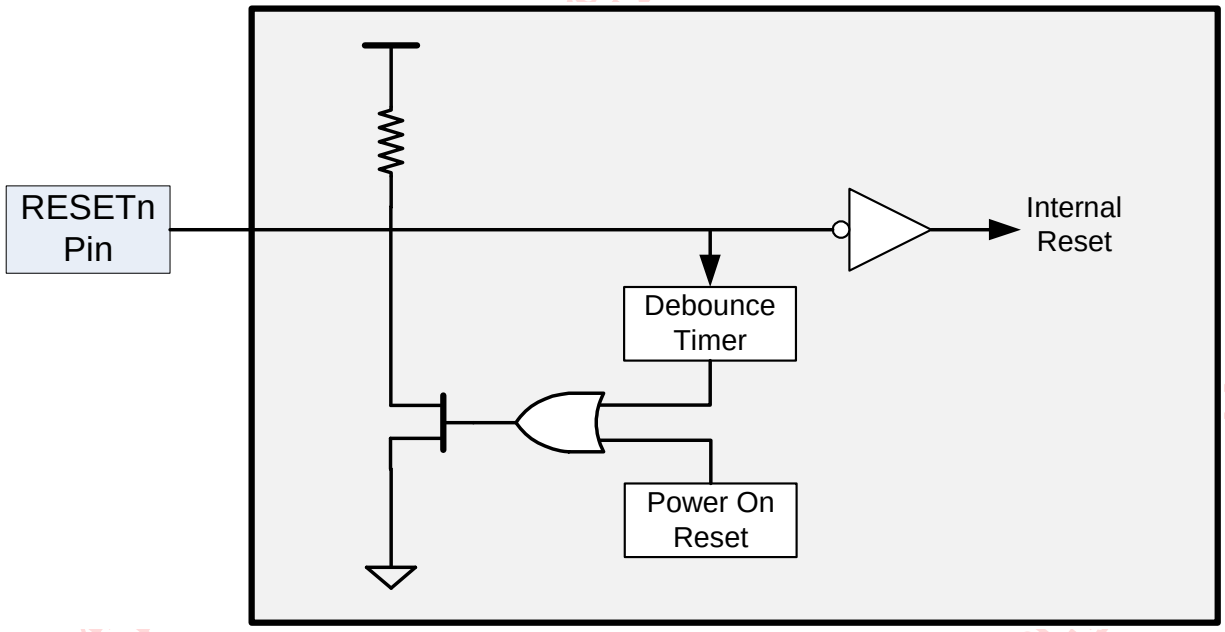


REAR PANEL

2.5 Reset Controller

The device has a built in reset controller which can eliminate the need for external reset components. The RESETn pin is a bi-directional signal which can be used to reset other devices on the same PCB. Figure 24 shows a simplified block diagram of the internal reset circuit.

Figure 24: Simplified Block Diagram of Internal Reset Circuitry



When power is first applied to the chip, the Power On Reset circuit will drive the RESETn pin low for a short time and then RESETn becomes an input. When the Reset timer detects an input high state on the RESETn pin it will drive RESETn low for an additional period before becoming an input again.

Because RESETn is a bi-directional pin, special design considerations may be needed.

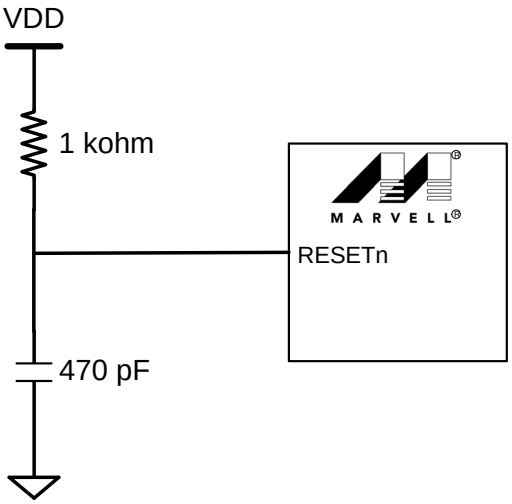
There are five common reset scenarios:

- No external reset source
- Push Button reset with a single device
- Reset driven by GPIO pin on a single device
- Reset driven by GPIO pin with multiple devices
- Push Button reset with multiple devices

2.5.1 No External Reset Source

When there is no external reset source on the board (either push button or external reset controller) it is recommended that the circuit shown in Figure 25 is used.

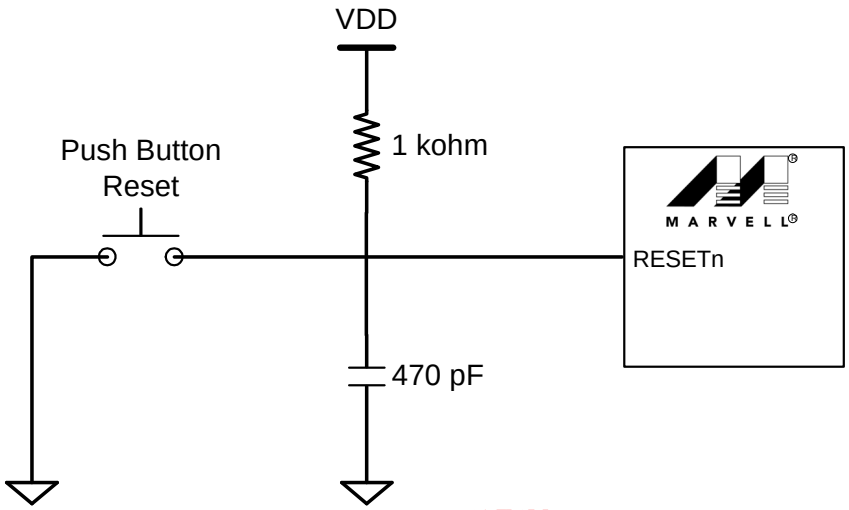
Figure 25: Recommended Circuit with No External Reset



2.5.2 Push Button Reset

In the case of a push button reset source or if there is no other reset controller on the board, The RESETn pin can generate its own reset pulse and can drive reset to other chips on the same board. Figure 26 shows the recommended circuit for applications with a push button.

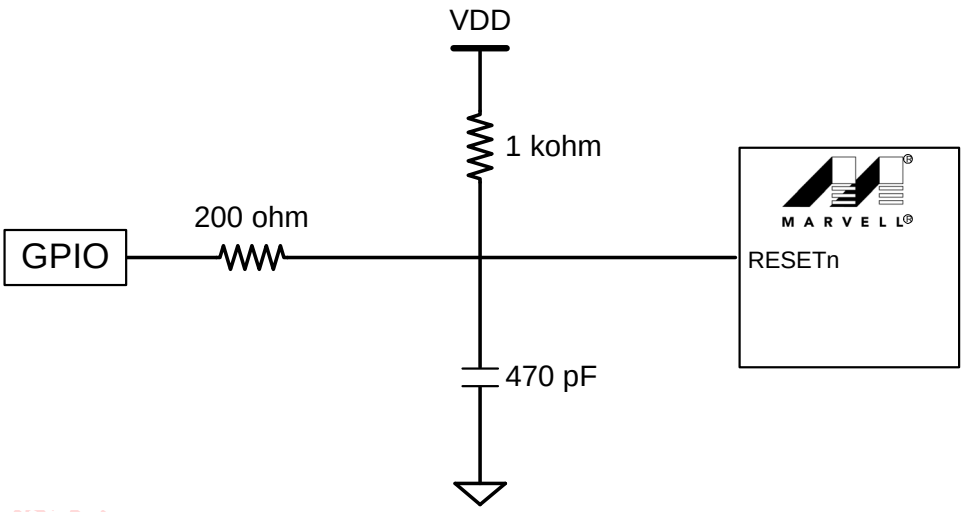
Figure 26: Push Button Reset Circuit



2.5.3 Reset Driven with GPIO Signal

When RESETn is driven with a GPIO or multi-purpose pin, it is possible for the GPIO pin to drive output high while the RESETn pin to drives output low. In this case one or both parts could be damaged if there is no current limiting resistor between them. The circuit in Figure 27 is recommended in this case.

Figure 27: Reset Connected to GPIO Pin

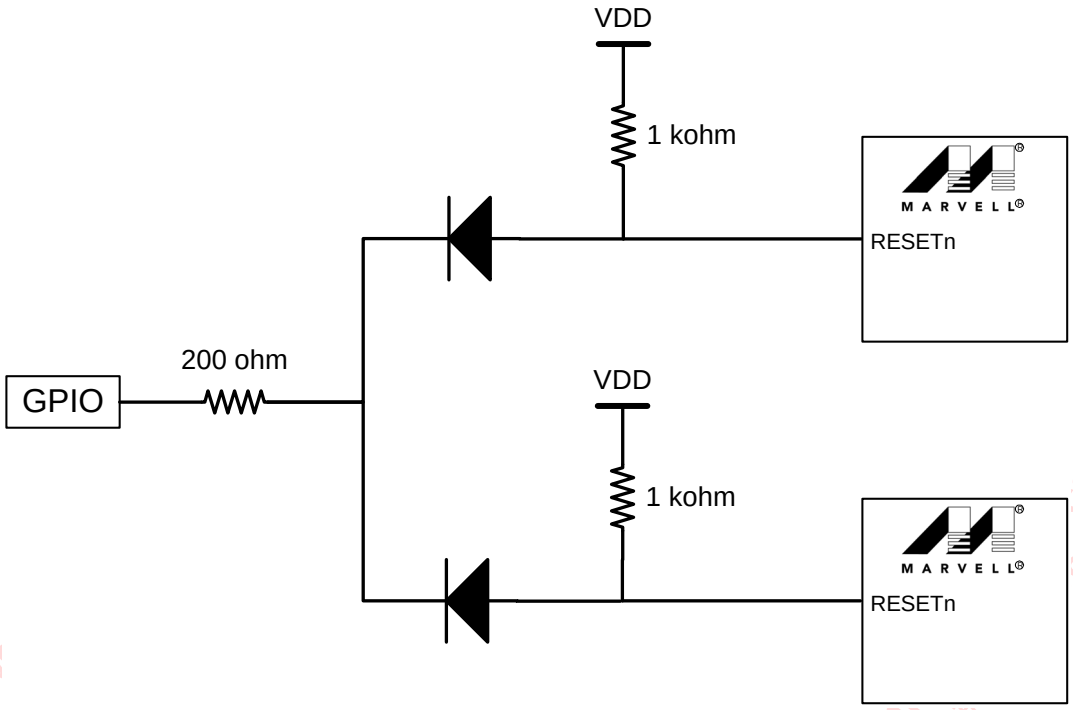


When the GPIO drives output high while the RESETn pin drives low the 200 ohm resistor will limit current and prevent pad damage. Note the value of the resistors may have to be changed based on the specific characteristics of the GPIO pin. The resistor values should be chosen so that voltage on the RESETn pin is below the V_{IL} max voltage threshold.

2.5.4 Reset Driven with GPIO Signal with Multiple Devices

On a design with multiple parts with built in reset controllers, a general purpose diode can be used to prevent the devices from continuously resetting each other. The circuit in Figure 28 is recommended in this case.

Figure 28: Circuit with Multiple Built-in Reset Controllers On Board

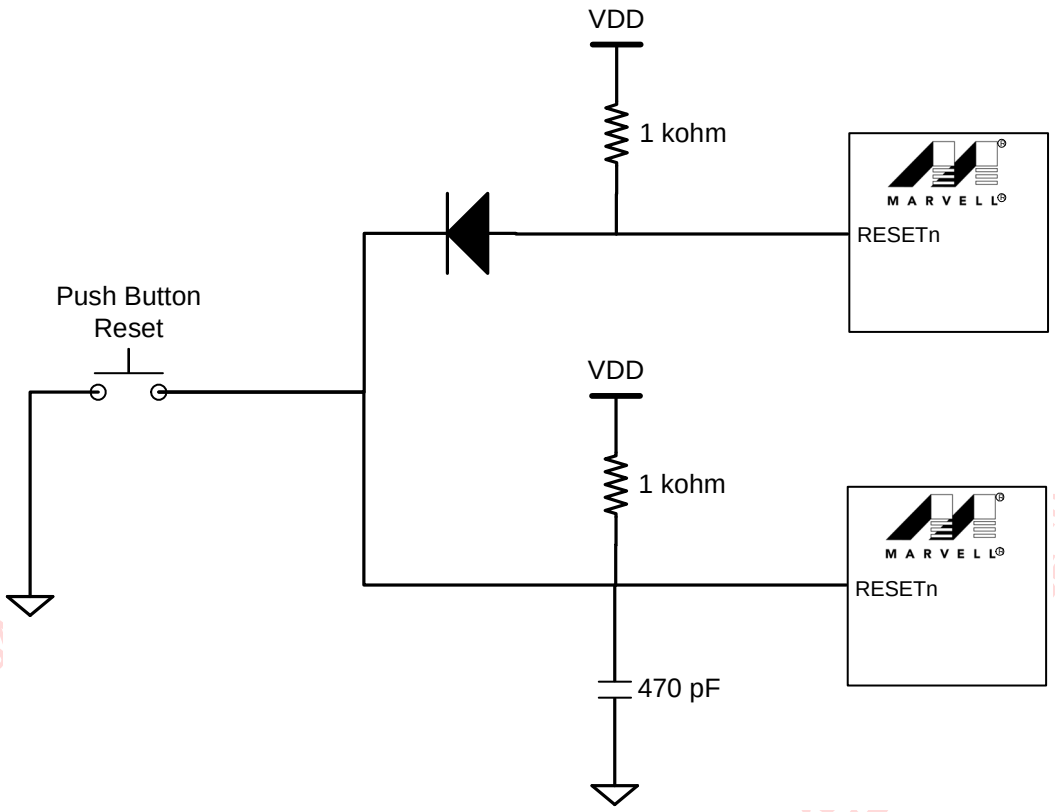


Because there is no push button switch to debounce, the 470 pF cap is optional.

2.5.5 Push Button Reset with Multiple Devices

If multiple devices are used with a push button reset, the circuit in Figure 29 is recommended. In this instance, a general purpose diode can be used to prevent the devices from continuously resetting each other.

Figure 29: Design with Two Reset Controllers and Using a Push Button Switch



In this case only one diode is needed. The 470 pF cap is only needed on the push button side of the diode for debounce.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 25: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on any 3.3V signal with respect to VSS	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on any 2.5V signal with respect to VSS	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.8)}$	Power Supply Voltage on any 1.8V supply with respect to VSS	-0.5	1.8	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
$V_{DD(1.0)}$	Power Supply Voltage on any 1.0V supply with respect to VSS	-0.5	1.0	+3.6 or $V_{DD(1.8)}$ +0.5[3] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to VSS	-0.5		+3.6 or V_{DDO_PIN}[4] +0.5[5] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[6]	°C

1. VDD(2.5) must never be more than 0.5V greater than VDD(3.3) or damage will result. Power must be applied to VDD(3.3) before or at the same time as VDD(2.5).
2. VDD(1.8) must never be more than 0.5V greater than VDD(2.5) or damage will result. Power must be applied to VDD(2.5) before or at the same time as VDD(1.8).
3. VDD(1.0) must never be more than 0.5V greater than VDD(1.8) or damage will result. Power must be applied to VDD(1.8) before or at the same time as VDD(1.0).
4. The VDDO pad ring has separate I/O power supply options. Therefore, the voltage applied to a group of I/O pins must follow what is defined in Section 1.
5. VPIN must never be more than 0.5V greater than VDDO or damage will result.
6. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

3.2 Recommended Operating Conditions

Table 26: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For any 3.3V supply pin[1]	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For any 2.5V supply pin[2]	2.375	2.5	2.625	V
$V_{DD(1.8)}$	1.8V power supply	For any 1.8V supply pin	1.710	1.8	1.890	V
$V_{DD(1.0)}$	1.0V power supply	For any 1.0V supply pin	.950	1.0	1.050	V
T_A	Ambient operating temperature[3]	Commercial parts	0		70	°C
		Industrial parts[4]	-40		85	°C
T_J	Maximum junction temperature				125[2]	°C
RSET	Internal bias reference	External resistor value required to be placed between RSET and VSS pins	4950	5000	5050	Ω

1. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
2. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
3. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on "TJ Thermal Calculations" for more information.
4. Industrial parts have an “I” following the commercial part numbers. See Section 5.1, Ordering Part Numbers and Package Markings, on page 107.

3.3 Thermal Conditions

3.3.1 Thermal Conditions for the 88E6172/88E6176 device 128-pin TQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 128-Pin TQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		24.8		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		21.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		20.4		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		19.7		°C/W
Ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 128-Pin TQFP package $\Psi_{JT} = (T_J - T_{TOP})/P$. T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.22		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.33		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.42		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.48		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 128-Pin TQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		7.7		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 128-Pin TQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		15.5		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

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Note

The following current consumption numbers are shown when external supplies are used. If the internal regulators are used the current consumption will not change. However, the power consumed inside the package will increase. Care must be exercised when calculating the total current drawn on a rail when internal regulators are used. For example, if the internal regulator (VDD33) is used to generate 1.8V internally, then the 68 mA consumed by the Px_AVDD rails has to be added to the current consumption of the 3.3V supply.

Table 27: 88E6176 Device Current Consumption

Pins	Parameter	Condition	Min	Typ	Max	Units
Px_AVDD33	3.3V power to analog core for each Gig PHY interface	All ports active (Port 0 - Port 4 at 1000 Mbps)		279		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		71		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		148		mA
		EEE disabled, all ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		283		mA
		EEE disabled, all ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		71		mA
		EEE disabled, all ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		73		mA
		Reset		3		mA
		No link on any port		3		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		42		mA

Table 27: 88E6176 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
Px_AVDD18	1.8V power to analog core for each Gig PHY interface	All ports active (Port 0 - Port 4 at 1000 Mbps)		338		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		157		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		103		mA
		EEE disabled, all ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		338		mA
		EEE disabled, all ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		157		mA
		EEE disabled, all ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		103		mA
		Reset		51		mA
		No link on any port		72		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		130		mA
EE_VDDO	3.3V to EEPROM and LED pins.	All ports active at 1000 Mbps		17		mA
		All ports active at 100 Mbps		8		mA
		All ports active at 10 Mbps		8		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		14		mA
		EEE disabled, all ports idle and linked at 100 Mbps		7		mA
		EEE disabled, all ports idle and linked at 10 Mbps		7		mA
		Reset		16		mA
		No link on any port		2		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		15		mA

Table 27: 88E6176 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
VDDO	3.3V to SMI CPU bus and Port 5's and Port 6's GMII/MII I/O pins.	All ports active at 1000 Mbps		72		mA
		All ports active at 100 Mbps		17		mA
		All ports active at 10 Mbps		7		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		38		mA
		EEE disabled, all ports idle and linked at 100 Mbps		14		mA
		EEE disabled, all ports idle and linked at 10 Mbps		8		mA
		Reset		3		mA
		No link on any port		3		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		35		mA
	2.5V to SMI CPU bus and Port 5's and Port 6's GMII/MII I/O pins.	All ports active at 1000 Mbps		54		mA
		All ports active at 100 Mbps		11		mA
		All ports active at 10 Mbps		3		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		24		mA
		EEE disabled, all ports idle and linked at 100 Mbps		9		mA
		EEE disabled, all ports idle and linked at 10 Mbps		4		mA
		Reset		1		mA
		No link on any port		1		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		22		mA
	1.8V to SMI CPU bus and Port 5's and Port 6's GMII/MII I/O pins.	All ports active at 1000 Mbps		38		mA
		All ports active at 100 Mbps		6		mA
		All ports active at 10 Mbps		2		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		13		mA
		EEE disabled, all ports idle and linked at 100 Mbps		5		mA
		EEE disabled, all ports idle and linked at 10 Mbps		1		mA
		Reset		1		mA
		No link on any port		1		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		22		mA

Table 27: 88E6176 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
VDD_ CORE	1.0V power to digital core	All ports active at 1000 Mbps		474		mA
		All ports active at 100 Mbps		162		mA
		All ports active at 10 Mbps		121		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		436		mA
		EEE disabled, all ports idle and linked at 100 Mbps		159		mA
		EEE disabled, all ports idle and linked at 10 Mbps		120		mA
		Reset		31		mA
		No link on any port		122		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		163		mA

3.5 DC Electrical Characteristics

3.5.1 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 28: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	XTAL_IN		1.4		1.99	V
		All others	VDDO = 3.135	2.2			V
			VDDO = 2.375V	1.7			V
			VDDO = 1.710V	1.2			V
V_{IL}	Low level input voltage	XTAL_IN		-0.3		0.54	V
		All others	VDDO = 3.135	-0.4		0.94	V
			VDDO = 2.375V	-0.4		0.7	V
			VDDO = 1.710V	-0.4		0.51	V
V_{OH}	High level output voltage	LED pins	I_{OH} = -8 mA	VDDO - 0.4			V
		All others (except INTn [1])	I_{OH} = -4 mA	VDDO - 0.4			V
V_{OL}	Low level output voltage	INTn and LED pins	I_{OL}= 8 mA			0.4	V
		All others	I_{OL}= 4 mA			0.4	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DD}$			+ 10 - 50	µA
		With pull-down resistor	$0<V_{IN}<V_{DD}$			+ 50 - 10	µA
		XTAL_IN - with internal resistor				±80	µA
		All others	$0<V_{IN}<V_{DD}$			±10	µA
C_{IN}	Input capacitance	XTAL_IN			5		pF
		All others				5	pF

1. The INTn is an active low, open drain pin. See INTn description in the Signal Description.

3.5.2 RESETn

Table 29: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	RESETn		VDDO * 70%			V
V_{IL}	Low level input voltage	RESETn				VDDO * 30%	V

3.5.3 SGMII Interface

SGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website ftp://ftp-eng.cisco/smii/sgmii.pdf. It uses a modified LVDS specification based on the IEEE standard 1596.3. Refer to that standard for the exact definition of the terminology used in the following table. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

3.5.3.1 Transmitter DC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1400	mV
V_{OL}	Output Voltage Low	700			mV
V_{RING}	Output Ringing			10	%
$\|V_{OD}\|$[2]	Output Voltage Swing (differential, peak)	Programmable - see Table 30.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 3.5.3.2 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40		60	Ωs
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when S_OUT+ and S_OUT- are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

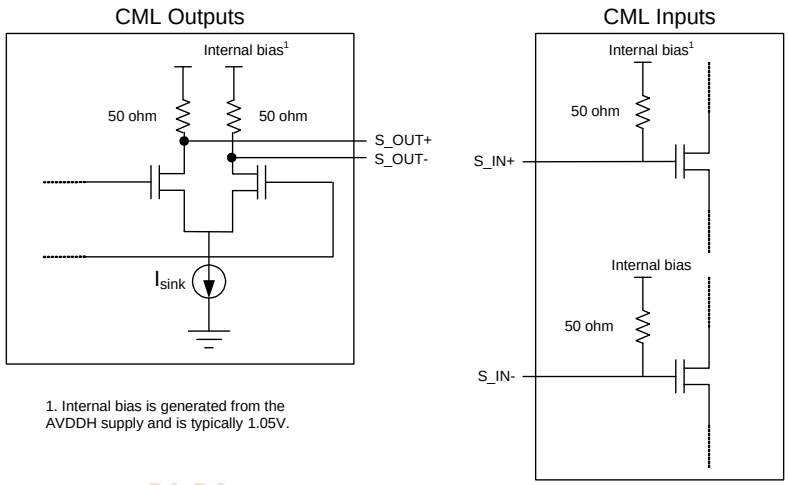
1. Parameters are measured with outputs AC connected with 100 ohm differential load.
2. Output amplitude is programmable by writing to Register 26_1.2:0.

Table 30: Programming SGMII Output Amplitude

Register 26_1 Bits	Field	Description
2:0	SGMII/Fiber Output Amplitude[1]	Differential voltage peak measured. Note that internal bias minus the differential peak voltage must be greater than 700 mV. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

1. Cisco SGMII specification limits are |VOD| = 150 mV - 400 mV peak differential.

Figure 30: CML I/Os



1. Internal bias is generated from the AVDDH supply and is typically 1.05V.

3.5.3.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Figure 30 for details. (If AVDD18 is used to generate the internal bias, the internal bias value will typically be 1.05V.)
- The output voltage swing is programmed by Register 26_1.2:0 (see Table 30).
- Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing. See Figure 31 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the input structure shown in the CML Inputs diagram in Figure 32. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

- Voffset (i.e., common mode voltage) = internal bias - (single-ended peak-peak voltage swing/2). See Figure 32 for details.
- If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 31: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

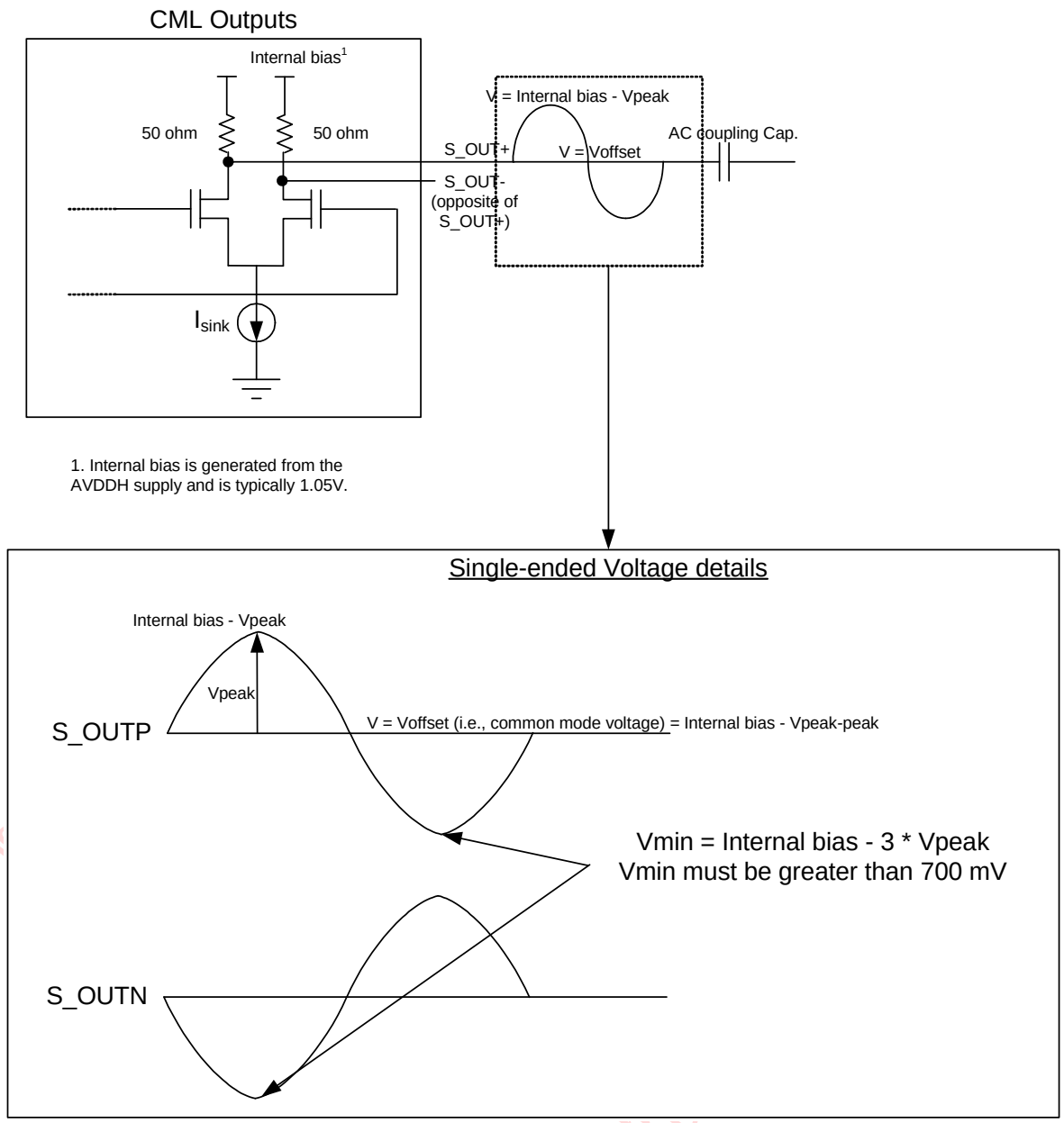
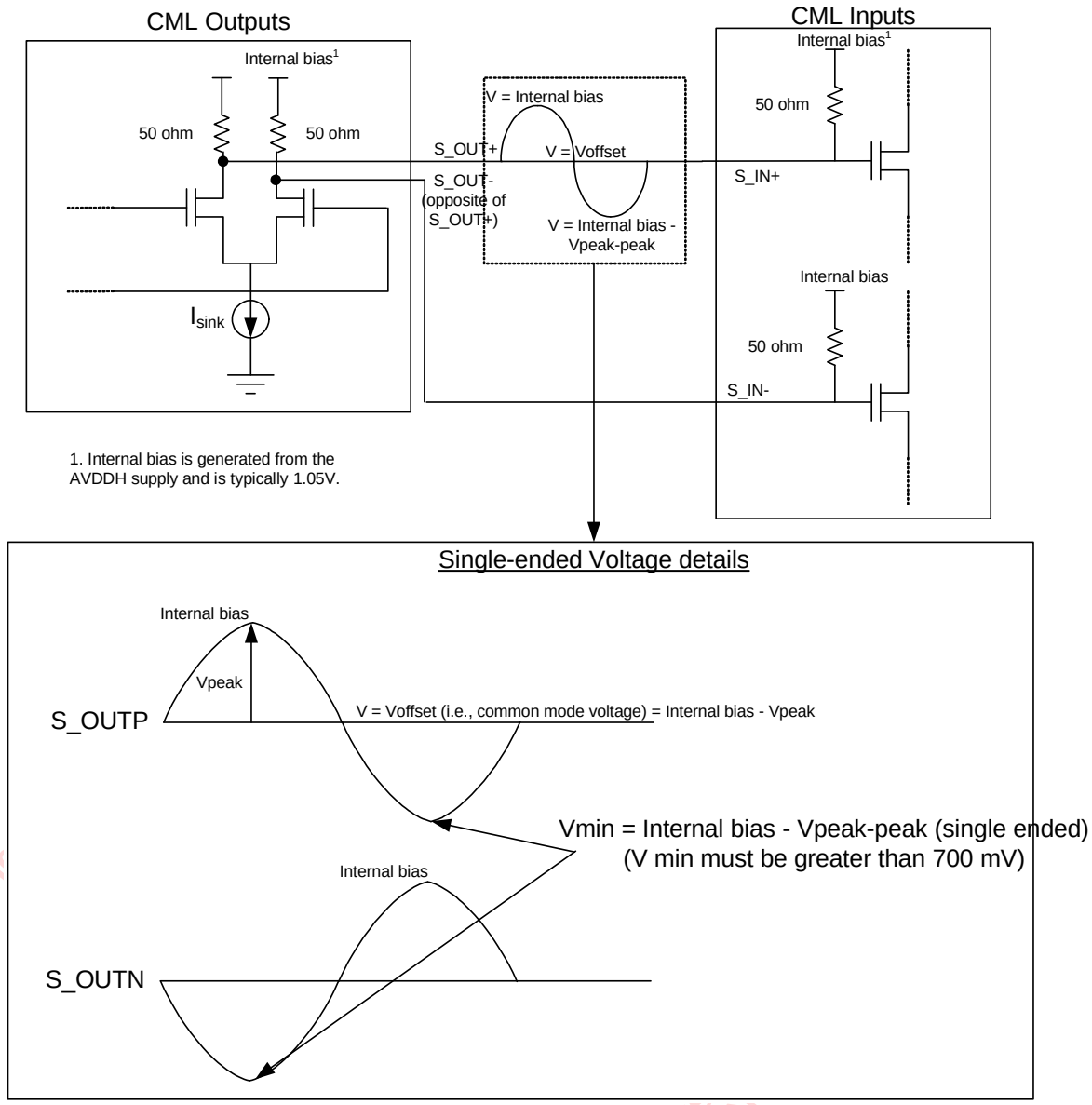


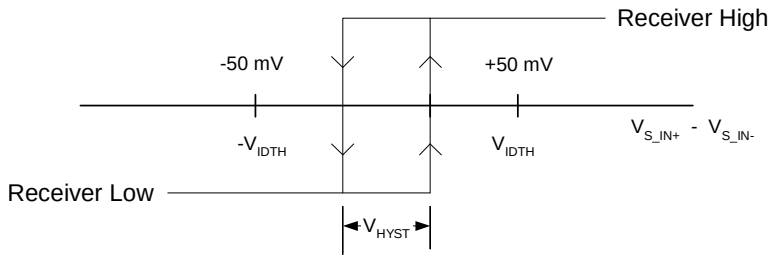
Figure 32: DC connection to a CML receiver



3.5.3.3 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input Voltage range a or b	675		1725	mV
V_{IDTH}	Input Differential Threshold	-50		+50	mV
V_{HYST}	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 Ω Differential Input Impedance	80		120	Ω

Figure 33: Input Differential Hysteresis



3.6 AC Electrical Specifications

3.6.1 Reset and Configuration Timing

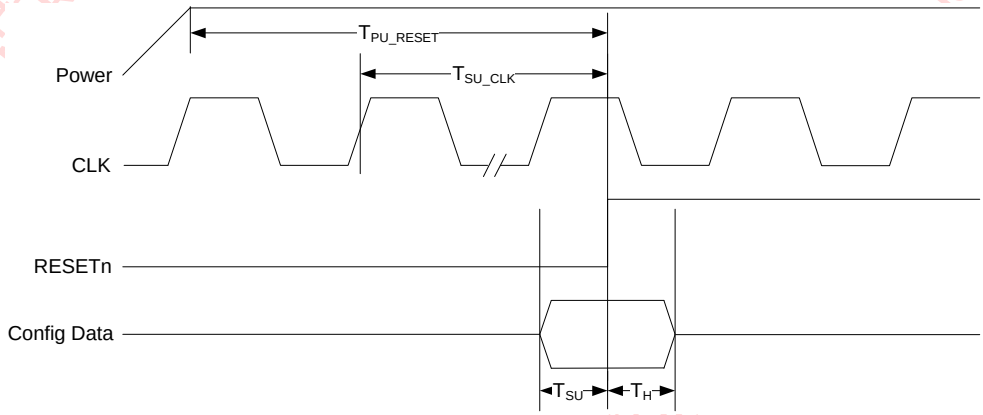
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 31: Reset and Configuration

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or sub-sequent resets after power up	10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			Clks
T_{SU}	Configuration data valid prior to RESETn de-asserted[1]		200			ns
T_{HD}	Config data valid after RESETn de-asserted		0			ns

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn. All configuration pins that become outputs during normal operation will remain tri-stated for 40 ns after the rising edge of RESETn.

Figure 34: Reset and Configuration Timing



3.6.2 Clock Timing

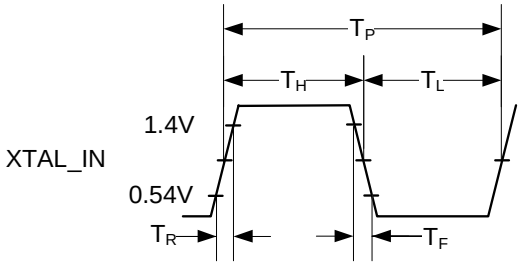
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 32: IEEE DC Transceiver Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns
T_H	XTAL_IN high time		16			ns
T_L	XTAL_IN low time		16			ns
T_R	XTAL_IN rise				3	ns
T_F	XTAL_IN fall				3	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[2]				200	ps[3]

1. If the crystal option is used, ensure that the frequency is 25.000 MHz ± 50 ppm.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 35: Oscillator Clock Timing



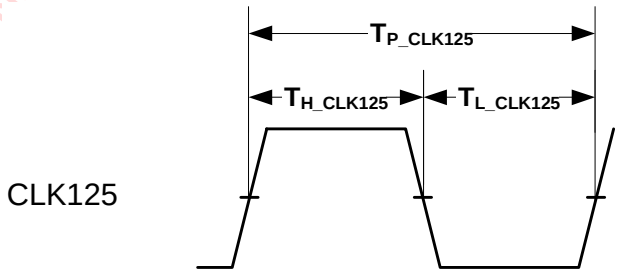
3.6.3 CLK125 Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Table 33: CLK125 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_CLK125}	CLK125 Period		8 -50 ppm	8	8 +50 ppm	ns
T_{H_CLK125}	CLK125 High time		3.5	4	4.4	ns
T_{L_CLK125}	CLK125 Low time		3.5	4	4.4	ns
T_{J_CLK125}	CLK125 Total Jitter		-	-	80	ps (peak-peak)
T_{P_CD}	CLK125 power up to stable clock delay				300	µs

Figure 36: CLK125 Timing



3.7 GMII Timing

3.7.1 GMII Transmit Timing

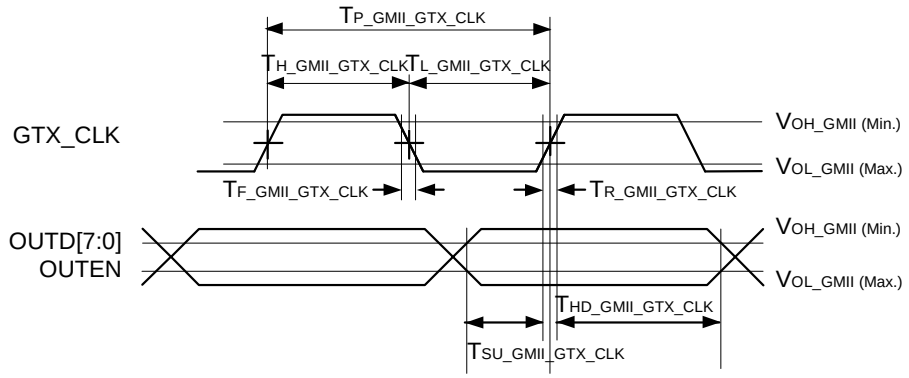
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 34: GMII Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_GTX\_CLK}$	GMII output to clock		2.5			ns
$T_{HD\_GMII\_GTX\_CLK}$	GMII clock to output		0.5			ns
$T_{H\_GMII\_GTX\_CLK}$	GTX_CLK High		2.5[1]		5.5	ns
$T_{L\_GMII\_GTX\_CLK}$	GTX_CLK Low		2.5[1]		5.5	ns
$T_{P\_GMII\_GTX\_CLK}$	GTX_CLK Period		7.5[1]	8.0		ns
$T_{R\_GMII\_GTX\_CLK}$	GTX_CLK Rise Time				1.0	ns
$T_{F\_GMII\_GTX\_CLK}$	GTX_CLK Fall Time				1.0	ns
$T_{RSLEW\_GMII\_GTX\_CLK}$	GTX_CLK Rising Slew Rate		0.6[2]			V/ns
$T_{FSLEW\_GMII\_GTX\_CLK}$	GTX_CLK Falling Slew Rate		0.6[2]			V/ns

1. GTX_CLK numbers not guaranteed during transition between 10/100/1000BASE-T operation.
2. Instantaneous change during internal VIH_GMII (Min.) and VIL_GMII (Max.).

Figure 37: GMII Transmit Timing



3.7.2 GMII Receive Timing

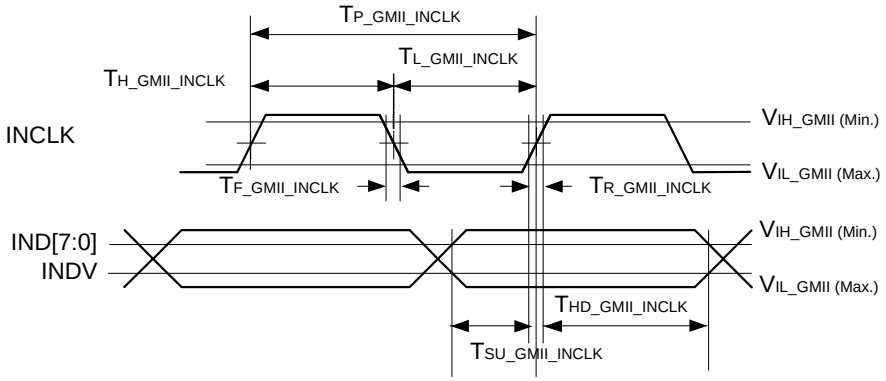
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 35: GMII Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_INCLK}$	GMII Setup Time		2.0			ns
$T_{HD\_GMII\_INCLK}$	GMII Hold Time		0			ns
$T_{H\_GMII\_INCLK}$	INCLK High		2.5[1]			ns
$T_{L\_GMII\_INCLK}$	INCLK Low		2.5[1]			ns
$T_{P\_GMII\_INCLK}$	INCLK Period		7.5[1]	8.0	8.5	ns
F_{GMII_INCLK}	INCLK Frequency		125[1] -100 ppm		125 +100 ppm	MHz
$T_{R\_GMII\_INCLK}$	INCLK Rise Time				1.0	ns
$T_{F\_GMII\_INCLK}$	INCLK Fall Time				1.0	ns

1. RX_CLK toggle rate is “don’t care” if link is down, or if not in 1000BASE-T mode.

Figure 38: GMII Receive Timing



3.8 MII Timing

3.8.1 MII PHY Mode Receive Timing - 100 Mbps

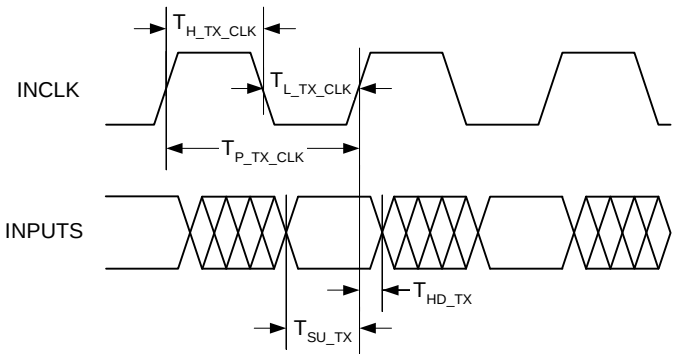
In PHY mode, the P[x]_INCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 36: MII PHY Mode Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$[1]	P[x]_INCLK period	10BASE mode		400		ns
		100BASE mode		40		ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		15			ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		0			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 39: MII PHY Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

3.8.2 MII PHY Mode Transmit Timing - 100 Mbps

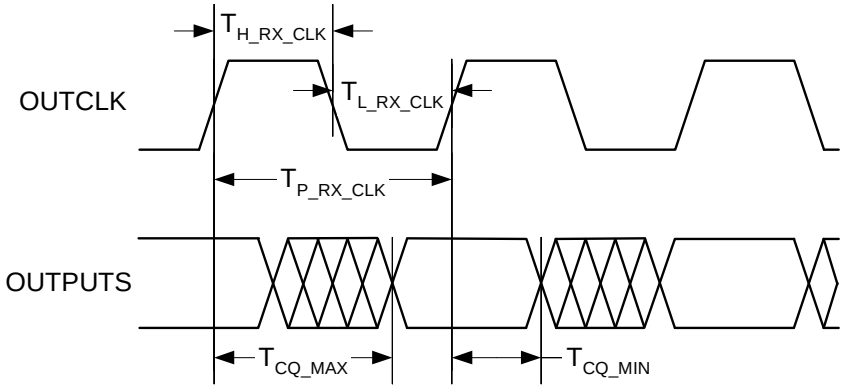
In PHY mode, the P[x]_OUTCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 37: MII PHY Mode Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	10BASE mode		400		ns
		100BASE mode		40		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid				25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		10			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 40: MII PHY Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an output in this mode.

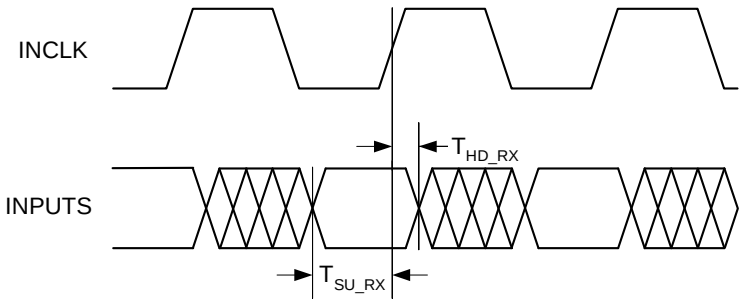
3.8.3 MII MAC Mode Receive Timing

In MAC mode, the P[x]_INCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 38: MII Receive Timing - MAC Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	10			ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	10			ns

Figure 41: MII MAC Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

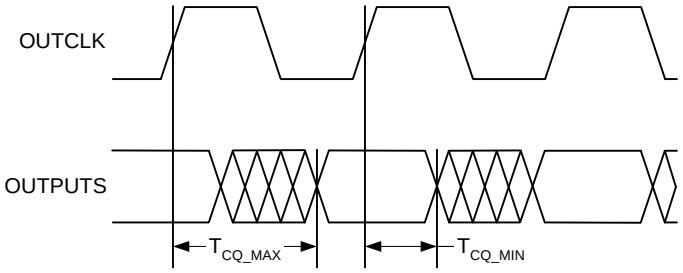
3.8.4 MII MAC Mode Transmit Timing

In MAC mode, the P[x]_OUTCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 39: MII MAC Mode Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid	With 10 pF load			25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) invalid	With 10 pF load	0			ns

Figure 42: MII MAC Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an input in this mode.

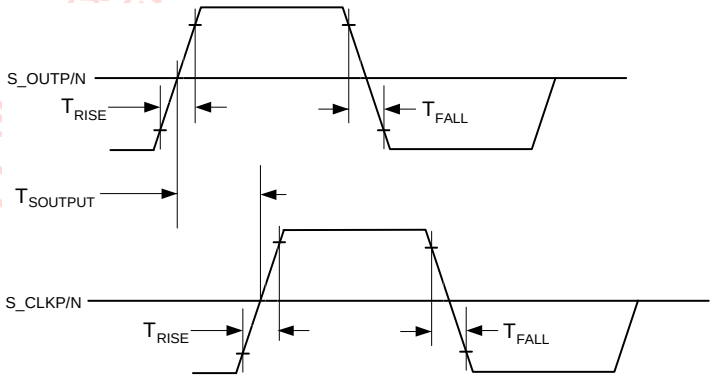
3.9 SGMII Timing (88E6176 Only)

3.9.1 SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{SOUTPUT}$[2]	SERDES output to RxClk_P/N	360	400	440	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.
2. Measured at 50% of the transition.

Figure 43: Serial Interface Rise and Fall Times



3.9.2 SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

3.10 RGMII Timing

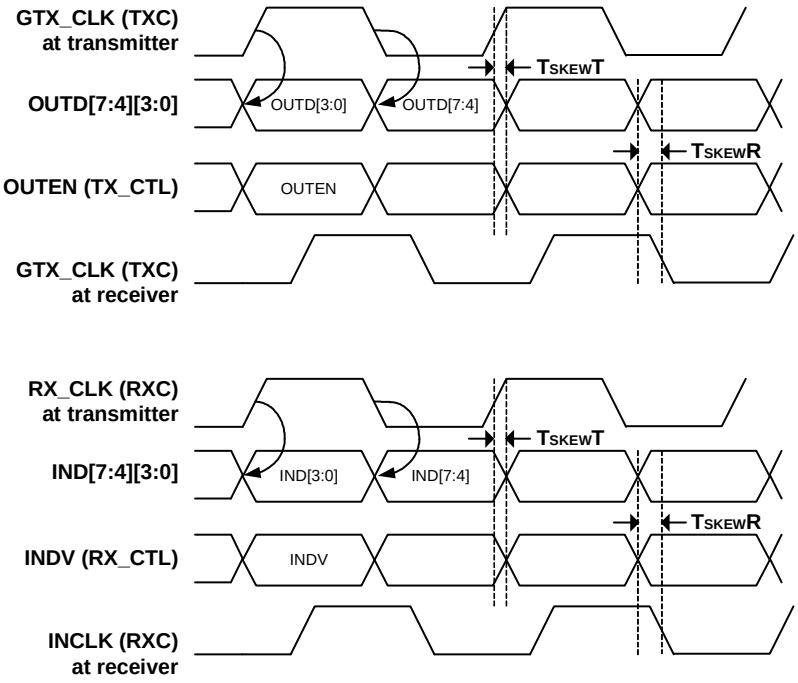
Table 40: RGMII Interface Timing

For other timing modes see Section 3.10.1, RGMII Timing for Different RGMII Modes, on page 95.

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 44: RGMII Multiplexing and Timing



3.10.1 RGMII Timing for Different RGMII Modes

3.10.1.1 RGMII Transmit Timing

Table 41: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{sskew}	RGMII Transmit Delay Control (bit 3) = 0	-0.5		0.5	ns

Figure 45: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 0

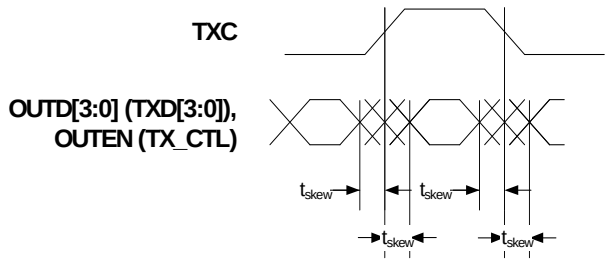
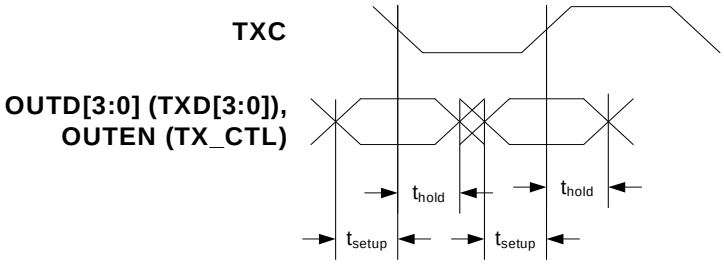


Table 42: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Transmit Delay Control (bit 3) = 1	1.2			ns
t_{hold}		1.0			ns

Figure 46: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 1



3.10.1.2 RGMII Receive Timing

Table 43: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 0	1.0			ns
t_{hold}		0.8			ns

Figure 47: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0

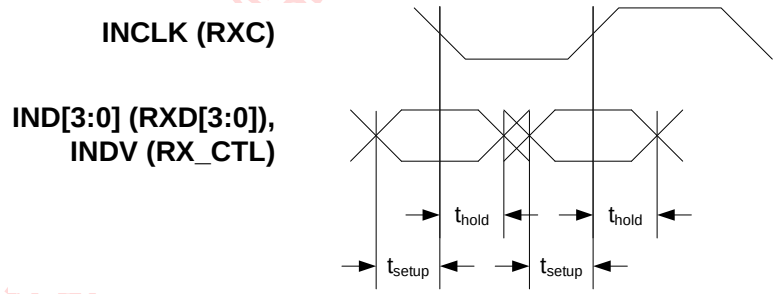
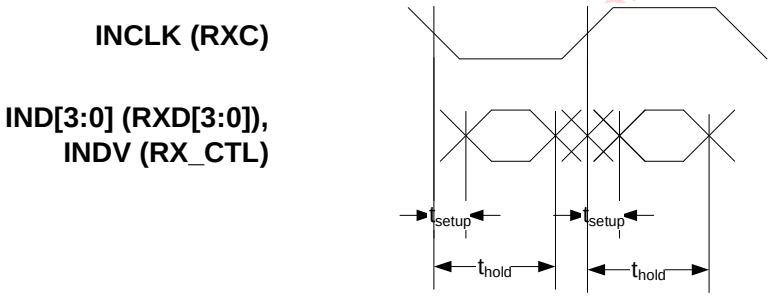


Table 44: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 1	-0.9			ns
t_{hold}		2.7			ns

Figure 48: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1



3.11 RMII Timing

3.11.1 RMII Receive Timing

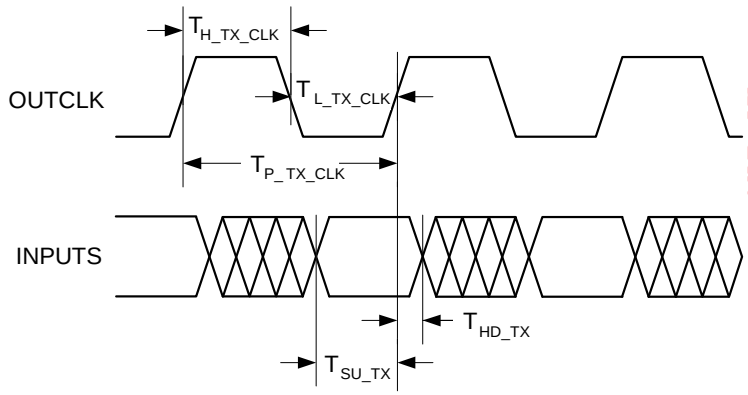
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 45: RMII Receive Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_OUTCLK period[1]	100BASE mode		20		ns
$T_{H\_TX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{SU_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid prior to P[x]_OUTCLK going high.		4			ns
T_{HD_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid after P[x]_OUTCLK going high.		2			ns

1. 50 MHz for 100 Mbps.

Figure 49: RMII Receive Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the input data. It is an output in this mode.

3.11.2 RMII Transmit Timing

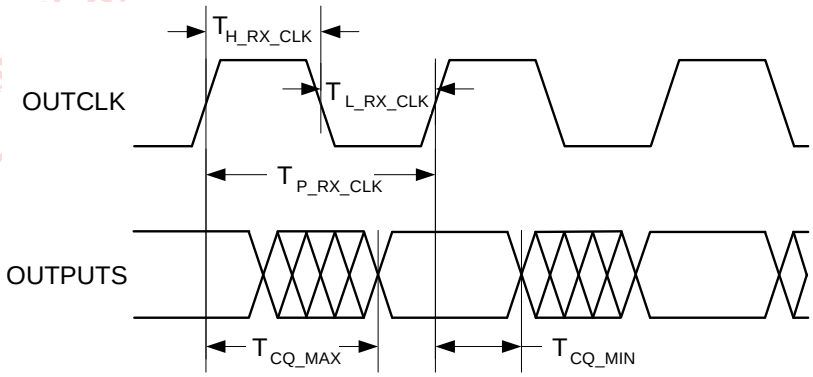
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 46: RMII Transmit Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	100BASE mode		20		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[1:0], P[x]_OUTEN) valid				16	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[1:0], P[x]_OUTEN) invalid		2			ns

1. 50 MHz for 100 Mbps.

Figure 50: RMII Transmit Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.12 Serial Management Interface (SMI) Timing

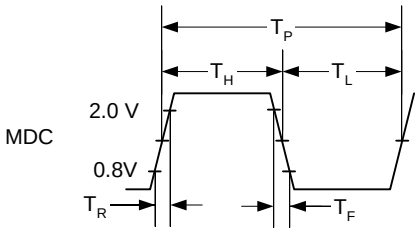
3.12.1 SMI Clock Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 47: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		120			ns	8.33 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	

Figure 51: SMI Clock Timing (CPU Set)



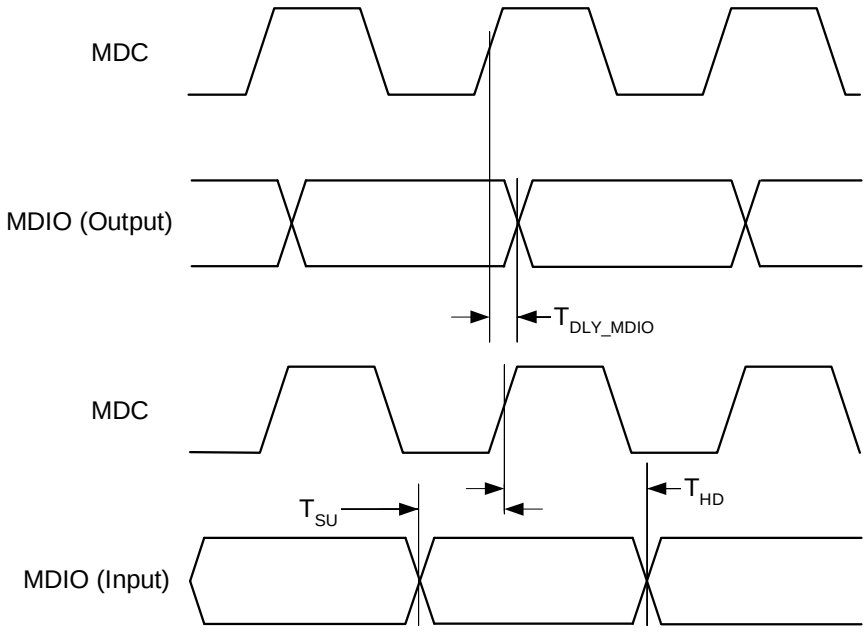
3.12.2 SMI Data Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 48: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		30	ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 52: SMI Data Timing



3.12.3 SMI Timing (PHY Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 49: SMI Clock Timing (PHY Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		120[1]			ns	8.33 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	
T_{TX_SU}	MDIO output setup time		10			ns	2
T_{TX_HD}	MDIO output hold time		10			ns	2
T_{RX_SU}	MDIO input setup time						
T_{RX_HD}	MDIO input hold time						
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		5	ns	3

1. MDC_PHY will track MDC_CPU when the PPU is disabled. When the PPU is enabled the MDC_PHY period will be 240 ns.
2. MDIO input setup and hold time is intentionally sampled with respect to the MDC falling edge.
3. MDIO data is intentionally clocked out on the falling edge of MDC.

Figure 53: SMI Timing Output (PHY Mode)

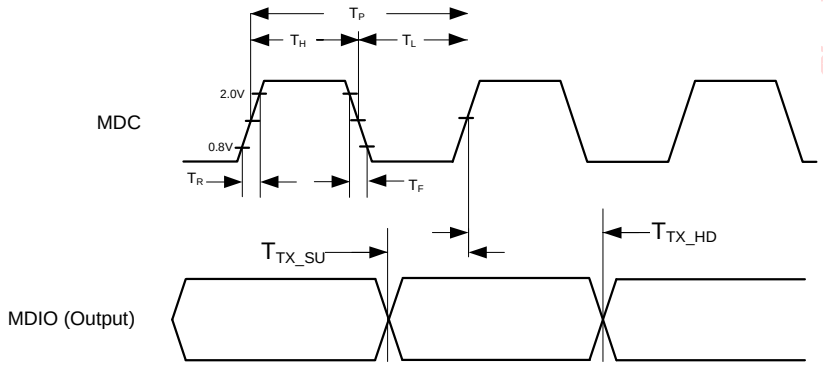
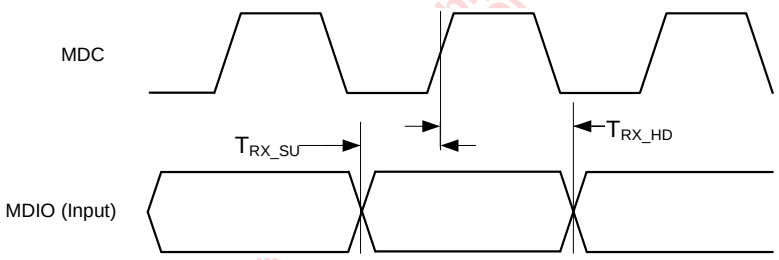


Figure 54: SMI Timing Input (PHY Mode)



3.13 EEPROM Timing

3.13.1 2-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 50: 2-Wire EEPROM Input Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			20000		ns
T_H	EE_CLK high time			10000		ns
T_L	EE_CLK low time			10000		ns
T_{IN}	EE_CLK input time		50		5000	ns

Figure 55: 2-Wire Input Timing

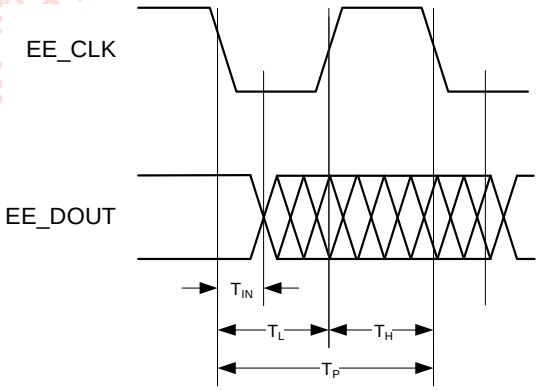
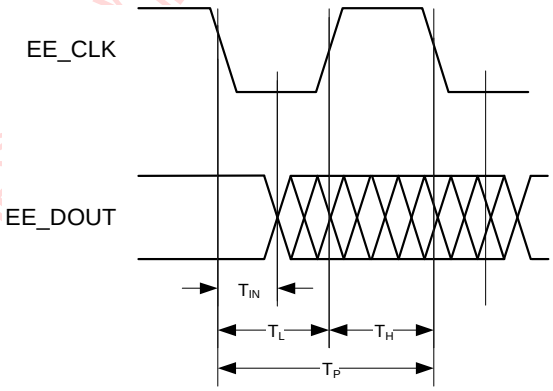


Table 51: 2-Wire EEPROM Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			20000		ns
T_H	EE_CLK high time			10000		ns
T_L	EE_CLK low time			10000		ns
T_{IN}	EE_CLK output time		0		10000	ns

Figure 56: 2-Wire Output Timing



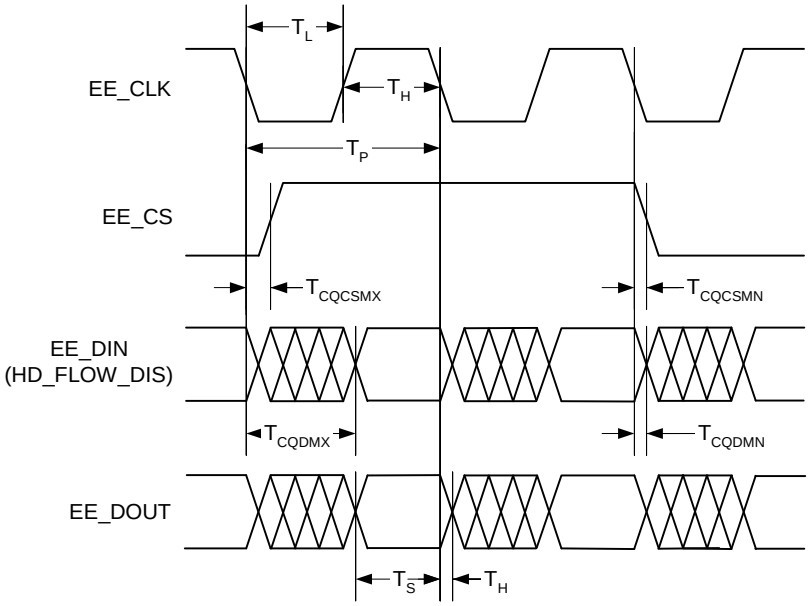
3.13.2 4-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 52: 4-Wire EEPROM Timing

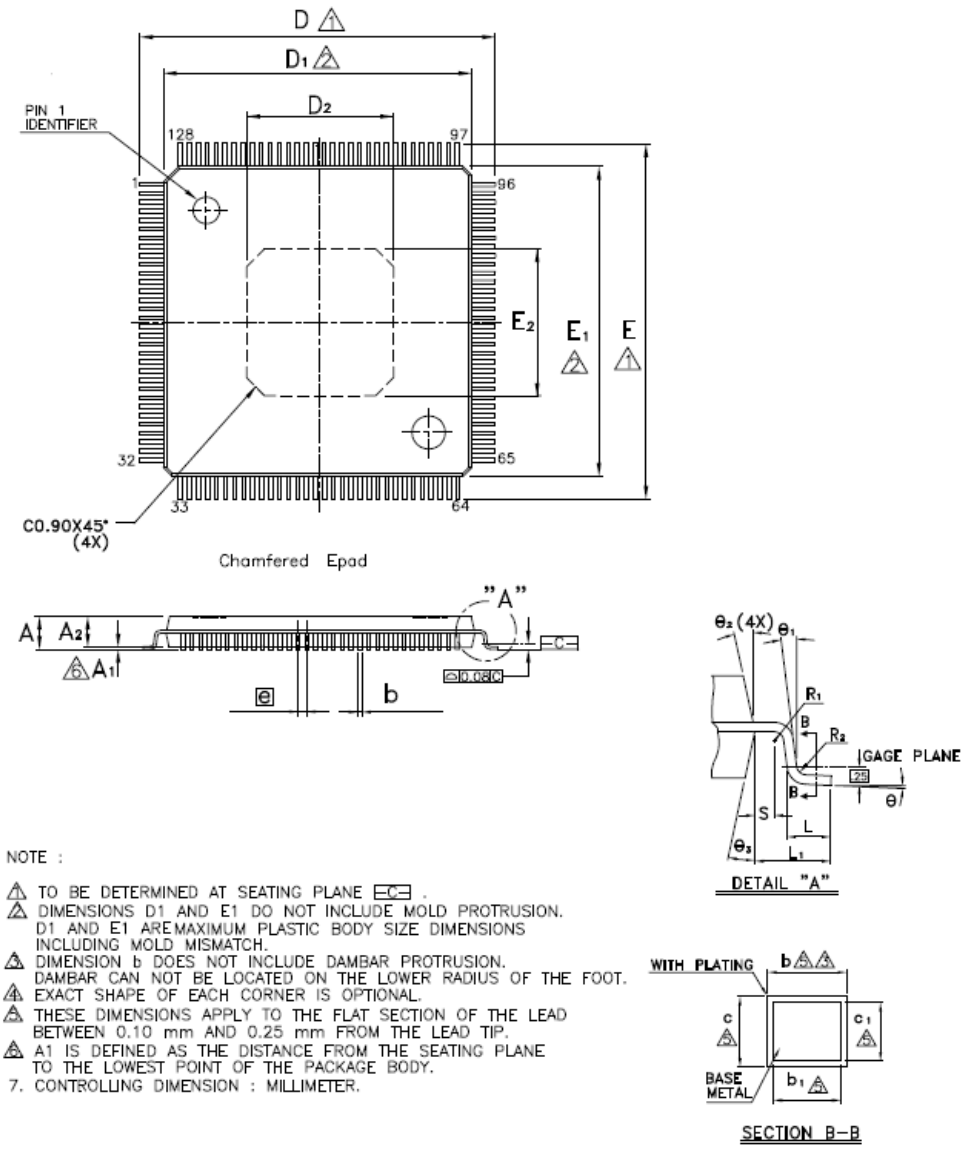
Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			10000		ns
T_H	EE_CLK high time			5000		ns
T_L	EE_CLK low time			5000		ns
T_{CQCSMX}	Serial EEPROM chip select valid	Referenced to EE_CLK			5	ns
T_{CQCSMN}	Serial EEPROM chip select invalid				5	ns
T_{CQDMX}	Serial EEPROM data transmitted to EEPROM valid				10	ns
T_{CQDMN}	Serial EEPROM data transmitted to EEPROM invalid		0			ns
T_S	Setup time for data received from EEPROM		10			ns
T_H	Hold time for data received from EEPROM		10			ns

Figure 57: 4-Wire EEPROM Timing



4 Package Mechanical Dimensions

Figure 58: 88E6172/88E6176 128-pin TQFP EPAD Package Mechanical Drawings



NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Table 53: 88E6172/88E6176 128-pin TQFP EPAD Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	--	--	1.20
A_1	0.05	--	0.15
A_2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	--	0.20
c_1	0.09	--	0.16
D	16.00 BSC		
D_1	14.00 BSC		
E	16.00 BSC		
E_1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	0.20
S	0.20	--	--
D_2	5.89 mm BSC		
E_2	5.31 mm BSC		
θ	0°	3.5°	7°
θ_1	0°	--	--
θ_2	11°	12°	13°
θ_3	11°	12°	13°

5 Ordering Information

5.1 Ordering Part Numbers and Package Markings

Figure 59 shows the ordering part numbering scheme for the devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 59: Sample Part Number

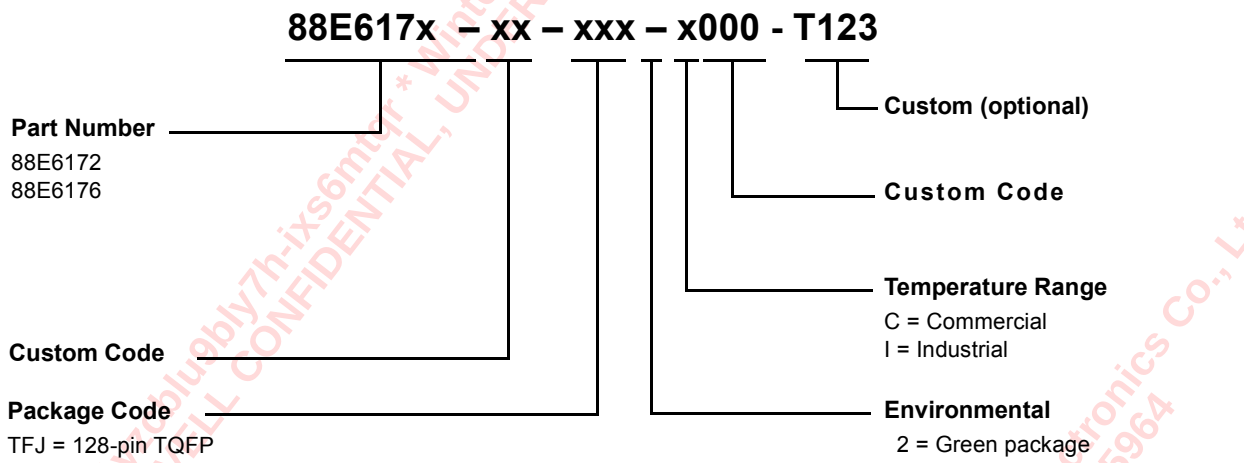


Table 54: Commercial Part Order Options

Package Type	Part Order Number
88E6172 128-pin TQFP	88E6172-xx-TFJ2C000
88E6176 128-pin TQFP	88E6176-xx-TFJ2C000

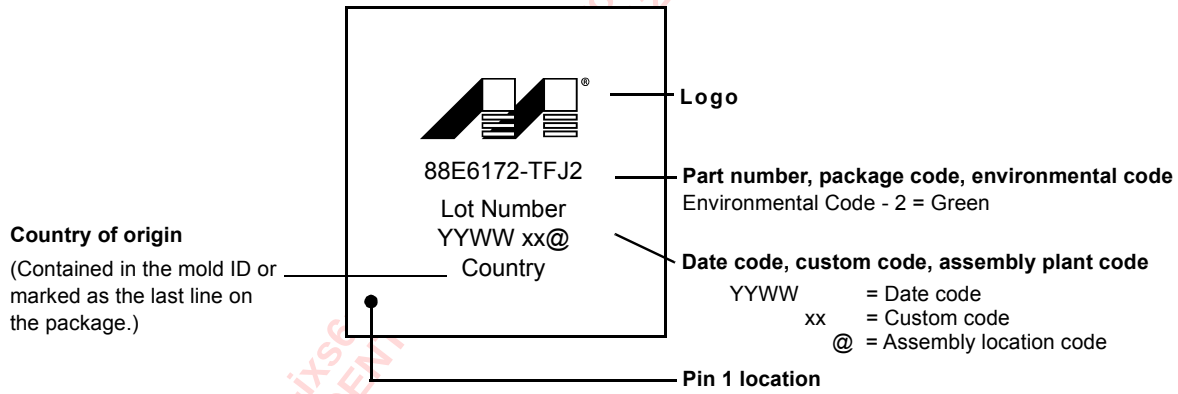
Table 55: Industrial Part Order Option

Package Type	Part Order Number
88E6176 128-pin TQFP	88E6176-xx-TFJ2I000

5.2 Commercial Marking Examples

Figure 60 is an example of the package marking and pin 1 location for the 88E6172 128-pin TQFP Commercial Green compliant package.

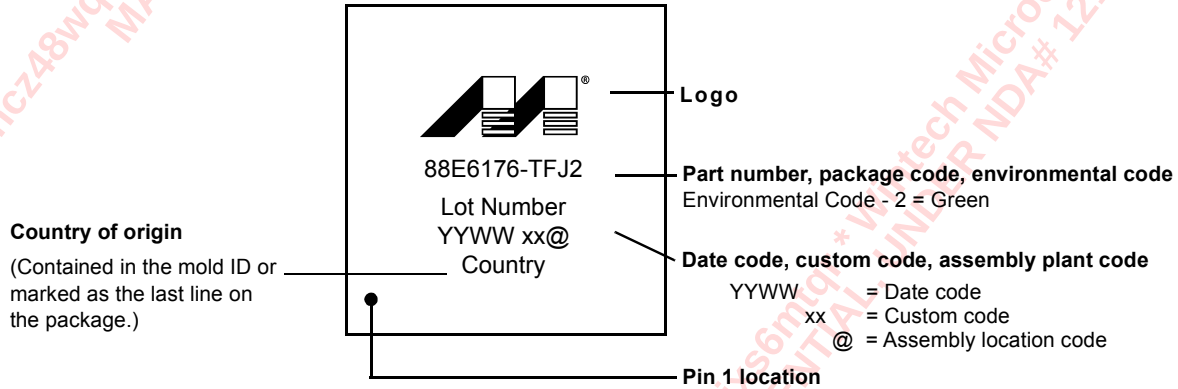
Figure 60: 88E6172 128-pin TQFP Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 61 is an example of the package marking and pin 1 location for the 88E6176 128-pin TQFP Commercial Green compliant package.

Figure 61: 88E6176 128-pin TQFP Commercial Green Compliant Package Marking and Pin 1 Location

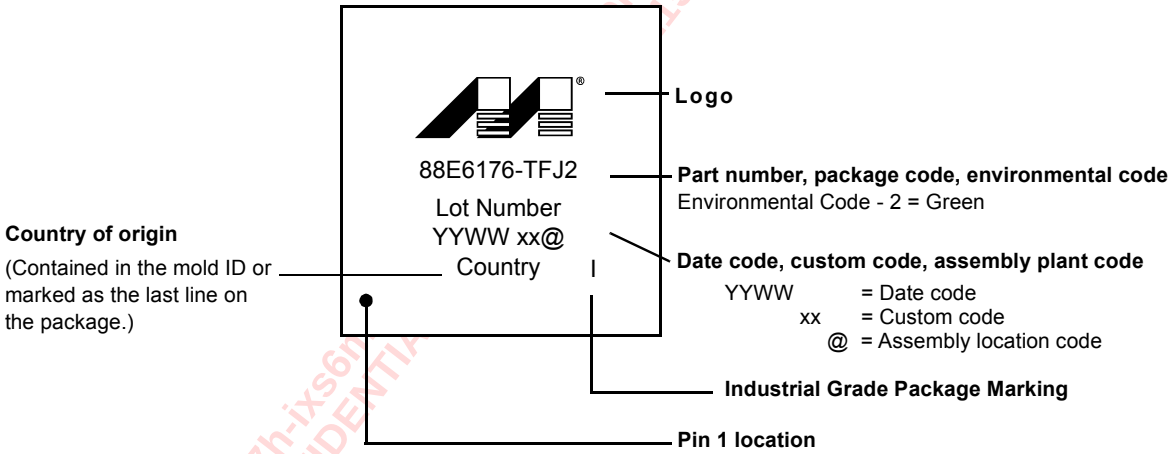


Note: The above example is not drawn to scale. Location of markings is approximate.

5.3 Industrial Marking Example

Figure 62 is an example of the package marking and pin 1 location for the 88E6176 128-pin TQFP Industrial Green compliant package.

Figure 62: 88E6176 128-pin TQFP Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.988.8279

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