Design Specification

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1. State diagram

There are 5 situation we may need to do the translation: fetch instruction, LDB, LDW, STB, STW.

When we are in supervisor mode, we don't need to do the translation, so I turn the translation off by checking PSR[15] in state 24.

And also, in order to allocate state number correctly, I made some changes of state number done before this lab. I have shown these changes in state diagram.

2. Datapath

I add 5 more register: VECTOR, X, Y, WRITE, EXCBR.

VECTOR is used to store the entry of interrupt/exception.

X is used to tell whether the translation is from fetch or LDB/LDW/STB/STW.

Y is used to determine unaligned access.

WRITE is used to tell if the instruction is STB/STW.

EXCBR is used to determine if there is an exception caused by protection or page fault.

3. Microsequencer

In order to return to correct state after translation, I use "IDR" and "MYIRD" to get the return state number in RETURN register. RETURN register is specified by signal X, which tells whether the translation is from fetch or LDB/LDW/STB/STW.

4. New control signal

VECTORMUX: select input of Vector

LD.VECTOR: load Vector signal

GateVECTOR: drive bus to give out the address of subroutine

LD.EXCBR: load EXCBR signal

LD.X: load X signal

LD.Y: load Y signal

LD.WRITE: load WRITE signal

XMUX: **select input of X**

YMUX: select input of Y

WRITEMUX: select input of WRITE

GATELOGIC1:   drive bus to give out the PTBR+2page_number

GATELOGIC2:   drive bus to give out the PFN' VA[8:0]

LD.VA: load VA signal

LD.RETURN: load RETURN signal

MODEMUX: in microsequencer, select IR[15] or PSR[15]

BEMUX: in microsequencer, select BEN or EXCBR

RYMUX: in microsequencer, select Ready or Y

SETMDR0:   load signal, used to set the reference bit. Also used to set modified bit if write.