Han Zheng

+1 7346619348 |hanhz@umich.edu |Ann Arbor, MI

EDUCATION

University of Michigan, Ann Arbor **Ann Arbor, MI**
MS Electrical and Computer Engineering (Intergrated Circuit and VLSI track) *September 2022-April 2024*

- **Courses:** VLSI Design I, Monolith Amplifier Circuits, Computer Architecture, Programming I, VLSI for ML and Wireless Comm

University of Liverpool **Liverpool, UK**
BEng (Hons) Telecommunications Engineering ***(First Class Honors)*** *September 2018-July 2022*

Xi'an Jiaotong-Liverpool University (XJTLU) **Suzhou, CHINA**
BEng Telecommunications Engineering ***(Rank: Top 10% / GPA: 3.86/4.00)*** *September 2018-July 2022*

- **Honors & Awards:** Outstanding Student (2020), University Academic Excellence Award (Top 5%, Year 2020/2021)

PROJECTS

A Two-staged 16-bit RISC Processor Integrated with a Fully Customized Near-Memory Computing SRAM, UMich **Ann Arbor, MI**
Course Project, EECS 427 VLSI Design I *January 2023-April 2023*

- Finished schematics, layout design and verification for a 16-bit 2-staged pipelined RISC processor including a Register file, a logarithmic shifter, and ALU with Carry-Select Adder
- Using Innovus for APR and physical design of the RISC Processor, complete chip-level integration of subblock and pad ring
- Designed an in/near-memory compute SRAM with Bit-Serial Logic/Arithmetic Operations for in/near-memory Computing

An R10K-style, Two-way superscalar, RISC-V Processor, UMich **Ann Arbor, MI**
Course Project, EECS 470 Computer Architecture *September 2022-December 2022*

- Designed and synthesized a MIPS R10K style renaming, Out-of-Order microprocessor supporting RISC-V ISA
- Implemented 2-way superscalar with branch prediction, Load and Store Queue and Victim Caches
- Validated and integrated components such as I-cache, D-cache, Reservation Station, Reorder Buffer, Physical Register File, Free List
- Completed the project with System Verilog, synthesized under 20ns clock period with average CPI=3.4

An Automatic Gain Control (AGC) Amplifier for Ultra Wideband Applications, UMich **Ann Arbor, MI**
Course Project, EECS 413 Monolith Amplifier Circuits *September 2022-December 2022*

- Designed an AGC system consisting of Variable Gain Amplifier (VGA), Peak Detector, Error Amplifier, Loop Filter and Bandgap Voltage Reference using Cadence Virtuoso in CMOS IBM 130nm process with 2.84mW power consumption
- Achieved the VGA performance with 26.5dB gain range and 460MHZ bandwidth, the 2-stage operational amplifier with 53dB gain, 102.52MHz GBW and 60.325° phase margin under miller compensation
- Analyzed and calculated transistor sizing by specification and opeartion mode, compressed the AGC system overall gain to be stable with the closed-loop feedback to the control voltage of VGA

PROFESSIONAL EXPERIENCE

Summer Undergraduate Research Fellowships, XJTLU **Suzhou, CHINA**
Research Assistant *May 2021-September 2021*

- Participated in a team of 5 on the investigation of GaN-based power IC (PMICs) from literature reviews, simulations, IC fabrication to characteristics analysis
- Reviewed, classified, and summarized publications on Gate Driver to evaluate and compare cutting-edge methodologies
- Designed and conducted simulation analysis on standard cell logic circuits in GaN process for control and drving circuit design such as NAND, NOR, DFF logic gate
- Validated the performance of IC chips in terms of rising time, falling time, dV/dt, di/dt and the voltage change using probe stations and semiconductor analyzer; enhanced performance by decreasing the logic low voltage from 3-4V to 1.4V
- Utilized instruments such as photolithography machine to fabricate the IC chip in cleanrooms

China United Network Communications Group Co. **Chengdu, CHINA**
Maintainance Engineer Intern, Department of Operation and Maintenance *July 2019-August 2019*

- Conducted regular monitoring and maintenance of mobile communication signals using professional tools and equipments
- Detected signal jammers in places such as underground parking lots and cooperated with the State Radio Regulatory Commission to remove illegal signal amplifiers
- Tested communication quality including WCDMA and LTE by using the Pioneer APP while cooperating with staff from Huawei and Ericsson in order to address a wide range of client concerns
- Measured the network quality in 3 new regions and authored reports recommending the construction department to build base stations

SKILLS

Technical: Python, Cadence Virtuoso, System Verilog, Verilog, C, MATLAB, LaTeX, ARM assembly language, Advanced Design System (ADS), Origin, LTspice, AHDL, Microsoft Office
Languages: Mandarin (Native), English (Advanced)