Ce(Derek) Kang

Looking for fulltime position in digital(VLSI) design or verification (Available Immediately)
1215E Vista del Cerro Dr, Tempe, AZ ◆ 480-696-9114 ◆ ckang12@asu.edu

EDUCATION

Arizona State University (August.2012-May.2014) Tempe AZ

MS in Electrical Engineering, IC design GPA:3.66/4.0

Relevant Coursework:

Advanced VLSI design, VLSI Design, Memory system, Computer Architecture, Semiconductor Device Theory, Advanced hardware design(verilog & system verilog), Digital Signal Processing, Advanced analog circuit design.

University of Electronic Science and Technology at Xi'an (August.2008-July.2012) Xi'an China

BS in Electronic Information Engineering GPA: 85/100

SKILL

Digital circuit design & verification (whole design flow: logic design, physical design, APR, VMM);

Software: Cadence 6 (hspice, virtuoso, 45nm, 32nm), RTL compiler, Encounter , ModelSim, Questa;

Languages: Verilog HDL, System Verilog, C language, Matlab, Perl(learning), Assembly Language, C++ (learning).

EXPERIENCE

Error detection and correction block design April 2013

- Designed an extensible hamming code error detection and correction module from logic design to physical design for the microprocessor. Did the **whole design flow** by myself.
- **Verilog coding** with ModelSim then synthesized the designed module with **RC Compiler** to meet a specific power and combinational delay requirement. Implemented **encounter** to design floor plan, power plan, well-tap addition, place & route, CTS, optimization .
- The error detection and correction block can detect and correct single bit error and detect double bit error in data.

Asynchronous FIFO design March 2014

- Implemented the asynchronous FIFO design with **verilog**. The sub level includes the memory, pointer, comparator, synchronizer and pointer conversion(gray code decoder).
- Utilized **system verilog** to test the FIFO function, built the DUT verification environment include packet class, interface, driver class, receiver class, scoreboard , environment class and top-level testbench.
- Covered all the corner cases and debugged the design problems like sequential timing analysis.

1GHz, 8kB, 32-bit, two way set associative, L1 cache design Dec 2013

- Designed the cache in 28nm technology node based on late way select architecture in a team of 3. Each 2KB Memory bank comprised of 6T based SRAM cells, row and column decoders, write drivers, and sense amplifier.
- Worked on SRAM cell, decoder and hit/miss detection architecture along with tag arrays using dynamic NOR comparators and Multiplexers.
- Tested the logic of the whole design with 4 corner process simulations. Used Nanotime to verify timing of my design.

Single Cycle MIPS Processor design (RTL) Jan 2014

- Designed a 32-bit MIPS CPU with **verilog** include ALU, decoder, PC selector and top-level control logic, memories in a team of 4.
- Worked on PC selector and memory coding, also worked on the top-level connectivity.
- Developed testbenches and debugged the timing problems through ModelSim simulation to make the whole design work.

A 32 word x 64-bit register file with 3 write and 4 read ports memory design Sep 2013

- Designed register file cell, decoder and set dominant latches in 28nm technology.
- Completed the static timing analysis, dynamic circuit analysis, corner simulations and power considerations for a reliable read and write operation over all the process corners
- Analyzed the design for race through, setup and hold violations, minimum supply voltage and fixed them.

Graduate Design: RFID Reader Antenna March 2012

- Used HFSS to design excellent performance antennas which are small size, low cost, used in RFID reader.
- Read many essays, reached and designed broadband planar dipole antenna whose size is 90*90mm2, frequency is 915MHz, gain is 5.15dB.
- Taped out the antenna and used the vector network analyzer to measure the performance.

SUMMER INTERN

FPGA design, SPI protocol implementation in Dalian Victor R&D Center Ltd(China) Summer 2013

- Verilog HDL based SPI transceiver module design.
- Simulated the design through ISE design suite. Then hardware verification in a Spartan 6 device.