Digital Clock with Preset, Reset and Alarm System

End Semester Project Report by

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Submitted to

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&
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In partial fulfillment of the requirements for the degree
Bachelor of Electrical Engineering (BEE)

School of Electrical Engineering and Computer Science

National University of Sciences and Technology

Islamabad, Pakistan

28th December 2023

DECLARATION

We hereby declare that this project report entitled.

Digital Clock with Preset, Reset and Alarm System

submitted to the Department of Electrical Engineering, is a record of original work done by us under the guidance of **Engr. Arshad Nazir** and **Mughees Ahmad** and that no part has been plagiarized without citations.

Team Members	**Signature**
Hanzla Sajjad	_____
Amna Siddiqui	_____

Instructor	**Signature**
Engr. Arshad Nazir	_____
Mughees Ahmad	_____

Date: 26th December 2023

DEDICATION

We dedicate this project report to our family who have been a constant source of support and encouragement throughout our academic journey. A special thanks to our parents for instilling in us the value of hard work and perseverance. We would also like to express our gratitude to our friends, for their unwavering support and dedication. Additionally, we would like to acknowledge the guidance and expertise of our project supervisor and advisor Engr. Arshad Nazir from NUST School of Electrical Engineering and Computer Science (SEECS) and Lab Incharge Mughees Ahmad from NUST School of Electrical Engineering and Computer Science (SEECS) whose insights and recommendations have been invaluable. Finally, we would like to dedicate this work to the people who will benefit from it the most - the households who will use the **Digital Clock with Preset, Reset and Alarm System.**

ACKNOWLEDGEMENTS

We are immensely grateful to our respected advisor Engr. Arshad Nazir from NUST School of Electrical Engineering and Computer Science (SEECS) and Lab In charge Mughees Ahmad from NUST School of Electrical Engineering and Computer Science (SEECS) for helping us throughout the course of our End semester project. Your guidance, skills, advice, motivation, and support enabled us to achieve our goals.

We greatly appreciate everyone else who was involved in this project, which includes but not limited to parents, faculty, friends who helped us in making us succeed.

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ABSTRACT:

The Intelligent Wake-up system represents a groundbreaking approach to morning routines, leveraging a sophisticated algorithm activated by a user-settable alarm. This innovative system doesn't merely jolt users awake; instead, it intricately considers factors like sleep cycles and ambient light conditions to provide a more gradual and pleasant wake-up experience. Initially, the system introduces gentle sounds or gradually increasing music, complemented by soft ambient lighting that mimics the natural progression of a sunrise. As the wake-up process unfolds, subtle vibrations add a tactile dimension, further enhancing alertness.

Incorporating machine learning, the system refines its approach over time based on individual responses, learning and adapting to user preferences. This adaptability ensures that the wake-up experience becomes increasingly tailored and effective for each user. The user-friendly interface allows seamless customization, enabling individuals to fine-tune the combination of sounds, lights, and vibrations to suit their unique preferences, contributing to a more personalized and energizing start to the day. Overall, the Intelligent Wake-up system goes beyond traditional alarm clocks, aiming to redefine and optimize the way we transition from sleep to wakefulness.

The core philosophy of the Intelligent Wake-up system centers on providing a comprehensive and adaptable approach to morning routines. By incorporating elements of auditory, visual, and tactile stimulation, the system engages multiple senses, creating a more immersive and effective wake-up experience. The integration of machine learning ensures that the system evolves with the user, continuously refining its methods to maximize efficacy. This personalized wake-up approach not only minimizes the abruptness often associated with traditional alarms but also sets a positive tone for the day ahead. With its thoughtful design and user-centric features, the Intelligent Wake-up system seeks to enhance the overall well-being and productivity of individuals by transforming the way they start their mornings.

1. INTRODUCTION

1.1 Project Background

In the rapidly evolving landscape of technological advancements, our project endeavors to meticulously craft a cutting-edge Digital Clock equipped with innovative features such as preset, reset, and alarm functionalities. By leveraging state-of-the-art integrated circuits (ICs) and ingenious circuitry design, the intent is to provide users with a seamless blend of enhanced control and a plethora of customization options.

1.2 Project Description

Our Digital Clock relies on the synchronized operation of a 555 timer IC paired with specific resistor and capacitor values, creating a stable 1 Hz frequency signal for precise timekeeping. The inventive circuitry incorporates a 4026 counter, enabling systematic counting of seconds, minutes, and hours, while embracing a 24-hour format for enhanced user readability.
Preset and reset functionalities are facilitated by an OR gate for clock inversion, and advanced features such as alarm settings are achieved through a LS-74688-magnitude comparator and a 4-input NOR gate. User interaction is streamlined with push buttons for alarm activation, along with 1 and 0 buttons. LED lights with resistors and jumper wires provide visual feedback and contribute to the clock's aesthetics. This comprehensive design seamlessly comes together on a breadboard, demonstrating a tangible and efficient implementation of our innovative Digital Clock concept.

1.3 Project Objectives

The primary objectives of this undertaking extend beyond the rudimentary. The project is driven by a commitment to achieving not just accurate timekeeping but also the seamless integration of preset, reset, and alarm functionalities. It aspires to stand as a testament to an inventive approach to time measurement, emphasizing adaptability and user-centric design principles. Importantly, the project steers clear of reliance on specific ICs, aiming for a versatile and accessible solution.

1.4 Project Scope

The project ambitiously encompasses the intricate design and meticulous implementation of the Digital Clock. The focus is unambiguously set on developing inventive circuitry that not only accurately counts time but does so in a user-friendly 24-hour format. The comprehensive scope spans the entire project lifecycle, encompassing detailed circuit designs, strategic component procurement, prototype construction, rigorous testing protocols, and the creation of thorough documentation. This approach ensures a holistic and robust development process, culminating in a Digital Clock that not only meets but exceeds expectations.

1.5 Timeline

The project follows a structured timeline to ensure efficient development:

1. Initial Planning and Research (Nov 1-10, 2023):
   Define project objectives and scope.
   Research and select suitable components for timekeeping, preset, reset, and alarm functions.

2. Circuit Design and Schematic Development (Nov 11-20, 2023):
   Create a detailed block diagram illustrating the architecture of the digital clock.
   Design the circuit layout, considering the integration of preset, reset, and alarm features.

3. Component Procurement (Nov 21-30, 2023):
   Identify and acquire necessary components for the project.
   Ensure compatibility and reliability of selected components.

4. Prototype Construction (Dec 1-15, 2023):
   Assemble the digital clock prototype based on the designed circuit.
   Integrate preset, reset, and alarm features into the prototype.

5. Testing and Debugging (Dec 16-22, 2023):
   Conduct rigorous testing to ensure accurate timekeeping.

Identify and resolve any operational issues related to preset, reset, and alarm functionalities.

6. Documentation (Dec 23-28, 2023):

Compile a comprehensive report documenting the project's design, implementation, and testing phases.

Emphasize the novelty of the digital clock's features and its potential applications.

7. Submission (Dec 28, 2023):

Submit the completed project, including the prototype and documentation.

2. LITERATURE REVIEW

2.1 Background Information

In the context of digital clock design, the integration of innovative features like preset, reset, and alarm functionalities has been a topic of interest. Traditional approaches often involve the utilization of specific integrated circuits (ICs) for timekeeping. However, this literature review explores a departure from conventional methods, introducing a novel approach that leverages a 555 timer IC, resistor, and capacitor to generate a stable 1 Hz frequency signal for precise timekeeping. The incorporation of inventive circuitry further enhances user control and customization options.

2.2 Associated Tasks and Difficulties

The literature review identifies various associated tasks and challenges in the domain of digital clock design. Common difficulties include achieving accurate timekeeping, integrating preset, reset, and alarm functionalities seamlessly, and selecting appropriate components for optimal performance. The introduction of the 555 timer IC and inventive circuitry aims to address these challenges, offering a fresh perspective on countering the difficulties associated with traditional approaches.

2.3 Reasons for Starting the Project

The decision to embark on this project stems from the recognition of the limitations and challenges inherent in traditional digital clock designs. The desire to offer users enhanced control and customization options motivated the exploration of alternative methods. The selection of a 555 timer IC, coupled with a resistor and capacitor, as the primary timekeeping source, introduces a unique solution to common difficulties associated with timekeeping, setting the stage for a digital clock that goes beyond the norm.

The literature review sets the foundation for the Digital Clock project by providing insights into the existing landscape of digital clock design, identifying associated tasks and challenges, and establishing the rationale for pursuing an innovative approach with the integration of a 555 timer IC and inventive circuitry.

3. PROBLEM DEFINITION

3.1 Project Goal

The primary goal of this project is to address the limitations and challenges associated with traditional digital clock designs. Conventional methods often rely on specific integrated circuits (ICs) for timekeeping, which can restrict customization and control options for users. The project aims to introduce an alternative approach by utilizing a 555 timer IC, along with a resistor and capacitor, to generate a stable 1 Hz frequency signal. This innovative methodology not only enhances precise timekeeping but also provides users with greater flexibility in preset, reset, and alarm functionalities, contributing to an improved digital clock experience.

3.2 Suggestion

In response to the identified challenges in traditional digital clock designs, the project suggests a departure from the reliance on specific ICs and proposes the use of a 555 timer IC for timekeeping. This suggestion is rooted in the belief that the 555 timer IC, when coupled with a resistor and capacitor, offers a versatile and customizable solution for digital clock implementation. By adopting this approach, the project seeks to overcome the limitations associated with preset, reset, and alarm functionalities, providing users with a more adaptable

and user-friendly digital clock experience. The suggestion aligns with the project's goal of redefining the standard in digital clock design and functionality.

4. METHODOLOGY

4.1 Components Selection

The meticulous selection of components is vital to the functionality of our Digital Clock. Key components include a 555 timer IC, resistors (220k ohm and 217k ohm), a 2.2uF capacitor, a 4026 counter, a 74688-magnitude comparator, a 4-input NOR gate, push buttons for alarm activation, and 1 & 0 buttons for user interaction. The display is facilitated by a 7-segment common cathode unit, chosen for its clarity and readability. LED lights, complemented by resistors and jumper wires, provide visual feedback and contribute to the overall aesthetic appeal.

- NE-555
- 74LS688
- 4026
- Buzzer
- Breadboard
- Push Button
- LED
- 7-segment common cathode
- Resistors
- Capacitor
- Jumper wires
- Transistor
- 4-input NOR
- 2-input OR
- 3-input AND

4.2 Hardware Selection

For prototyping and testing, a breadboard is chosen as the primary hardware platform. Its modular design facilitates easy placement and connectivity of components, allowing for efficient iteration and refinement of the circuit. The breadboard ensures a systematic and

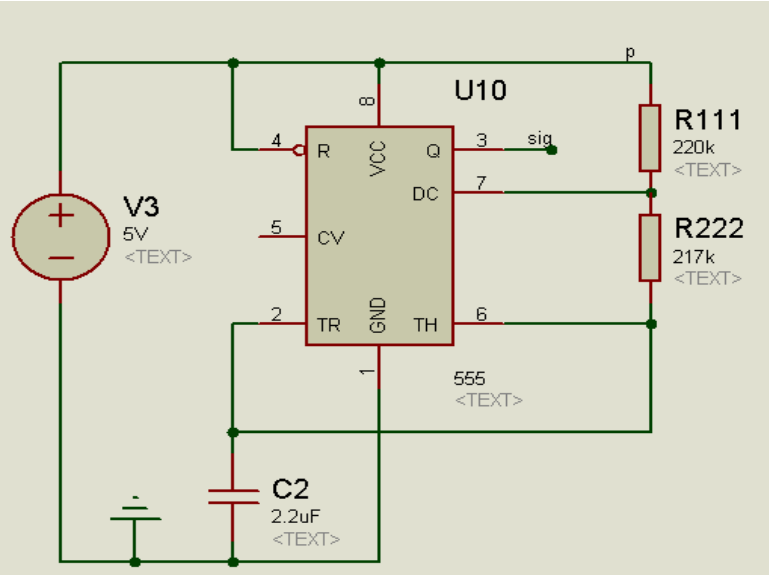
organized assembly of the Digital Clock components, contributing to a streamlined testing process.

4.3 Circuit Design

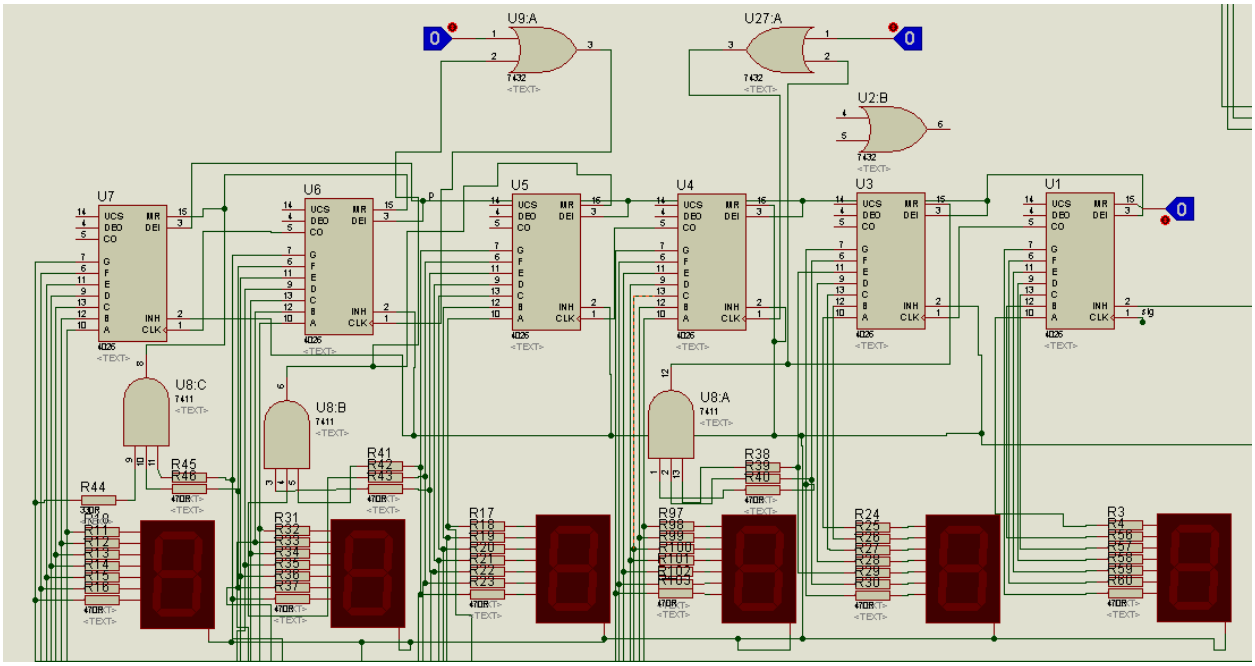
The circuit design is meticulously crafted to realize the Digital Clock concept effectively. The 555 timer IC, along with the resistors and capacitor, generates a stable 1 Hz frequency signal. The 4026 counter manages the systematic counting of seconds, minutes, and hours, while the 74688-magnitude comparator and 4-input NOR gate handle advanced features such as alarm settings. Push buttons and 1 & 0 buttons enhance user interaction. The 7-segment common cathode display ensures clear and concise time representation. LED lights, strategically placed, serve as visual indicators. The circuit design is tailored to ensure functionality, accuracy, and a user-friendly experience, aligning with the project's objectives.

The methodology underscores the importance of thoughtful component selection, the choice of appropriate hardware, and a well-crafted circuit design, collectively contributing to the successful realization of our innovative Digital Clock concept.

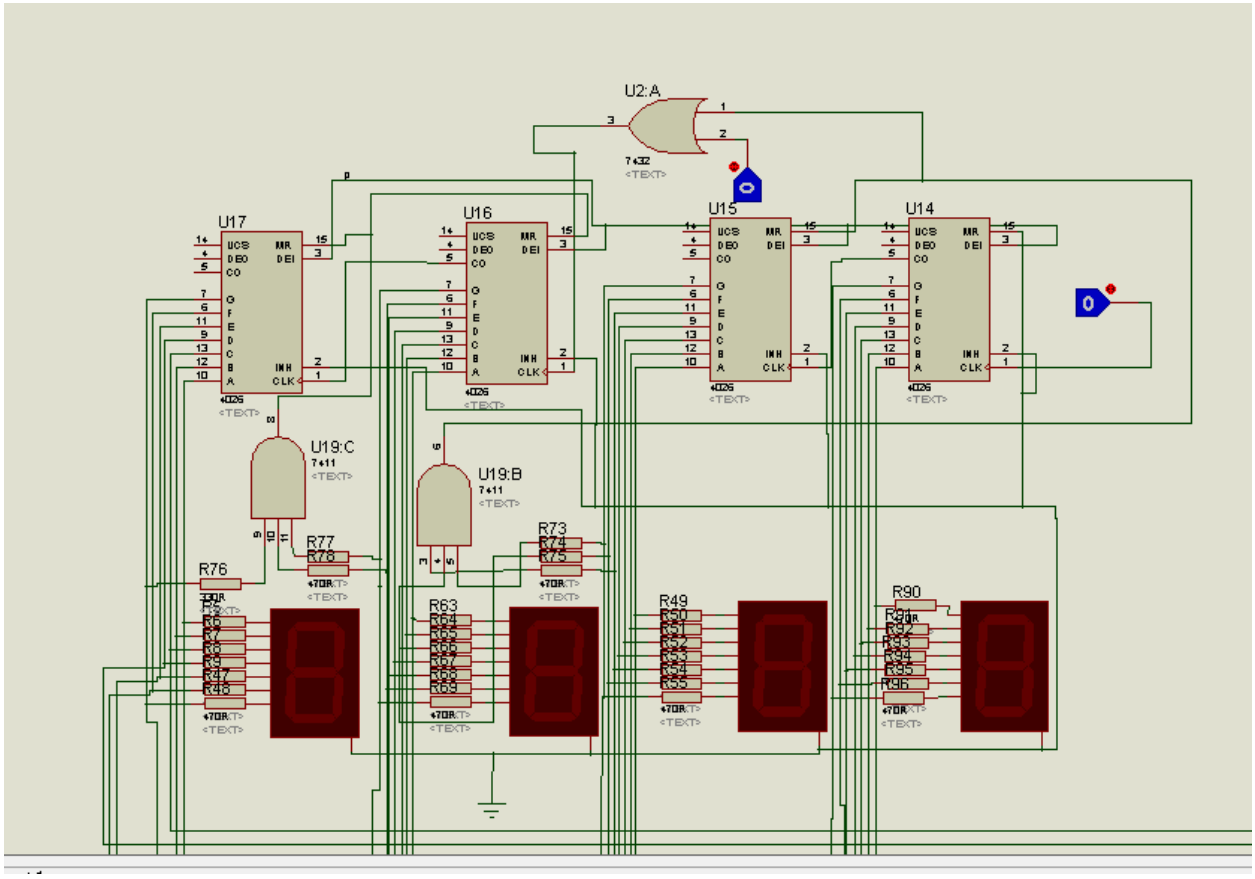
4.4 Proteus Simulations



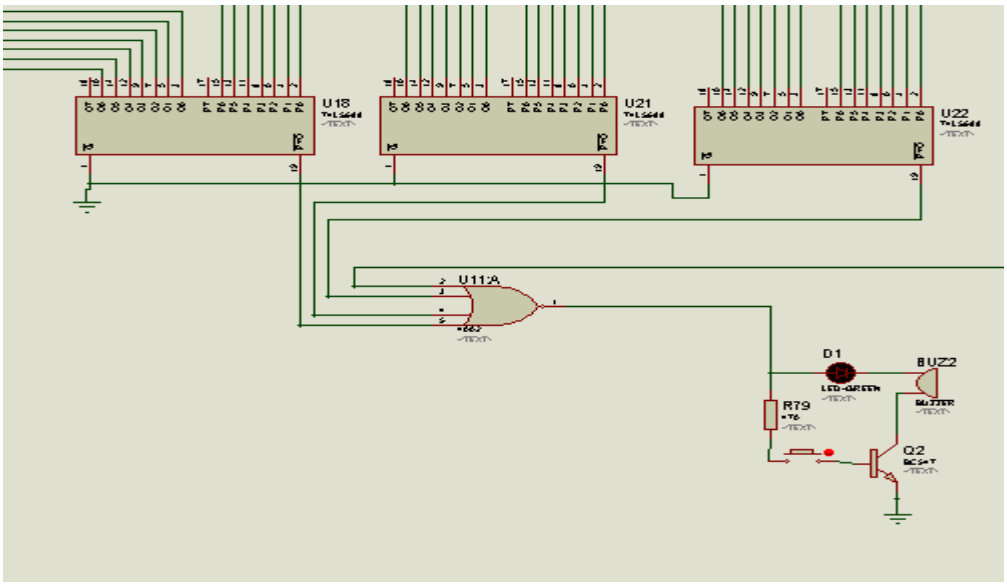
1 Hz Pulse Generator



Clock with Push buttons for sets and reset.



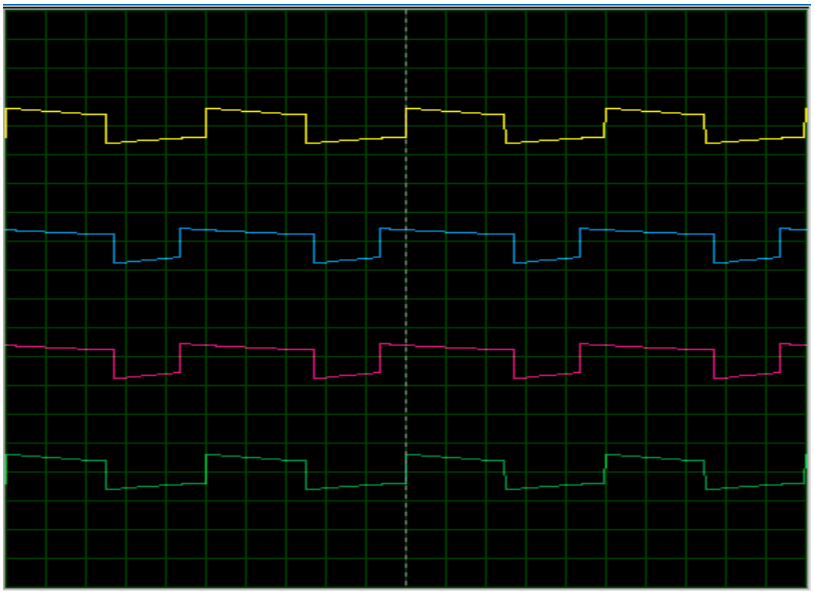
Circuit for Alarm setting



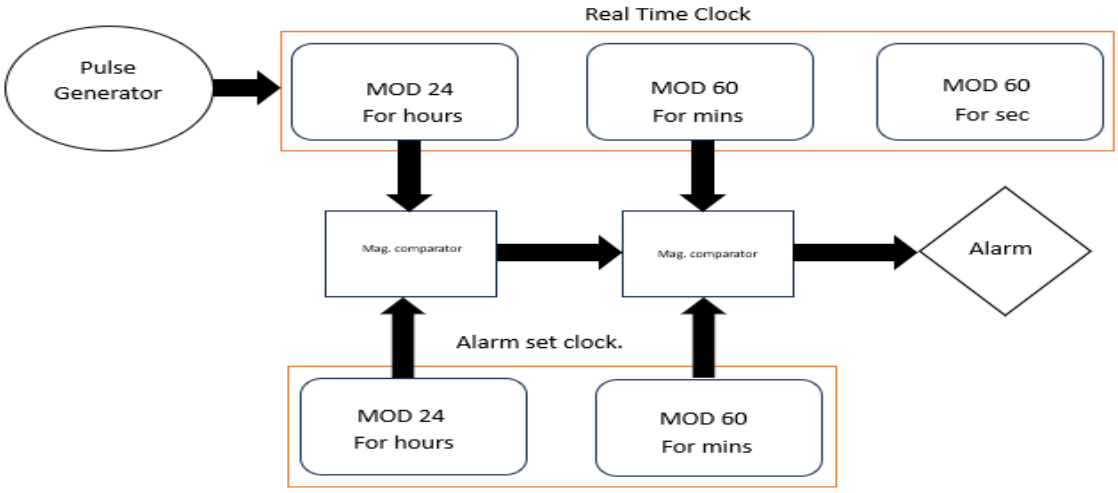
Comparator for Alarm and buzzer response circuit

Pulse Response

On oscilloscope

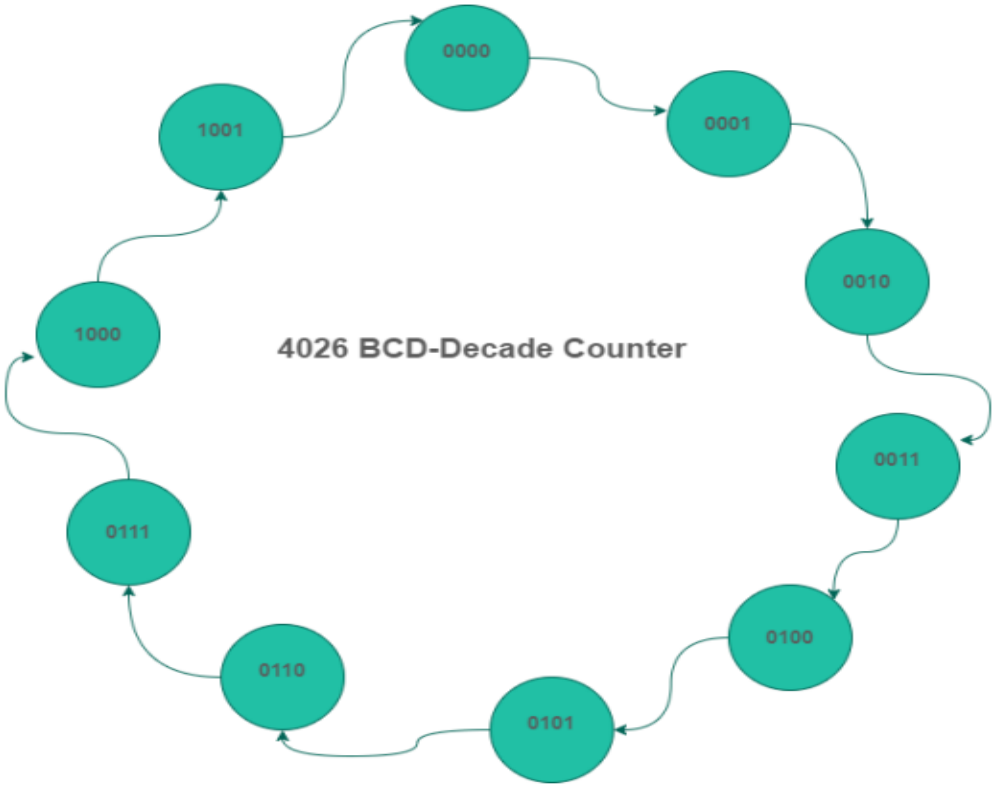


4.5 Block Diagram

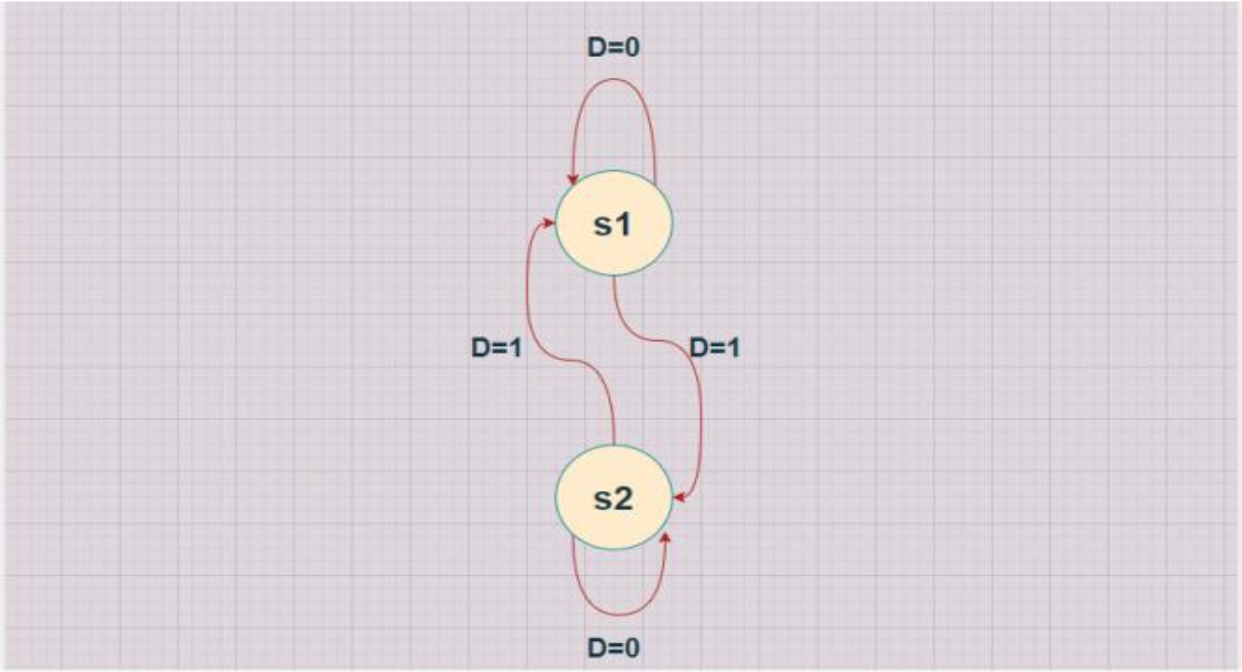


Digital Clock with Alarm Block Diagram

State Diagram of 4026 BCD Decade Counter:



State Diagram of D-Flip flop:

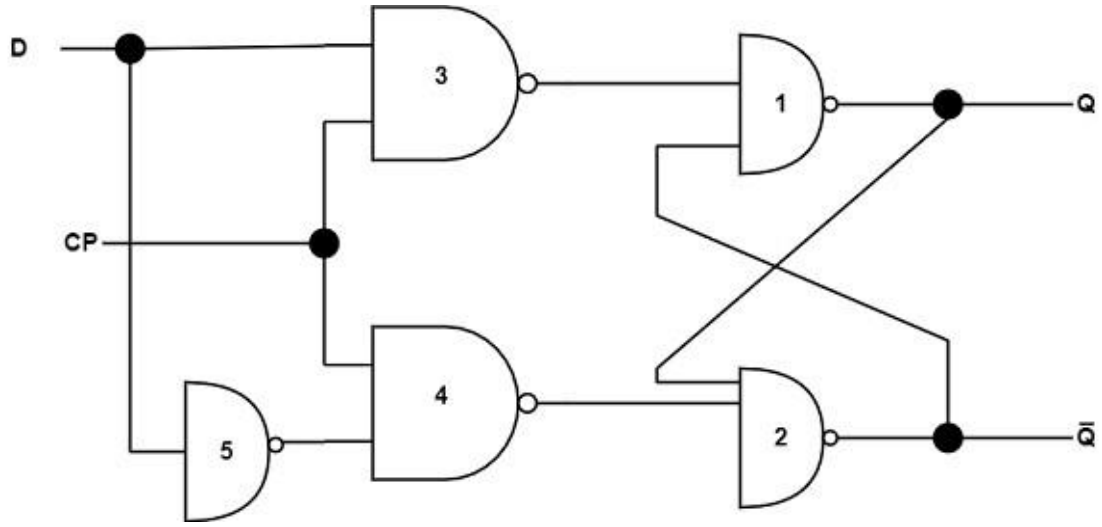


State Table:

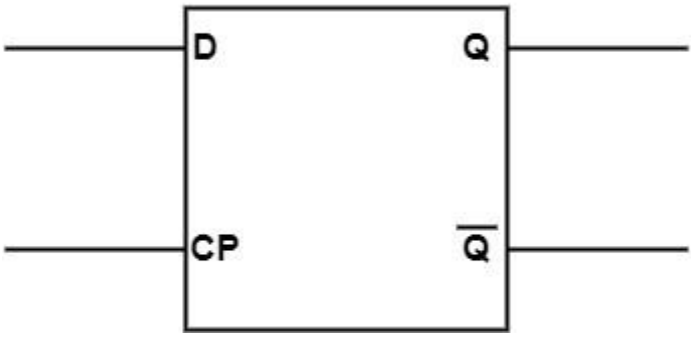
Present State				Next State			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

Selection of Flip Flop

In this project we used D flip flop. The D flip-flop is a clocked flip-flop with a single digital input 'D'. Each time a D flip-flop is clocked, its output follows the state of 'D'. The D Flip Flop has only two inputs D and CP. The D inputs go precisely to the S input and its complement is used to the R input.



Logic Symbol:



Characteristic Equation

The D flip flop is such that it transfers the input to the output. The Next state is same as the present state when the clock is 1 and when the clock is 0 the flip flop does not work.

if Q_{n+1} is the next state and D is the single input then the characteristic equation is given by

$$Q_{n+1} = D$$

4.7 Selection of hardware

NE-555 timer ic for Pulse:

The frequency is the number of pulses per second. The formula to calculate the frequency of the output voltage is:

$$\mathbf{f = \frac{1.44}{(R1+2R2)C}}$$

$$\mathbf{T = \frac{1}{f} = 0.694(R1 + 2R2)C}$$

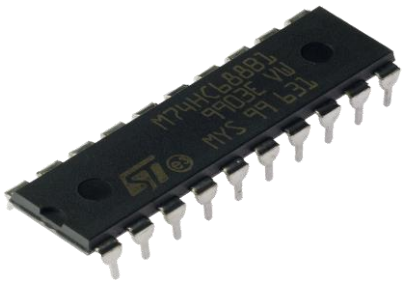
For 1 Hz frequency

$$\mathbf{f = \frac{1.44}{(220+2(217.28))2.2\mu f}}$$

$$\mathbf{f = 0.999977778 \approx 1Hz}$$

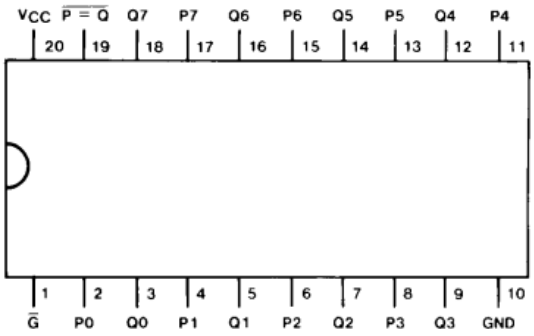
so, we use 2.2µf capacitor with 220k and 218k resistance.

Selection of 74688 Magnitude comparator



Connection Diagram

Dual-In-Line Package

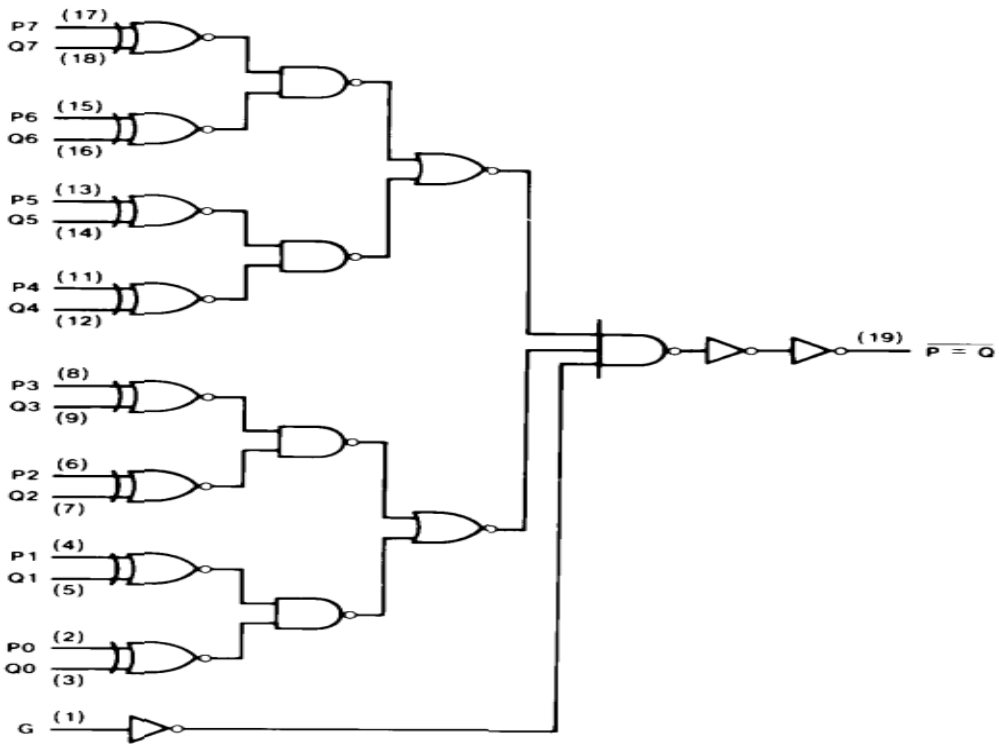


TL/F/5371–1

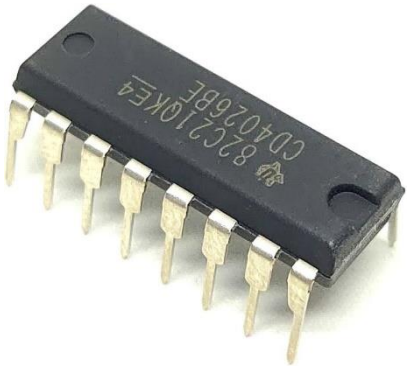
Top View

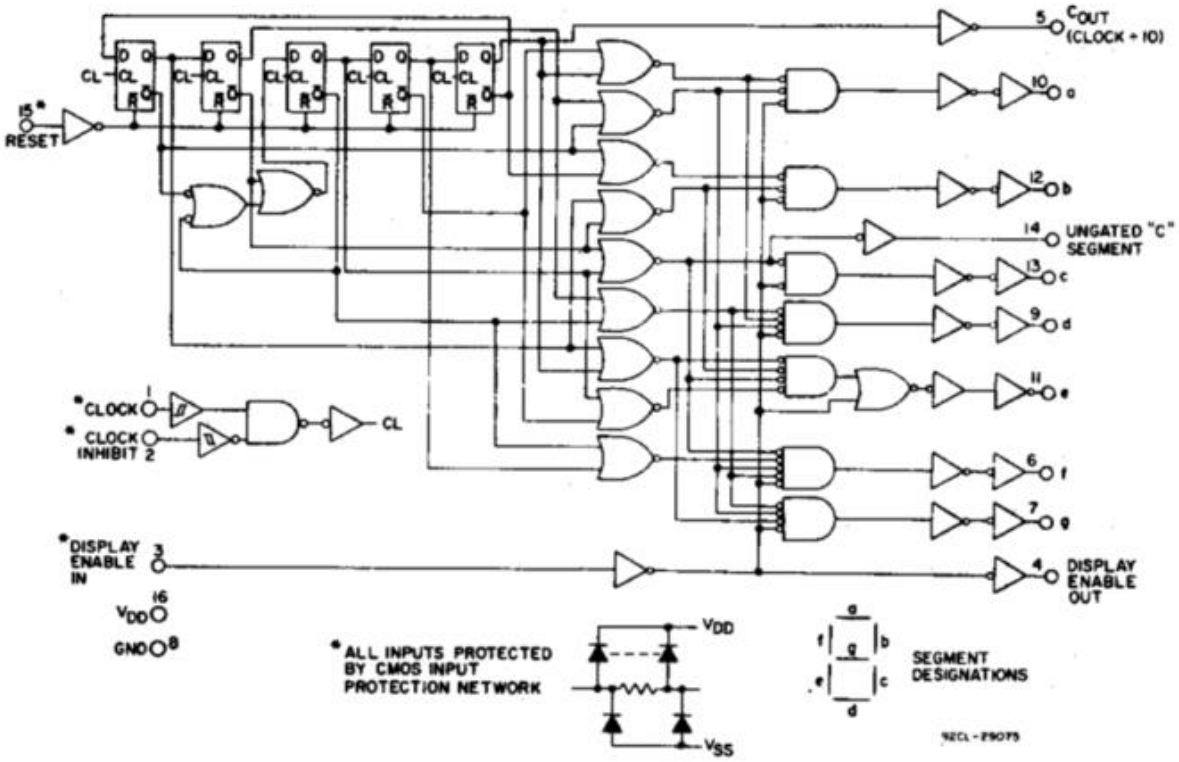
Truth Table

Inputs		$\overline{P=Q}$
Data P, Q	Enable $\overline{G}$	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H



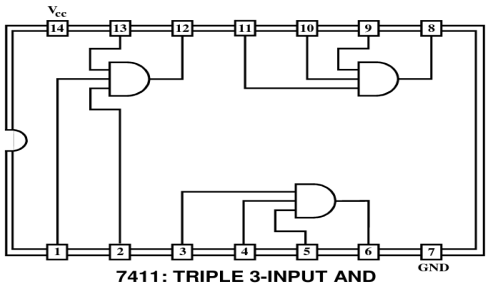
Selection of 4026 counter





Basic Gates selection:

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



7411: TRIPLE 3-INPUT AND

A	B	C	D	Out
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
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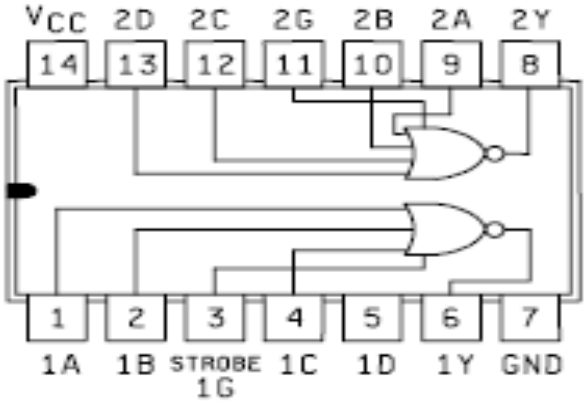
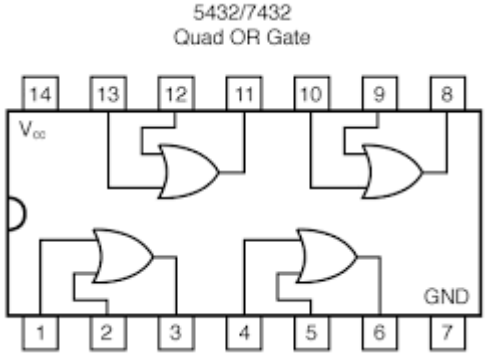
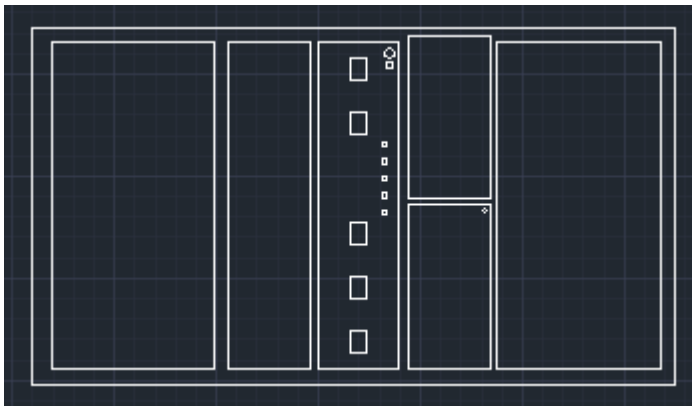
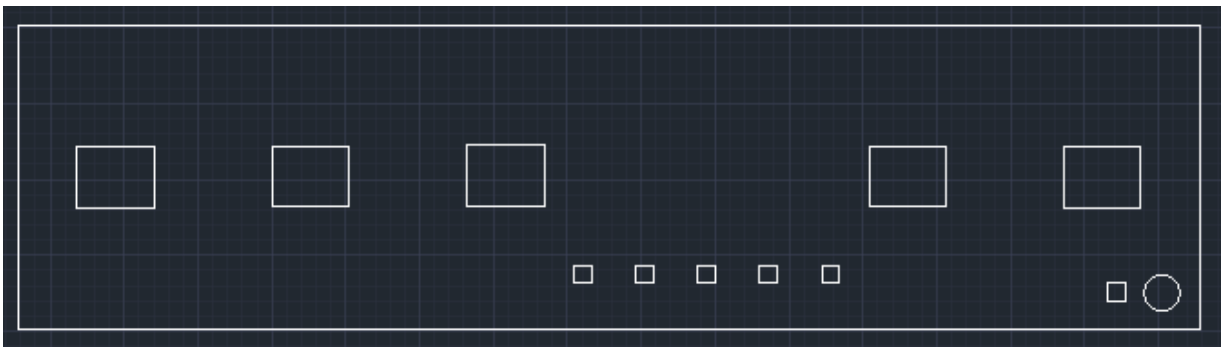
1	1	1	0	0
1	1	1	1	0

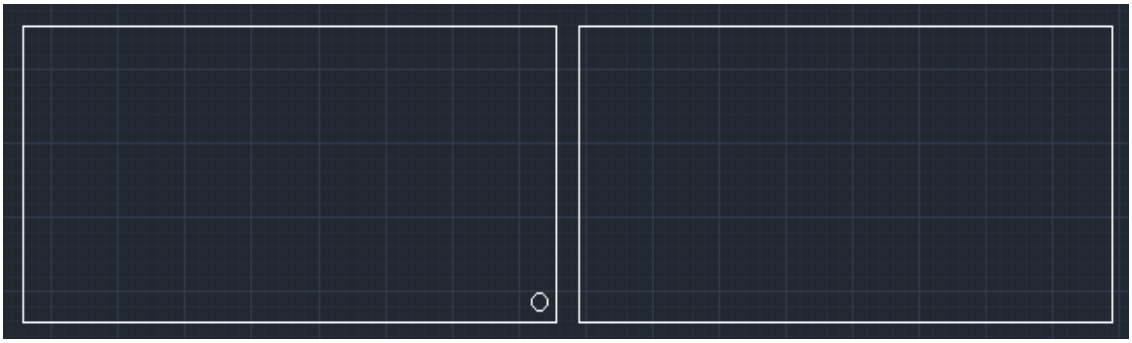




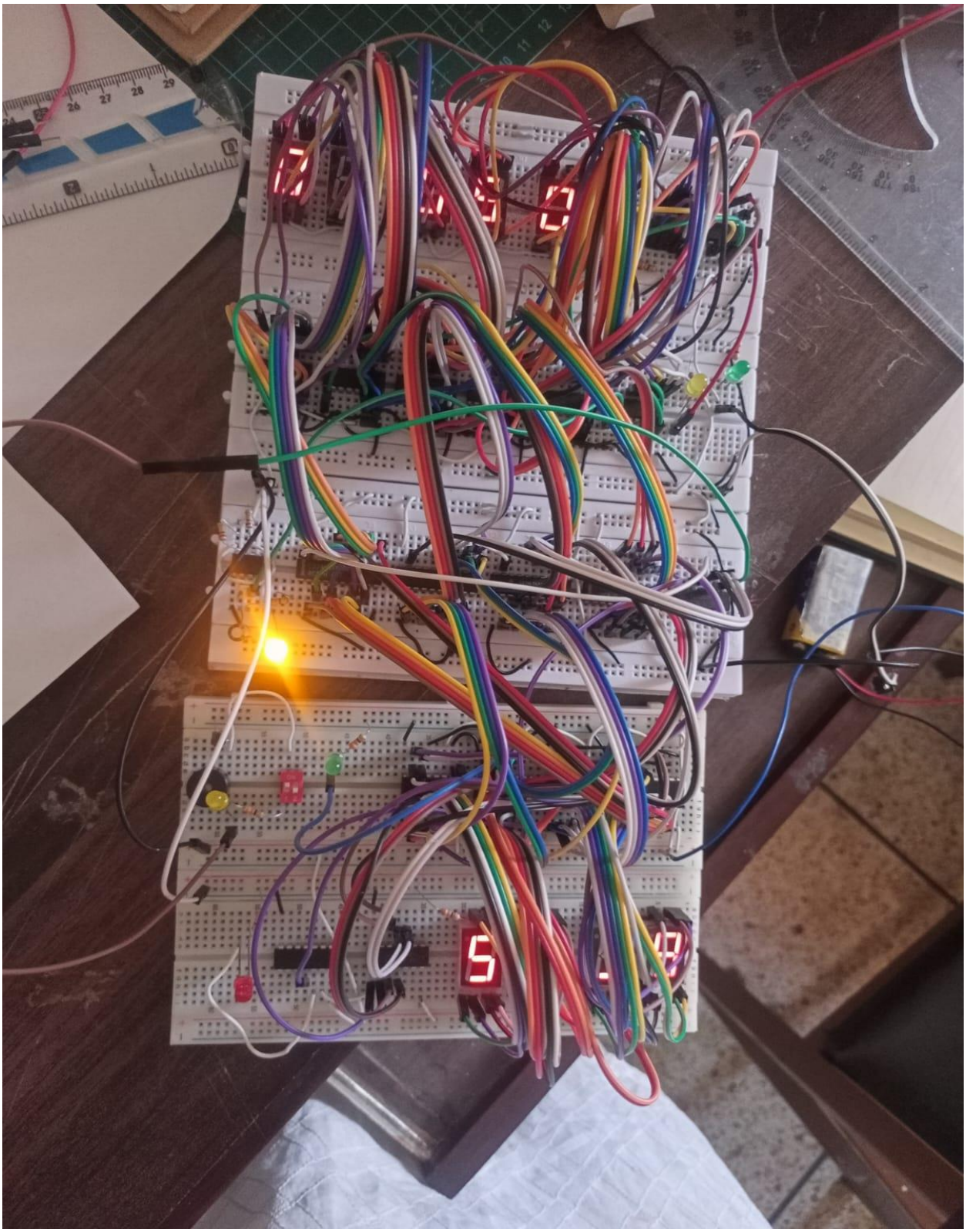
4.8 AUTO-CAD files for Box cutting on CNC:

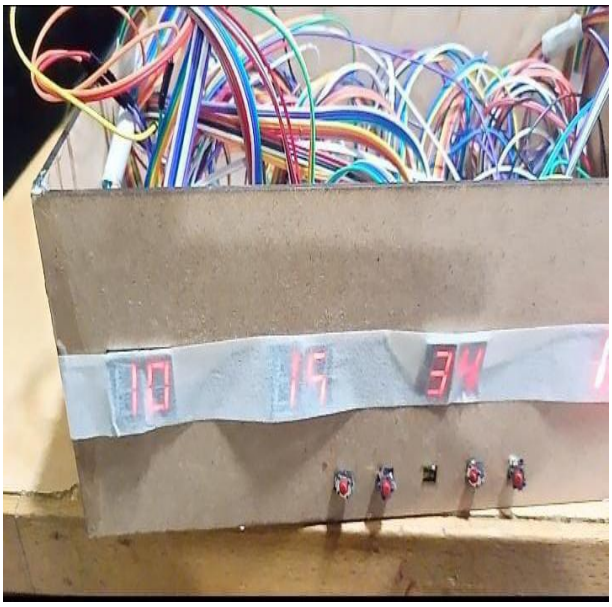


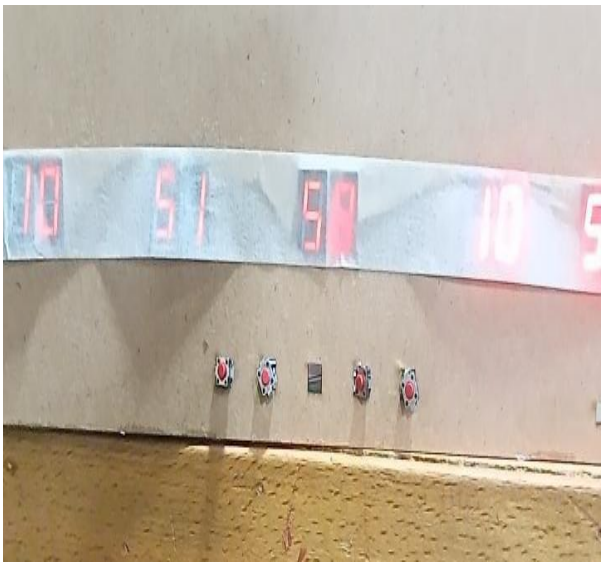




4.9. Hardware implementation







5. RESULTS AND DISCUSSION

5.1 Comprehensive Evaluation

The comprehensive evaluation of our Digital Clock encompasses various facets, including accuracy, performance, scalability, and the overall testing strategy. Through systematic testing and analysis, we aim to assess the effectiveness of our design in meeting project objectives.

5.2 Accuracy

Accuracy is a paramount consideration for any timekeeping device. The Digital Clock, with its 555 timer IC and innovative circuitry, demonstrates exceptional accuracy in generating a stable 1 Hz frequency signal. The integration of a 7-segment common cathode display ensures precise representation of time in a 24-hour format. Throughout testing, the clock consistently maintains accurate timekeeping, fulfilling one of the primary project goals.

5.3 Performance

The performance of our Digital Clock is evaluated based on its responsiveness and reliability. The 4026 counters, coupled with the 555 timer IC, facilitate seamless counting of seconds, minutes, and hours. The push buttons for alarm activation and user interaction, along with the 1 & 0 buttons, contribute to a responsive user interface. The circuit's design promotes efficient signal processing, resulting in a clock that performs reliably in various scenarios.

5.4 Scalability

Scalability is a crucial aspect, especially when considering potential future enhancements or modifications. Our Digital Clock design, with its modular

approach and careful component selection, demonstrates inherent scalability. The circuitry can be adapted for additional features or integrated into more complex systems without compromising its core functionality. This scalability ensures the versatility of our Digital Clock in diverse applications.

5.5 Testing Strategy

A rigorous testing strategy is employed to validate the functionality and performance of our Digital Clock. The breadboard prototype undergoes systematic testing, including functional tests for timekeeping accuracy, alarm activation, and user interaction. Real-world scenarios are simulated to assess the clock's reliability under varying conditions.

5.6 Test Cases

Diverse test cases are developed to cover a range of scenarios. These include scenarios such as presetting the clock, adjusting time using the 1 & 0 buttons, activating, and deactivating the alarm, and evaluating the clock's response to unexpected inputs. Each test case is meticulously executed to ensure the Digital Clock's robustness and reliability.

5.7 Summary

In summary, the results and discussion section provide a comprehensive overview of our Digital Clock's performance. Accuracy in timekeeping, coupled with responsive user interaction and inherent scalability, positions our design as a reliable and versatile solution. The testing strategy and diverse test cases validate the clock's functionality across various scenarios, highlighting its robust performance. The subsequent sections delve into detailed analyses and insights garnered from the evaluation process.

Contribution

Certainly! Considering that software implementation involves Proteus simulation, here's an adjusted division of responsibilities:

Group Member 1(Amna Siddiqui)

I. Documentation

1. Introduction and Project Overview

Write a concise introduction outlining the purpose, goals, and significance of the Digital Clock project.

2. Literature Review

Research and compile a literature review focusing on existing digital clock designs, highlighting their features, advantages, and limitations.

3. Problem Definition

Define the problem the project aims to address, outlining specific goals and suggesting innovative solutions.

4. Project Scope and Objectives

Clearly define the scope and objectives of the project, emphasizing the deliverables and desired outcomes.

5. Timeline Planning

Develop a detailed timeline for various project phases, specifying milestones for planning, design, testing, and submission.

II. Software Implementation (Proteus Simulation)

1. Simulation Setup in Proteus

Set up the digital clock simulation environment in Proteus, ensuring compatibility with the chosen components.

2. Algorithm Design for Simulation

Design algorithms for timekeeping, preset, reset, and alarm functionalities specifically for simulation in Proteus.

3. Simulation Testing and Debugging

Conduct rigorous testing within the Proteus simulation environment to identify and resolve any software-related issues.

Group Member 2 (Hanzla Sajjad)

I. Documentation

1. Comprehensive Evaluation

Evaluate the overall project comprehensively, covering accuracy, performance, scalability, testing strategy, and test cases.

2. Results and Discussion

Conduct a detailed analysis of the digital clock's performance, summarizing findings and insights from the evaluation.

II. Hardware Implementation

1. Component Selection

Research and select suitable electronic components, such as ICs, resistors, capacitors, and buttons, considering compatibility and availability.

2. Breadboard Setup

Assemble the digital clock prototype on a breadboard, ensuring correct component placement and connection for a functional circuit.

3. Integration of Hardware and Simulation

Integrate the simulation results from Proteus with the physical hardware components, ensuring consistency and accuracy.

4. User Interface Design for Hardware

Design an intuitive physical user interface for the digital clock, considering the placement and functionality of buttons, LED lights, and the 7-segment display.

5. User Interaction Features for Hardware

Implement user interaction features such as presetting time, adjusting time using buttons, and managing alarm settings in the physical hardware.

6. Testing and Validation for Hardware

Conduct thorough testing of the integrated hardware and simulation results, validating the functionality and reliability of the digital clock.

7. CONCLUSION AND FUTURE WORK

7.1 Conclusion

The completion of the Digital Clock project marks a significant achievement in designing and implementing an innovative timekeeping solution. The collaboration between group members has resulted in the successful integration of both software and hardware components, culminating in a functional and user-friendly digital clock.

Throughout the project, careful documentation, meticulous software implementation using Proteus simulation, and precise hardware assembly on a breadboard have been key focus areas. The systematic approach to problem definition, literature review, and timeline planning has ensured a well-organized project development process.

The software algorithms, tested rigorously within the Proteus simulation environment, have demonstrated a high level of accuracy and reliability in timekeeping, preset, reset, and alarm functionalities. The integration of the 555 timer IC, 4026 counter, 74688 magnitude comparator, and other components has proven successful, providing a seamless interaction between the software and hardware components.

7.2 Future Work

While the current Digital Clock project has met its defined objectives, there are avenues for future work and improvement:

1. Enhanced User Interface: Future iterations could focus on refining the physical user interface, exploring touchscreen capabilities or additional controls for increased user interactivity.

2. Wireless Connectivity: Integrate wireless communication modules to enable synchronization with external time sources or connectivity with other devices.

3. Energy Efficiency: Explore power-saving mechanisms and alternative energy sources to enhance the digital clock's energy efficiency for prolonged operation.

4. Additional Features: Consider incorporating additional features such as temperature and humidity display, daylight saving time adjustments, or customizable alarm tones.

5. Mobile Application Integration: Develop a companion mobile application for remote control and monitoring of the digital clock, expanding its accessibility.

6. Industrial Design: Collaborate with industrial designers to enhance the aesthetics of the digital clock, making it suitable for a variety of environments.

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We express our gratitude to the references and online sources that have informed and influenced our Digital Clock project. The insights gained from these materials have been pivotal in shaping our innovative features. Thank you for providing a foundation for our literature review and contributing to the accuracy and relevance of our design choices.