1	/12
2	/10
3	/8

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.004 Computation Structures
Spring 2015

Quiz #3: April 17, 2015

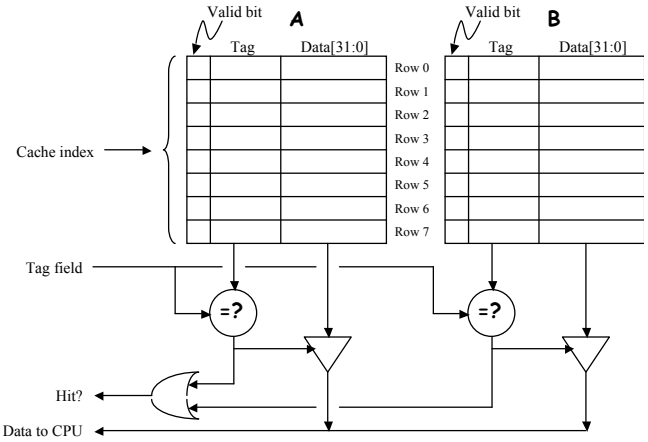
Name	*Athena login name*	*Score*

Michael	*Philippe*	*Miriam*	*Ciara*	*Louis*
☐ WF 10, 34-302	☐ WF 12, 34-301	☐ WF 2, 34-301	☐ WF 12, 34-302	☐ WF 2, 34-302
☐ WF 11, 34-302	☐ WF 1, 34-301	☐ WF 3, 34-301	☐ WF 1, 34-302	☐ WF 3, 34-302

Please enter your name and Athena login name in the spaces above. Enter your answers in the spaces provided after each question. You can use the extra white space and the backs of the pages for scratch work.

Problem 1. Caches (12 Points)

Consider the diagram to the right for a 2-way set associative cache to be used with our Beta design. Each cache line holds a single 32-bit word of data along with its associated tag and valid bit (0 when the cache line is invalid, 1 when the cache line is valid).



(A) (2 points) The Beta produces 32-bit byte addresses, A[31:0]. To ensure the best cache performance, which address bits should be used for the cache index? For the tag field?

address bits used for cache index: A[4 : 2]

address bits used for tag field: A[31 : 5]

(B) (2 points) Suppose the Beta does a read of location 0x5678. Identify which cache location(s) would be checked to see if that location is in the cache. For each location specify the cache section (A or B) and row number (0 through 7). E.g., **3A** for row 3, section A. If there is a cache hit on this access what would be the contents of the tag data for the cache line that holds the data for this location?

cache location(s) checked on access to 0x5678: 6A, 6B

cache tag data on hit for location 0x5678 (hex): 0x 2B3

(C) (2 points) Assume that checking the cache on each read takes 1 cycle and that refilling the cache on a miss takes an *additional* 8 cycles. If we wanted the *average* access time over many reads to be 1.1 cycles, what is the minimum hit ratio the cache must achieve during that period of time? You needn't simplify your answer.

minimum hit ratio for 1.1 cycle average access time: H+(1-H)*9 = 1.1
H = 7.9/8

(D) (2 points) Estimate the approximate cache hit ratio for the following program. Assume the cache is empty before execution begins (all the valid bits are 0) and that an LRU replacement strategy is used. Remember the cache is used for both instruction and data (LD) accesses.

```
      . = 0
      CMOVE(source,R0)
      CMOVE(0,R1)
      CMOVE(0x1000,R2)
loop: LD(R0,0,R3)
      ADDC(R0,4,R0)
      ADD(R3,R1,R1)
      SUBC(R2,1,R2)
      BNE(R2,loop)
      ST(R1,source)
      HALT()

      . = 0x100
source:
      . = . + 0x4000 // Set source to 0x100, reserve 1000 words
```

approximate hit ratio: 5/6

(E) (4 points) After the program of part (D) has finished execution what information is stored in row 4 of the cache? Give the addresses for the two locations that are cached (one in each of the sections) or briefly explain why that information can't be determined.

Addresses whose data is cached in "Row 4": 0x10 **and** 0x40F0

Problem 2. New Beta Instructions (10 Points)

Consider adding the following instructions to the Beta instruction set, for implementation on the Beta hardware shown in lecture (see diagram included in the reference material at the end of this quiz). You're allowed to change how the control signals are generated but no modifications to the datapath are permitted.

For each instruction either fill in the appropriate values for the control signals in the table below or **put a line through the whole row if the instruction cannot be implemented** using the existing Beta datapath. Use "—" to indicate a "don't care" value for a control signal. The values can be a function of Z (which is 1 when Reg[Ra] is zero).

LDX(Ra, Rb, Rc) // Load indexed
EA ← Reg[Ra] + Reg[Rb]
Reg[Rc] ← Mem[EA]
PC ← PC + 4

STX(Ra, Rb, Rc) // Store indexed
EA ← Reg[Ra] + Reg[Rb]
Mem[EA] ← Reg[Rc]
PC ← PC + 4

MVZC(Ra, literal, Rc) // Move constant if zero
If Reg[Ra] == 0 then Reg[Rc] ← SXT(literal)
PC ← PC + 4

SOB(Ra, literal, Rc) // Subtract one and branch
PC ← PC + 4
EA ← PC + 4*SEXT(literal)
tmp ← Reg[Ra]
Reg[Rc] ← Reg[Ra] – 1
if tmp != 0 then PC ← EA

ARA(Ra, literal, Rc) // Add Relative Address
Reg[Rc] ← Reg[Rc] + PC + 4 + 4*SEXT(literal)
PC ← PC + 4

(FILL IN TABLE BELOW)

Instr	ALUFN	WERF	BSEL	WDSEL	MOE	MWR	RA2SEL	PCSEL	ASEL	WASEL
LDX	+	1	0	2	1	0	0	0	0	0
STX										
MVZC	B	Z	1	1	-	0	-	0	-	0
SOB										
ARA	+	1	0	1	-	0	1	0	1	0

Problem 3 (8 Points): Pipelined Beta

A 5-stage pipelined Beta with full bypassing and annulment of instructions following taken branches has been running the program below for a while (it's code from Problem 1D). A snapshot of the execution starting at cycle 1001 is shown in the pipeline diagram to the right.

```
…
loop: LD(R0,0,R3)
      ADDC(R0,4,R0)
      ADD(R3,R1,R1)
      SUBC(R2,1,R2)
      BNE(R2,loop)
      ST(R1,sum)
…
```

Cycle #	1001	1002	1003	1004	1005	1006	1007	1008
IF	LD	ADDC	ADD	SUBC	SUBC	BNE	ST	LD
RF	NOP	LD	ADDC	ADD	ADD	SUBC	BNE	NOP
ALU	BNE	NOP	LD	ADDC	NOP	ADD	SUBC	BNE
MEM	SUBC	BNE	NOP	LD	ADDC	NOP	ADD	SUBC
WB	ADD	SUBC	BNE	NOP	LD	ADDC	NOP	ADD

(A) (1 Point) The program reads from registers R0, R1, R2, and R3. In a pipelined processor, sometimes the register contents come from the register file and sometimes from a bypass path. Circle the register number below if its contents came from the register file at least once during cycles 1001 through 1008.

Register contents read from register file at least once: …(R0)…(R1)…(R2)… R3

(B) (1 Point each) Referring to the cycle numbers at the top of the pipeline diagram, please indicate the cycle numbers for which the specified signal had the specified value. Write NONE if the signal did not have that value during any of cycles 1001 through 1008.

Cycle(s) when STALL was 1: 1004

Cycle(s) when $IRSrc^{IF}$ was not 0: 1007

Cycle(s) when $IRSrc^{RF}$ was not 0: 1004

Cycle(s) when $IRSrc^{ALU}$ was not 0: NONE

Cycle(s) when either bypass was from ALU stage: 1007

Cycle(s) when either bypass was from MEM stage: NON

Cycle(s) when either bypass was from WB stage: 1005

END OF QUIZ 3!