1	/5
2	/6
3	/6
4	/8
5	/5

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.004 Computation Structures
Spring 2015

Quiz #1: February 27, 2015

Name			*Athena login name*	*Score*
Michael	*Philippe*	*Miriam*	*Ciara*	*Louis*
☐ WF 10, 34-302	☐ WF 12, 34-301	☐ WF 2, 34-301	☐ WF 12, 34-302	☐ WF 2, 34-302
☐ WF 11, 34-302	☐ WF 1, 34-301	☐ WF 3, 34-301	☐ WF 1, 34-302	☐ WF 3, 34-302

Please enter your name and Athena login name in the spaces above. Enter your answers in the spaces provided after each question. You can use the extra white space and the backs of the pages for scratch work.

Problem 1. Potpourri (5 Points)

(A) I've randomly selected a letter from the alphabet and tell you that my selection is neither "X", "Y", nor "Z". How much information have I given you about my letter?

Bits of info (number or formula): log_2 26/23

(B) What is the smallest (most negative) integer that can be represented as an 8-bit two's-complement integer? Give your answer as a decimal integer.

Smallest 8-bit two's-complement integer: -128

(C) Ternary logic functions use 3-valued logic. How many ternary functions of two (ternary) inputs are there? Hint: How many rows are in a ternary truth table? How many different ways can we fill in the output column?

Number of 2-input ternary functions (number or formula): 3^9

(D) A single CMOS gate, consisting of an output node connected to a single pullup circuit containing one or more PFETs and a single pulldown circuit containing one or more NFETs (as described in lecture), computes $F(A,B)$. F has the property that for all A, $F(A,0) = \overline{F(A,1)}$. What can you say about the value of $F(1,0)$?

(circle one): F(1,0) = (1) **.. 0 … can't tell**

(E) A 2-input OR gate is made by combining a lenient NOR gate with an inverter. The resulting OR gate is lenient …

Circle one: **NEVER** **SOMETIMES** (**ALWAYS**)

Problem 2. Variable-length Codes (6 points)

NerdLink is a new web-based startup that aims to keep MIT EECS students in touch with their parents. NerdLink streamlines parental communication by providing each student with an online choice of one of the five messages, then automatically fills in boilerplate and emails the parent a long and charming version of the message. The five messages, and their relative probabilities, are listed below:

Message #	*Message to parents*	*p(Message)*
M1	Send money!	60%
M2	I love this course called 6.004	8%
M3	I'm changing my major to Poetry	2%
M4	I'm getting a 5.0 this term!	1%
M5	Nothing much is new… (none of the above)	29%

NerdLink's initial implementation conveyed each message using a fixed-length code.

(A) (1 point) What is the average number of bits needed to convey a message, using a fixed-length code?

Average bits/message, using fixed-length code: 3

(B) (1 point) Given the probability distribution of the messages, what is the *actual* amount of information conveyed by message M5? Your answer may be a formula.

Actual information content of M5: log_2 1/29%

(C) (1 point) To enable error correction, the fixed-length code for a given message is sent *five* times. Using the five copies of the received message, in the worst case how many bit errors can be corrected at the receiver?

Worst-case number of bit errors that can be corrected: 2

NerdLink, wanting to economize on communication costs, has hired you as a consultant to design a Huffman code for sending the messages.

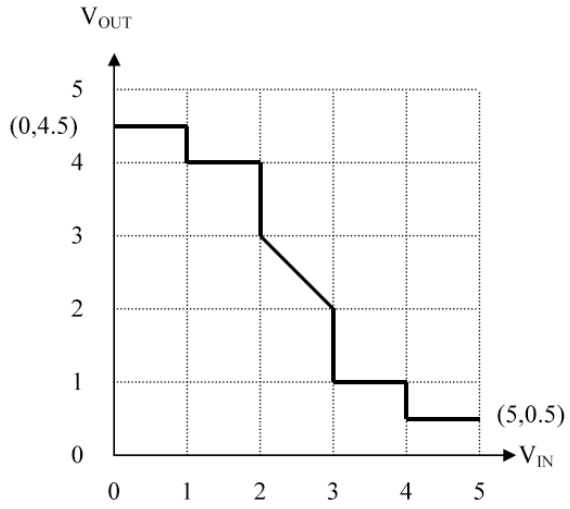
(D) (3 points) Give the **number of bits** sent by your Huffman code for each message, and the average number of bits transmitted per message using your code (a formula will be fine).

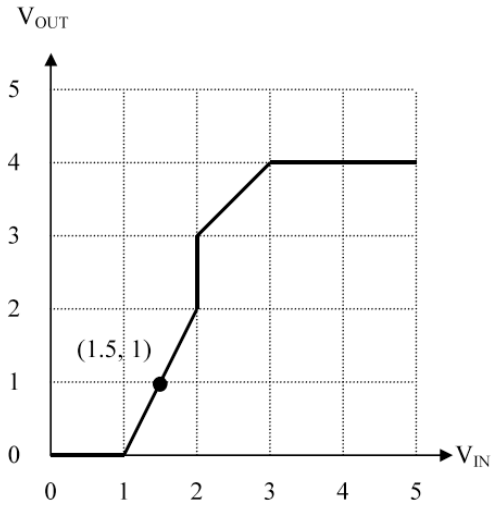
Number of bits for M1: 0 **M2:** 110 **M3:** 1110 **M4:** 1111 **M5:** 10

Average bits/message, using your code: 1.54

Problem 3. Static Discipline (6 points)

Following are voltage transfer characteristics of devices to be used in a new logic family as an inverter and buffer, respectively:



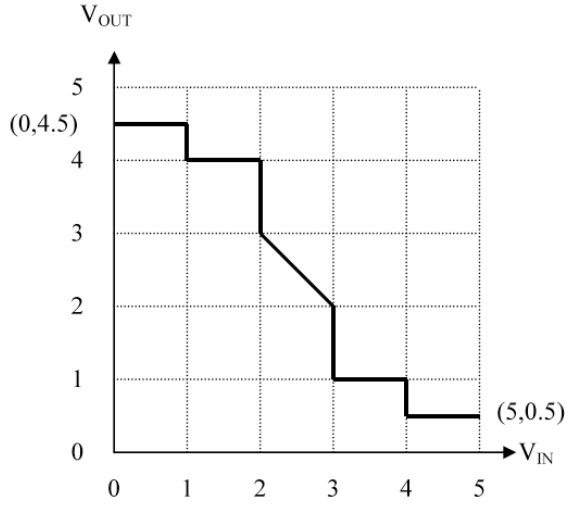


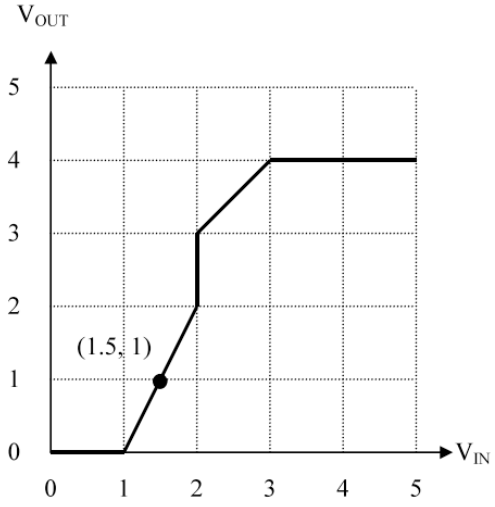
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize each of the noise margins.

V_{OL} = 1.0 **V_{IL} =** 1.5 **V_{IH} =** 3.0 **V_{OH} =** 4.0

Low Noise Margin = 0.5 **High Noise Margin =** 1.0

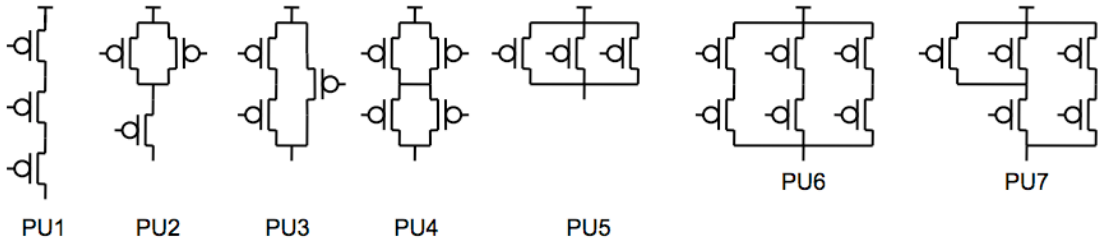
Scratch copy of the VTC diagrams:





Problem 4. CMOS Logic (8 points)

You are trying to select pullups for several 3-input CMOS gate designs. The Pullups Galore web site offers seven different pullups, given names PU1 through PU7, diagrammed below:



The web site explains that the customer can choose which inputs are connected to each PFET, allowing their pullups to be used in various ways to build gates with various numbers of inputs. Since Pullups Galore charges by transistor, you are interested in selecting pullups using the minimum number of transistors for each of the 3-input gates you are designing.

For each of the following 3-input Boolean functions, choose the appropriate pullup design, i.e., the one which, properly connected, implements that gate's pullup using the *minimum number* of transistors. This may require minimizing the logic equation first. If none of the above pullups meets this goal, write "NONE".

(A) $F(A,B,C) = \overline{A} + \overline{B} + \overline{C}$ **Choice or NONE:** PU5

(B) $F(A,B,C) = \overline{A} + \overline{B \cdot C}$ **Choice or NONE:** PU5

(C) $F(A,B,C) = \overline{A + B \cdot C}$ **Choice or NONE:** PU2

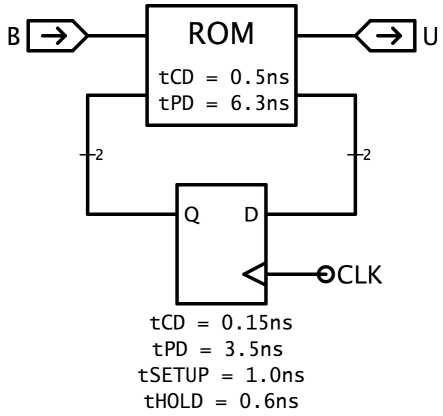
(D) $F(A,B,C) = A + \overline{B \cdot C}$ **Choice or NONE:** NONE

(E) $F(A,B,C) = \overline{(A+B)} + \overline{(B+C)} + \overline{(A+C)}$ **Choice or NONE:** PU7

(F) $F(A,B,C) = \overline{(A+C) \cdot B}$ **Choice or NONE:** PU3

Problem 5. Sequential Logic (5 points)

The diagram for a particular sequential circuit is shown below. You may assume that the B input has been appropriately synchronized with CLK.



(A) (1 Point) How many bits are stored in the ROM?

***Total* size of ROM, in bits:** 24

(B) (1 Point) What is the smallest value for the period of CLK which will guarantee the dynamic discipline is obeyed?

smallest value for t_{CLK} (ns): 10.8

(D) (2 Points) What are the smallest setup and hold times for the B input with respect to the active edge of CLK that ensures the necessary timing specifications are met?

smallest setup time for B input (ns): 7.3

smallest hold time for B input (ns): 0.1

(E) (1 point) A summer intern has proposed using a new version of the ROM with timing specifications that are twice as fast (t_{CD} = 0.25ns, t_{PD} = 3.15ns). Help her out by computing the revised minimum for t_{CLK} that guarantees the dynamic discipline is obeyed, or write NONE and provide a one-sentence explanation as to why the ROM can't be used

revised smallest value for t_{CLK} (ns) or NONE: NONE

t_CD, Reg + t_CD, ROM < t_HOLD, Reg

END OF QUIZ 1!