Analog IC Design (ENE521000) Hsin Chen

Homework #1

Due date : Mar. 20th, 2025

Please submit your report (*.pdf) and netlist file (*.sp) to the EECLASS system.
Please name your file as *hw1_student number.pdf, hw1_student number_x.sp*
e.g. hw1_100061501_1c.sp represents .sp file for question 1(c).
Note:
Don't use black color in background for your screen capture figures.
List calculation/design process clearly and mark proper information of all plots/figures required.

(1) Above-threshold Device parameters and Amplifier Design

Consider the amplifier in Fig.1 with **C_L=1pF and V_{DD}=1.8V**. Please design the transistor sizes, $(W/L)_i$, to achieve a small-signal gain of $A_V \equiv v_o/v_i > 60(V/V), f_{3dB} > 650kHz,\ Power \leq 250\mu W$

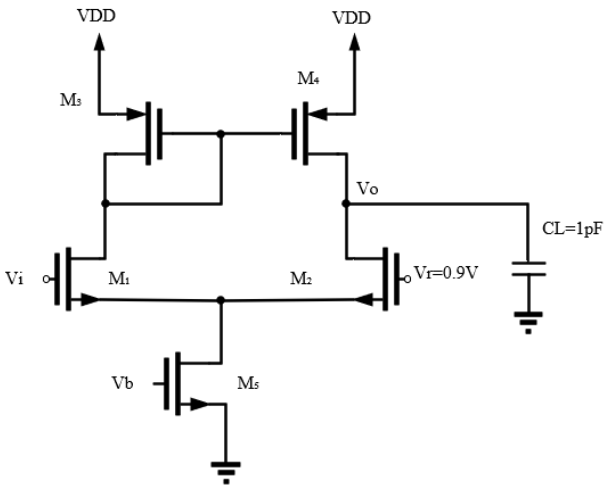

Fig.1

a) **Estimate the values of the Level-1 parameters** in Table.1-1 for both NMOS & PMOS transistors according to the equations in Table.1-1 and parameter values in your Spice file (*.l). Please give the units for the parameters in your report.
(Hint : Select one N_18.x and one P_18.x (e.g. N_18.1) models, which you may use in your design, from the Spice file.)

b) Use the Level-1 parameters obtained in (a) to design (W/L)i **by hand calculation**.
(Hint : You could start from determining a biasing current which your think is proper, and then check whether f_{3dB} and A_V are satisfied)

c) With $(W/L)_i$ set to the values designed in (b), Use **Virtuoso Spectre** to **(i)** calculate the operating modes, g_m, r_o of all transistors when $v_I = v_{REF}$ = 0.9V. Give the **summary of circuit operations** in your report. **(ii)** sweep the DC value of v_O with v_I sweeping from 0 to VDD. Give **the plot of v_O v.s. v_I** in your report, and **mark maximum gain value** on the plot. **(iii)** sweep the frequency response of **v_O/v_I** as $v_I = v_{REF}$ = 0.9V. Give **the plot of the frequency response.**

d) **Compare the differences** between simulation results and hand calculation, and **discuss which Level-1 parameters estimated in (a)** is imprecise, and thus causing these differences.) **Re-estimate these Level-1 parameters** that you think imprecise by sweeping the I_d-V_{gs} or I_d-V_{ds} of individual transistors in Spectre and then extracting parameters values from the simulated I-V curves.

e) Use re-estimated Level-1 parameters to design $(W/L)_i$ **by hand calculation**.

f) Use Spectre to simulate the design in (e). Give **summary of circuit operations, the plot of v_O v.s. v_I,** and **the frequency response** in your report. If necessary, repeat step (e)-(f) to **tune** the (W/L)i to meet $A_V > 60,\ f_{3dB} > 650kHz,$ and the DC biasing conditions you designed. **Please explain all the adjustments you made.**

Parameter	Equation	Unit
V_{TH0}	V_{TH0}	V
K	$\mu_0 C_{ox}$ where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$	$\mu A/V^2$
λ	Use 0.02 for NMOS and 0.04 for PMOS	
γ	$\frac{\sqrt{2\varepsilon_{si} q N_{SUB}}}{C_{ox}}$	$V^{1/2}$
$2\lvert\phi_F\rvert$	$2\frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right)$	V

Note：N_{SUB} correspond to "nch" in the Spice model we use

Tabel.1-1: Level 1 parameters of a MOS transistor

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
$\varepsilon 0$	Permittivity of free space	8.854×10^{-14}	F/cm
ε_{si}	Permittivity of silicon	$11.7\ \varepsilon_0$	F/cm
ε_{ox}	Permittivity of SiO_2	$3.9\ \varepsilon_0$	F/cm

Table.1-2: Silicon constants

(2) Subthreshold Device parameters and Amplifier Design

Consider the differential amplifier in Fig.2 with **C_L=1pF and V_{DD}=1V.** Please follow the steps below to **design** the sizes of all transistors to satisfy the specifications in Table.2-1

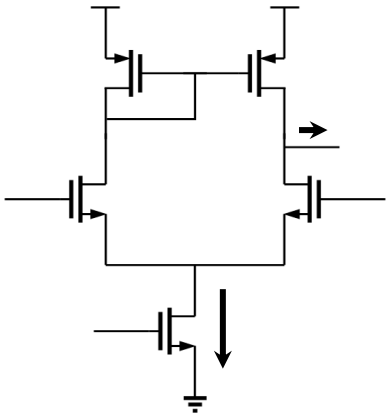

Fig.2

	Specifications	Units
DC characteristics	*Max.* $P_{diss} \leqq 500$ ($V_{DD} = 1V$)	nW
AC characteristics	$A_V \geqq 60$	V/V
	$f_{3dB} \geqq 10k$	Hz
Transient characteristic	Slew rate $\geqq 0.3$	V/μs

Table.2-1

a) Choose a size (W/L) for a PMOS and an NMOS transistors. Use Spectre to simulate and plot the I_D-V_{GS} curves of the selected NMOS and PMOS operating in the **subthreshold region**. According to the model (equation) of I_D-V_{GS} in subthreshold operation, **extract the parameters I_{s0}** and **κ** from the simulated curves. In your report, please show the Spectre-simulated I_D-V_{GS} curves and describe clearly how the parameters are derived. Afterwards, please **plot a figure that compares** (a) the I_D-V_{GS} curve simulated by Spectre with (b) the I_D-V_{GS} curve generated according to the equation with the extracted **I_{s0}** and **κ.**

b) Describe clearly how you **select the biasing current and voltage**, as well as how you **calculate all transistor sizes** in your design.

c) Use **DC analysis** in Spectre to simulate I_{out} versus (V^+-V^-) as V^-=0.5V and V^+ sweeps from 0 to 1V. Does I_{out} agree with your derivation in the question (b)? Is the **power dissipation** smaller than 500nW? If not, please adjust the transistor sizes, explain the adjustments you made, and show the simulated result of the new design in your report.

d) Use **AC analysis** to simulate the frequency response of the amplifier and show the result in your report. Is the specification of **AC characteristics** achieved? If not, please adjust the transistor sizes, explain the adjustments you made, and show the simulated result of the new design in your report.

e) Connect the amplifier as a unit-gain buffer. Use **transient analysis** to apply a step input from 0.25 to 0.75 V and plot the corresponding transient response of Vout in your report. Is the **slew rate** achieved? If not, please adjust the transistor sizes, explain the adjustments you made, and show the simulated result of the new design in your report.