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Minilab 2 report

Project Overview:

This minilab is implementing the MAC unit, which is a part of the miniproject TPUv1.

Interfaces:

#(parameter BITS_AB=8,

parameter BITS_C=16)

input clk, rst_n, WrEn, en, // Aout, Bout, Cout will only update if en is set

input signed [BITS_AB-1:0] Ain,

input signed [BITS_AB-1:0] Bin,

input signed [BITS_C-1:0] Cin, // Cout will be Cin if WrEn is set

output reg signed [BITS_AB-1:0] Aout,

output reg signed [BITS_AB-1:0] Bout,

output reg signed [BITS_C-1:0] Cout

Each clock cycle, if en is set, WrEn is not Aout, Bout, and Cout will be updated to its newest value. If en is not set, Aout, Bout, and Cout will keep its value. If both en and WrEn is set, Cout will take an external value from Cin.

Testbench Approach and Implementation:

The testbench is self-checking and prints out test information in the console. Currently, the testbench initializes 8x8 = 64 instances of the MAC unit and feeds simple or random values to them. The result is then compared with a precalculated table to check for any error. Two “task” are implemented to reduce redundancy of code, where each takes a input to either Ain and Bin or Cin, then it feeds them to the test modules. The testbench is sufficiently commented should there be any confusion.

Code coverage:

To check all different combination of WrEn and en, there is a separate test which feeds some random values into Cin to test its functionality. The situation where en = 0 is checked implicitly by waiting one extra cycle after en = 0 is asserted to ensure registers keep their value. The test routine also checks the situation where en = 1 against simple and random values.

Result:

```
# 0008,0008,0008,0008,0008,0008,0008,0008,
# 0008,0008,0008,0008,0008,0008,0008,0008,
# 0008,0008,0008,0008,0008,0008,0008,0008,
# 0008,0008,0008,0008,0008,0008,0008,0008,
# ------------------------------------
# ------------------------------------
# SIMPLE TEST PASSED!
# ------------------------------------
# Below is Adata
# d7,63,a8,bf,ac,4c,b9,fa,
# 93,8a,74,a9,ba,bb,25,2f,
# 66,37,70,02,98,5a,a2,70,
# d8,75,3e,ea,a8,3e,22,69,
# ad,81,f7,ee,3c,fc,36,9c,
# 96,b5,56,ee,5f,8a,8f,40,
# ca,83,b5,5d,e1,07,ff,d8,
# b7,3e,05,17,68,3c,eb,12,
# ------------------------------------
# Below is Bdata
# 67,05,c1,88,cc,0c,73,1c,
# f7,f5,40,2e,d9,5e,04,94,
# ee,b5,ad,f7,81,51,f7,ae,
# 5d,5e,14,d3,01,32,40,e7,
# 0f,b8,39,a2,22,a1,8c,fa,
# 34,73,74,39,c9,47,67,3e,
# 54,91,b9,87,d8,7a,4d,16,
# de,59,1a,b9,cb,2e,c7,55,
# ------------------------------------
# Below is the expected result
# ce9d,5353,5d1c,8684,1580,0b3a,1298,0091,
# a450,b600,9c94,14ec,e43f,0431,b7fc,0cea,
# fe6d,74ed,0790,1d60,81b3,63b0,495e,053a,
# e417,2a50,1b02,2a63,a366,8d54,1bd9,ef6b,
# fede,b303,e89a,fedb,3db2,b781,de42,1234,
# 8b6c,d8de,ef92,0adb,2099,88db,3ced,e6fe,
# 1a51,3ad4,061b,0da6,4666,cfc9,1925,32d3,
# f174,0ff5,5ba3,153f,0378,fcb1,c471,ea47,
# ------------------------------------
# ------------------------------------
# RANDOM TEST PASSED!
# ** Note: $stop    : /filespace/h/hwang663/ECE554/minilab2/tpumac_tb.sv(48)
#    Time: 245 ns  Iteration: 1  Instance: /tpumac_tb
# Break in Module tpumac_tb at /filespace/h/hwang663/ECE554/minilab2/tpun
```