Zhikai Huang

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EDUCATION

ETH Zürich Zürich, Switzerland
Master of Science in Biomedical Engineering, GPA: 5.4/6.0 2019-2022
Thesis: A Continuous-Time Input Pipelined SAR ADC With Predictive Offset Generation

Xi'an Jiaotong University Xi'an, China
Bachelor of Science in Electronics Engineering, GPA: 89.5/100 2015-2019
Thesis: Digital Back-End Design of a Battery State-of-Charge Estimation Algorithm Without Current Detection

McGill University Montreal, Canada
MITACS Research Scholar Program 2018.6-2018.9
Topics: Measurement of Thermal Noise Floor in Nitrogen Vacancy Centers

RESEARCH INTERESTS

• Mixed-Signal Circuits Design, Bioelectronics and Biosensors, Neuromorphic Computing, etc.

PUBLICATIONS

• Alfio Di Mauro, Arpan Suravi Prasad, **Zhikai Huang**, Matteo Spallanzani, Francesco Conti, Luca Benini, "SNE: an Energy-Proportional Digital Accelerator for Sparse Event-Based Convolutions", Design Automation and Test in Europe Conference (DATE), 2022

• **Zhikai Huang,** Hesam Omdeh Ghiasi, Taekwang Jang, "A Continuous-Time Input Pipelined SAR ADC With Predictive Offset Generation", In preparation

RESEARCH EXPERIENCE

Integrated Systems Laboratory, ETH Zürich | Advisor: Prof. Taekwang Jang Zürich, Switzerland
A Continuous-Time Input Pipelined SAR ADC With Predictive Offset Generation 2021.11-2022.05

• Designed a continuous-time input pipelined SAR ADC with reduced input capacitance, achieving 1.439 uW with 12.83 bits ENOB at 40kSPS, FoMw=4.95fJ/step and FoMs=171.4dB
• Innovation 1: Analog prediction based on signal first and second order derivatives to limit residue signal swing
• Innovation 2: The analog prediction is embedded in the SAR loop that is compact and power efficient

Integrated Systems Laboratory , ETH Zürich | Advisor: Prof. Taekwang Jang Zürich, Switzerland
A Low-Power, Low-Noise, High Linearity Acoustic Sensor Front-End 2021.06-2022.11

• Designed a 0.97 NEF 0.44uW, 20Hz-20kHz BW three-stage inverter-stacking based low noise amplifier
• Designed a THD<1% large output-swing variable gain amplifier with cross-coupled capacitor bank
• Designed a 8-bit synchronous SAR ADC Verilog-A model, estimate resolution limit with statistical modeling

Integrated Systems Laboratory, ETH Zürich | Advisor: Prof. Taekwang Jang Zürich, Switzerland
A High Linearity Chopper-Stabilized Amplifier for Closed-loop Neural Recording 2021.3-2021.06

• Designed a 4.27 uW neural recording chopper amplifier that is capable of handling in-band 80-mVpp differential artifacts and 650-mVpp common-mode artifacts
• Designed the DC servo loop with multi duty-cycled resistors to achieve sub-Hz corner frequency

• Designed the auxiliary path for the chopper amplifier that achieves 40.7X input impedance boosting

Digital Circuits and Systems Lab, ETH Zurich | Advisor: Prof. Luca Benini Zürich, Switzerland
Spiking Neural Network-based 3-DoF Pose Estimation for Event-based SOC 2020.03-2020.6
• Implemented a convolutional spiking neural network capable of regressing an event camera's 3 DoF angular velocity from its raw output stream, enabling ego-motion estimation
• Proposed novel time-averaging regularization for neural network to improve the estimation accuracy
• Quantized the network within 4 bits with less than 1% performance degradation so that it is deployable on the chip designed in the group

Sensors Research Group, ETH Zurich | Advisor: Prof. Tobi Delbruck Zürich,Switzerland
An Analog Multiply-Accumulate Unit for Neural Network Acceleration 2021.03-2021.6
• Designed a 5.9 pJ/MAC 6bit x 3bit analog multiply-accumulate unit with 3200 um^2
• Innovation 1: The multiplying DAC is implemented with cascaded current splitters with complementary topology
• Innovation 2: The accumulator is implemented with a novel interleaving sample and hold circuit

SKILLS

Programming: Verilog (2+ years), System Verilog (2+ years), PyTorch (2+ years), MATLAB (6+ years)
Language: English - Full professional proficiency | Chinese - Native
Experiments: oscilloscope, vector analyzer, soldering, probe station, PCB design

AWARDS

• China Goverment Scholarship for Overseas Visiting (MITACS & CSC, 2018)
• Samsung Scholarship (Xi'an Jiaotong University, 2018)
• Excellent Student Award (Xi'an Jiaotong University, 2017)

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