1. Each stage of pipelines
    a. IF: Instruction fetch. Fetches next instruction's address and store it for the next cycle. At the end of this stage, the next instruction's address will be passed to the ID stage.
    b. ID: Instruction decode. This stage decodes the instruction address passed from fetch stage, fetch registers, and pass the instruction to the execution stage.
    c. EX: execution. Execute the instruction with registers passed from ID stage.
    d. MEM: memory access. Read and write data to the memory.
    e. WB: register write back. Write back registers to the register file.
2. K=number of instructions Nk = number of cycles
   Let k = 5, when Ik is passed in, the first instruction just gets moved out of the pipeline, and Nk=5 at this stage. Therefore, when Ik is finished, Nk = 4+k. When k goes to infinite, Nk/k = $\infty/(4+\infty)$, which is approaching to 1. Therefore, $\lim k \to \infty$ Nk/k = 1.
3.
   1). Active stages: IF, ID, EX, WB. Inactive stage: MEM
   2). Active stages: IF, ID, EX, MEM, WB
   3). Active stages: IF, ID Inactive stages: EX, MEM, WB

4. for EX buffer, there is the case that it needs to return a ZERO, which is 1 bit. Therefore, it needs 97 bits. For MEM buffer, it needs a bit for memory read or memory write. Therefore, it needs 97 bits.