Fuzzing Deep Learning Compilers with HirGen

Anonymous Author(s)

ABSTRACT

Deep Learning (DL) compilers are widely adopted to optimize advanced DL models for efficient deployment on diverse hardware. Their quality has profound effect on the quality of compiled DL models. A recent bug study shows that the optimization of high-level *intermediate representation* (IR) is the most error-prone compilation stage. Bugs in this stage are accountable for 44.92% of the whole collected ones. However, existing testing techniques do not consider high-level optimization related features (e.g. high-level IR), and are therefore weak in exposing bugs at this stage. To bridge this gap, we propose HirGen, an automated testing technique that aims to effectively expose coding mistakes in the optimization of high-level IR. The design of HirGen includes 1) three coverage criteria to generate diverse and valid computational graphs; 2) full use of high-level IR's language features to generate diverse IRs; 3) three test oracles inspired from both differential testing and metamorphic testing. HirGen has successfully detected 21 bugs that occur at TVM, with 17 bugs confirmed and 12 fixed. Further, we construct four baselines using the state-of-the-art DL compiler fuzzers that can cover the high-level optimization stage. Our experiment results show that HirGen can detect 10 crashes and inconsistencies that cannot be detected by the baselines in 48 hours. We further validate the usefulness of our proposed coverage criteria and test oracles in evaluation.

CCS CONCEPTS

• **Software and its engineering → Software testing and debugging**.

KEYWORDS

Deep Learning Compiler, Software Testing

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1 INTRODUCTION

Deep learning (DL) compilers, such as TVM [1], Glow [2], XLA [3] and nGraph [4], have shown the effectiveness in optimizing advanced DL models for efficient model deployment at diverse devices [5]. They take as input a DL model, extract its computational graph, and re-represent the DL model using intermediate representations (IRs) [5]. DL compilers consist of multiple compilation stages, which include high-level and low-level optimizations. DL compilers arrange these two optimizations in order with high-level optimization first and low-level optimization second. The optimizations aim to compile deep learning models into binary executables that can run efficiently on target hardware devices.

Like conventional compilers[6, 7], DL compilers are prone to bugs. These bugs can cause undesired compiler behaviors, such as crash, unexpected wrong behavior and poor performance [8]. These undesired behaviors could result in catastrophic effects on the correctness and reliability of mission-critical DL applications (*e.g.*, autonomous driving cars [9] and aircraft collision avoidance systems [10]).

Techniques have been recently proposed to detect bugs in DL compilers, including TZER [11], TVMFuzz [12], MT-DLComp [13] and NNSmith [14]. Despite preliminary reported success in bug detection for TVM, they are inefficient in revealing bugs that occur in high-level optimization, which accounts for 44.92% of the bugs found in DL compilers [8]. TZER and TVMFuzz [11, 12] are proposed to detect low-level optimization bugs in a DL compiler with generated low-level IRs. Since these two techniques test DL compilers by mutating low-level IR, and low-level IR cannot be used by high-level optimization, they theoretically cannot detect bugs in high-level optimization stage. MT-DLComp [13] tests a DL compiler by constructing mutated DL models. Since its mutation strategies only insert operators that yield zero, the kinds of operators and the available places to insert these operators are limited. Therefore, it cannot generate models of diverse computational graphs to cover corner high-level optimization cases. In test oracle design, MT-DLComp does not take advantage of the language features of high-level IR and high-level optimizations. As a result, it cannot effectively detect bugs in high-level optimizations (We will prove it in section 5). NNSmith [14] mainly focuses on revealing the hidden defects in DL compilers, such as arithmetic problem, fragile type system, poor support for specific data layouts, by generating computational graphs and inputs. Since it's generation process and test oracle design do not consider language features of high-level IR in DL model generation, and do not consider high-level optimizations in test oracle design, it cannot efficiently detect high-level optimization related bugs. In Section 5, we will show NNSmith is orthogonal to HirGen in terms of bug detection ability.

To bridge the gap, we propose the first DL compiler fuzzing technique that focuses on high-level optimization: HirGen. HirGen is designed to satisfy the following four objectives: 1) the satisfaction of integrity constraints, such as type match and tensor shape match, that govern high-level IR to avoid early crash before invoking optimization, 2) the exploration of diversity of computational graph, 3) utilization of high-level IR language features for construction of diverse high-level IRs, 4) the capability of detecting multiple types of optimization bugs. To achieve the first objective, HirGen performs type checking and shape checking in each operator node

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insertion by leveraging the information, including type, shape and connection information, of the existing nodes. After insertion, HirGen also updates the information of the new node for future use. To meet the second objective, HirGen incorporates a coverage-guided strategy to explore diverse operator nodes, operator edges and the combination of operator type and data type. To meet the third objective, HirGen can construct diverse high-level IRs from a single computational graph to achieve full use of IR's language features. To meet the fourth objective, HirGen incorporates three test oracles, two of which are designed purposely for DL compilers. An example of test oracles is that a model should not make different prediction after optimization. Besides functional correctness, HirGen can also test the robustness of DL compilers. Specifically, HirGen provides an option of generating invalid computational graphs that violate type constraints and shape constraints [15]. The option aims to test whether DL compilers can catch such invalid computational graphs and throw the expected exceptions. In this way, HirGen can also detect bugs caused by incorrect exception handling.

Following existing works on DL compiler testing, we evaluate the performance of HirGen on TVM, which is the most popular DL compiler. In baseline selection, we choose 1) TVMfuzz (with lower-case f), preliminary proof-of-concept application from a bug study [8]. The tool is chosen because it is the only testing technique focusing on detecting bugs arising from high-level optimizations in DL compilers; 2) MT-DLComp [13], a metamorphic testing framework that can cover high-level optimization stage; 3) LEMON [16], a fuzzing technique for DL library (e.g., Tensorflow [17], PyTorch [18]) testing; and 4) NNSmith [14], a generation-based DL compiler fuzzer. Our experimental results show that 1) HirGen can detect 10 distinct crashes or inconsistencies that are not detectable by other techniques in two-day's execution; 2) TVMfuzz, MT-DLComp and LEMON are all inefficient in detecting bugs, they found a total of three crashes, two of which are also detectable by HirGen; 3) NNSmith is also efficient in bug detecting, detecting 14 distinct crashes. But with the exception of one crash, the crashes they found were all orthogonal to the crashes and inconsistencies found by HirGen. Besides this comparison experiment, we examine the usefulness of the coverage-guided strategy in generating diverse computational graph by an ablation study.

In summary, we make three major contributions.

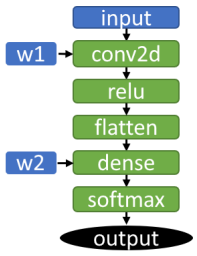
- This work introduces a new focus on testing the most bug-prone stage, high-level optimization, of DL compilers. We propose a computational graph generation algorithm and three test oracles to detect bugs of diverse root causes in the implementation of high-level optimization.
- We have implemented HirGen, a fuzzing technique targeting at TVM. HirGen is implemented in 3K lines of C++ code. It has detected 21 bugs, of which 17 have been confirmed, 12 have been fixed and 14 were previously unknown. Among the 17 confirmed bugs, 14 are highly related to high-level optimizations and three are about low-level optimization and deployable code generation. Furthermore, we have conducted an experimental study to compare HirGen with TVMfuzz, MT-DLComp, LEMON and NNSmith, the state-of-the-art testing techniques that can cover high-level optimization stage. We have also discussed the utility of each component of HirGen.
- We release HirGen, the details of detected bugs and experiment data at https://github.com/anonymousWork000/HirGen.

2 BACKGROUND

2.1 DL Compilers

DL compiler takes as input DL models. These models can be constructed with the help of DL frameworks, such as Tensorflow[17] and PyTorch[18]. After interpreting the input model's computational graph (will be detailed in the next subsection), the DL compiler converts it into high-level IR. Each node in the computational graph is represented by one or several IR expressions. For instance, a *conv2d* (two-dimensional convolution) node is represented by *nn.conv2d* in the high-level IR of TVM. DL compilers then optimize the computational graph at the high-level IR. For instance, a static subgraph independent of inputs can be optimized through constant folding at IR. After optimization, high-level IR is translated into low-level IR for further optimization. In this step, a high-level IR expression (e.g., `nn.conv2d`) is expanded into a nested loop of low-level computation instructions. Subsequently, low-level optimizations are performed to improve efficiency. For instance, loop tiling can be performed at low-level optimization to accelerate the computation of *conv2d* on a specified hardware device. Finally, low-level IR is translated into deployable code for diverse hardware using traditional compilers and platforms.

2.2 Computational Graph and High-level IR




```
def @main(
    %conv2d_input,
    %v_param_1: Tensor[(6, 1, 5, 5), float32],
    %v_param_2: Tensor[(6), float32],
    %v_param_3: Tensor[(4704, 4704), float32],
    %v_param_4: Tensor[(4704), float32]) {
  %0 = nn.conv2d(%conv2d_input, %v_param_1,
       padding=[2, 2, 2, 2], channels=6,
       kernel_size=[5, 5]);
  %1 = nn.bias_add(%0, %v_param_2);
  %2 = nn.relu(%1);
  %3 = transpose(%2, axes=[0, 2, 3, 1]);
  %4 = nn.batch_flatten(%3);
  %5 = nn.dense(%4, %v_param_3, units=4704);
  %6 = nn.bias_add(%5, %v_param_4);
  nn.softmax(%6, axis=1)
}
```

(a) Computational Graph **(b) High-level IR**

Figure 1: Computational Graph and the Corresponding High-level IR

A computational graph is a directed graph that expresses the data flow in computation. High-level IR, also known as graph-level IR, is an intermediate representation to express computational graph. In DL community, high-level IR is widely used for describing computational graph by DL compilers (e.g., TVM) and also frameworks (e.g., ONNX). Figure 1a illustrates the computational graph of a 2-dimensional convolutional neural network, where variable/-constant nodes and operator nodes are colored in blue and green, respectively. The end of a graph is denoted by a black ellipse. Arrows in this graph represent data flows. Specifically, variable nodes and constant nodes are the starting point of a data flow, passing their data to the next nodes while operator nodes work as a relay to extend the data flow, passing the results they calculate. Figure 1b illustrates an example of TVM's high-level IR, Relay IR, of the

computational graph in Figure 1a. This IR is not unique, but is rewrittable in multiple other ways in the same semantics by utilizing IR language features. For instance, Relay offers first-citizen functions to separate the main function into multiple functions with complex call chain. And ONNX also plans to support this feature in the future[1].

3 APPROACH

This section presents the design and underlying methodology of HirGen whose workflow is given in Figure 2. HirGen maintains

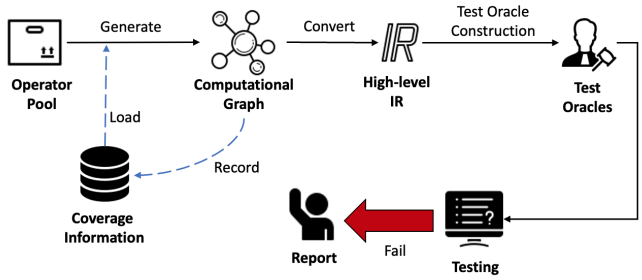


Figure 2: Workflow of HirGen

a pool of 58 operators that can be expressed by high-level IRs in popular high-level framework (e.g. Relay [19], ONNX [20]). HirGen first loads existing coverage information, generates a computational graph based on it, and updates coverage information from the newest graph. Then, HirGen leverages an high-level framework such as Relay or ONNX, to convert the graph into a high-level IR and feeds it into the DL compiler. To capture the defects in the target DL compiler more sufficiently, HirGen constructs three test oracles from the spirits of differential testing and metamorphic testing. Any test case that violates the oracles is regarded as a witness to a bug of the compiler and will be reported to developers. The remainder of this section is divided into three parts. In Section 3.1, we will elaborate the details of our computational graph generation algorithm. Section 3.2 will present how to utilize the language features of high-level IR and convert computational graph into high-level IR. In Section 3.3, we will introduce the design of our created test oracles.

3.1 Computational Graph Generation

3.1.1 Overview. We consider the generation of computational graph as a process of continuously inserting various operator nodes into the initially empty graph $CG = \{\}$ until the number of operator nodes equals to the number required. Generally speaking, HirGen selects one operator from the operator pool, loads the operator into CG as a node nd, and constructs connection between nd and other existing nodes. In these steps, HirGen maintains node information, including data type, tensor shape and connection information, for each node. To improve the diversity of the graph, HirGen also involves three coverage criteria and tries to improve the coverage in each insertion of node.

[1]https://github.com/onnx/onnx/blob/main/docs/Operators.md

With these prerequisites, HirGen provides two generation modes. To generate valid computational graphs, HirGen utilizes the above-mentioned node information for strict type checking and shape checking. In this way, each insertion is valid and breaks no constraint. We call this mode *strict generation*. On the other hand, strictly following the constraints may miss the opportunity to test the exception handling ability of DL compilers when constraints are violated. Therefore, HirGen also provides *disruptive generation* to deliberately break type constraints and shape constraints. We will first elaborate strict generation and then disruptive generation.

3.1.2 Node Information. Inserting a node into CG requires node information of all existing nodes to perform type-checking and shape-checking. Node information describes the typical features of node, and such information is essential to promise the correctness of each insertion. For instance, in the insertion of an operator named add that sums two nodes, HirGen first checks all available nodes (including operator nodes, variable nodes and constant nodes) and selects two nodes n_a and n_b from available nodes, such that n_a and n_b have the compatible tensor shapes and data types, and their data types are acceptable by the operator add. Each type of node has its own node information, as detailed in Table 1.

Node Type	Node Information
variable	$dataType$, $tensorShape$
constant	$dataType$, $tensorShape$, $value$
operator	$dataType$, $parentNodes$, $tensorShape$ = INFERENCE($parentNodes$)

Table 1: Node Information

Specifically, HirGen considers the following three types of nodes, namely, *variable*, *constant* and *operator*.

(1) *Variable* node. It involves data type $dataType$ and tensor shape $tensorShape$ describing the details of the tensor wrapped in this node. $dataType$ corresponds to the data type of all elements in this tensor, such as $int64$ and $float32$. $tensorShape$ is a vector of the scale of all dimensions in the tensor.
(2) *Constant* node. Besides the $dataType$ and $tensorShape$, *constant* node includes the value of tensor $value$ as a part of its information.
(3) *Operator* node. Operators require parameter(s) and thus they are all connected with other nodes in the graph. To document this connection information for each operator node, Besides $dataType$, HirGen records its parent node(s) $parentNodes$ to which this node connects and records its tensor shape inferred from parent node(s).

3.1.3 Coverage Guidance. To let HirGen intelligently generate diverse computational graph with in-depth thoughts about selection of data type, operator, etc, we design three coverage criteria.

(1) **Operator-datatype Coverage**. Let op_i be the i_{th} operator in the operator pool. Let $dtype_j$ be the j_{th} data type in the collection of data types. Let $Cov(op_i, dtype_j)$ be 1 when op_i has once been inserted into the graph as a node with data type $dtype_j$. Otherwise, it is 0.
(2) **Operator-shape Coverage**. Let op_i be the i_{th} operator in the operator pool. Let *shape* be the shape of the output tensor of this operator node after being inserted into the graph. Let

$Cov(op_i, shape)$ be 1 if op_i has once been inserted into the graph as a node with tensor shape *shape*, and 0 otherwise.

(3) **Operator-edge Coverage**. Let op_i and op_j be the i_{th} and j_{th} operator in the operator pool. Let $Cov(op_i, op_j)$ be 1 if there exists one edge from op_i to op_j, and 0 otherwise.

The design of the first two coverage criteria are motivated by the fact that type problem and shape problem are the two major root causes of DL compiler bugs [8]. The design of the third one tries to complicate the data flow of the computational graph since the third coverage encourages HirGen to interleave different operators in a computational graph. Specifically, with operator-datatype coverage, HirGen is encouraged to 1) involve different operators into the graph and 2) utilize diverse data types since data type problem is a big concern for DL compilers [8]. With operator-shape coverage, HirGen is encouraged to try various calculation with diverse tensor shapes and thus increase the probability of encountering calculation problem, such as poor implementation of some operator in special shape or different calculation results on different platform. With operator-edge coverage, HirGen is guided to connect the new operator node to the existing operator nodes instead of variable nodes and constant nodes. In this way, the generated computational graph contains more complex and deep data flow instead of parallel connection of several simple data flows. In implementation, we can easily extend operator-edge coverage to operator-path coverage with 3 or more operator nodes included. In this way, we can explore a more diverse and complicated computational graph, but at the cost of greater time costs. HirGen is encouraged to explore the diversity of computational graph by increasing these three coverages. Therefore, we name our computational graph generation approach *coverage-guided* generation.

3.1.4 Strict Generation. Algorithm 1 presents how HirGen strictly generates computational graph with type-checking and shape-checking by two procedures. GENERATION is the main procedure. This procedure takes as input the required number of operators *rOpNum* contained in computational graph. It outputs a computational graph of which the number of operators equals to *rOpNum*. PREINSERT is the auxiliary procedure. It details how HirGen embeds type-checking and shape-checking in generation. GENERATION procedure includes the following two main parts.

Initialization. HirGen performs initialization from Line 2 to Line 6. Specifically, computational graph *CG* is initialized as empty and the number of operators *opnum* in *CG* is set to 0. Operator Pool and data type set are both initialized for future use.

Generation Loop. In each iteration (Lines 7-18), HirGen generates an operator node, updates its node information and finally inserts it into *CG* if new coverage is explored. Specifically, HirGen first randomly selects an operator and data type (Line 8, 9). Then it seeks for connection from *CG* and infers the tensor shape of the operator node *opNode* built from the newly selected operator (Line 10). Subsequently, HirGen calculates coverage and performs update and insertion if new coverage is explored (Line 11-17). The exploration of new coverage is detected by any increment of the three coverages defined in section 3.1.3. During update, HirGen adds *opnum* by 1, updates coverage and node information of *opNode*. The generation loop stops when *opnum* equals *rOpNum* and HirGen returns *CG* eventually.

Algorithm 1 Computational Graph Generation

```
1:  procedure GENERATION(rOpNum)
2:      CG ← {}
3:      opnum ← 0
4:      opPool ← {add, subtract, multiply, divide, ...}
5:      dataTypeSet ← {int64, int32, int16, int8, uint64, uint32,
6:                     uint16, uint8, float64, float32, bool}
7:      repeat
8:          opNode ← SELECT(opPool)
9:          dataType ← SELECT(dataTypeSet)
10:         connection, shape, CG ← PREINSERT(opNode, dataType, CG)
11:         coverage ← CALCULATECOVERAGE(opNode, dataType, connection, shape)
12:         if NEWCOVERAGE(coverage) then
13:             opnum ← opnum + 1
14:             UPDATECOVERAGE(coverage)
15:             opNode.info ← (connection, shape, dataType)
16:             CG ← CG ⋃ {node}
17:         end if
18:     until opnum = rOpNum
19:     return CG
20: end procedure
21: procedure PREINSERT(opNode, dataType, CG)
22:     availableNodes ← TYPECHECK(CG, dataType)
23:     nodeGroup1, nodeGroup2, ... ← SHAPECHECK(availableNodes)
24:     paramNodes ← SELECT (nodeGroup1, nodeGroup2, ...)
25:     if NODENOTENOUGH(paramNodes) then
26:         node1, node2, ... ← CREATE(dataType, paramNodes)
27:         CG ← CG ⋃ {node1, node2, ...}
28:         paramNodes ← paramNodes ⋃ {node1, node2, ...}
29:     end if
30:     for node IN paramNodes do
31:         connection ← (opNode, node)
32:     end for
33:     shape ← INFERENCE(connection)
34:     return connection, shape, CG
35: end procedure
```

Procedure PREINSERT shows the details of building connection between *opNode* and existing nodes of *CG* and shape inference. With type-checking (Line 22) and shape-checking (Line 23), HirGen sorts out several node groups from *CG*. All nodes of each node groups are mutually shape-compatible and nodes from these groups are all type-compatible with *opNode*. Then HirGen selects a node group and dumps all its nodes into *paramNodes* (Line 24). The number of required parameter nodes is fixed for each kind of operator. In implementation, HirGen has a certain probability of connecting one node to an operator node for multiple times, such as connecting one variable node to add node for twice, meaning add the node to itself. But to complicate data flow, HirGen discourages this behavior in favor of connecting the required number of different nodes. Therefore, if the number of parameter nodes in *paramNodes* are insufficient for *opNode*, HirGen has large probability in creating variable nodes or constant nodes that are shape-compatible with all parameter nodes and type-compatible with *opNode*, inserts them into *CG* and updates *paramNode* (Line 25-29). Finally, HirGen creates connection information (Line 30-32), infers tensor shape of *opNode* and returns them both plus the possibly updated *CG*.

3.1.5 Disruptive Generation Algorithm. Disruptive generation is similar to strict generation. It also needs coverage to memorize what type constraints and shape constraints have been broken. In addition, node information is also required. Since it contains data type and tensor shape of each node, which is necessary for breaking constraints. Specifically, during disruptive generation, HirGen purposely 1) connects operator node to other node(s) with the data type(s) it can not accept in TVM (e.g., add operator with `bool` data type), and 2) connects nodes that are type-incompatible

or shape-incompatible (e.g., add two nodes of which the shapes are `[3,4]` and `[2,3]` respectively).

3.2 High-level IR Generation

High-level IR generation is simple with the help of existing high-level frameworks, such as Relay and ONNX. Taking Relay as example, it provides ample APIs for receiving node information of various types of nodes and diverse operator nodes. For instance, `relay.var` takes as inputs its name, data type and tensor shape, and `relay.add` takes as input only its connection information. These APIs contain strict type constraints and shape constraints and it is easy to crash early before optimization if the computational graph contains error.

Besides the plain conversion by loading each node into its corresponding high-level expressions and assembling them into a high-level IR, we can also utilize the primitive features of these high-level frameworks. Take Relay for example, to improve expressivity, it allows using a function to wrap a subgraph and call the function in other ones. ONNX also plans to support this feature by supporting Function API. To better utilize these features, we also consider extracting a subgraph from the generated computational graph and wrap it with a high-level function. In this way, we can better test how DL compilers tackle the situation where functions are included.

Algorithm 2 Conversion from Computational Graph to High-level IR

```
1:  procedure CONVERSION(CG)
2:      Functions ← {}
3:      Expressions ← {}
4:      for node IN CG do
5:          Expressions ← LOAD(node.info, Functions, Expressions)
6:          if ROLL() == func then
7:              inputNodes, outputNodes ← ANALYZE(Expressions)
8:              function ← COMPOSEFUNCTION (inputNodes, outputNodes)
9:              Functions ← Functions ⋃ function
10:             Expressions ← {}
11:         end if
12:     end for
13:     return Expressions ⋃ Functions
14: end procedure
15: procedure LOAD(node.info, Functions, Expressions)
16:     expression ← CONSTRUCTEXPRESSION (node.info)
17:     if PARENTINFUNCTION(node.info) then
18:         functions ← FIND(node.info)
19:         callExprs ← CREATECALLEXPRESSION(functions)
20:         Expressions ← Expressions ⋃ {callExprs}
21:     end if
22:     Expressions ← Expressions ⋃ {expression}
23:     return Expressions
24: end procedure
```

The overall algorithm of converting computational graph into high-level IR is shown in Algorithm 2. CONVERSION procedure takes as input computational graph *CG* and outputs its corresponding high-level IR. During initialization, HirGen creates two empty sets, named *Functions* and *Expressions* respectively (Line 2, 3). They represent the collection of functions and high-level expressions, respectively. In the for loop (Line 4-12), HirGen traverses all nodes in *CG*, loads each node into high-level expression and update *Expressions* (Line 5). Then it randomly selects a set of high-level expressions and wraps them with a function (Line 6-11). To compose a function, HirGen first analyzes the input nodes and output nodes of the underlying subgraph of the expressions (Line 7). Then it composes a function using these nodes (Line 8. Finally, HirGen updates *Functions* and *Expressions* (Line 9-10). CONVERSION procedure returns the union of *Expressions* and *Functions* as High-level IR. LOAD procedure presents the detail of loading a node into high-level expression. During loading, HirGen takes care of connection information by inquiring whether the node connects to other nodes wrapped in function(s) (Line 17), if it is the case, then a call expression is created (Line 19). This procedure return *Expressions* after update.

3.3 Test Oracles

Test oracle is an important mechanism to determine if a test passes or fails. In this paper, we consider three test oracles in total. Any failed test case determined by these oracles will be reported.

3.3.1 $Oracle_1$: Crash. Crash is widely used in test oracle construction to decide whether the testing fails [11]. Besides, according to the statistics in a compiler bug study [8], the number of bugs with crash symptom occupy 59.37% of all collected 603 bugs. This huge proportion shows a urgent need to take crash seriously. As for crash bugs detected when type-checking and shape-checking are turned off, we only report the bug if the crash is a segmentation fault because other crashes with detailed bug trace is largely due to explicit violation of constraints in the computational graph. As for other crash bugs, we report them all since the generated computational graph under checking strictly follows all constraints in TVM and the crash is largely due to the poor implementation of TVM.

3.3.2 $Oracle_2$: Result Inconsistency among original high-level IR, optimized high-level IR and mutated high-level IR. Intuitively, high-level optimization is only related to performance boost such as calculation acceleration and memory cost saving, but can not change results. In addition to involving high-level optimization, we also design a mutation strategy named function rewrite to generate mutated high-level IRs who has the same output as the original high-level IR given the same input. This mutation strategy is inspired by Relay's support for functional programming features. By function rewriting, we can better utilize Relay's expressions and better test TVM with richer high-level IRs. Specifically, this mutation strategy can rewrite function expressions in high-level IR in the following ways.

- Turn a global function f into the local closure of another newly created global function g. g has the same parameters as f and its returned value is a call to f with these parameters. After this tuning, this mutation also substitute all calls to f with calls to g.
- Wrap a function f with an empty function g which returns f and also change all calls to f to calls to the call to g.
- Call a function f and return the call in another function g, then substitute all calls to f with calls to g.

The mutated high-level IR only differs from the original high-level IR in the function call chain. Therefore, it is sound to expect the same calculation results among these three high-level IRs given the same input. This metamorphic relation inspires us to form this oracle. In addition to different calculation results, if the original high-level IR passes compilation and runtime but the optimized one or mutated one fails in one of these two processes, we also count it as result inconsistency.

3.3.3 $Oracle_3$: Result Inconsistency across hardware devices. To maintain the same predictive capability of a DL model on different supported hardware devices, TVM should promise to output the same results on diverse hardware given the same input to a DL model. And similar to $Oracle_2$, inconsistent execution status (e.g., crash on CPU but execute well on GPU) is also counted as result inconsistency. Following this common sense, we build $Oracle_3$ with the spirit of different testing. Given any high-level IR, after compiling it with multiple provided compilation approaches, feeding an input and executing it on CPU and GPU, it is reasonable to expect the same calculation results.

4 EXPERIMENT SETUP

4.1 Research Questions

In this study, we aim to address the following research questions:

RQ1 How effective is HirGen in detecting bugs of TVM?
RQ2 Are all the test oracles effective in detecting bugs?
RQ3 Are bugs found by HirGen highly related to high-level optimization?
RQ4 Is disruptive generation useful in finding exception handling bugs?
RQ5 Can coverage-guided generation benefit the diversity of graph?

4.2 HirGen Implementation

We implement HirGen in C++ with around 3K lines of code. Our implementation involves 58 operators to generate computational graph, 25 high-level optimizations for catch optimization bugs and four compilation methods to conduct testing.

4.2.1 Operators. In total, HirGen includes 58 operators supported by TVM, including 23 binary operators and 35 unary operators. And it is easy to extend HirGen with other operators. The following lists are the two groups of operators involved by HirGen.

- binary operators: `Add`, `Subtract`, `Multiply`, `Divide`, `Power`, `Mod`, `Floor Mod`, `Floor Divide`, `Logical And`, `Logical Or`, `Logical Xor`, `Bitwise And`, `Bitwise Or`, `Equal`, `Not Equal`, `Less`, `LessEqual`, `Greater`, `GreaterEqual`, `Maximum`, `Minimum`, `Right Shift`, `Left Shift`.
- unary operators: `Log`, `Log2`, `Log10`, `Tan`, `Tanh`, `Cos`, `Cosh`, `Sin`, `Sinh`, `Acos`, `Acosh`, `Asin`, `Asinh`, `Atan`, `Atanh`, `Exp`, `Erf`, `Sqrt`, `Rsqrt`, `Sigmoid`, `Floor`, `Ceil`, `Trunc`, `Round`, `Abs`, `Sign`, `Negative`, `Logical not`, `Bitwise not`, `Zeros Like`, `Ones Like`, `Copy`, `isNan`, `isFinite`, `isInf`.

4.2.2 Optimization and Compilation Methods. We select in total 25 high-level optimizations supported by TVM[2] The main reason for choosing these high-level optimizations in TVM is our generated computational graph can trigger them. Besides collecting these high-level optimizations, we also utilize different compilation methods provided by TVM. Different compilation methods deal with different scenarios and include different optimization sequences. Overall, we include `relay.build()`, `relay.build_module.create_executor('debug')`, `relay.build_module.create_executor('graph')` and `relay.build_module.create_executor('vm')` in HirGen. Besides these high-level optimizations, it is easy to extend HirGen with other optimizations.

4.3 Bug Report

For each bug we have found, we report it in one of the three channels: 1) upload the bug-triggered script and experiment environment on TVM Community[3]; 2) report the bug on Github Issue[4] with reproducible script, experimental environment, and most importantly, our analysis on the reason for triggering it; 3) create a pull request with the elaboration of this bug and our code patch. We choose our reporting channels primarily based on our expertise of the problem. For the least familiar bug, we submit it on TVM Community in the form of question to get rid of misdiagnosis. Then, we wait for an official fix or some comments from developers on this problem. For the most familiar one, we directly fix it, and we succeed in creating two pull requests and fixing two bugs. For other situations, we choose the second way and leave some comments on how to fix the bug.

4.4 Baseline Selection

4.4.1 TVMfuzz. TVMfuzz is a preliminary proof-of-concept application for fuzzing TVM[8]. It can learn TVM API call chains from unit test scripts, then re-order and mutate them. By learning from high-level IR and optimization related unit test scripts, TVMfuzz can cover this stage.

4.4.2 MT-DLComp. MT-DLComp is an automated testing framework for DL compilers[13]. It mutates existing DL models to generate equivalent models and test DL compilers by three oracles. Though this technique is not specially created for detecting bugs in high-level optimization, it can cover this bug-prone stage. Therefore, we also include it as a baseline.

4.4.3 LEMON. LEMON is a testing technique for deep learning frameworks[21]. It generates Keras [22] models by mutating existing models. By setting different backends of Keras, LEMON detects prediction difference incurred by these backends. Though LEMON is not for testing DL compiler, we can retrofit it to barely achieve the goal. In short, we remain the mutation part to generate new models and test DL compilers by two test oracles: 1) crash, and 2) above-threshold prediction difference between original Keras models and compiled Keras models.

4.4.4 NNSmith. NNSmith is a generation-based fuzzer for DL compilers [14]. During generation, it generates diverse computational graphs, converts them into DL models using different DL frameworks, and uses gradient-guided search to generate inputs. During testing, it conducts differential testing among several DL compilers. In the testing process, NNSmith captures all prediction difference and crashes.

4.5 Metrics

To compare HirGen with these four baselines in the ability of detecting bugs in high-level optimization stage, we execute each or

[2]https://github.com/anonymousWork000/HirGen/blob/experiment/optimizations

[3]https://discuss.tvm.apache.org/

[4]https://github.com/apache/tvm/issues

them separately for two days. To be fair, we only execute HirGen in strict generation mode, since all other three techniques can only generate valid DL models and APIs. As for bug counting, we utilize the informative stack trace and bug text provided by TVM and manually check bug duplication. Following existing works [23], failures with same bug text and same bug trace are regarded as duplicates. We also use this metric in the comparison between coverage-guided generation and no-guide generation in the answer to RQ5.

4.6 Experiment Environment

We conducted experiments on a server with Intel(R) Xeon(R) CPU, NVIDIA GeForce GTX1080Ti GPU, and 128 RAM, coordinated with 64-bit Ubuntu 16.04 OS.

5 EVALUATION

5.1 RQ1: Bug Detection Capability of HirGen

5.1.1 Summary of Detected Bugs by HirGen. Until now, HirGen has found 21 bugs, of which 17 have been confirmed, 12 have been fixed in the main branch of TVM and 14 are previously unknown to developers. Table 2 presents all details about all the confirmed bugs discovered by HirGen, including their symptoms, root causes, the test oracles detecting them, the fixing status and whether they are previously unknown. Symptom includes crash and inconsistency. The former means that TVM terminates unexpectedly while the latter means that different results or statuses are caught in testing. We also manually investigate the root cause of each bug adopting the taxonomy of a recent bug study [8]. Specifically, We carefully compare these bugs with the collected historical bugs and assign each of them with a root cause.

The root causes of these bugs are divided into the following classes:

- Type Problem. This category of bugs is triggered by data type related problems, including incorrect type inference, incomplete implementation of an operator on one data type, etc.
- Incorrect Exception Handling. This category of bugs occurs when TVM lacks rich and readable warning messages or even has no handling of some extreme situations. This kind of bugs are related to the robustness of TVM.
- Incorrect Numerical Computation. This root cause involves incorrect numerical computations, values, or usages.
- Internal API Incompatibility. This category of bugs is triggered because TVM can not handle the combination of some APIs correctly. For instance, unexpected refuse of one combination of several high-level optimizations is counted as this kind of bug.
- Memory Allocation Problem. This root cause refers to the poor or incorrect memory allocation.

Check mark in *Previously Unknown* column in Table 2 means that the corresponding bug was unknown before we reported it. Since we tested TVM v0.9 (commit id: 124813f) at the beginning of our experiment and TVM was evolving fast, we found some cases early in the experiment that crashed on the version we tested but worked fine on the latest version. These bugs have been actually fixed before being reported and thus marked as previously known bugs.

5.1.2 Comparison with State-of-the-art Techniques. We conducted a comparison experiment among HirGen and other three state-of-the-art DL compiler fuzzers, named TVMfuzz, MT-DLComp, LEMON and NNSmith respectively, to compare their bug detection ability. All tests are executed on TVM v0.9 (commit id: 124813f). This version is the initial TVM version we began our first testing using HirGen. After two-day execution, HirGen detected 11 distinct crashes and inconsistencies, TVMfuzz detected three distinct crashes, of which only one bug has not been detected by HirGen, while MT-DLComp and LEMON detected nothing. As for NNSmith, it detected 14 distinct crashes. Among them, five are related to the data layout support problem. They are captured with bug message such as *"WCHN layout is not supported"*. Three are about TVM's fragile type system. They are captured because TVM cannot support type match such as *int32* and *int64*. Among other crashes, only one is related to high-level optimization. This crash is about incorrect type inference and was also detected by HirGen. Besides crashes, NNSmith can also detect prediction difference among several DL compilers, which is out of the scope of testing focus of HirGen. In other words, HirGen and NNSmith have orthogonal contribution in bug detection. These bugs have been released in HirGen repository.

5.2 RQ2: Effectiveness of Test Oracles

To demonstrate the effectiveness of our test oracles, we conduct a case study of several representative confirmed bugs detected by each test oracle.

$Oracle_1$: *Crash*. $Oracle_1$ caught the most bugs among all test oracles. In total, it finds eight bugs of three root causes, including *Incorrect Numerical Computation*, *Incorrect Exception Handling*, *Memory Allocation Problem*.

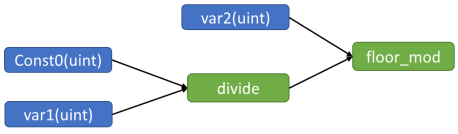


Figure 3: The Computational Graph to Trigger Bug_1

Incorrect Numerical Computation. Take Bug_1 as an example. The computational graph to trigger this bug is presented in Figure 3. In this graph, a `divide` operator first calculates the result of dividing a constant by a variable and then passes the calculation result R to `floor_mod` as dividend. All involved variable nodes and constant nodes are of data type *uint* and this type finally flows into `floor_mod`. However, TVM pre-calculates the possible value range of R and detects it could probably be 0. Therefore, TVM incorrectly throws an exception and terminates even before we give values to $var1$ and $var2$, This bug only happens when the data type is *uint* and is caused by incorrect value range estimation. After developers confirmed this bug and fixed `const_int_bound` analyzer, this numerical computation related bug was fixed.

Incorrect Exception Handling. Bug_{11}, Bug_{12} and Bug_{13} are three bugs of Incorrect Exception Handling. They are detected under disruptive generation. To trigger these bugs, HirGen must generate

Table 2: Confirmed Bugs found by HirGen

Bug ID	Symptom	Root Cause	Test Oracle	Status	Previously Unknown
1	Crash	Incorrect Numerical Computation	$Oracle_1$	Fixed	✓
2	Inconsistency	Incorrect Exception Handling	$Oracle_2$	Confirmed	✓
3	Crash	Incorrect Exception Handling	$Oracle_1$	Fixed	✓
4	Crash	Incorrect Exception Handling	$Oracle_1$	Fixed	
5	Crash	Incorrect Exception Handling	$Oracle_1$	Fixed	✓
6	Inconsistency	Incorrect Exception Handling	$Oracle_2$	Fixed	✓
7	Inconsistency	Type Problem	$Oracle_2$	Fixed	
8	Inconsistency	Type Problem	$Oracle_2$	Fixed	
9	Inconsistency	Internal API Incompatibility	$Oracle_2$	Fixed	✓
10	Inconsistency	Incorrect Exception Handling	$Oracle_2$	Fixed	
11	Crash	Incorrect Exception Handling	$Oracle_1$	Fixed	
12	Crash	Incorrect Exception Handling	$Oracle_1$	Fixed	
13	Crash	Incorrect Exception Handling	$Oracle_1$	Fixed	
14	Crash	Memory Allocation Problem	$Oracle_1$	Confirmed	✓
15	Inconsistency	Incorrect Numerical Computation	$Oracle_3$	Confirmed	✓
16	Inconsistency	Incorrect Numerical Computation	$Oracle_3$	Confirmed	✓
17	Inconsistency	Incorrect Numerical Computation	$Oracle_3$	Confirmed	✓

computational graphs containing obvious breaks of constraints. Take Bug_{11} for example, its corresponding computational graph includes a constant node of type $int16$, a `tan` operator node and the connection between these two nodes. The constant node passes its $int16$ data to the operator node. In this tiny subgraph, HirGen purposely breaks the constraint that `tan` only accepts $float$ data type defined in TVM and receives a segmentation fault during compilation. This is because TVM does not have exception handling for this operator and its unacceptable data types.

Memory Allocation Problem. Bug_{14} is the only bug of root cause, named Memory Allocation Problem. Specifically, when HirGen leverages `relay.shape_of` to infer to tensor shape of variable node with static tensor shape $(1, 2)$, an unexpected crash happens with warning message `Cannot allocate memory symbolic tensor shape [?, ?]`.

$Oracle_2$: Result Inconsistency among original high-level IR, optimized high-level IR and mutated high-level IR. $Oracle_2$ caught a total of six confirmed bugs, and five of them have been fixed. These bugs are caused by three different root causes, including *Incorrect Exception Handling*, *Type Problem* and *Internal API Incompatibility*.

Incorrect Exception Handling. Take Bug_{10} as an example HirGen catches this bug because it finds a high-level IR passes compilation while its optimized version fails. Specifically, HirGen places `FirstOrderGradient` before `FuseOps` in a optimization sequence and detects that TVM cannot successfully handle this optimization sequence. This is because exception handling is too strict. Concretely, TVM performs a traversal on the high-level IR after `FirstOrderGradient` for conducting `FuseOps`. When visiting a constant node, TVM finds this node is not scalar because `FirstOrderGradient` has rewritten this attribute. Therefore, TVM throws an exception and the compilation terminates. However, this check about scalar attribute is too strict and does not consider data type. A fix for this bug completes this exception handling and makes the optimized version successfully passes compilation. Besides, Bug_6 is also a representative, detected by our effort in utilizing IR language features. HirGen takes advantage of first-ciziten functions in Relay IR and tries to return a function in another function. Since TVM v0.9 cannot well support the lowering of this high-level language feature into low-level counterpart, segmentation fault is thrown. The effort in utilizing high-level IR's language features also help us find Bug_5, Bug_7 and Bug_8.

Type Problem. Take Bug_8 for instance. This bug is found with function rewrite mutation. Specifically, after changing a global function f into the local closure of another empty global function g and return f in g, TVM can not infer the type of g. This is because after successfully inferring the type of f, this type information is lost when TVM begins to infer the type of g.

Internal API Incompatibility. Take Bug_9 for example. This bug is detected because `relay.build_module.create_executor('vm')` fails, but compilation in other ways run smoothly. Specifically, after HirGen transforms high-level IR into a A Norm Form. Compilation with virtual machine cannot figure out the bound relation between x_{91} and a global function. However, other compilation ways do not encounter this problem.

$Oracle_3$: Result Inconsistency across hardware devices. $Oracle_3$ caught a total of three confirmed bugs, but none of them has been fixed. This is because difference among computation results on CPU and GPU is caused by platform specific differences. More specifically, LLVM and CUDA has different implementations on the same operator, while TVM lacks full specification about this operator or lacks complete warning message of using this operator. Developers responded with a confirmation of this deficiency but they consider it unnecessary to remedy it without it violating the effectiveness of TVM seriously.

Take Bug_{15} as an example. HirGen creates a simple computational graph containing a `right_shift` operator node. This operator node takes as input two other variable nodes. Subsequently, HirGen first generates the corresponding high-level IR, then compiles the IR with `relay.build` to generate runtime model and finally creates the input and run runtime model on CPU and GPU to get two computation results. When the second variable is larger than the first one, results are inconsistent. This is because this situation incurs a poison value in LLVM and the use of it in an operator is undefined. Though this confirmed bug does not come from poor implementation of TVM but from problems in external compiler, it is still confusing to users when their DL model triggers this inconsistency. The refinement of the exception handling system could be a compromise approach for this ill situation.

5.3 RQ3: Relation between our found bugs and high-level Optimization.

As a DL compiler fuzzer focusing on high-level optimization, HirGen is capable of detecting bugs in high-level optimization or bugs highly related to this stage. In this subsection, we manually study the code patch of each fixed bug detected by HirGen and analyze their relationship with high-level optimization and how the detection of them improve this stage.

Bug_2, Bug_8, Bug_9, Bug_{10} are bugs detected in high-level optimization. Bug-triggered pattern for these four bugs are similar: after high-level optimizations, HirGen detects a violation of $Oracle_2$. These bugs show inability to optimize the structure several high-level optimizations should have optimized, and incompatibility among several optimizations. For instance, Bug_8 shows that after performing `InferType` on one function, the solved types cannot be passed to the next function and thus triggers a type problem. Bug_{10} shows `FuseOp` can not be well performed after performing `FirstOrderGradient`. Fix of these bugs directly improves performance of the optimization and facilitates the possibility of multiple optimization combinations.

Besides, HirGen finds eight bugs with crash symptom and all of them trigger crash during compilation. Except for Bug_{11}, Bug_{12} and Bug_{13}, all other bugs are directly related to high-level optimization. To improve efficiency, TVM calls `OptimizeImpl` during compilation and invokes 11 high-level optimization implicitly. These optimizations work by one or several passes on the high-level IR, which performs rewrite at any optimizable expression. In each pass, all expressions in high-level IR are visited and assertions embedded in TVM check each expression. Bugs in this process may prevent high-level optimizations from being well executed, or even result in a crash to stop the optimization. Fix for these bugs are actually fix for required IR passes needed by high-level optimizations.

Although our approach is proposed for high-level optimization, the test cases generated by our approach can also execute the low-level optimization and deployable code generation. Thus, it has the side effect of testing the other stages. And the results also confirm it. Bug_{15}, Bug_{16} and Bug_{17} are all related to low-level part and backend of TVM. They are detected due to inconsistent calculation results on different backends (LLVM and CUDA) given the same inputs. These bugs show the need to better couple TVM with these backends.

5.4 RQ4: Contribution of Disruptive Generation

During experiments, we have generated 170 computational graphs with different bug-triggering combinations of operator, data type and tensor shape. All these graphs can incur crash of TVM with only "segmentation fault" information, showing the deficiency of exception handling ability. In the latest TVM version, all these bugs have been fixed. All these obvious breaks of constraints trigger crash with detailed bug information now. By comparing the bug information of the latest TVM, we found there are three bugs in total found by these 170 graphs.

5.5 RQ5: Contribution of Coverage-guided generation to The Diversity of Graph

To generate diverse computational graphs with various data types, tensor shapes and operators, we design three coverage criteria. To answer this RQ, We implement a simplified version of HirGen, saying HirGen$_r$. HirGen$_r$ is identical to HirGen except that HirGen$_r$ is not guided to generate computational graphs, but generate graphs randomly. We have conducted two experiments for comparison between these two techniques.

The first experiment is about the bug detection ability of HirGen and HirGen$_r$ under strict generation mode. In this experiment, we executed these two techniques for two days separately and collect all failing tests. HirGen found 11 bugs out of 24 failing tests, while HirGen$_r$ found 8 bugs out of 37 failing tests. This result shows that 1) HirGen has better bug detection ability than HirGen$_r$, and 2) with coverage-guided generation, HirGen can avoid triggering duplicate failure and focus on finding new bugs.

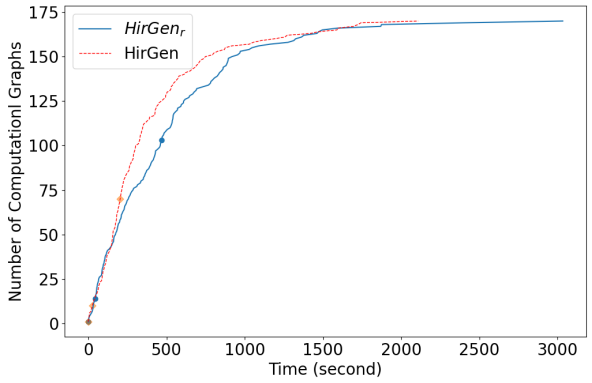


Figure 4: HirGen *vs.* HirGen$_r$ under Disruptive Generation

The second experiment is similar to the second one. In this experiment, we compare the bug detection ability of HirGen and HirGen$_r$ under disruptive generation mode. Since disruptive generation promises that each insertion contains a violation of constraints and must trigger failure, there is no need to generate multiple-operator graph. Therefore, we utilize these two techniques to generate computational graphs that contain only one operator. Figure 4 presents the experiment results. HirGen and HirGen$_r$ both generated 170 bug-triggered computational graphs, each of which contains unique tuple of (*operator*, *tensor shape*, *data type*). In this

figure, HirGen shows more exploratory nature in diversity of graph and thus detects bugs faster. Besides, two techniques both found 3 bugs using these 170 graphs. And the timestamps of bug detection are also marked in this figure, showing that HirGen found bugs faster than HirGen$_r$.

These two experiments show that coverage-guided generation help HirGen become more exploratory in the diversity of computational graphs. Therefore, HirGen can detect more bugs and find them in faster speed.

6 THREATS TO VALIDITY

The *internal* threat validity mainly lies in the implementation of HirGen. To reduce this threat, two authors of this paper have carefully checked and tested the functionality of all components of HirGen.

The *external* threat validity mainly lies in the DL compiler we chose in our study. Until now, TVM is one of the most popular and active open-source DL compilers, with 8K stars in Github. Though HirGen now mainly supports converting its generated computational graph into high-level IR of TVM with Relay. The technical approach of it is also useful for testing other DL compilers with the help of ONNX[20]. And we also have one experimental version to support ONNX. ONNX is an open format to represent diverse DL models defined by various DL frameworks and is supported by currectly popular DL compilers. Similar to Relay, we can use ONNX's APIs to easily convert a computational graph into high-level IR of ONNX. This IR is transformable to high-level IRs of existing DL compilers. And more support for ONNX to test more DL compilers is also our future work.

The *construct* threat mainly lies in randomness. In computational graph generation, though with coverage guidance, the selection of operator and connection also involves randomness. To alleviate the negative impact of construct threat, we 1) conducted bug detection ability comparison experiment for a sufficient time, and 2) conducted the first and the third experiment in section 5.5 for 10 times to assure the stability of the experimental results.

7 RELATED WORK

HirGen is a generation-based fuzzer for DL compiler testing. In this section, we introduce two categories of related work in this section, including generation-based fuzzing and DL compiler testing.

Generation-based Fuzzing. Generation-based fuzzing is a class of common fuzzing techniques [24–28]. Different from mutation-based fuzzing that mutates existing seed inputs to create new test inputs, generation-based fuzzing constructs new inputs from scratch according to some pre-defined grammar models. Since generation-based fuzzing does not rely on the seed inputs, it may cover more diverse input space that is not covered by the seed inputs and trigger more code logic of the program under test[29, 30].

Generation-based fuzzing has been widely used in many domains, such as C compilers [28] and so on [25–27, 31]. However, these techniques cannot be directed adopted to test DL compilers due to its characteristics. To our best knowledge, TVMFuzz[12] is the first generation-based technique to fuzzing low-level IR and low-level optimization of TVM. However, this open-source fuzzer can not cover high-level optimization and thus is incapable of detecting bugs in this most bug-prone stage. Different from TVMFuzz, HirGen is able to generate complicated and valid computational graphs independently from scratch to cover high-level optimization stage. This work is also achievable in different approaches by other generation-based fuzzers, such as GraphFuzzer [23] for inference engine and NNSmith for DL compilers [14]. To distinguish from these techniques, HirGen also utilizes IR language features and generates diverse high-level IRs. In this way, HirGen can effectively detect bugs related to high-level optimization.

DL Compiler Testing. With the development of DL compiler, the importance of DL compiler testing has been noticed by more and more researchers. To our best knowledge, existing DL compiler testing technique can be divided into two categories according to their testing focus. MT-DLComp [13] aims at testing the whole workflow of four DL compilers, including TVM, Glow, NNFusion and Tensorflow XLA. This technique performs mutation on existing DL models and involves three test oracles from the spirit of metamorphic testing. During testing, it treats all tested Compilers as a black box and test if DL compilers corrupt the predictive capability of DL models. NNSmith [14] is also of this category. It generates computational graphs and their inputs from scratch and use them to fuzz the whole DL compilers. These two technique can find prediction difference related bugs and NNSmith is also able to detect other problems, such as data layout problem, poor support for type match, etc. Different from MT-DLComp and NNSmith, several other techniques[8, 11, 12] focus on the testing of single stage but not the whole workflow. Besides, they perform white-box testing to utilize knowledge gained from codebase to achieve more efficient and effective testing results. For instance, TZER[11] collects low-level IR passes and mutates them to focus on bug detection in low-level optimizations, while the above-mentioned TVMfuzz focuses on high-level optimization with generation-based approaches. Similar to these techniques, HirGen also focuses on single stage: high-level optimization. This stage is the most vulnerable to bugs and has not been systematically studied by previous literature. HirGen is therefore proposed to fill this gap.

8 CONCLUSION

High-level optimization is the most bug-prone stage in the workflow of DL compilers. However, there is no systematic study on testing this stage. To fill this gap, we offer HirGen, a generation-based fuzzer with effective computational graph generation approach and three test oracles. Different from existing works, HirGen can explore more complicated and valid high-level IR and thus detect deeper bugs. Besides, three test oracles in HirGen also improve its capability of detecting bugs of various root causes. In total, HirGen has detected 21 bugs, of which 17 have been confirmed and 12 have been fixed. Our effort has been recognized by TVM community and improved the robustness and functional correctness of high-level optimization.

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