浙江大学 2011～2012 学年 春夏 学期

《 计算机组成 》课程期末考试试卷（A）

课程号： 21186031 ，开课学院：计算机学院/软件学院　　任课老师:

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式： 闭 卷，允许带 一页 A4 纸手写笔记 入场，笔记署名，不得互借
交卷方式： 试卷名字朝外对折整齐，草稿纸、笔记与试卷一起上交 。
考试日期： 2012 年 06 月 18 日(10:30～12:30) ，考试时间： 120 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____ 学号：_____ 所属院系：_____

题序	一.10	二.20	三.25	四.30	五.15	总 分.100
得分						
评卷人						

I. True or False(10x1%; √/×)

eg.	1	2	3	4	5	6	7	8	9	10
√										

eg: TLB: translation-lookaside buffer

1、 Good design demands no compromise ×

2、 callee-saved register: A register saved by the routine making a procedure call. ×

3、 pseudoinstruction: A common variation of assembly language instructions often treated as if it were an instruction in its own right. √

4、 **biased notation**: A notation that represents the most negative value by 00……00two and the most positive value by 11……11two, with 0 typically having the value 10……00two, thereby biasing the number such that the number plus the bias has a nonnegative representation. √

5、 write-through: A scheme that handles writes by updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced. ×

6、 SRAM needs be refreshed periodically. ×

7、 The ability to share functional units within the execution of a single instruction is the only advantage of a multicycle design. ×

8、 In virtual memory, the number of entries of a page table is equals to the physical page number. ×

9、 asynchronous bus: A bus that uses a handshaking protocol for coordinating usage rather than a clock; can accommodate a wide variety of devices of differing speeds. √

10、 The advantage of polling is that it can save a lot of processor time. ×

II. Choose 1 best answer. (10x2%)

eg.	1	2	3	4	5	6	7	8	9	10
C	C	C	B	C	D	B	C	A	B	C

eg. 1KB means (____) bytes。
A: 1 B: 1000 C: 1024 D: 1024*1024

1、 Today's computers are built on 2 key principles: (____)
①Instruction are represented as numbers.
②Programs can be stored in memory to be read or written just like numbers.
③Make the common case fast.
④Every instruction can be conditionally executed.
A: ①③ B: ②④ C: ①② D: ③④

2、 According to the IEEE754 single precision, (____) is -∞.
A: 0xFF00_0000 B: 0xFF100_0000
C: 0xFF80_0000 D: 0xFFFFF_FFFF

3、 Memory (____) needs be refreshed periodically.
A: SRAM B: DRAM C: EPROM D: FLASH

4、 Increasing associativity can reduce (____).
A: Compulsory misses(cold-start misses)
B: Capacity misses
C: Conflict misses(collision misses)
D: All three misses

5、 Assume an 8Kx8bits memory is composed of 2Kx4bit chips. The first address of the chip which contains the address 0B1FH is (____).
A: 0000h B: 0600h C: 0700h D: 0800h

6、 For a virtual memory with TLB, which of following will be run first during memory access? (____)
A: test cache hit B: test TLB hit
C: test physical memory hit D: test dirty bit

7、 Consider a virtual memory system with 32-bit virtual byte address, 4KB/page, 32 bits each entry. The physical memory is 512MB. Then, the total size of page table needs (____).
A: 1MB B: about 3MB C: 4MB D: 8MB

8、 Which of the following I/O mechanisms requires the least hardware support?
A: Polling B: Interrupt C: DMA
D: All the above don't require hardware support at all

9、 (____) is not a BUS.
A: PCI B: CPI C: ISA D: SCSI

10、 The major disadvantage of a bus is (____).
A: versatility B: Low cost
C: To create a communication bottleneck
D: Slower data access

III. (25%):

1) (10%) Put the corresponding letters for each 32-bit value in order from least to greatest.
(**Hint:** the question isn't asking you to write down what each one is, it only asks for the relative order!)

A: 0xFF000000 (IEEE754 single precision)
B: 0xFF000000 (2's complement)
C: 0xFF000000 (sign-magnitude)
D: 0xFF000000 (biased notation移码)
E: 0xF0000000 (2's complement)
F: 0xF0000000 (1's complement)

Least←	**A**	**F**	**C**	**E**	**B**	**D**	→Greatest

2) (15%): Suppose **float** $s1>$s0>0; $s3=0xFF000000, $s4=0x00800000. Try to do the MIPS programming for making:

$s2 = $s1 + $s0.

```
        OR    $S5,$S4,$S3 ;0xFF80_0000
        NOR   $S6,$S5,$S5 ;0x007F_FFFF
        AND   $T1,$S1,$S5 ;e1
        AND   $T0,$S0,$S5 ;e0
        AND   $T3,$S1,$S6 ;
        OR    $T3,$T3,$S4 ;M1
        AND   $T2,$S0,$S6 ;
        OR    $T2,$T2,$S4 ;M0
```

```
R1:     SLT   $T4,$$T0,$T1
        BEQ   $T4,$ZERO,R2
        SRL   $T2,$T2,1    ;->
        ADD   $T0,$T0,$S4
        J     R1
R2:     ADD   $T3,$T3,$T2 ;+
R3:     AND   $T4,$T3,$S3
        BEQ   $T4,$ZERO,R4
        SRL   $T3,$T3,1
        ADD   $T1,$T1,$S4
        J     R3:
R4:     AND   $T3,$T3,$S6
        ADD   $S2,$T1,$T3
#
```

IV、(30%): Memory

1) (15%): Consider a memory system with the following properties:

	R/W time	**Size**
Cache	2ns	256KB
DRAM	20ns	4GB
Disk	20ms	400GB

We use TAG at Cache and Page Table in virtual memory for data addressing. Try to make a quantitative analysis(定量分析) for the questions:

1. Why does Cache and Virtual take different way? Shell we use Page-Table (Block-Table) for Cache?
2. Why don't use direct-mapping or set-associative in virtual memory?

1、设：16B/Block
Block table = (4G/16) * (log(256K/16)+1) /8 = 256M*15/8 = 120MB
2、全相联可提高命中率。

2)(15%) 1G main memory, byte-addressing, 128KB Cache. Now a data locate at **0x123456**(byte-addressing), will mapping to which cache unit in different situation below, and how about its TAG and Total cache size?

0x123456	**The data will Mapping to (*block(s)*)**	**TAG**		**Tatal Size**
		TAG for the data(Hex)	bits	
Direct-mapped, 16 bytes/block	0x345	0x9	15	(15+1)*8K/8+ 128K=144KB
Direct-mapped, 64 bytes/block	0xD1	0x9	15	(15+1)*2K/8+ 128K=132KB
2-Way set associative 16 bytes/block	0x345 *2+0,+1	0x12	16	(16+1)*8K/8+ 128K=145KB
4-Way set associative 32 bytes/block	0x1A2 *4+0,+1,+2,+3	0x24	17	(17+1)*4K/8+ 128K=137KB

V、(15%)Design: Multicycle CPU implementation

MIPS is a register-register architecture, where arithmetic source and destinations must be registers. But let's say we wanted to add a register-memory instruction to the multicycle datapath:

Addm rd, rs, rt # rd = rs + Mem[rt]

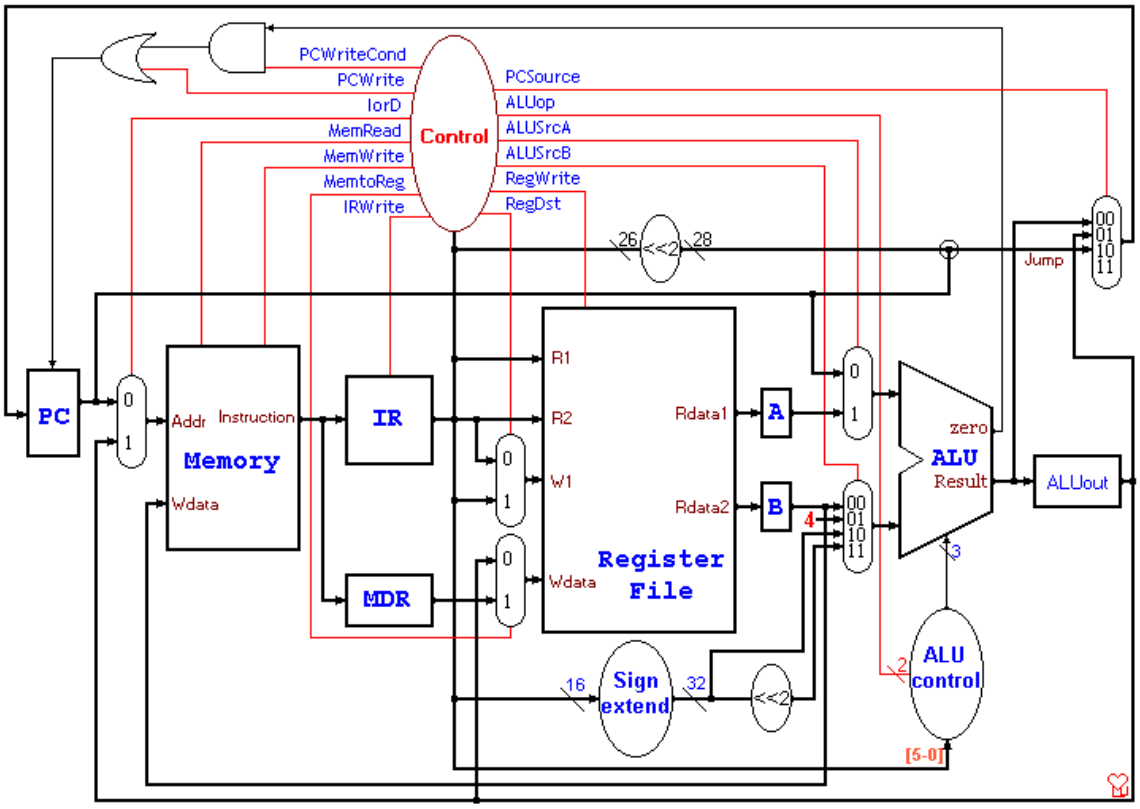
1.(3%)Machine code in Binary;

1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
OpCode																															
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

2.(4%) show what changes are needed to support addm in the multicycle datapath.

3.(8%) Complete this finite state machine diagram for the addm instruction. Be sure to include any new control signals you may have added.

0、	1、	2、
3、	4、	5、


PCWriteCond
PCWrite
IorD
MemRead
MemWrite
MemtoReg
IRWrite
Control
PCSource
ALUop
ALUSrcA
ALUSrcB
RegWrite
RegDst
26
<<2
28
Jump
00
01
10
11
PC
0
1
Addr
Instruction
Memory
Wdata
IR
MDR
R1
R2
W1
Wdata
Register
File
Rdata1
Rdata2
A
B
4
zero
ALU
Result
ALUout
3
2
ALU
control
[5-0]
16
Sign
extend
32
<<2