RISC-V-Compile

PCSource PCWR IF/ID EX/MEM

Braken

Jump/Jal_Target

Branch_Target ID/EX MEM/WB ID_PCurrent WB_PCurrent ID_IR WB_IR WB_RegWrite MEM_RegWrite EX_RegWrite RegWrite WB_DatatoReg DatatoReg MEM_DatatoReg EX_DatatoReg ID_PCurrent EX_Jump/Jal Jump/Jal [⊥]MEM_Jump/Jal Branch_Target Branch Main EX_Branch MEM_Branch Jump/Jal_Target● EX_WR MEM_WR EX_MIO MIO decoder → MEM_MIO EX_ALUC ImmSel → EX_ALUS cr_A ALUScr_B EX_ALUScr_B MEM_Target WB RegWrite MEM/WB Latcher WB_Dat atoReg Rom_addr rs1=ID_IR [19:15] MWR MEM_ALUO WB_ALUQ Rs_addr_A WB_MDR Rt_addr_B rdata_A Instruction WE rs1_data Memory MEM_zero EX_ALUO MEM_ALUO **Registers** Ram_addr Rom_out rd=ID_IR [11-7] Wt_addr rdata_B EX_B Result Data Memory Data_ir Data_out Din **Dout** Wt_data EX_B MEM_Datao clk • EX_rd rd_addr clkImmSel Imm32 WB_rd MEM_rd **CPU ID_IR** [31:20][19:12][11:7] WB_WData flush reserve (Data Hazard)

EXE_Stage

MEM_Stage

WB_Stage

ID_Stage

IF_Stage