浙江大学

# 本科实验报告

课程名称：计算机组成

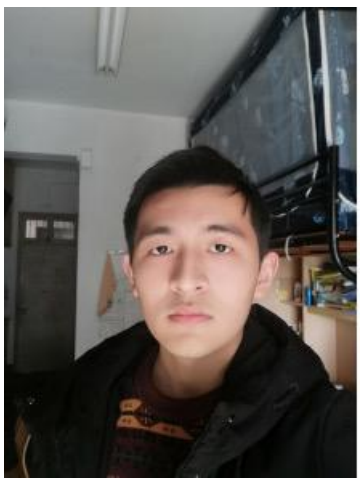
姓　　名：黄海烽

学　　院：计算机科学与技术学院

专　　业：计算机科学与技术

学　　号：3180102339

生活照：



指导教师：洪奇军

2020 年 3 月 22 日

**实验三--IP 核集成 SOC 设计——建立 CPU 调试、测试和应用环境实验报告**

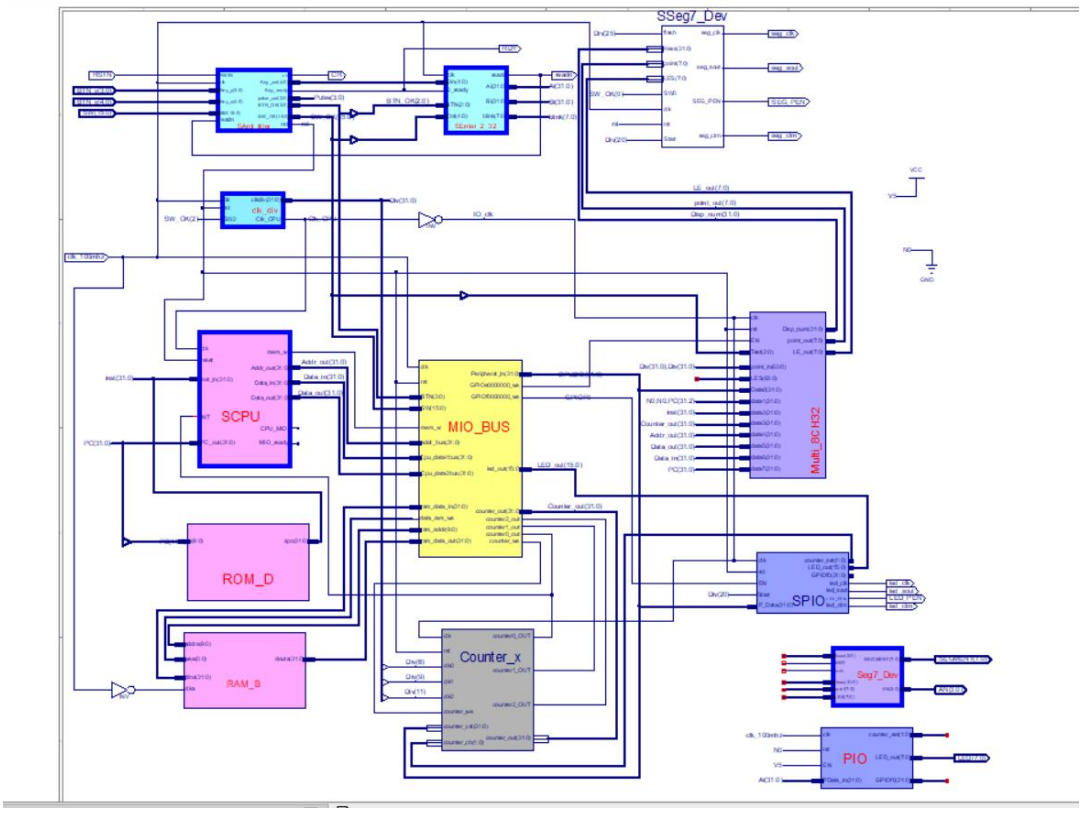
姓名：黄海烽　　学号：3180102339　　专业：计算机科学与技术

课程名称：计算机组成　　同组学生姓名：无

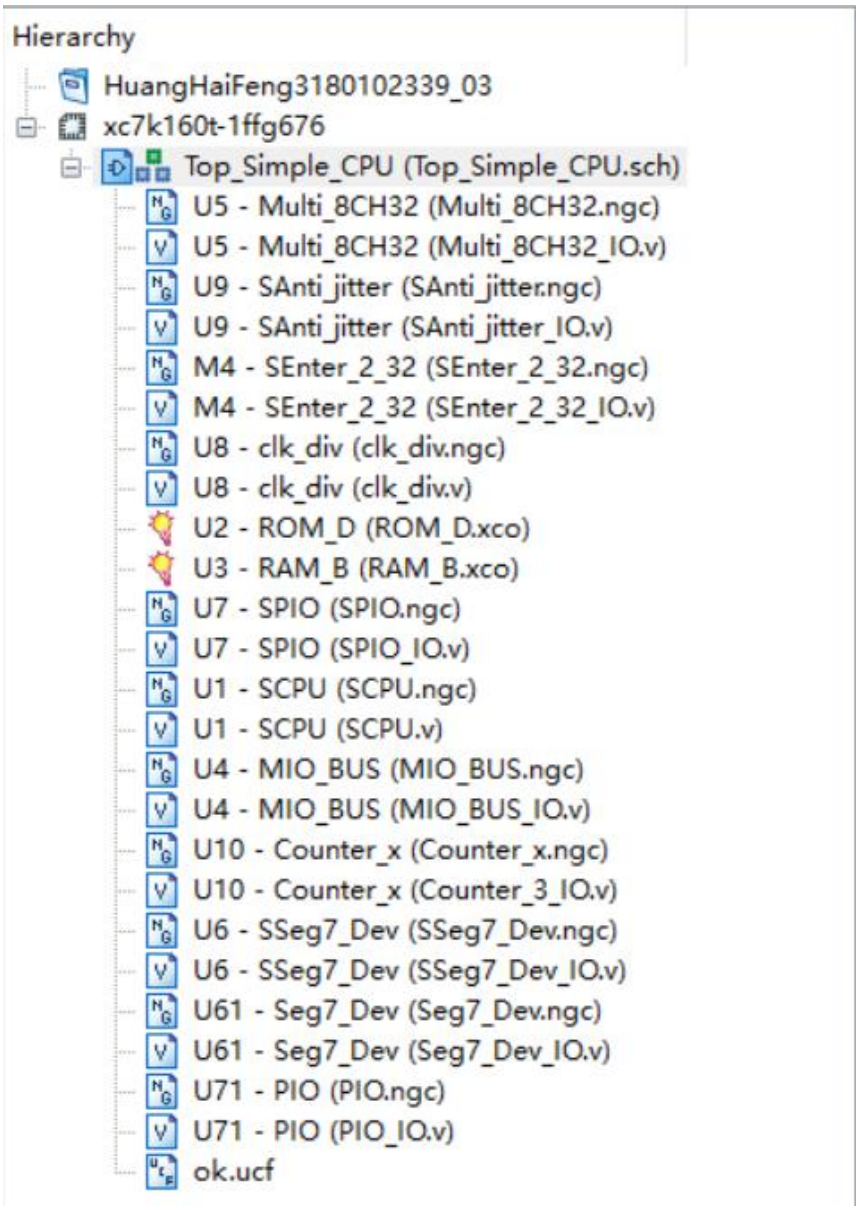
实验时间：2020-03-22　　实验地点：家　　指导老师：洪奇军

# 一、操作方法与实验步骤

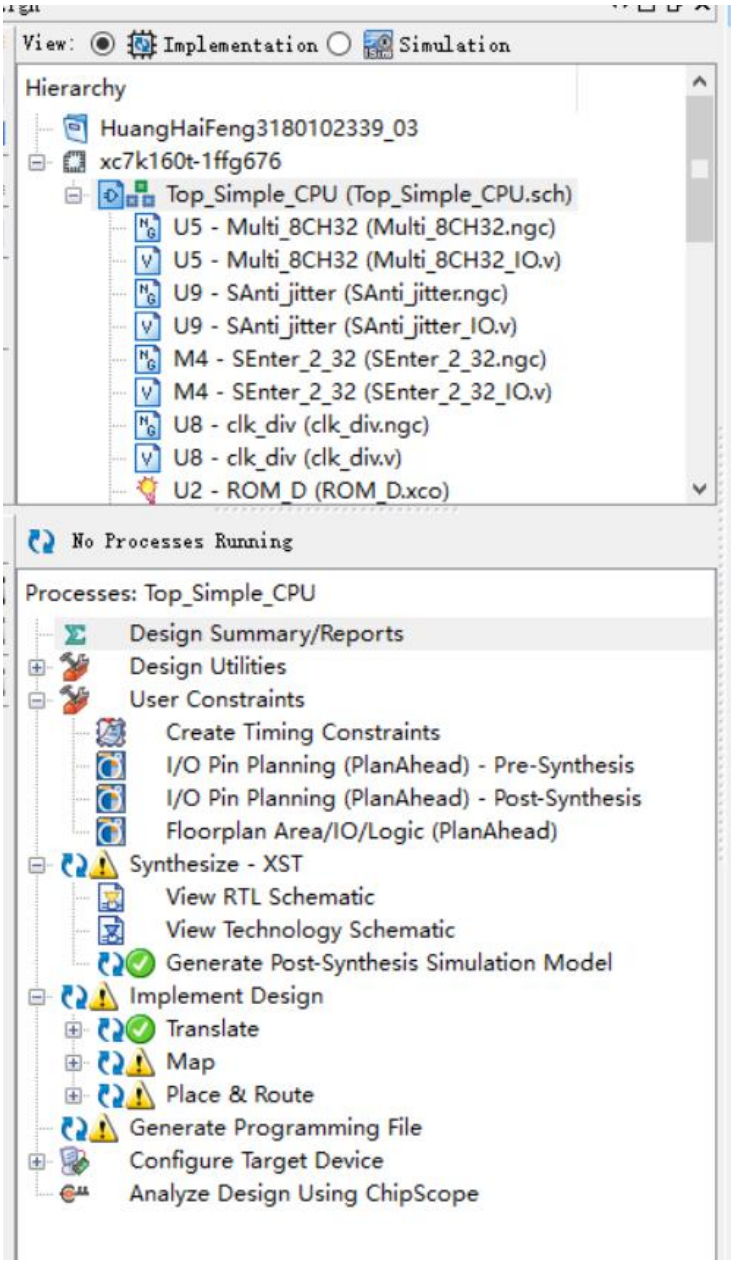
1. 顶层模块：




顶层电路图


Hierarchy
HuangHaiFeng3180102339_03
xc7k160t-1ffg676
Top_Simple_CPU (Top_Simple_CPU.sch)
U5 - Multi_8CH32 (Multi_8CH32.ngc)
U5 - Multi_8CH32 (Multi_8CH32_IO.v)
U9 - SAnti_jitter (SAnti_jitter.ngc)
U9 - SAnti_jitter (SAnti_jitter_IO.v)
M4 - SEnter_2_32 (SEnter_2_32.ngc)
M4 - SEnter_2_32 (SEnter_2_32_IO.v)
U8 - clk_div (clk_div.ngc)
U8 - clk_div (clk_div.v)
U2 - ROM_D (ROM_D.xco)
U3 - RAM_B (RAM_B.xco)
U7 - SPIO (SPIO.ngc)
U7 - SPIO (SPIO_IO.v)
U1 - SCPU (SCPU.ngc)
U1 - SCPU (SCPU.v)
U4 - MIO_BUS (MIO_BUS.ngc)
U4 - MIO_BUS (MIO_BUS_IO.v)
U10 - Counter_x (Counter_x.ngc)
U10 - Counter_x (Counter_3_IO.v)
U6 - SSeg7_Dev (SSeg7_Dev.ngc)
U6 - SSeg7_Dev (SSeg7_Dev_IO.v)
U61 - Seg7_Dev (Seg7_Dev.ngc)
U61 - Seg7_Dev (Seg7_Dev_IO.v)
U71 - PIO (PIO.ngc)
U71 - PIO (PIO_IO.v)
ok.ucf

工程目录




Design 窗口运行成功

## 2.引脚约束说明：

```
NET "clk_100mhz"              LOC = AC18      | IOSTANDARD = LVCMOS18 ;
NET "RSTN"                    LOC = W13       | IOSTANDARD = LVCMOS18 ;
NET "clk_100mhz"              TNM_NET = TM_CLK ;
TIMESPEC TS_CLK_100M      = PERIOD "TM_CLK"       10 ns HIGH 50%;

NET "led_clk"           LOC = N26       | IOSTANDARD = LVCMOS33 ;
NET "led_clrn"          LOC = N24       | IOSTANDARD = LVCMOS33 ;
NET "led_sout"          LOC = M26       | IOSTANDARD = LVCMOS33 ;
NET "LED_PEN"           LOC = P18       | IOSTANDARD = LVCMOS33 ;

NET "seg_clk"           LOC = M24       | IOSTANDARD = LVCMOS33 ;
NET "seg_clrn"          LOC = M20       | IOSTANDARD = LVCMOS33 ;
NET "seg_sout"          LOC = L24       | IOSTANDARD = LVCMOS33 ;
NET "SEG_PEN"           LOC = R18       | IOSTANDARD = LVCMOS33 ;

NET "RDY"         LOC = U21       | IOSTANDARD = LVCMOS33 ;
NET "readn"       LOC = U22       | IOSTANDARD = LVCMOS33 ;
NET "CR"          LOC = V22       | IOSTANDARD = LVCMOS33 ;
#NET "tri_led1_r_n"        LOC = U24       | IOSTANDARD = LVCMOS18 ;
#NET "tri_led1_g_n"        LOC = U25       | IOSTANDARD = LVCMOS18 ;
#NET "tri_led1_b_n"        LOC = V23       | IOSTANDARD = LVCMOS18 ;

NET "BTN_x[0]"          LOC = V17       | IOSTANDARD = LVCMOS18 ;
NET "BTN_x[1]"          LOC = W18       | IOSTANDARD = LVCMOS18 ;
NET "BTN_x[2]"          LOC = W19       | IOSTANDARD = LVCMOS18 ;
NET "BTN_x[3]"          LOC = W15       | IOSTANDARD = LVCMOS18 ;
NET "BTN_x[4]"          LOC = W16       | IOSTANDARD = LVCMOS18 ;



NET "BTN_y[0]"          LOC = V18       | IOSTANDARD = LVCMOS18 ;
NET "BTN_y[1]"          LOC = V19       | IOSTANDARD = LVCMOS18 ;
NET "BTN_y[2]"          LOC = V14       | IOSTANDARD = LVCMOS18 ;
NET "BTN_y[3]"          LOC = W14       | IOSTANDARD = LVCMOS18 ;

NET "SW[0]"          LOC = AA10      | IOSTANDARD = LVCMOS15 ;
NET "SW[1]"          LOC = AB10      | IOSTANDARD = LVCMOS15 ;
NET "SW[2]"          LOC = AA13      | IOSTANDARD = LVCMOS15 ;
NET "SW[3]"          LOC = AA12      | IOSTANDARD = LVCMOS15 ;
NET "SW[4]"          LOC = Y13       | IOSTANDARD = LVCMOS15 ;
NET "SW[5]"          LOC = Y12       | IOSTANDARD = LVCMOS15 ;
NET "SW[6]"          LOC = AD11      | IOSTANDARD = LVCMOS15 ;
NET "SW[7]"          LOC = AD10      | IOSTANDARD = LVCMOS15 ;
NET "SW[8]"          LOC = AE10      | IOSTANDARD = LVCMOS15 ;
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NET "SW[9]"          LOC = AE12      | IOSTANDARD = LVCMOS15 ;
NET "SW[10]"         LOC = AF12      | IOSTANDARD = LVCMOS15 ;
NET "SW[11]"         LOC = AE8       | IOSTANDARD = LVCMOS15 ;
NET "SW[12]"         LOC = AF8       | IOSTANDARD = LVCMOS15 ;
NET "SW[13]"         LOC = AE13      | IOSTANDARD = LVCMOS15 ;
NET "SW[14]"         LOC = AF13      | IOSTANDARD = LVCMOS15 ;
NET "SW[15]"         LOC = AF10      | IOSTANDARD = LVCMOS15 ;


#AxDUNIO-IO
NET "Busser"         LOC = AF24      | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[0]"     LOC = AB22      | IOSTANDARD = LVCMOS33 ;#a
NET "SEGMENT[1]"     LOC = AD24      | IOSTANDARD = LVCMOS33 ;#b
NET "SEGMENT[2]"     LOC = AD23      | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[3]"     LOC = Y21       | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[4]"     LOC = W20       | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[5]"     LOC = AC24      | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[6]"     LOC = AC23      | IOSTANDARD = LVCMOS33 ;#g
NET "SEGMENT[7]"     LOC = AA22      | IOSTANDARD = LVCMOS33 ;#point

NET "AN[0]"          LOC = AD21      | IOSTANDARD = LVCMOS33 ;
NET "AN[1]"          LOC = AC21      | IOSTANDARD = LVCMOS33 ;
NET "AN[2]"          LOC = AB21      | IOSTANDARD = LVCMOS33 ;
NET "AN[3]"          LOC = AC22      | IOSTANDARD = LVCMOS33 ;

NET "LED[0]"         LOC = AB26      | IOSTANDARD = LVCMOS33 ;
NET "LED[1]"         LOC = W24       | IOSTANDARD = LVCMOS33 ;
NET "LED[2]"         LOC = W23       | IOSTANDARD = LVCMOS33 ;
NET "LED[3]"         LOC = AB25      | IOSTANDARD = LVCMOS33 ;
NET "LED[4]"         LOC = AA25      | IOSTANDARD = LVCMOS33 ;
NET "LED[5]"         LOC = W21       | IOSTANDARD = LVCMOS33 ;
NET "LED[6]"         LOC = V21       | IOSTANDARD = LVCMOS33 ;
NET "LED[7]"         LOC = W26       | IOSTANDARD = LVCMOS33 ;
```

# 三、讨论、心得

这次实验总体来说较为简单，有了实验 1 的经验，这次画电路图感觉更加熟练了，不过这次虽然在画电路的过程中没有出错，但在 translate 的时候还是出现了一些 error，搜索了一些资料后发现，这些 error 是因为实验 2 里的两个模块设

计存在的一些问题所导致的，于是先回去将实验 2 的 bug 修完，才最终解决了这个问题。

在还未下载到 SWORD 板上进行验证的情况下，确实还存在很多被我们忽视的问题，所以现在虽然做完实验但心里还是有些许忐忑，希望能早日回到学校，在实验室里解决掉这些问题。