浙江大学

本科实验报告

课程名称: 计算机组成

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生活照:

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2020 年 3 月 13 日

实验三——IP 核集成 SOC 设计，建立 CPU 调试、测试和应用环境简单实验报告

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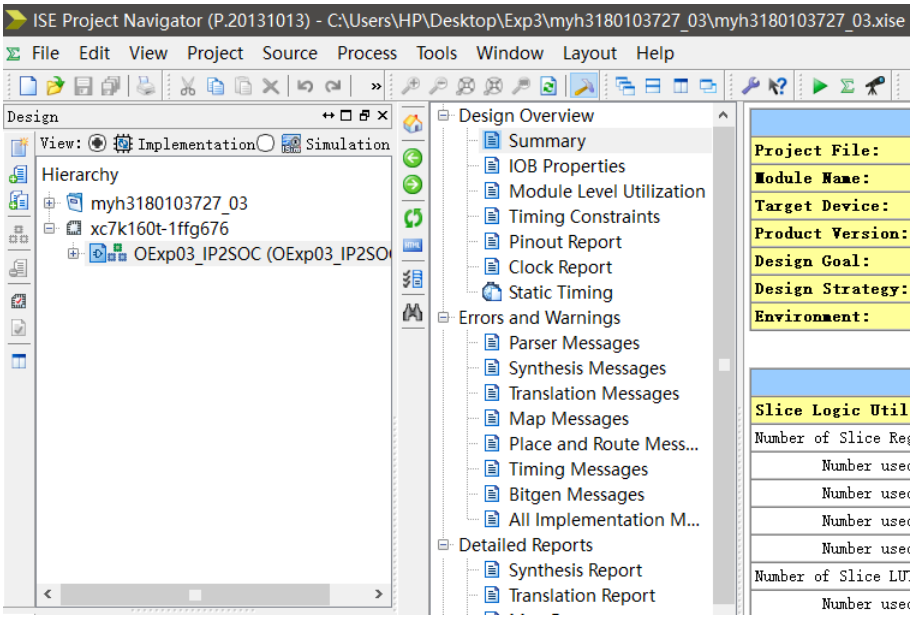
课程名称：计算机组成　同组学生姓名：无

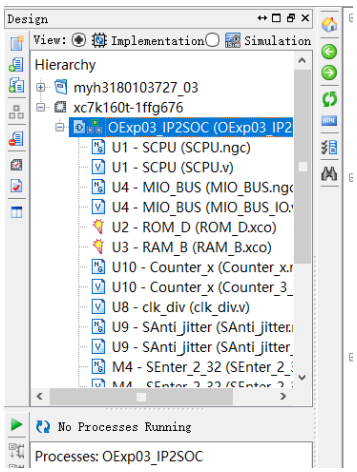
实验时间：2020.3.13　实验地点：　指导老师：洪奇军

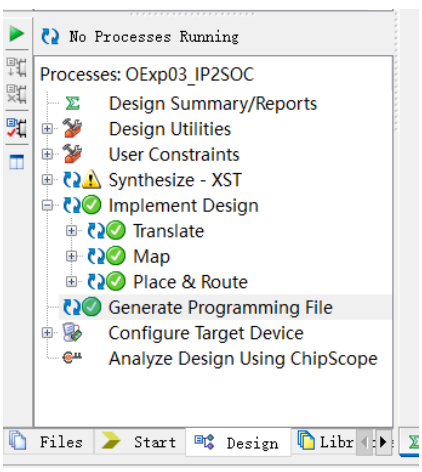
一、操作方法与实验步骤

工程名



Design 窗口运行成功详细说明





实验任务：建立 SOC 应用工程

1 新建工程 myh3180103727_03.xise。

2 添加第三方 IP 核 CPU（U1）,总线（U4）,开关去抖模块（U9）,数据输入模块（M4）, PIO（U71）。

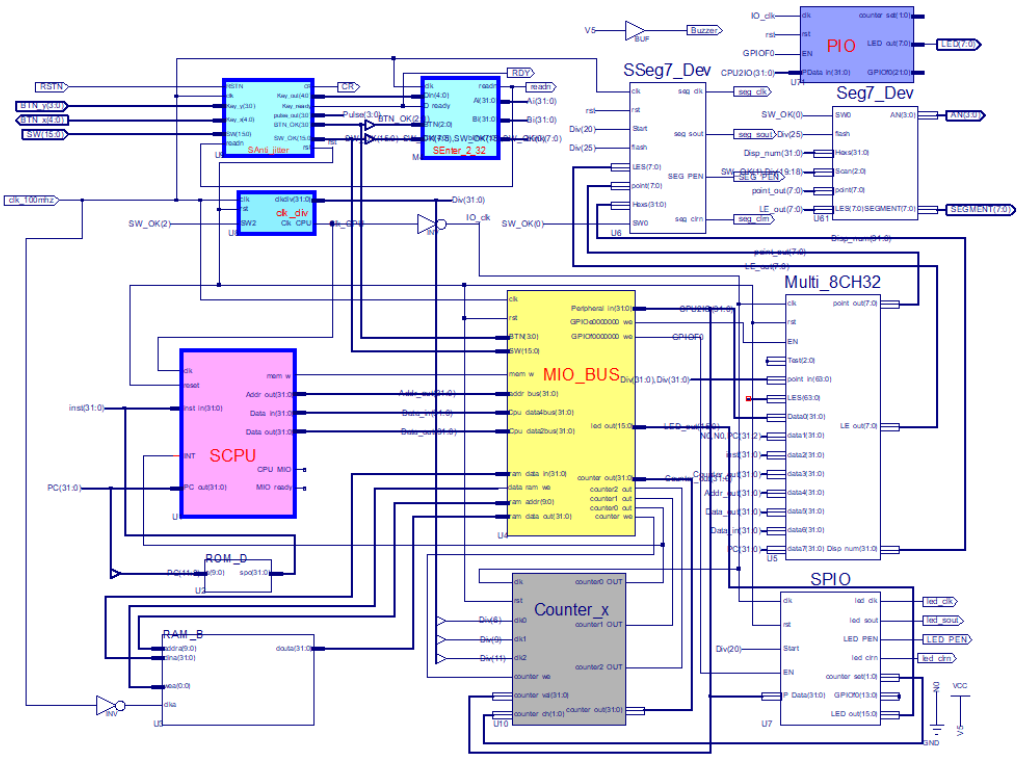
3 添加实验一、二中自己设计的模块：八数据通路模块（U5），七段显示模块（U6），LED 显示模块（U7），Arduino 七段显示模块（U61）。

4 添加通用分频模块 clk_div（U8）。

5 构建 ROM（U2），RAM（U3）IP 核，使用提供的 coe 文件。

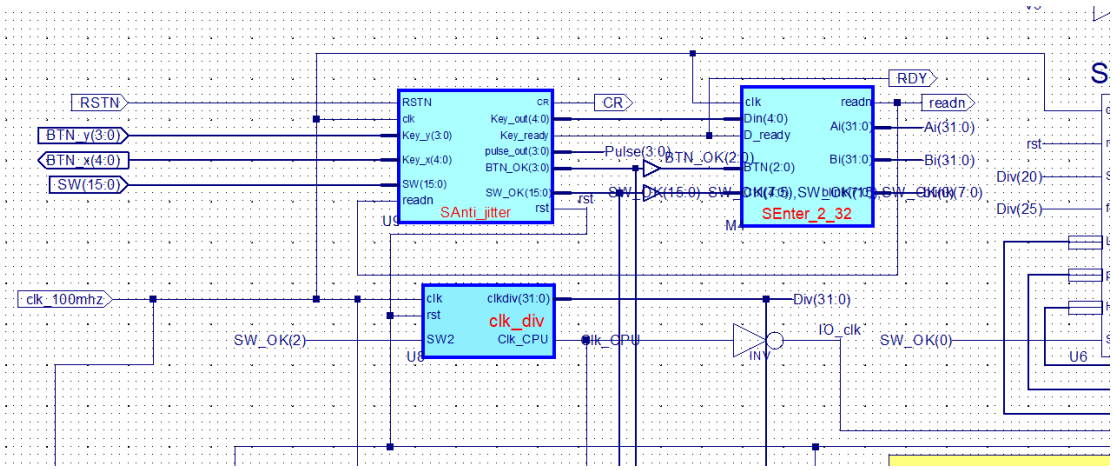
6 新建顶层模块文件 OExp03_IP2SOC.sch。绘制原理图

原理图全貌

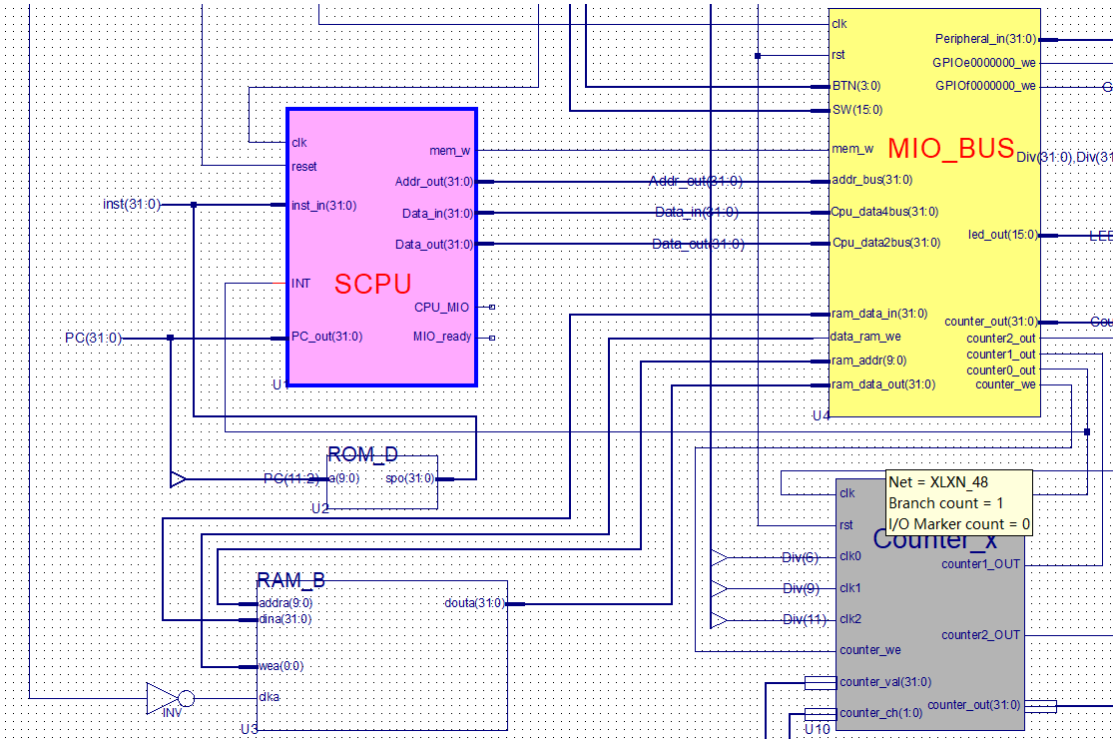


细节展示

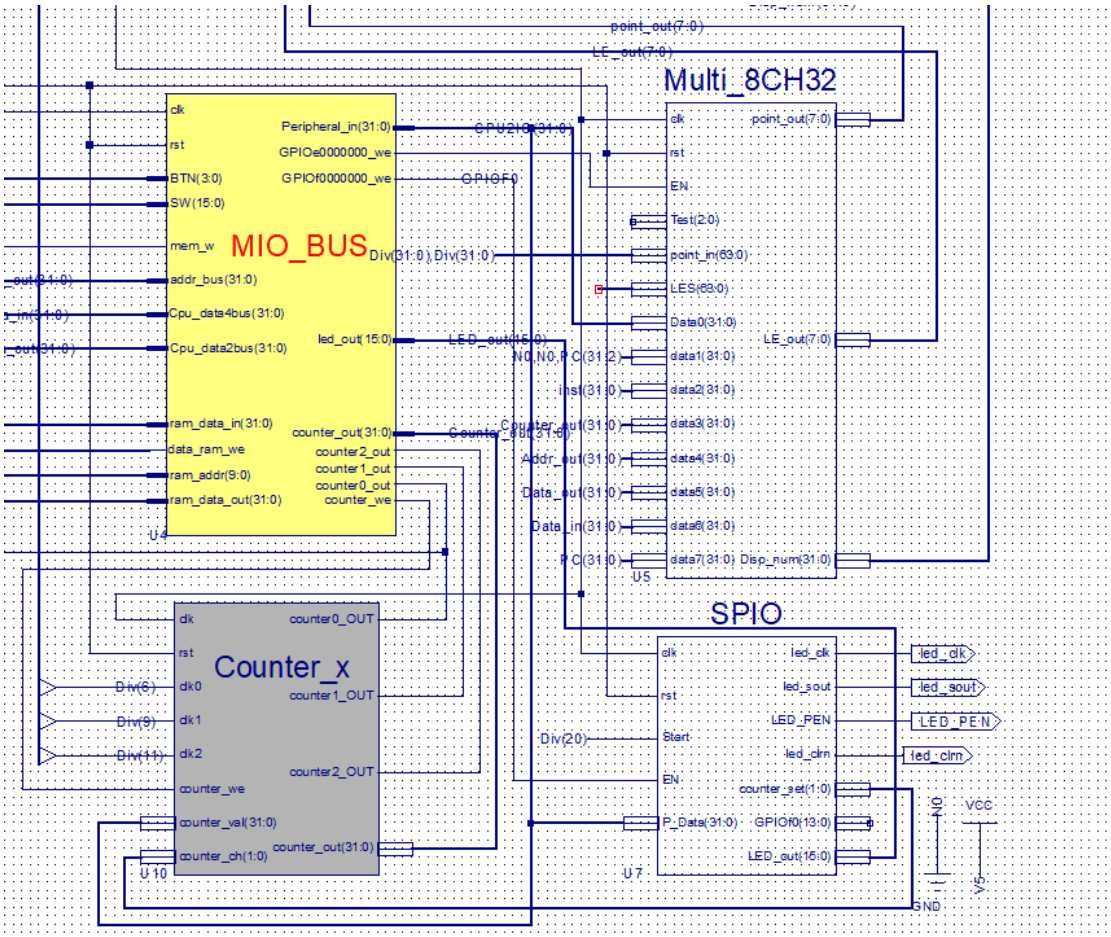
数据输入部分及时钟模块



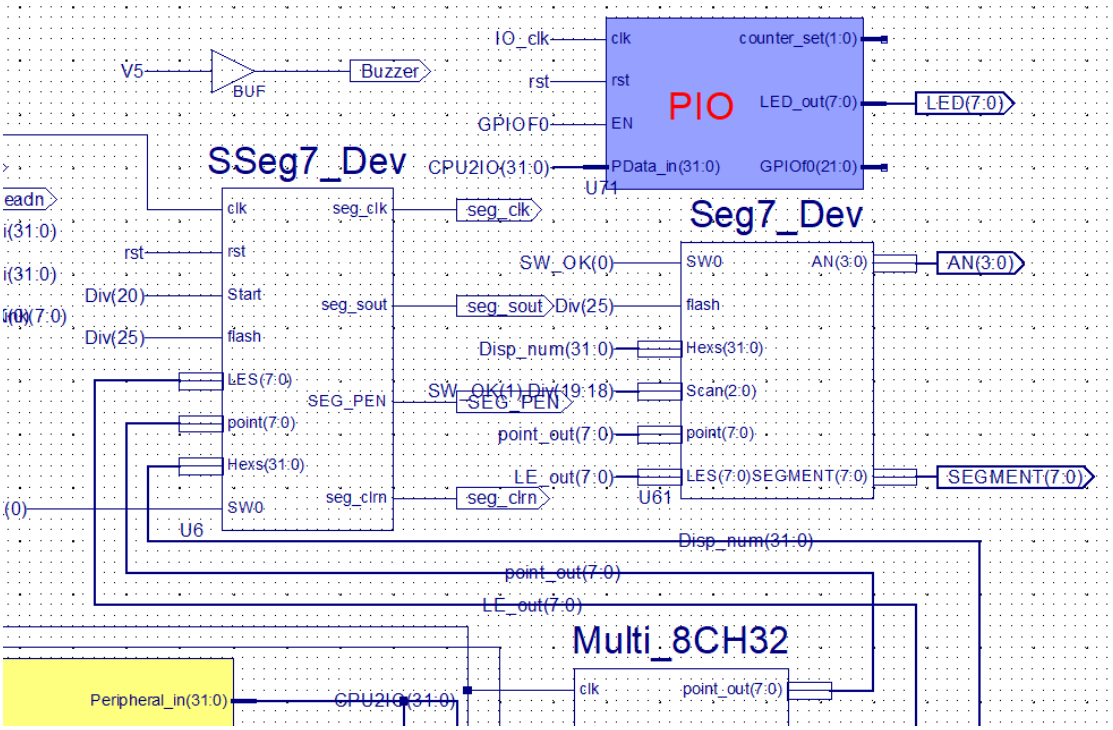
CPU 与数据存储模块



数据（命令）选择和 LED 模块



七段数码管和 Arduino 子板



7 书写引脚约束代码

```
1.  NET "clk_100mhz"                    LOC = AC18      | IOSTANDARD = LVCMOS18
    ;
2.  NET "RSTN"                          LOC = W13       | IOSTANDARD = LVCMOS18
    ;
3.  NET "clk_100mhz"                    TNM_NET = TM_CLK ;
4.  TIMESPEC TS_CLK_100M        = PERIOD "TM_CLK"       10 ns HIGH 50%;
5.
6.  NET "led_clk"               LOC = N26       | IOSTANDARD = LVCMOS33 ;
7.  NET "led_clrn"              LOC = N24       | IOSTANDARD = LVCMOS33 ;
8.  NET "led_sout"              LOC = M26       | IOSTANDARD = LVCMOS33 ;
9.  NET "LED_PEN"               LOC = P18       | IOSTANDARD = LVCMOS33 ;
10.
11. NET "seg_clk"               LOC = M24       | IOSTANDARD = LVCMOS33 ;
12. NET "seg_clrn"              LOC = M20       | IOSTANDARD = LVCMOS33 ;
13. NET "seg_sout"              LOC = L24       | IOSTANDARD = LVCMOS33 ;
14. NET "SEG_PEN"               LOC = R18       | IOSTANDARD = LVCMOS33 ;
15.
16. NET "RDY"           LOC = U21       | IOSTANDARD = LVCMOS33 ;
17. NET "readn"         LOC = U22       | IOSTANDARD = LVCMOS33 ;
18. NET "CR"                LOC = V22       | IOSTANDARD = LVCMOS33 ;
19. #NET "tri_led1_r_n"         LOC = U24       | IOSTANDARD = LVCMOS18 ;
20. #NET "tri_led1_g_n"         LOC = U25       | IOSTANDARD = LVCMOS18 ;
21. #NET "tri_led1_b_n"         LOC = V23       | IOSTANDARD = LVCMOS18 ;
```

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22.
23. NET "BTN_x[0]"          LOC = V17        | IOSTANDARD = LVCMOS18 ;
24. NET "BTN_x[1]"              LOC = W18       | IOSTANDARD = LVCMOS18 ;
25. NET "BTN_x[2]"              LOC = W19       | IOSTANDARD = LVCMOS18 ;
26. NET "BTN_x[3]"              LOC = W15       | IOSTANDARD = LVCMOS18 ;
27. NET "BTN_x[4]"              LOC = W16       | IOSTANDARD = LVCMOS18 ;
28.
29.
30.
31. NET "BTN_y[0]"              LOC = V18       | IOSTANDARD = LVCMOS18 ;
32. NET "BTN_y[1]"              LOC = V19       | IOSTANDARD = LVCMOS18 ;
33. NET "BTN_y[2]"              LOC = V14       | IOSTANDARD = LVCMOS18 ;
34. NET "BTN_y[3]"              LOC = W14       | IOSTANDARD = LVCMOS18 ;
35.
36. NET "SW[0]"             LOC = AA10      | IOSTANDARD = LVCMOS15 ;
37. NET "SW[1]"             LOC = AB10      | IOSTANDARD = LVCMOS15 ;
38. NET "SW[2]"             LOC = AA13      | IOSTANDARD = LVCMOS15 ;
39. NET "SW[3]"             LOC = AA12      | IOSTANDARD = LVCMOS15 ;
40. NET "SW[4]"             LOC = Y13       | IOSTANDARD = LVCMOS15 ;
41. NET "SW[5]"             LOC = Y12       | IOSTANDARD = LVCMOS15 ;
42. NET "SW[6]"             LOC = AD11      | IOSTANDARD = LVCMOS15 ;
43. NET "SW[7]"             LOC = AD10      | IOSTANDARD = LVCMOS15 ;
44. NET "SW[8]"             LOC = AE10      | IOSTANDARD = LVCMOS15 ;
45. NET "SW[9]"             LOC = AE12      | IOSTANDARD = LVCMOS15 ;
46. NET "SW[10]"            LOC = AF12      | IOSTANDARD = LVCMOS15 ;
47. NET "SW[11]"            LOC = AE8       | IOSTANDARD = LVCMOS15 ;
48. NET "SW[12]"            LOC = AF8       | IOSTANDARD = LVCMOS15 ;
49. NET "SW[13]"            LOC = AE13      | IOSTANDARD = LVCMOS15 ;
50. NET "SW[14]"            LOC = AF13      | IOSTANDARD = LVCMOS15 ;
51. NET "SW[15]"            LOC = AF10      | IOSTANDARD = LVCMOS15 ;
52.
53.
54. #ArDUNIO-IO
55. NET "Buzzer"            LOC = AF24      | IOSTANDARD = LVCMOS33 ;
56. NET "SEGMENT[0]"        LOC = AB22      | IOSTANDARD = LVCMOS33 ;#a
57. NET "SEGMENT[1]"        LOC = AD24       | IOSTANDARD = LVCMOS33 ;#b
58. NET "SEGMENT[2]"        LOC = AD23       | IOSTANDARD = LVCMOS33 ;
59. NET "SEGMENT[3]"        LOC = Y21        | IOSTANDARD = LVCMOS33 ;
60. NET "SEGMENT[4]"        LOC = W20        | IOSTANDARD = LVCMOS33 ;
61. NET "SEGMENT[5]"        LOC = AC24       | IOSTANDARD = LVCMOS33 ;
62. NET "SEGMENT[6]"        LOC = AC23       | IOSTANDARD = LVCMOS33 ;#g
63. NET "SEGMENT[7]"        LOC = AA22       | IOSTANDARD = LVCMOS33 ;#point
64.
65. NET "AN[0]"             LOC = AD21      | IOSTANDARD = LVCMOS33 ;
```

```
66. NET "AN[1]"             LOC = AC21      | IOSTANDARD = LVCMOS33 ;
67. NET "AN[2]"             LOC = AB21      | IOSTANDARD = LVCMOS33 ;
68. NET "AN[3]"             LOC = AC22      | IOSTANDARD = LVCMOS33 ;
69.
70. NET "LED[0]"            LOC = AB26      | IOSTANDARD = LVCMOS33 ;
71. NET "LED[1]"            LOC = W24       | IOSTANDARD = LVCMOS33 ;
72. NET "LED[2]"            LOC = W23       | IOSTANDARD = LVCMOS33 ;
73. NET "LED[3]"            LOC = AB25      | IOSTANDARD = LVCMOS33 ;
74. NET "LED[4]"            LOC = AA25      | IOSTANDARD = LVCMOS33 ;
75. NET "LED[5]"            LOC = W21       | IOSTANDARD = LVCMOS33 ;
76. NET "LED[6]"            LOC = V21       | IOSTANDARD = LVCMOS33 ;
77. NET "LED[7]"            LOC = W26       | IOSTANDARD = LVCMOS33 ;
```

二、实验结果与分析

顶层模块综合正确且生成 bit 文件成功。（见首页图）

三、讨论、心得

本次实验在前面两次实验的基础上，进一步建立了 CPU 调试测试环境，调用了 SCPU 和 MIO_BUS 以及 Counter_x 的 IP 核，更新了 RAM 和 ROM 的 coe 文件。由于前面实验的绘图基础，本次实验的绘制原理图过程比较顺利，模块排布也相对合理。

实验中将图中并不相连的导线命名相同时可以 merge。发现之后修改一处的名字，另一处也会修改。因此，在实验中，偶然错误命名了一根导线的名字，发现命名错后，将其修改，却忘了这根导线已与另一根错误命名的导线 merge（即相连），导致了名字的错乱以及端口属性（输入或输出）的混乱。之后只能删除相关导线重新画，这告诫我命名导线时要非常小心，尤其是会导致 merge 的导线命名。

本次实验让我对 SOC 有了更加深刻的认识，但同时，也有一些模块的原理尚不清楚（如 Count_x 模块），希望在之后的学习和实验中能够逐渐深入理解。