浙江大学 2014～2015 学年 春夏 学期

《 计算机组成 》课程期末考试试卷（A）

课程号： 21186031 ，开课学院：计算机学院　　任课老师：

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式： 闭 卷，允许带 一页 A4 纸手写笔记 入场，笔记署名，不得互借

交卷方式： 试卷名字朝外对折整齐，草稿纸、笔记与试卷一起上交 。

考试日期： 2015 年 07 月 09 日(10:30～12:30) ，考试时间： 120 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____学号：_____所属院系：_____

题序	一.10	二.40	三.15	四.15	五.20		总 分.100
得分							
评卷人							

Something may be needed:

OPcode: Beq:4, Bne:5, J:2, Lw:35, Sw:43
Function Code: Sub:34, Add:32
Register No. $s0:16, $t0:8

I. True or False(10x1%; √/×)

eg.	1	2	3	4	5	6	7	8	9	10
√										

eg: TLB: translation-lookaside buffer

1、 combinational logic: A group of logic elements that contain memory and hence whose value depends on the inputs as well as the current contents of the memory.

×

2、 Memory is storage area in Computer. In which programs are kept when they are running and that contains the data needed by the running programs.

10、asynchronous bus: A bus that uses a handshaking protocol for coordinating usage rather than a clock; can accommodate a wide variety of devices of differing speeds.

√

II. Choose 1 best answer. (20x2%)

eg.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
C																				

eg. 1KiB means (____) bytes。

A: 1　　B: 1000　　C: 1024　　D: 1024*1024

1、 What is the hexadecimal equivalent of 105 base 10?(____).

A: 151　　B: 69　　C: 36　　D: 54

B

2、 2's complement in 8 bits for -128 is (____)。

A: 0100 0000　B: 1000 0000　C: 0000 0000　D: Overflow

B

18、Today's computers are built on 2 key principles: (____)

①Make the common case fast.

②Instruction are represented as numbers.

③Every instruction can be conditionally executed.

④Programs can be stored in memory to be read or written just like numbers.

A: ①③　　B: ②④　　C: ①②　　D: ③④

B

20、There are no inherent meaning about binary bits 1010110100010000 0000000000000000. The following description which is the most correct (____)?

A It is two's complement of -0xAD100000

B It represent an unsigned interger: 0x52F00000

C A single precision floating-point number: $1.001*2^{-37}$

D A mips instruction: sw $s0,0($t0)

D

III. (15%)The C to Assemble:

Convert the C function below to MIPS/ARM assembly language. Make sure that your assembly language code could be called from a standard C program (that is to say, make sure you follow the MIPS/ARM calling conventions.

```
int min(int n, int *p){
int i, m=p[0];
  for (i=1;i<n;i++)
  if (p[i]<m) m=p[i];
  return m;
}
```

IV、(15%): To 2G main memory, byte-addressing, 256KB Cache, Please do.

1.(3%) Calculated different field of physical address and draw logical structure of Direct-mapped, assuming 4 bytes /block.

Tag	Index	Byte offset

V、(20%)Design:

1: 2-4 decoder design by logic gate.

2: Multicycle CPU implementation

MIPS is a register-register architecture, where arithmetic source and destinations must be registers. But let's say we wanted to add a register-memory instruction:

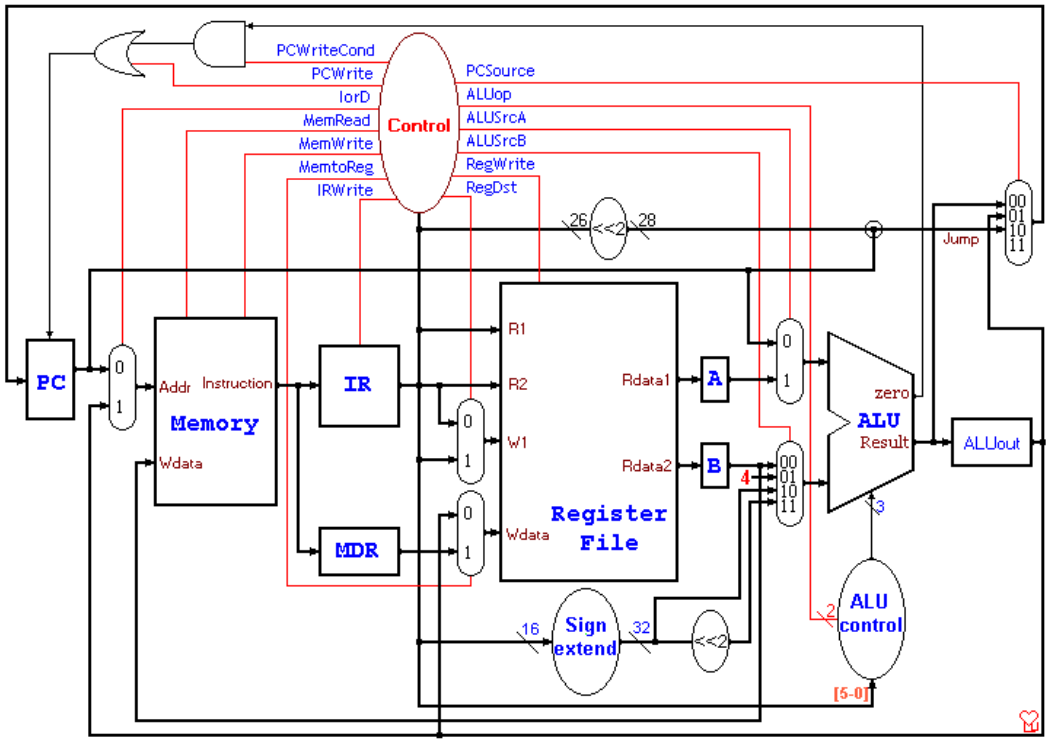
```
addm    $r1, dat($r2)
Execute to $r1 += Memory[$r2+dat]
```

1.(3%) Design Jalr instruction format: the instruction in binary number;

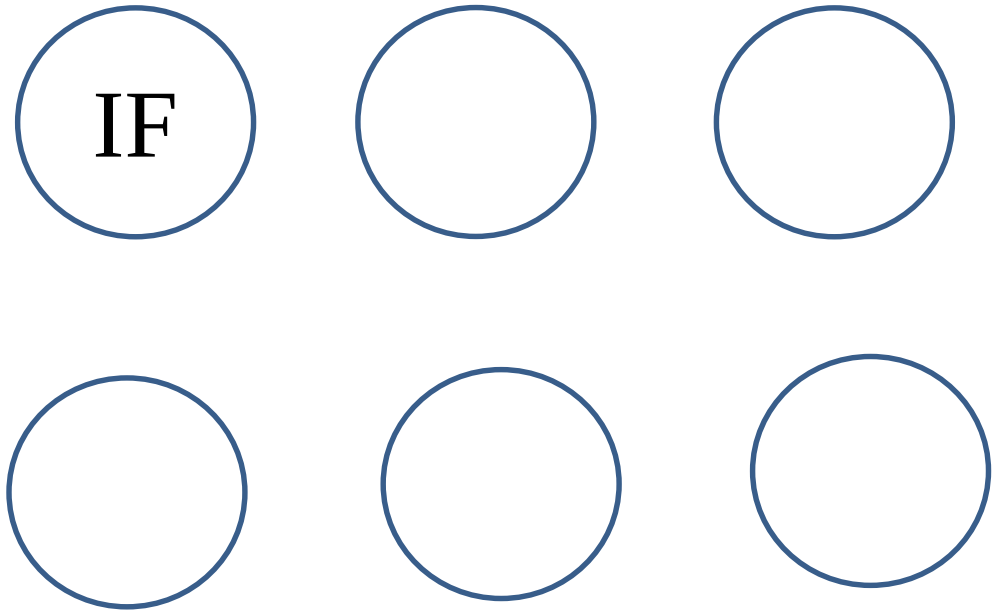
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
OpCode																															
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

2.(4%) Design datapath: May be to add any necessary elements and new signals and explain how to modify the data path;

3.(5%)In the following diagram Draw compatible Modification



4.(8%) Complete this finite state machine diagram for the Jalr instruction. Be sure to include any new control signals you may have added. For each state, fill the output signal values in the following table(only "Jalr" instruction state).



State / signals	IF								
ALUSrcA									
ALUSrcB1									
ALUSrcB0									
IRWrite									
RegWrite									
RegDst									
MemtoReg									
MemRead									
MemWrite									
IorD									
PCSource1									
PCSource0									
PCWrite									
PCWriteCond									