浙江大学

本科实验报告

课程名称：计算机组成

姓　　名：吴沁珈

学　　院：计算机科学与技术学院

专　　业：计算机科学与技术

学　　号：3180103776

生活照：

指导教师：洪奇军

2020 年　3 月 17 日

实验三　IP 核集成 SOC 设计实验报告

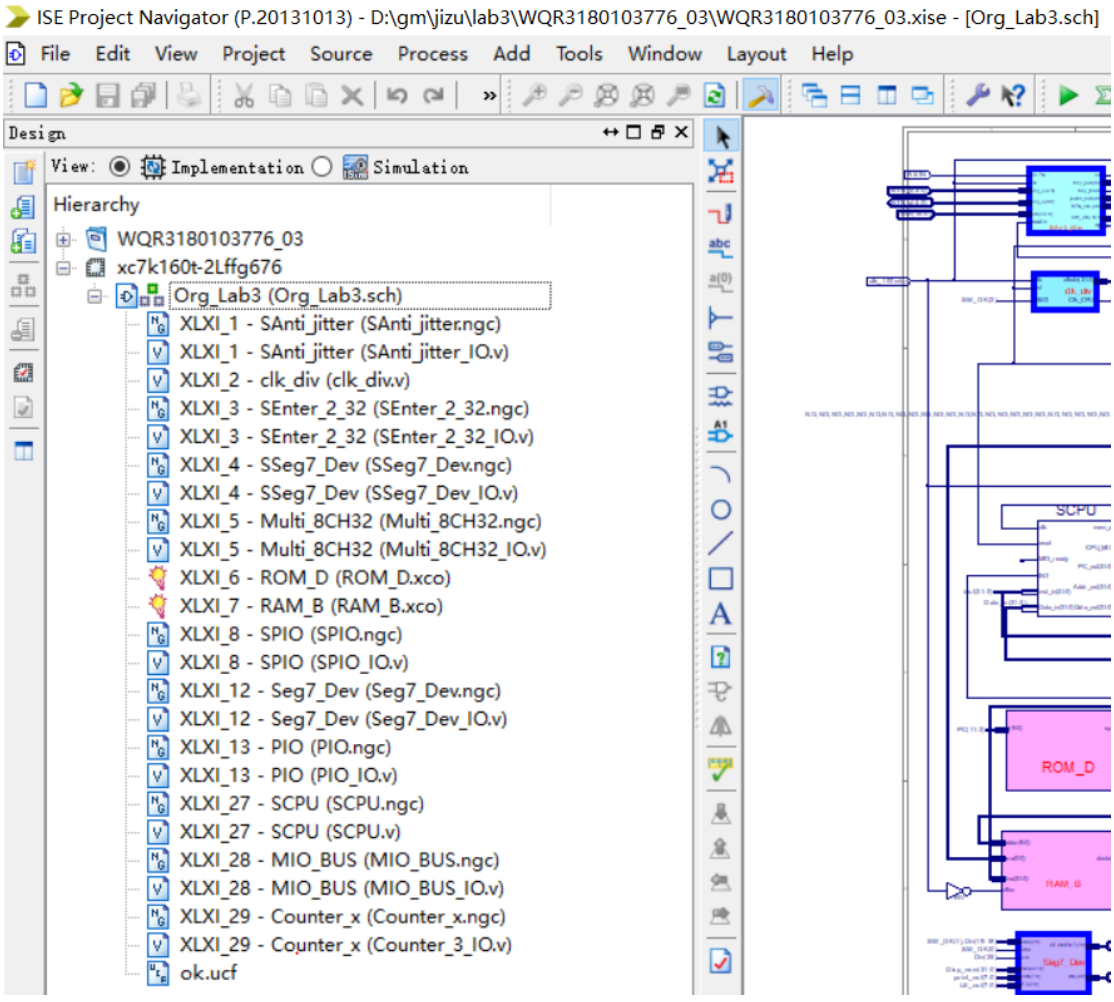
姓名：吴沁珅　学号：3180103776　专业：计算机科学与技术

课程名称：计算机组成　同组学生姓名：无

实验时间：2020-03-17　实验地点：　指导老师：　洪奇军

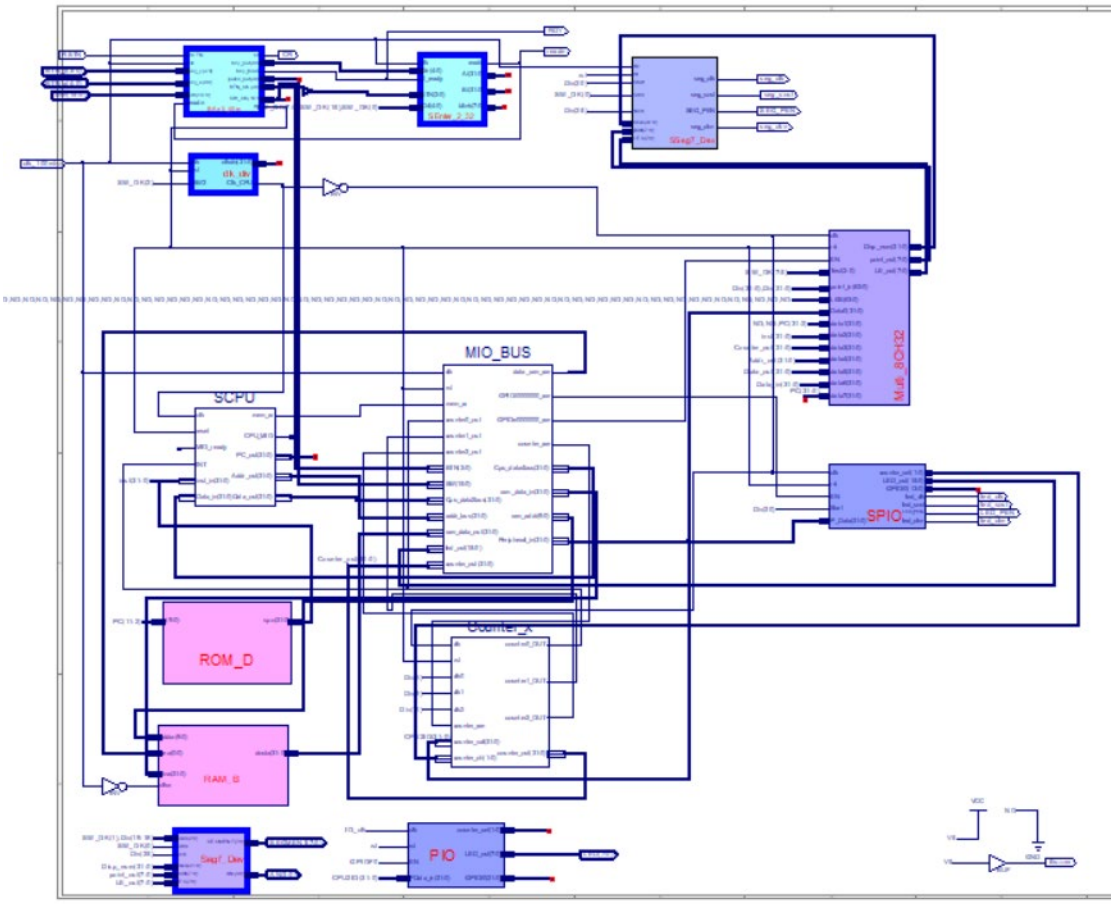
一、操作方法与实验步骤

（一）　代码设计层次结构图



（二） 各部分实现

1、 顶层模块设计

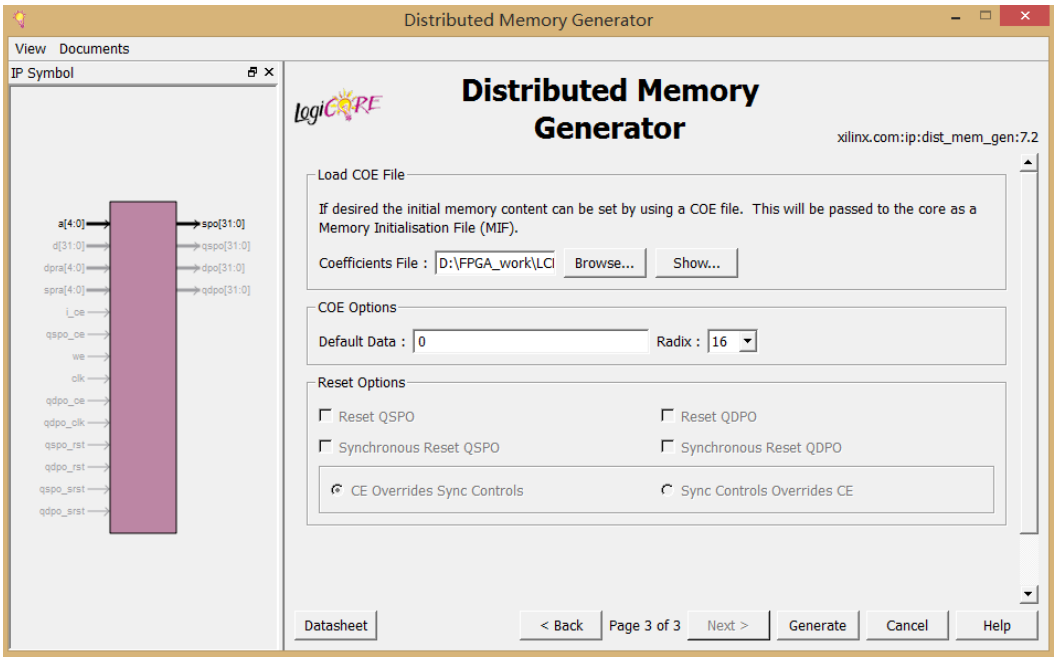


2、 大多数模块用提供的 v 文件和 ngc 文件以及实验二中的文件添加实现

3、 存储器 IP 核重新初始化

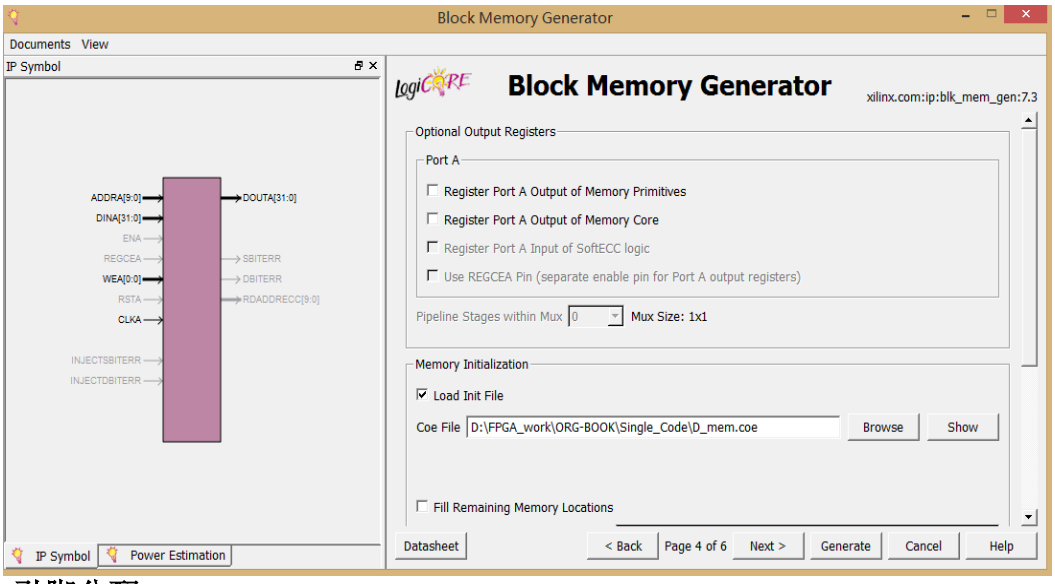
• ROM_B 重新初始化

在设计窗口双击 ROM_B 进入核管理向导，点击 Next，进入核参数配置第 3 页，点击“Browse...”选择初始化关联文件（I9_men.coe），点击 Generate 重新生成 ROM 核



• **RAM_B 初始化**

与 ROM 同样方法进入核管理向导，点击 Next 进入第 4 页，点击“Browse...”选择初始化关联文件（D_men.coe），点击 Generate 重新生成 ROM 核



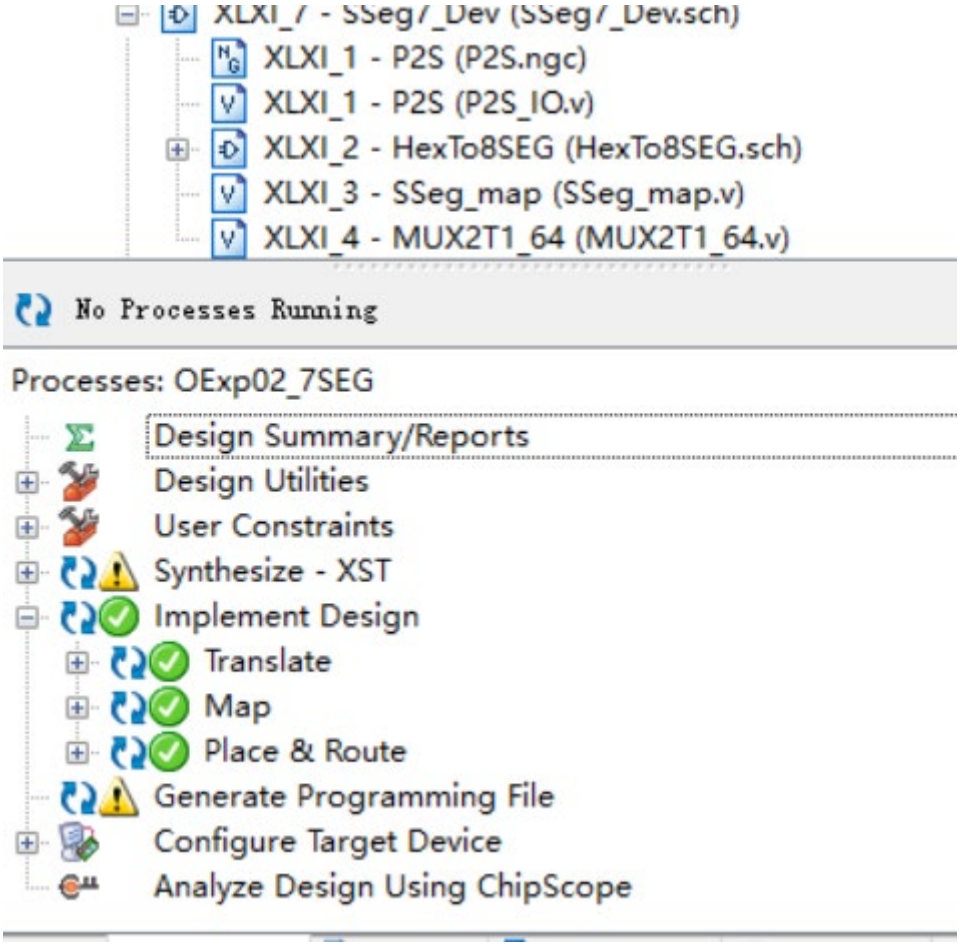
4、 引脚分配

```
#系统时钟
NET "clk_100mhz"          LOC = AC18          | IOSTANDARD = LVCMOS18 ;
NET "RSTN"                LOC = W13           | IOSTANDARD = LVCMOS18 ;
NET "clk_100mhz"          TNM_NET = TM_CLK ;
TIMESPEC TS_CLK_100M = PERIOD "TM_CLK"    10 ns HIGH 50%;
#LED 串行接口
NET "led_clk"             LOC = N26       |IOSTANDARD = LVCMOS33 ;
NET "led_clrn"            LOC = N24     | IOSTANDARD = LVCMOS33 ;
NET "led_sout"            LOC = M26     | IOSTANDARD = LVCMOS33 ;
NET "LED_PEN"             LOC = P18     | IOSTANDARD = LVCMOS33 ;
#七段码串行接口
NET "seg_clk"             LOC = M24     | IOSTANDARD = LVCMOS33 ;
NET "seg_clrn"            LOC = M20     | IOSTANDARD = LVCMOS33 ;
```

```
NET "seg_sout"          LOC = L24     | IOSTANDARD = LVCMOS33 ;
NET "SEG_PEN"           LOC = R18     | IOSTANDARD = LVCMOS33 ;
#三色信号灯：Tri_LED
NET "RDY"                   LOC = U21     | IOSTANDARD = LVCMOS33 ;#LED_nR0
NET "readn"                 LOC = U22     | IOSTANDARD = LVCMOS33 ;#LED_nG0
NET "CR"                    LOC = V22     | IOSTANDARD = LVCMOS33 ;#LED_nB0
#NET "LED_nR1"              LOC = U24     | IOSTANDARD = LVCMOS18 ;
#NET "LED_nG1"              LOC = U25     | IOSTANDARD = LVCMOS18 ;
#NET "LED_nB1"              LOC = V23     | IOSTANDARD = LVCMOS18 ;
#阵列式按键
NET "BTN_x[0]"          LOC = V17     | IOSTANDARD = LVCMOS18 ;#ROW0
NET "BTN_x[1]"          LOC = W18     | IOSTANDARD = LVCMOS18 ;#ROW1
NET "BTN_x[2]"          LOC = W19     | IOSTANDARD = LVCMOS18 ;#ROW2
NET "BTN_x[3]"          LOC = W15     | IOSTANDARD = LVCMOS18 ;#ROW3
NET "BTN_x[4]"          LOC = W16     | IOSTANDARD = LVCMOS18 ;#ROW4
NET "BTN_y[0]"          LOC = V18     | IOSTANDARD = LVCMOS18 ;#COL0
NET "BTN_y[1]"          LOC = V19     | IOSTANDARD = LVCMOS18 ;#COL1
NET "BTN_y[2]"          LOC = V14     | IOSTANDARD = LVCMOS18 ;#COL2
NET "BTN_y[3]"          LOC = W14     | IOSTANDARD = LVCMOS18 ;#COL3
#switch
NET "SW[0]"                 LOC = AA10    | IOSTANDARD = LVCMOS15 ;
NET "SW[1]"                 LOC = AB10    | IOSTANDARD = LVCMOS15 ;
NET "SW[2]"                 LOC = AA13    | IOSTANDARD = LVCMOS15 ;
NET "SW[3]"                 LOC = AA12    | IOSTANDARD = LVCMOS15 ;
NET "SW[4]"                 LOC = Y13     | IOSTANDARD = LVCMOS15 ;
NET "SW[5]"                 LOC = Y12     | IOSTANDARD = LVCMOS15 ;
NET "SW[6]"                 LOC = AD11    | IOSTANDARD = LVCMOS15 ;
NET "SW[7]"                 LOC = AD10    | IOSTANDARD = LVCMOS15 ;
NET "SW[8]"                 LOC = AE10    | IOSTANDARD = LVCMOS15 ;
NET "SW[9]"                 LOC = AE12    | IOSTANDARD = LVCMOS15 ;
NET "SW[10]"            LOC = AF12    | IOSTANDARD = LVCMOS15 ;
NET "SW[11]"            LOC = AE8     | IOSTANDARD = LVCMOS15 ;
NET "SW[12]"            LOC = AF8     | IOSTANDARD = LVCMOS15 ;
NET "SW[13]"            LOC = AE13    | IOSTANDARD = LVCMOS15 ;
NET "SW[14]"            LOC = AF13    | IOSTANDARD = LVCMOS15 ;
NET "SW[15]"            LOC = AF10    | IOSTANDARD = LVCMOS15 ;

#ArDUNIO-Sword-002-Basic IO
NET "Buzzer"            LOC = AF24    | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[0]"        LOC = AB22    | IOSTANDARD = LVCMOS33 ;#a
NET "SEGMENT[1]"        LOC = AD24     | IOSTANDARD = LVCMOS33 ;#b
NET "SEGMENT[2]"        LOC = AD23     | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[3]"        LOC = Y21      | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[4]"        LOC = W20      | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[5]"        LOC = AC24     | IOSTANDARD = LVCMOS33 ;
NET "SEGMENT[6]"        LOC = AC23     | IOSTANDARD = LVCMOS33 ;#g
NET "SEGMENT[7]"        LOC = AA22     | IOSTANDARD = LVCMOS33 ;#point


NET "AN[0]"             LOC = AD21    | IOSTANDARD = LVCMOS33 ;
NET "AN[1]"             LOC = AC21    | IOSTANDARD = LVCMOS33 ;
NET "AN[2]"             LOC = AB21    | IOSTANDARD = LVCMOS33 ;
NET "AN[3]"             LOC = AC22    | IOSTANDARD = LVCMOS33 ;

NET "LED[0]"            LOC = AB26    | IOSTANDARD = LVCMOS33 ;
NET "LED[1]"            LOC = W24     | IOSTANDARD = LVCMOS33 ;
NET "LED[2]"            LOC = W23     | IOSTANDARD = LVCMOS33 ;
NET "LED[3]"            LOC = AB25    | IOSTANDARD = LVCMOS33 ;
NET "LED[4]"            LOC = AA25    | IOSTANDARD = LVCMOS33 ;
NET "LED[5]"            LOC = W21     | IOSTANDARD = LVCMOS33 ;
NET "LED[6]"            LOC = V21     | IOSTANDARD = LVCMOS33 ;
NET "LED[7]"            LOC = W26     | IOSTANDARD = LVCMOS33 ;
```

```
#NET "PS2_clk"              LOC = N18     | IOSTANDARD = LVCMOS33 ;
#NET "PS2_data"       LOC = M19     | IOSTANDARD = LVCMOS33 ;

#NET "PS2_clk"              LOC = N18     | IOSTANDARD = LVCMOS33 | SLEW = FAST |    PULLUP ;
#NET "PS2_data"       LOC = M19     | IOSTANDARD = LVCMOS33 | SLEW = FAST | PULLUP ;

#NET "Blue[0]"              LOC = T20     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Blue[1]"              LOC = R20     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Blue[2]"              LOC = T22     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Blue[3]"              LOC = T23     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Green[0]"       LOC = R22     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Green[1]"       LOC = R23     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Green[2]"       LOC = T24     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Green[3]"       LOC = T25     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Red[0]"               LOC = N21     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Red[1]"               LOC = N22     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Red[2]"               LOC = R21     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "Red[3]"               LOC = P21     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "HSYNC"                LOC = M22     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
#NET "VSYNC"                LOC = M21     | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
```

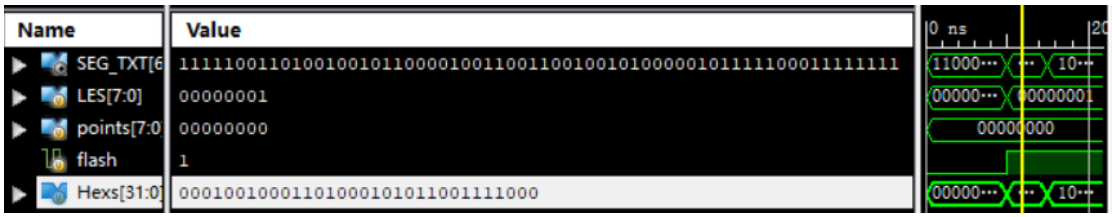
（三） Design 窗口运行成功



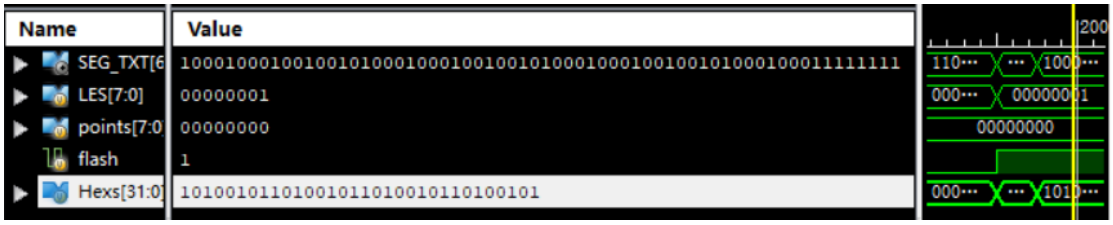
二、实验结果与分析

HexTo8SEG 仿真结果

1、Hexs=32'h12345678;

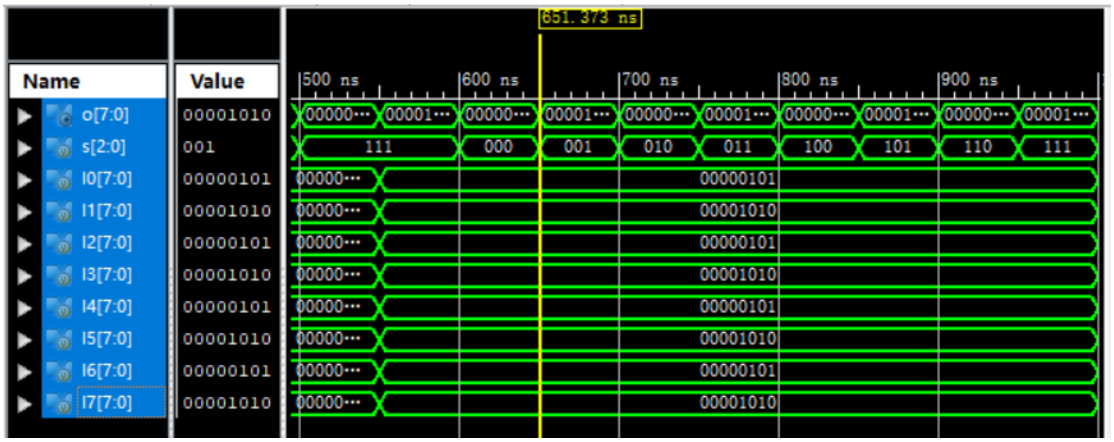


2、Hexs=32'hA5A5A5A5;



由仿真结果可知，Hexs 有输入时 SEG_TXT 有相应的输出

MUX8T1 仿真结果



由仿真结果可以看出，当 s[2:0]选择的是 000 第 0 个输入时，输出偏 o[7:0]输出的值恰好是 I0[7:0]的值，所以 s[2:0]可以选择 I0,I1,I2,I3,I4,I5,I6,I7 某一个中的八位二进制数字作为输出。

三、讨论、心得

1、本次实验在实验一实验二的基础上添加了 CPU 测试和应用环境

2、本次实验目前碰到的问题主要是 IP 核初始化，一开始添加进需要的文件，画好顶层图之后，Design 窗口运行正常，可是对 IP 核进行初始化之后，就一直报

错，说找不到初始化文件，后来只能重新生成了 IP 核再初始化。对 IP 核、coe 文件、SCPU 测试还比较陌生，具体功能实现也需要看物理验证的情况。