ECE385

Fall 2023

Experiment #1

Lab 1

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Lab section: ZY 10/Day & Time: 9.5
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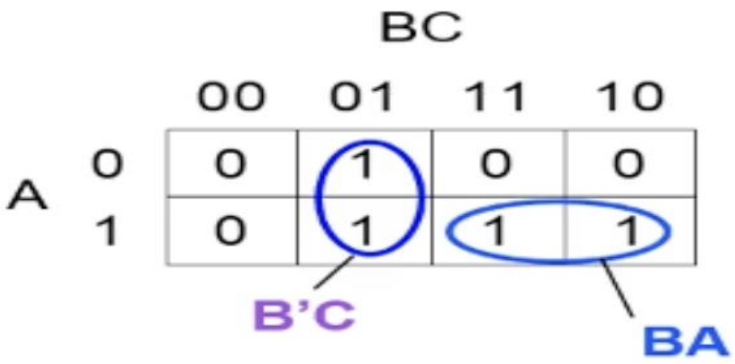
1. Introduction

The lab introduces the static hazard (Glitch) and show a way to solve the problem. By adding a term to the circuit, we can prevent the temporary 0 and make it constant 1. The lab introduces the way to write a report and implement circuit. It helps me review the concept like static hazards, debouncing, delays, glitches, K-maps, and logic diagrams.

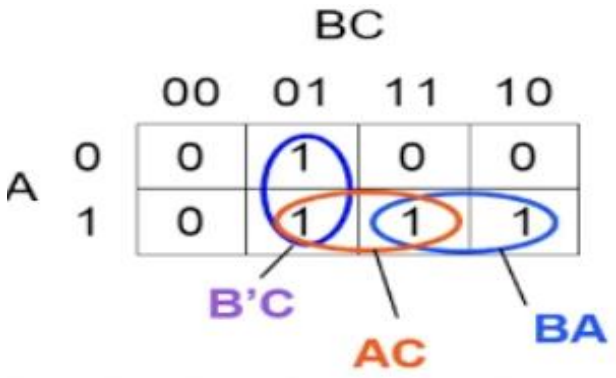
2. Description of Circuit

The essence of the circuit is a two-input MUX with two minterms and one extra term. The circuit is built by NAND gates. The purpose of the extra term was to prevent hazard which led to delay in the logic and may produce an unwanted output. The extra capacitors are used to add delay which make hazard static more obviously.

Kmap for MUX in part A:



Kmap for MUX in part B:



Boolean equation for part A:

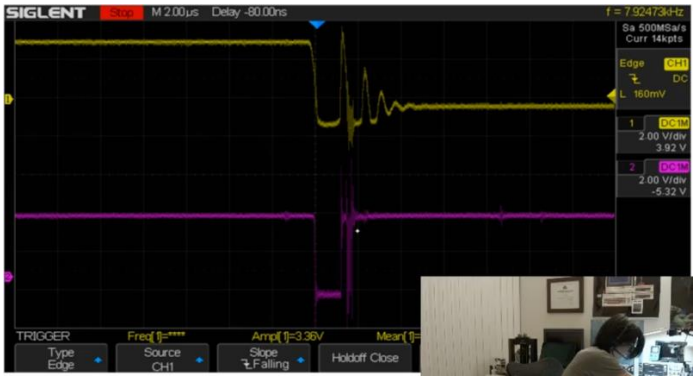
$$Z = BA + B'C$$

Boolean equation for part B:

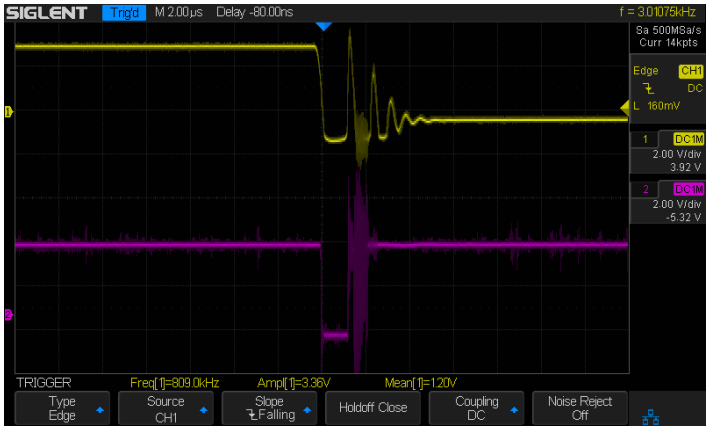
$$Z = BA + B'C + AC$$

The circuit is powered by 3.3V source on the FPGA board. Input B is 5V square wave. Additionally, capacitors are placed to the output of inverter (B) to enlarge the delay. I also put two decoupling capacitors to ground and power. They can reduce the noise.

Without capacitors

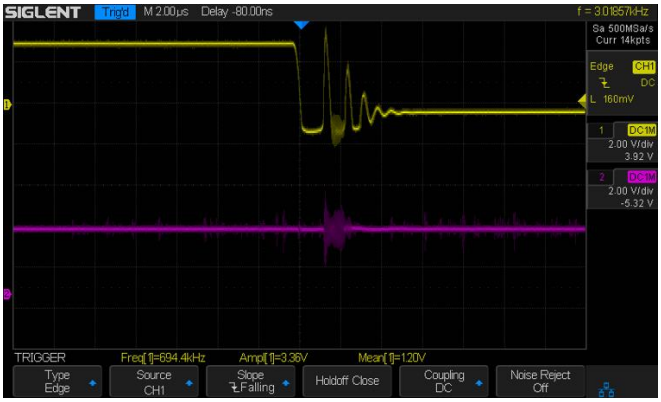


With capacitors



The circuit A have glitch because the exist of inverter which make the signal delay. To prevent the glitch caused by the inverter delay, we add extra terms (AC) in K-map. It covers both circle of BA and B'C

To implement the circuit. We design the circuit with NAND gate (7400). I use another chip 7400 since I need 3 more NAND gate. The output (purple) is displayed below.



We also analyze the truth table for A and B. After we build the circuit, we test the truth table.

Truth table A

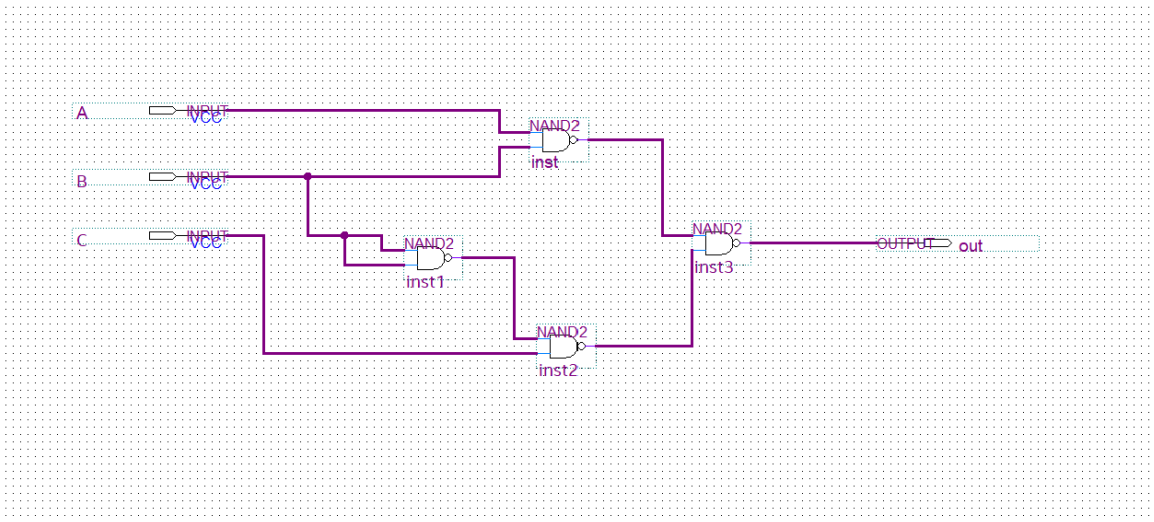
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth table B

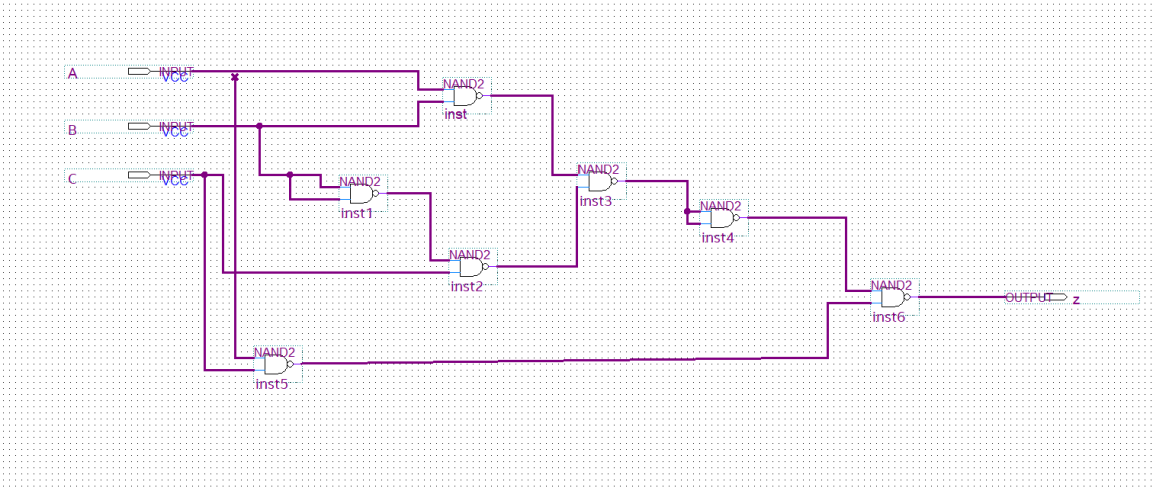
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. Logic Diagrams

For circuit A

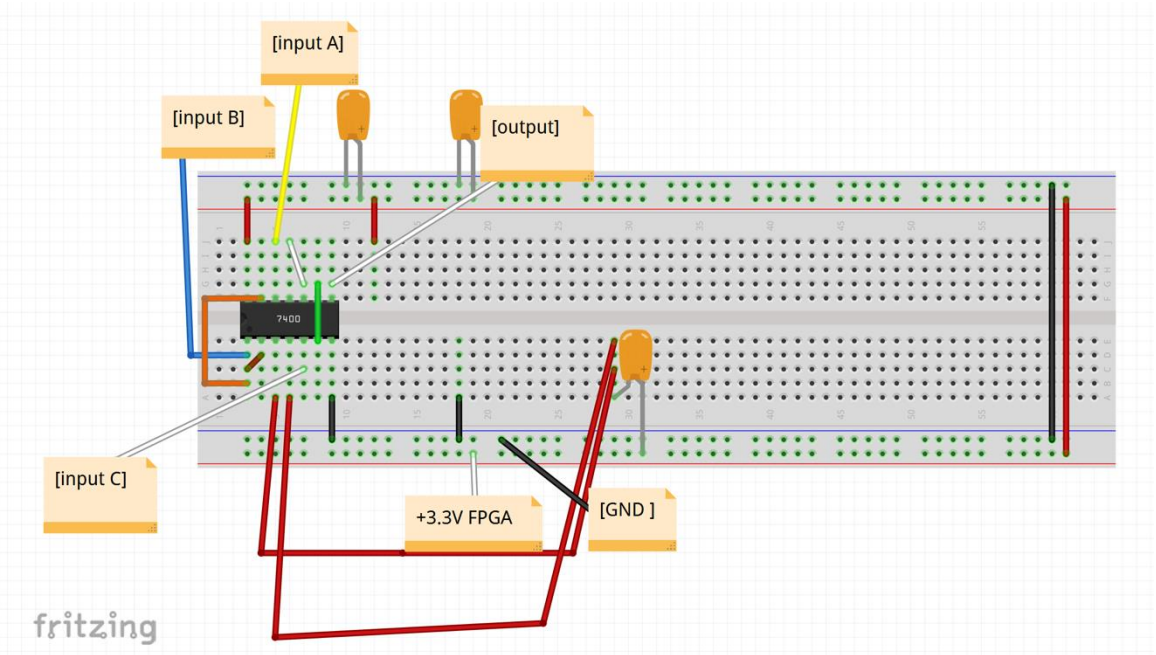


For circuit B

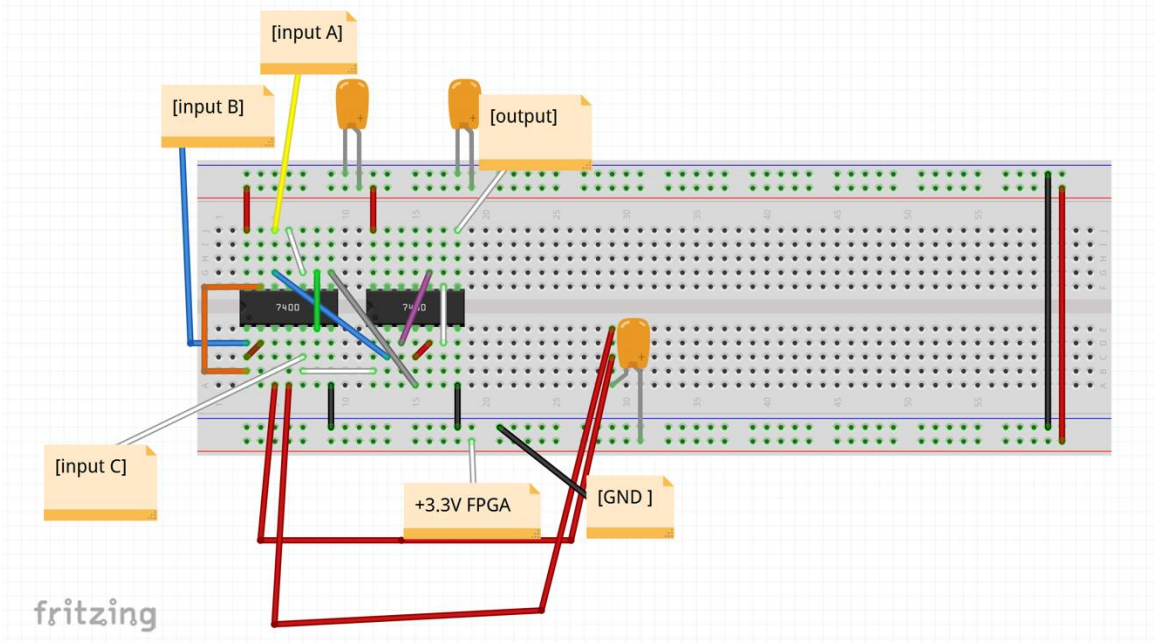


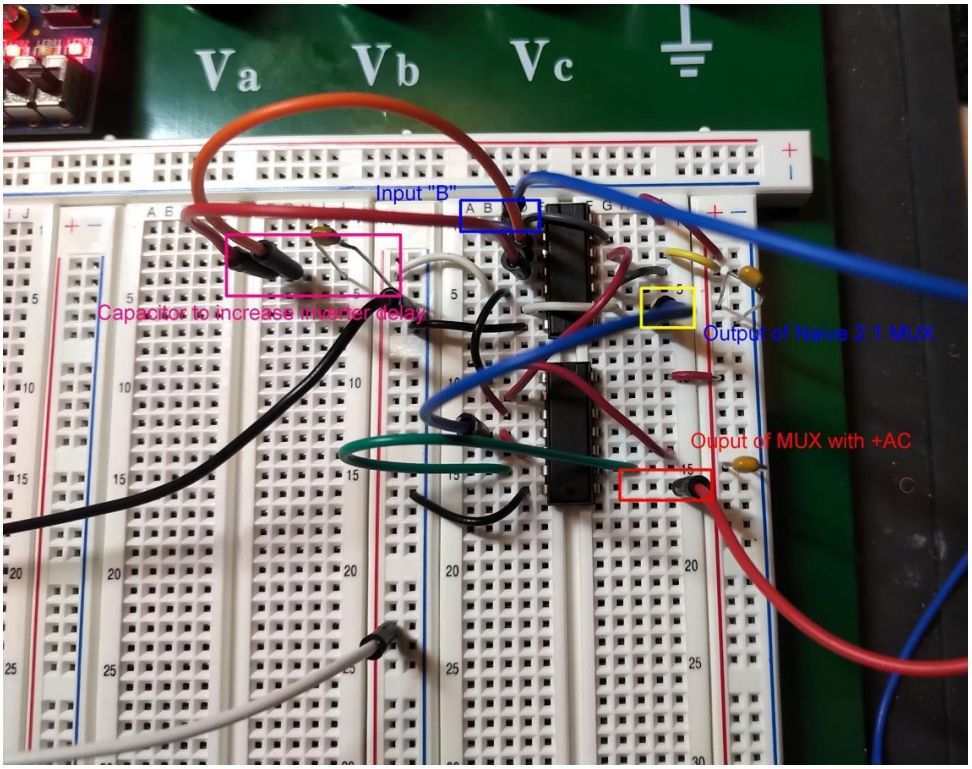
4. Component Layout

For circuit A



For circuit B





5. Answers to Pre-Lab Questions

1. Not all groups may observe static hazards (why?)

Because some delay influences the circuit or input remain unchanged for a while.

2. If you do not observe a static hazard, chain an odd number of inverters together in place of the single inverter from Figure 17 ***or*** *add a small capacitor to the output of the inverter until you observe a glitch. Why does the hazard appear when you do this?*

It aims to enlarge the glitch. The capacitor must be charge and discharge. It will increase the time that the signal goes into the logic gate.

6. Answers to Lab Questions

1. Complete a truth table of the output.

Same as part A

Truth table for A and B circuit:

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

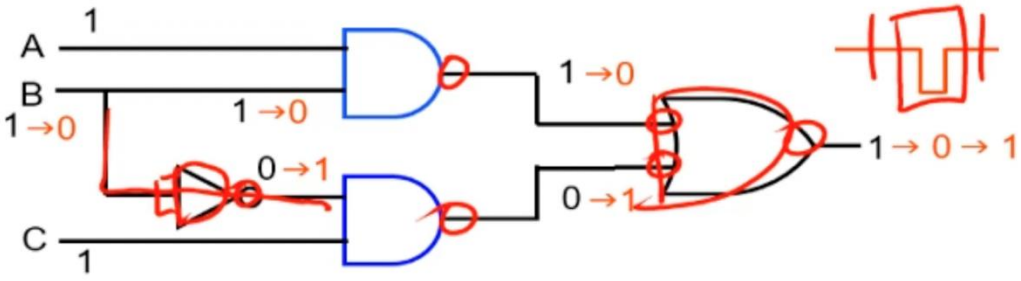
s

2. *Describe and save the output and explain any differences between it and the results obtained in part 2.*

In part A we have glitch while in part B we don't have glitch. There is no glitch in part B. Because we have added term AC in the circuit

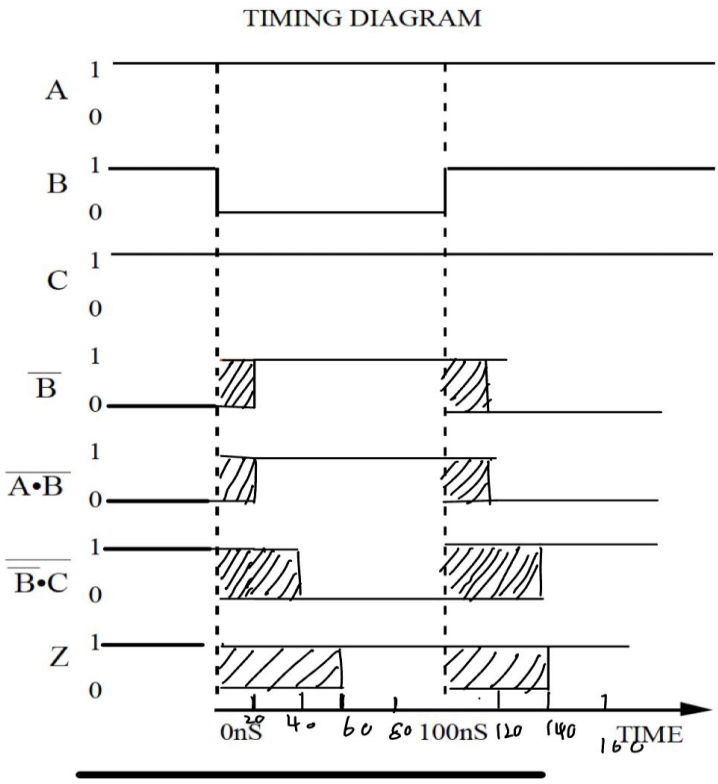
3 *Consider the following question and explain: for the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?*

Part A are more likely to observe a glitch when the input is changing from high to low (falling edge). It can be explained by the following diagram.
The upper NAND is not affected by delay, and it change to 1 immediately. However, due the inverter (NAND) in the lower NAND gate the input signal is still unchanged (0 AND 1) which get result 1. The result is (1AND1)'which is 0. After the delay, the lower NAND gate takes 1 from the inverter and causing output to rise back to 1.



7. Answers to Post-Lab Questions

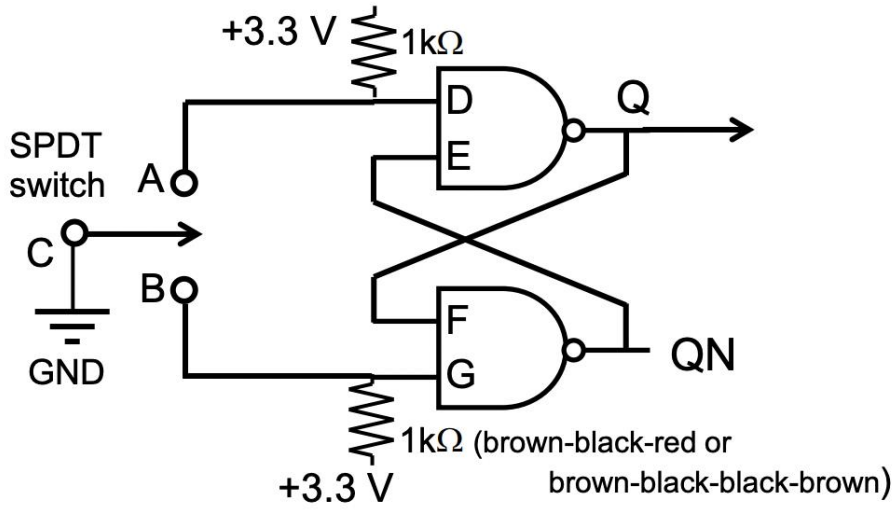
1.complete timing diagram for A



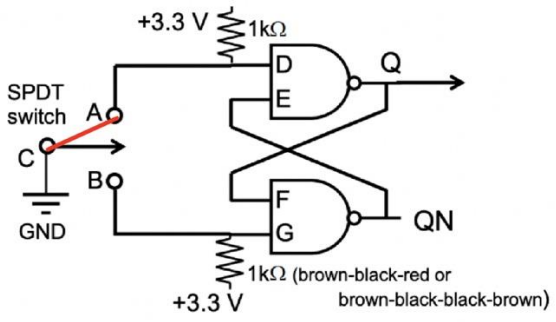
1. *How long does it take the output Z to stabilize on the falling edge of B (in. ns)? How. long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.*

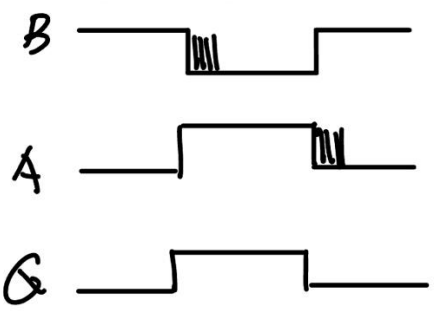
It takes Z 60ns(0-60ns) to stabilize on falling edge of B and takes 40ns(100-140ns) to stabilize on rising edge of B.
There are potential glitches on Z. This is because after the inverter gate like (NOT B, NOT AB). The later output will be influenced by the previous signal.

2. *Explain how and why the debouncer circuit given in General Guide (Figure 22) works. Specifically, what makes it behave like a switch and how the ill effect of. mechanical contact bounces are eliminated?*



When the switch is connected to A. The input D will connect directly to the ground. The first NAND gate is determined by input D and Q is 0. QN is 1
When the switch is connected to B. The input D will connect directly to the +3.3V. Input G is connected to the ground. The second NAND gate is determined by G. QN is 1, E is 1. Q is 0,
For the two cases, switch can change the output of two NAND gate. It behaves like a switch.

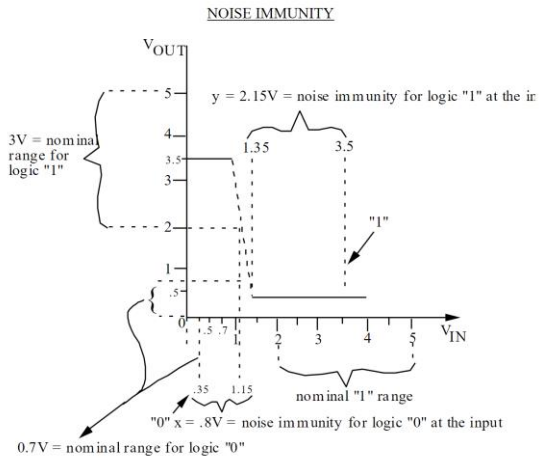




The This feedback output (Q or QN) would cause the output to be stored. When the switch bounce, output will not be determined by the input A and B.
Take connecting to A as an example. If the switch moves back and forth between the contacts. The latch maintains its state because '0' from the bottom NAND gate is fed back. The switch may move between the contacts, but the latch's output ensures it never bangs back and thus switch is bounce free. The same situation occurs when the switch is on B.

8 Answer to the GG 7.1

1. *What is the advantage of a larger noise immunity?*
   The large immunity will increase the stability of the circuit and the output would not be changed easily due to small change of the input.
2. *Why is the last inverter observed rather than simply the first?*
   Because input may contain noise which make the signal is between high signal and low signal. The first inverter can not invert the input signal. We should invert the signal several time to make sure it fall to 0 or increase to 1.
3. *How would you calculate the noise immunity for the inverter?*



Considering ideal inverter, given that the noise immunity for logic 0 will be 1.15 - 0.35 = 0.8 V, and the noise immunity for logic ”1” will be 3.5 - 1.35 = 2.15 V. Since 0.8<2.15. The overall noise immunity of inverter is 0.8.
However, for a real inverter, we should consider input within the nominal range.

4. *If we have two or more LEDs to monitor several signals, why is it a bad practice to share resistors?*
If LEDs are in parallel. Due to the dividing of the current, the current is divided into smaller one which will flow into LED. Each current may be too small to make the LED light and it will have trouble observing the signal when we want to use LED as debugging tool.

9. Conclusions

This lab introduces static hazard. Static hazard may happen because there are delays in some path of the circuit, due to the gate. It will change the output to eliminate static hazard, we can cover all adjacent min-terms in the K-map by adding additional terms. I also learned that mechanical switch may cause bounce in the circuit. I didn’t read that carefully at first. And that is the main reason I can’t operate lab2.1 at first. I learned about debouncer circuit which can solve the previous problem.