**ECE385**

Fall 2023

Experiment #3

**Lab 3**

Haoyu Huang

Lab section: ZY 16/Day & Time: 9.5

Your TA’s Name: Yang Zhou

1. **Introduction**

In this lab, we designed three different types of adders using SystemVerilog.

The first adder that we created was a Ripple Carry Adder. The adders consist of multiple full-adders which have inputs and outputs. They have carry-in, carry-out, input A, and B. Full-adders are connected to adjacent full-adders. The carry-out of previous adders is connected to the carry-in of another full-adder.

The Carry Lookahead Adder uses pre-computed logic expressions for propagating and generating bits (P, G, respectively. Predicting the carry-in in advance will save a lot of time waiting for the rippling of full-adders. Based on the previous carry-in input, propagating bits, and generating bits, the CLA predicts what the carry-out is.

The Carry Select Adder uses two sets of RCA adders for computing two different results with different carry-ins. Then we use a multiplexor to select between a carry-in value of either zero or on.

Ripple Carry Adder

i. Written description

The ripple adder consists of 16 full adders. We design 4-bit adders and connect four of them together. They have carry-in connected to carry-out. The former adder’s cin will wait for the rippled bit which means carry-in will ripple through full-adders. There are three inputs for 16-bit full-adders, A[15:0], B[15:0], and cin. There are two outputs S[15:0], and cout. For 4-bit full—adders, inputs, and outputs are similar, but A, B, and S are four bits.

The logical expression for full-adder are S = A^B^Cin, and c\_out = (A&B) | (A&c\_in) |(B&c\_in). The ripple adder calls the full adder 16 times with the previous c\_out connected to the next c\_in.

**2. Description of Circuit**

**3. Logic Diagrams**

**4. Component Layout**

**5. Answers to Pre-Lab Questions**

**7. Answers to Post-Lab Questions**

**8. Conclusions**