**ECE385**

Fall 2023

Experiment #4

**Lab 4**

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Lab section: ZY 10/Day & Time: 10.2

Your TA’s Name: Yang Zhou

**1.Introduction**

We implement a two's-complement, 16-bit multiplier operate 8-bit multiplications. We use two 8-bit registers A and B, one bit signal X and a nine-bit adder circuit to implement an add and shift algorithm which computes partial multiplications using the adder circuit. The algorithm consists of seven adds, eight shifts, and a subtract step to compute the final product.

**2. Written Description of Modules**

**Module: Hexdriver**(Hexdriver,sv)

Inputs: Clk, Reset, [3:0] in [4]

Outputs: [7:0] hex\_seg, [3:0] hex\_grid

Description: The module takes output bits of registers in the register unit. It will change 3-bits into Hex number and display on the FPGA. The input is array type (each 4-bits) which can take in 16 bits in total. It can convert upper 4bits and lower 4bits of register to each hex display respectively. Output is 8-bits hex\_seg and 4-bits hex\_grid. Hex\_seg is used to display numbers in LED. Every LED has 7 lights. Number can be expressed in 7 bits in LED. For example, 0 can be expressed as 11000000. Hex\_seg [7] is constant 1 in this case. Since FPGA has multiple HEX displays, hex\_grid will instruct the board to use specific displays.

Purpose: The module is used to display Hex numbers on FPGA boards, allowing the user to see the contents of registers A and B.

**Module: reg\_8 (reg\_8.sv)**

Input   Clk, Reset, Shift\_In, Load, Shift\_En, [7:0] D

Output [7:0] Data\_Out, Shift\_out

Description: The module implements the 8-bit register in block diagram.  The module is a positive edge clock-triggered 8-bit register. When the reset signal is high, the register is initialized with zeros. When the load signal is high, D [7:0] is loaded into the register.

Purpose: The 8-bit register store A and B value. It will be instantiated in register unit. The sum value will be loaded into register A.

**5. Answers to Pre-Lab Questions**

**6. Answers to Lab Questions**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Function | X | A | B | M | Next Step |
| Reset | 0 | 0000 0000 | 0000 0111 | 1 | ADD SW to A |
| ADD | 1 | 1100 0101 | 0000 0111 | 1 | Shift XAB |
| Shift | 1 | 1110 0010 | 1000 0011 | 1 | ADD SW to A |
| ADD | 1 | 1010 0111 | 1000 0011 | 1 | Shift XAB |
| Shift | 1 | 1101 0011 | 1100 0001 | 1 | ADD SW to A |
| ADD | 1 | 1001 1000 | 1100 0001 | 1 | Shift XAB |
| Shift | 1 | 1100 1100 | 0110 0000 | 0 | Shift 5 times: the last 5 bits are 0 |
| Shift 5 times | 1 | 1111 1110 | 0110 0011 | 1 | No need to ADD |

**7. Answers to Post-Lab Questions**

**8. Conclusions**