17091 PS2

Digital Power Conversion Using dsPIC® DSCs: Power Factor Correction

Class Objectives

- ## **When you finish this class you will:**
  - Understand what Power Factor Correction (PFC) is and its significance
  - Be able to identify different PFC topologies and their design implementations
  - Understand implementation of digital PFC
  - Know how to improve PFC performance through advanced adaptive control techniques

Agenda

- **Power Factor and its Significance**

- **How to Achieve Power Factor Correction**

- **Overview of Different Boost Type PFC Designs**

- **Digital PFC Using the dsPIC$^{®}$ DSC**

- **Advanced PFC Techniques**

- **Overview of 720W AC-DC Reference Design**

What is Power Factor?

- Power factor for an AC powered system is defined as the ratio of the real power flowing to the load, to the apparent power in the circuit.

$$PF = \frac{Real\ Power}{Apparent\ Power}$$

- PF is a dimensionless number between 0 and 1.
    - Power Factor is unity (1) when the voltage and current are in phase.
    - For two systems with the same real power, the system with the lower PF will have higher circulating currents (higher apparent power)
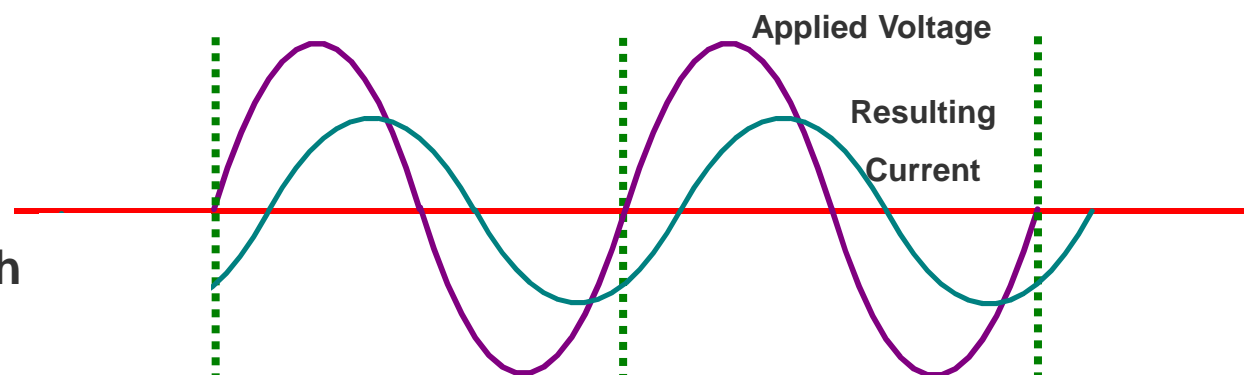
What is Power Factor?
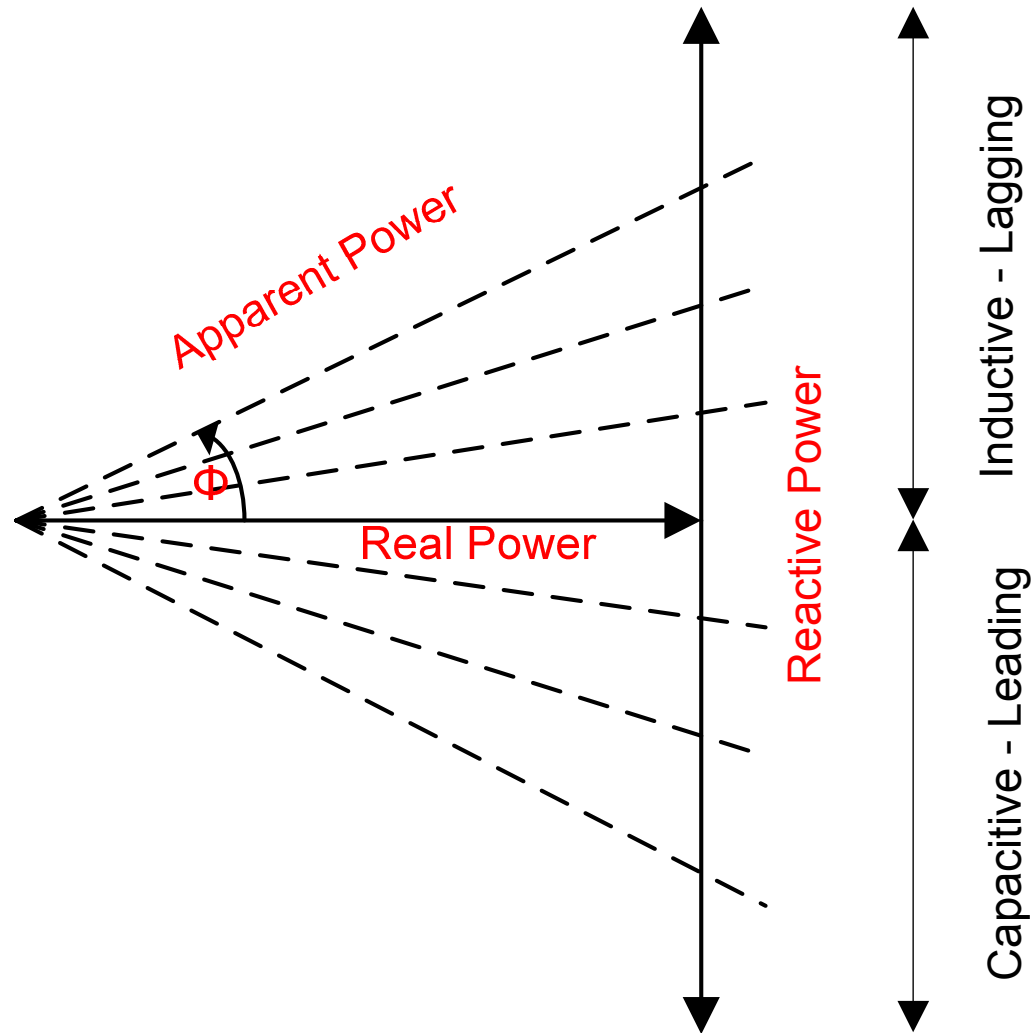
$$PF = \frac{Real\ Power}{Apparent\ Power} = \cos\emptyset$$

Applies for ideal sinusoidal waveforms for both voltage and current
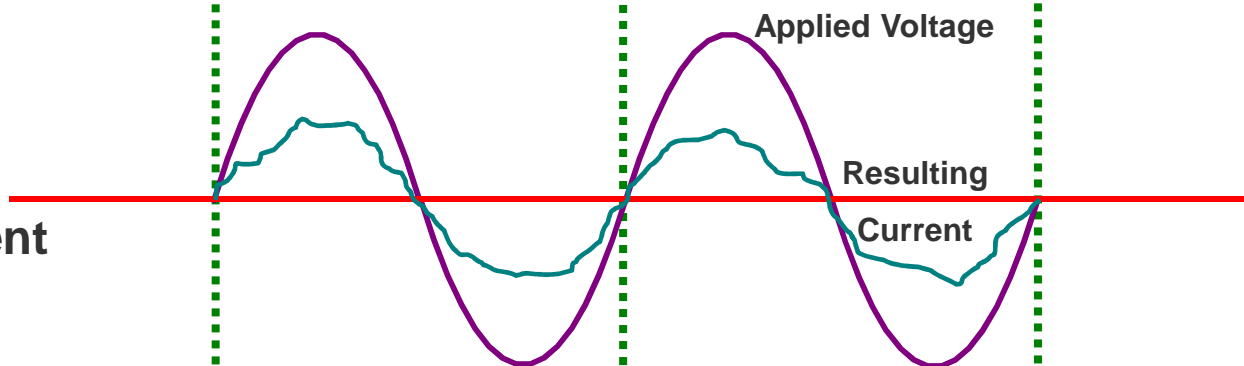
Examples of PF Degradation
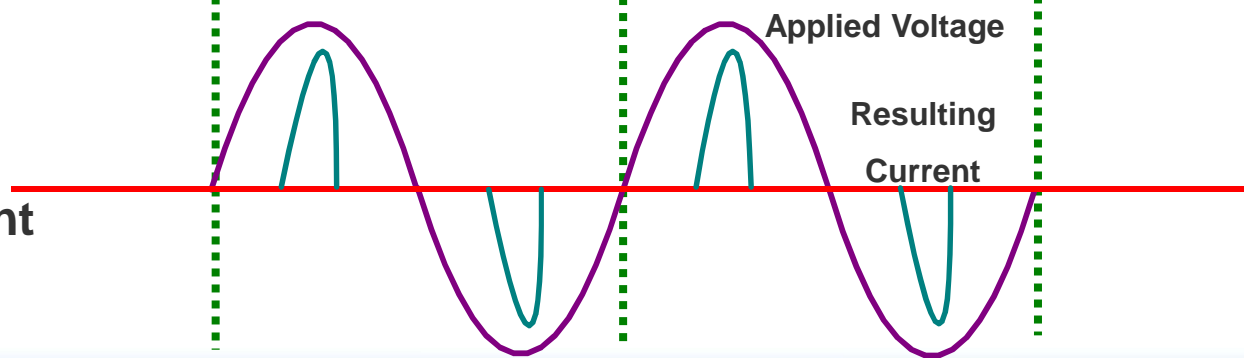
Case 1

Sinusoidal Current with phase shift

Applied Voltage

Resulting Current

Case 2

Semi-Sinusoidal Current with no phase shift

Applied Voltage

Resulting Current

Case 3

Non-Sinusoidal Current with phase shift

Applied Voltage

Resulting Current

Measuring Power Factor

Added Reactive Power due to distortion $\longrightarrow$ Not present when load is linear

Reactive Power
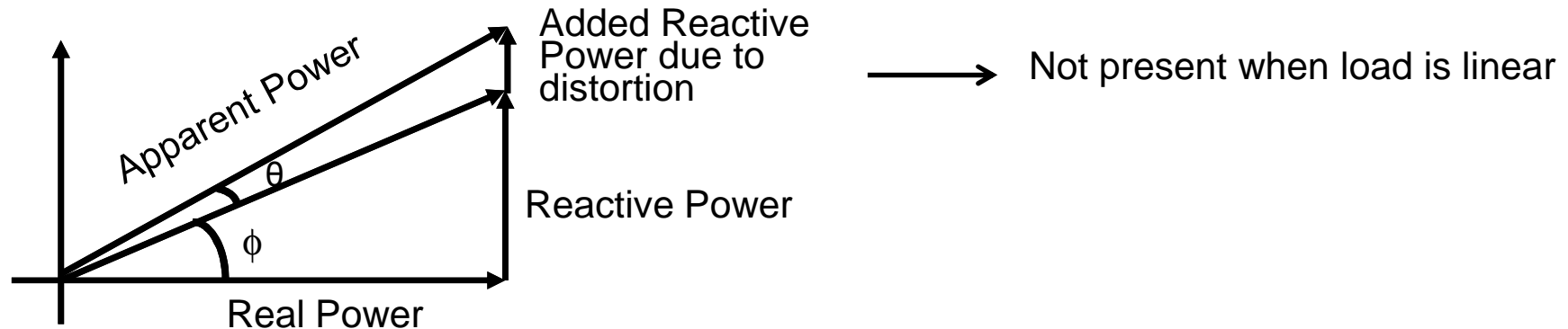
Real Power

Displacement factor = Real Power / apparent power = cos ϕ

Distortion Factor accounts for non-sinusoidal currents

$$\text{Power Factor} = \cos \phi * \underbrace{\sqrt{\frac{1}{1 + (I_2 / I_1)^2 + (I_3 / I_1)^2 + \ldots}}}_{\text{Distortion factor}} = \frac{\cos \phi}{\sqrt{1 + THD^2}}$$

$\underbrace{\cos \phi}_{\text{Displacement factor}}$

THD: Total Harmonic Distortion

Why Implement PFC?

- **Reduce Energy Loss**
  - Losses in active/passive elements
  - Losses in transmission and distribution
    - Energy needed by reactive elements

- **Reduce Cost**
  - Power generation, transmission and distribution capacities need to be over-sized
  - Power losses in the distribution system resulting in voltage sags, over-heating and even premature failure of equipment
  - Components with higher ratings needed for sustaining high harmonic peak currents

- **Regulation Requirements (i.e. EN61000-3-2)**
  - Limits up to the 40th Current harmonic are imposed
  - Applies to equipment greater than 75W and less than 1000W
  - Equipment with <= 16A per phase, 230V line voltage

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- Overview of Different Boost Type PFC Designs

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- Advanced PFC Techniques

- Overview of 720W AC-DC Reference Design

SMPS Without PFC

Off-line switch-mode power supply
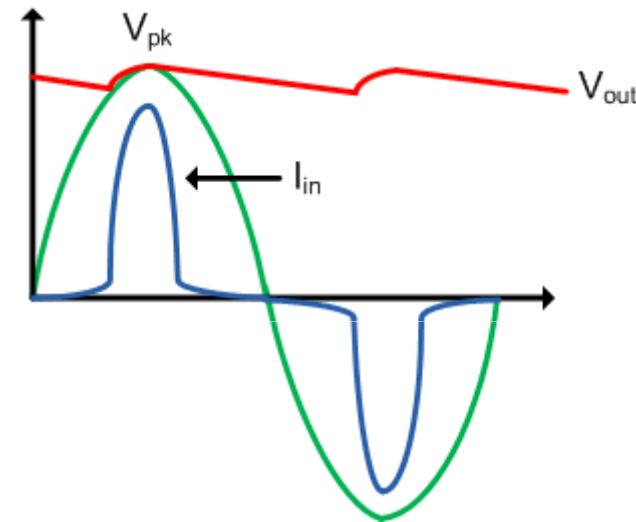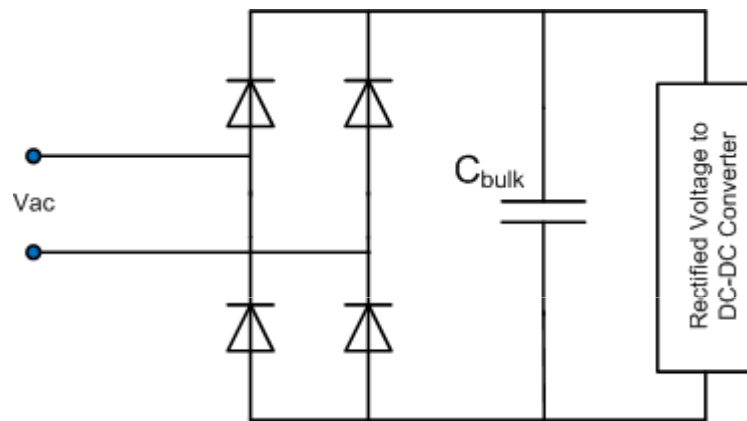
- C_{bulk} must be large enough to reduce voltage ripple and meet specified holdup requirements

- Restoring capacitor current occurs near the peak of AC input ($V_{ac} > V_{out}$), resulting in large current spikes

Adding PFC

- Recap -> We want to shape the input current to follow the input voltage (resistive load) to maximize real power available

- Two methods available:

  - Passive Power Factor Correction

  - Active Power Factor Correction

    - Low frequency

   - High Frequency – Main focus for this class
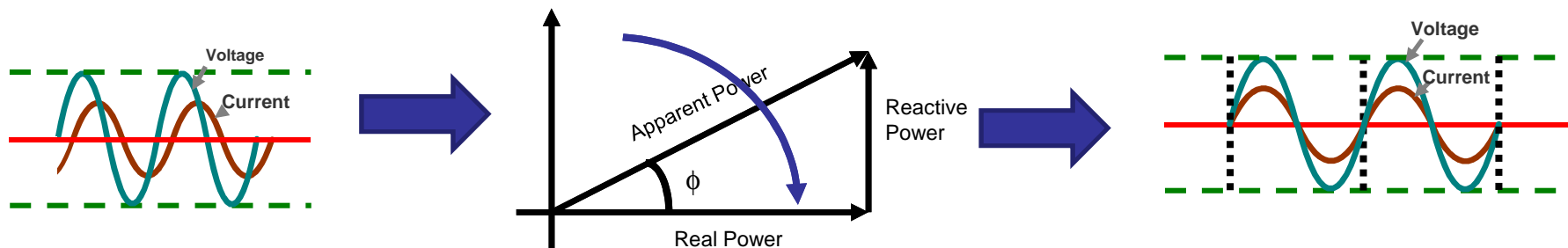
Passive PFC

- Passive PFC circuits incorporate passive filter components (inductor and capacitors) to compensate for the inherent power factor of the circuit (load).

- Pro's of Passive PFC
    - Common and simplest form of PFC
    - Cost effective at lower power ranges
    - Not a source of EMI

- Con's of Passive PFC
    - Poor PF: 0.7-0.8 (for SMPS applications)
    - Filter elements are large (AC line frequency)
    - Output rail voltage not regulated
    - High losses

Passive PFC Example

A 500W AC Induction motor connected to 208V 60Hz line voltage shows a PF of 0.65 (lagging). What capacitance is required to correct the phase shift and give unity PF?
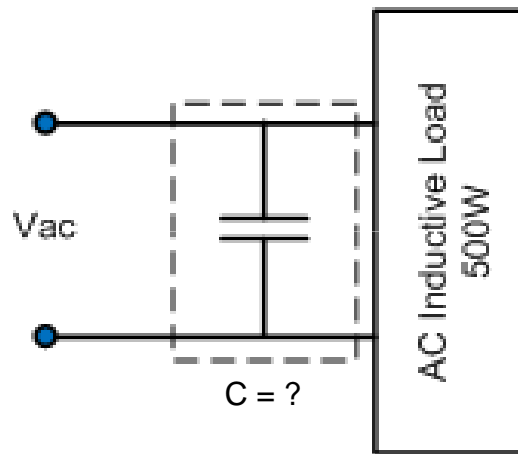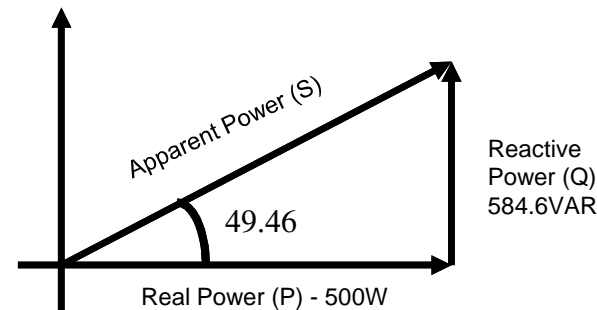

$$\cos^{-1} PF = \emptyset \qquad \emptyset = 49.46°$$

$$Q = P * \tan(\emptyset) \qquad Q = 584.6 VAR$$

$$X_c = \frac{V^2}{Q} \qquad X_c = 74 ohm$$

$$C = \frac{1}{2\pi f * X_c}$$

$$C = 35.8 uF$$

Apparent Power (S)

Reactive Power (Q) 584.6VAR

49.46

Real Power (P) - 500W
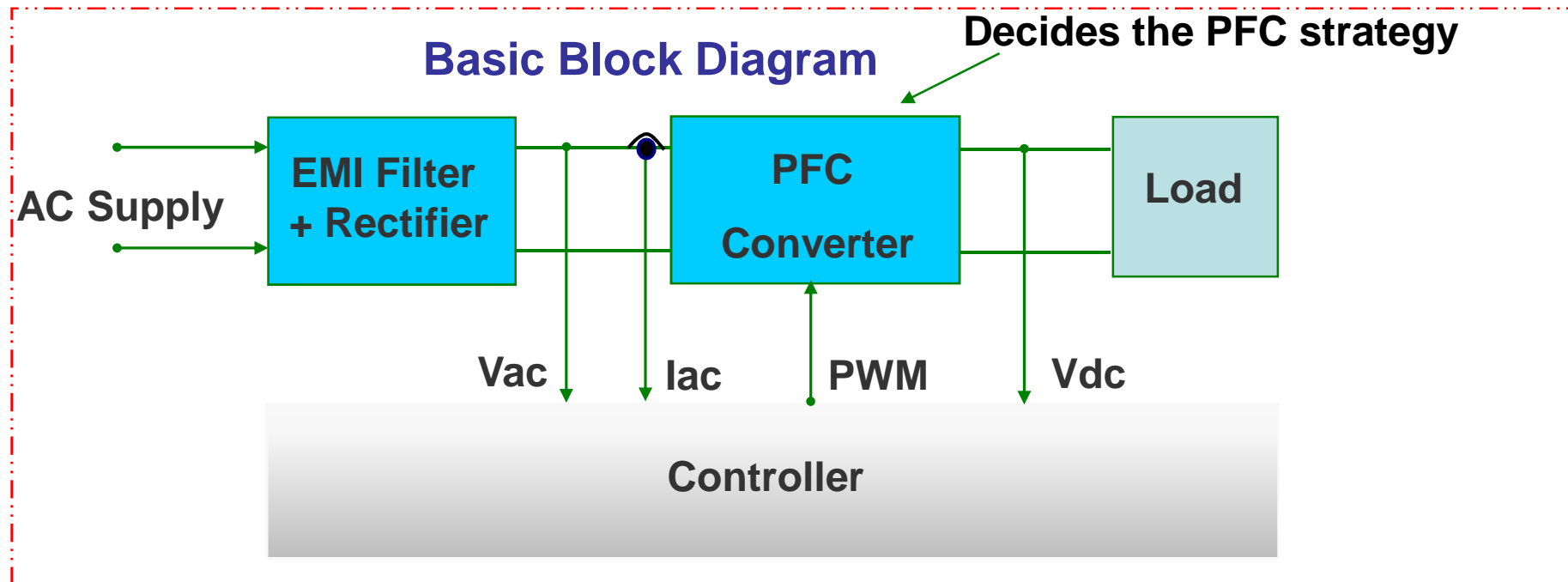
Active PFC

- An active power factor correction circuit uses feedback circuitry along with a switch mode converter (high switching frequency) to change the wave shape of the current drawn to improve the power factor.

- Implemented in most switch mode power supplies

- Con's of Active PFC
    - Complexity
    - More expensive but smaller form factor

- Pro's of Active PFC
    - PF up to 0.998
    - Very low THD (corrects for distortion and displacement)
    - Corrects for AC input voltage (universal mains)
   - Regulated output voltage

Active PFC Block Diagram

Basic Block Diagram

Decides the PFC strategy

```
AC Supply → [EMI Filter + Rectifier] → [PFC Converter] → [Load]
```

Vac   Iac   PWM   Vdc

Controller

Typical Active PFC Requirements:
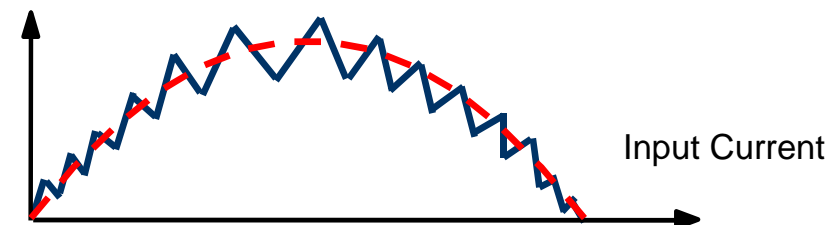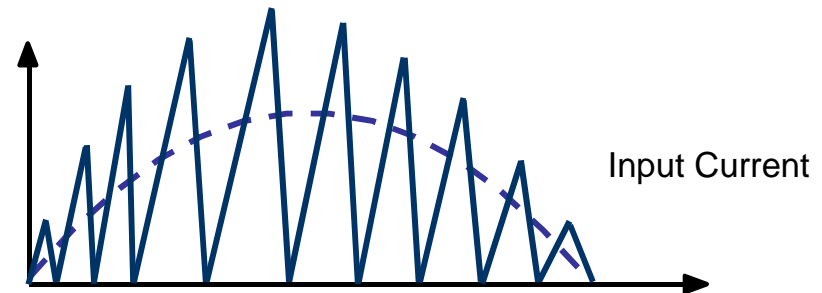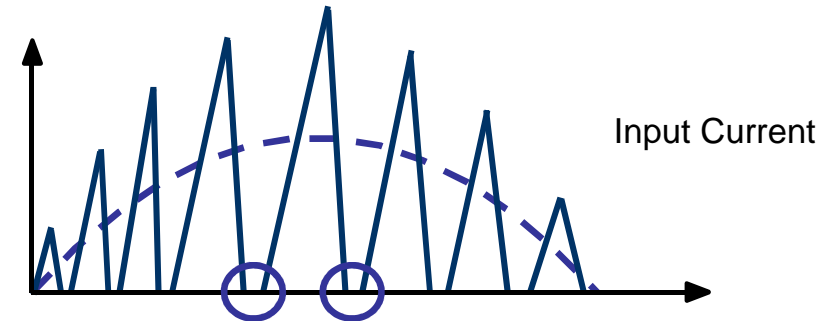- Feedback Voltage
- Input Voltage/Current
- Compensation network (controller)
- PWM

Active PFC Solutions

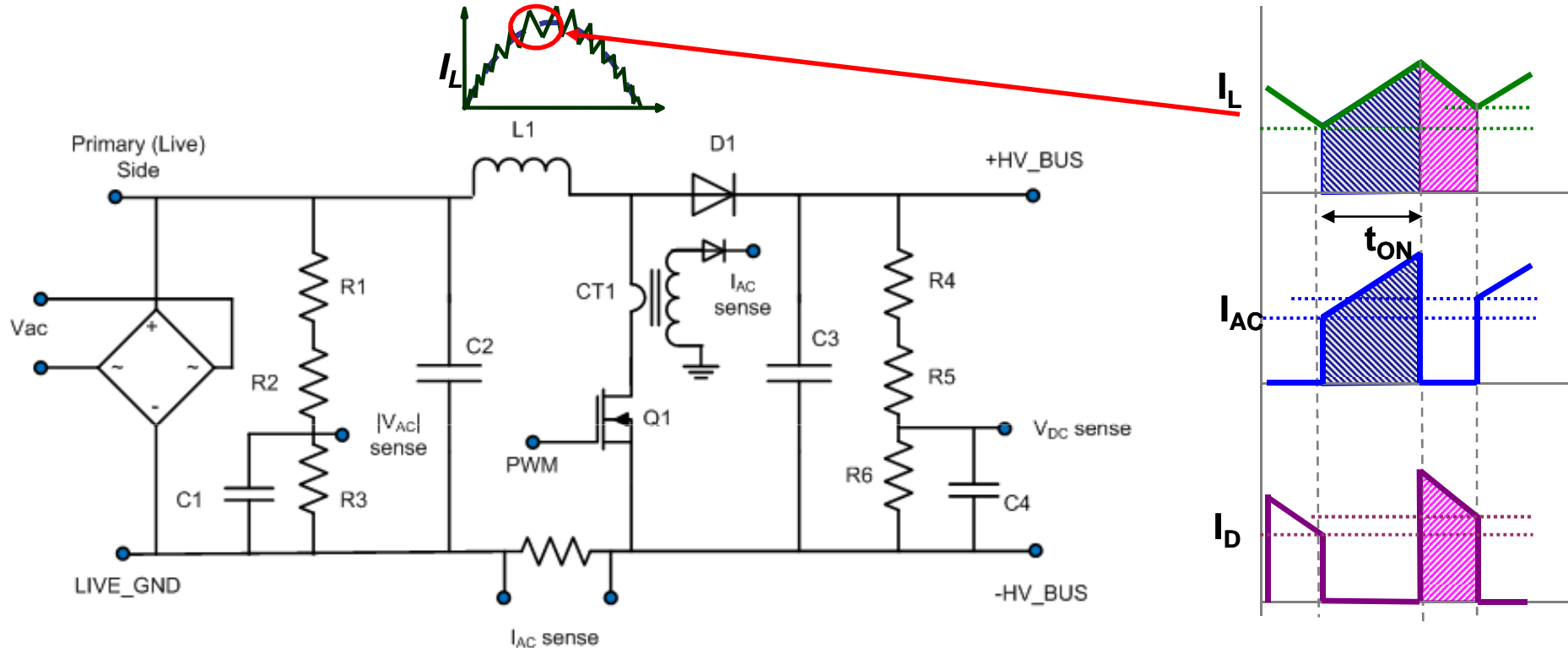### Buck Converter

Boost Converter

Buck-Boost Converter
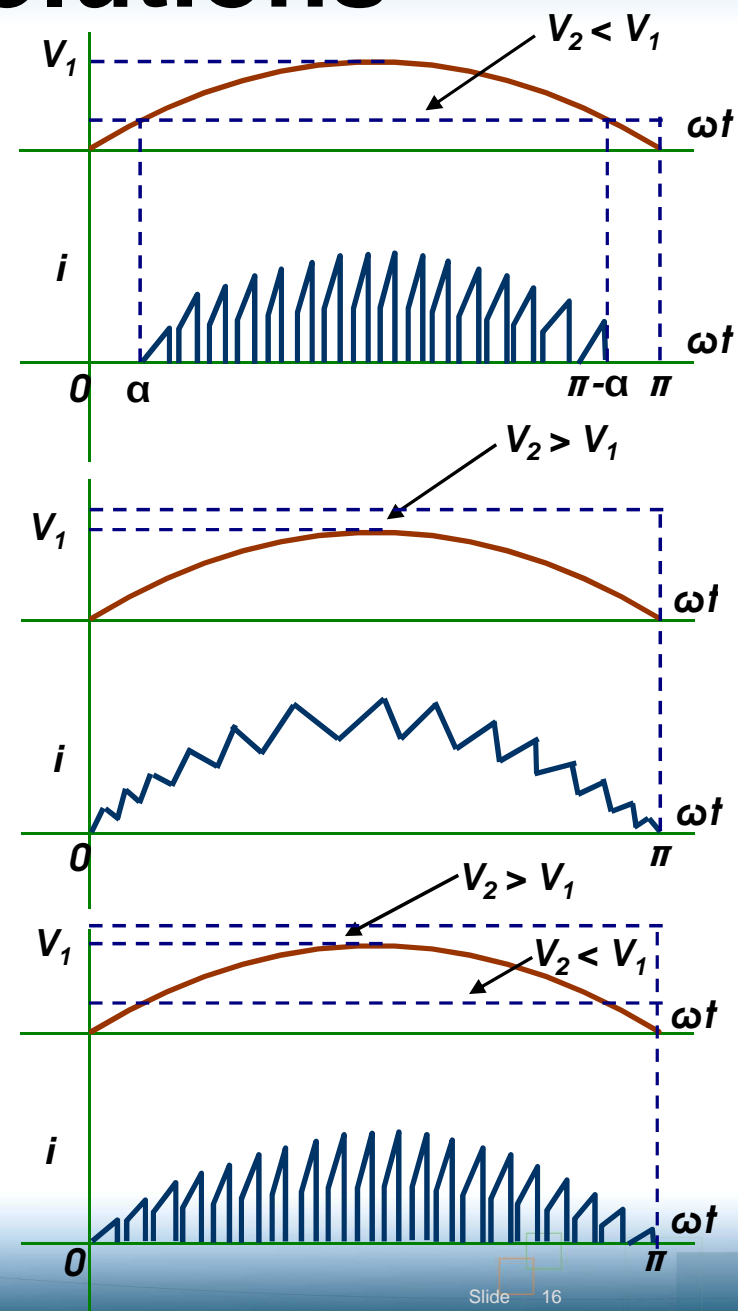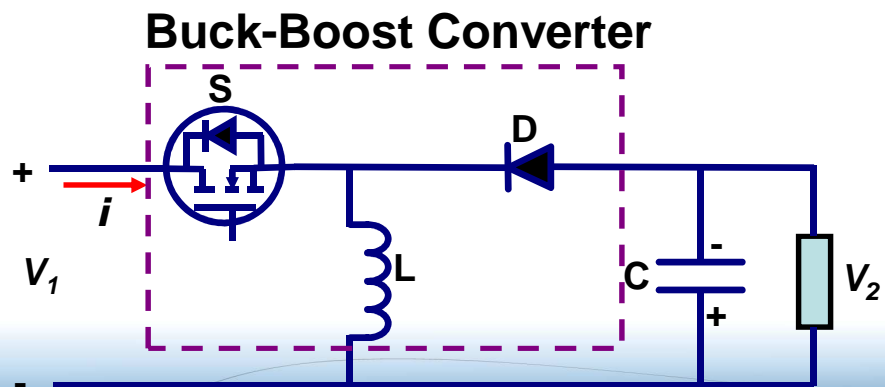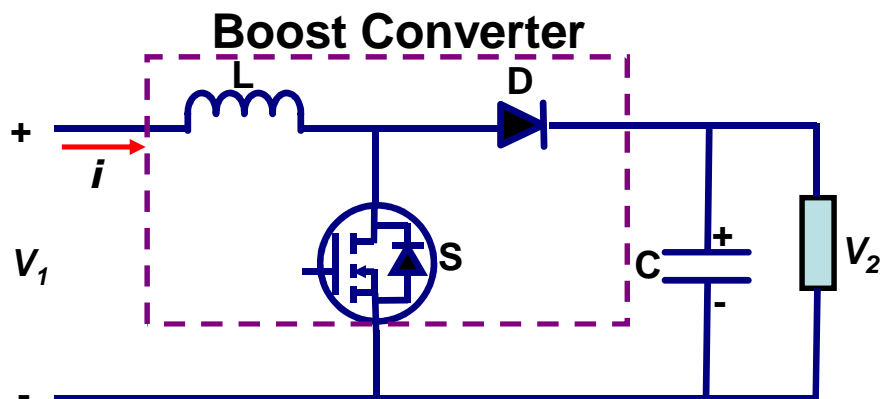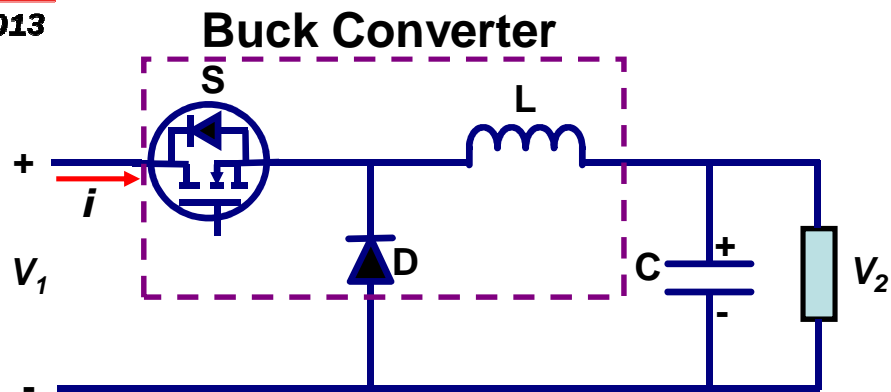
Boost Converter Operating Modes

- **Discontinuous Conduction Mode**

  Input Current

- **Critical Conduction Mode**

  Input Current

- **Continuous Conduction Mode**

  Input Current

Active PFC Example

Average Current Mode Control

The average current through the inductor is made to follow the input voltage profile to improve Power Factor and minimize current harmonics

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Interleaved PFC
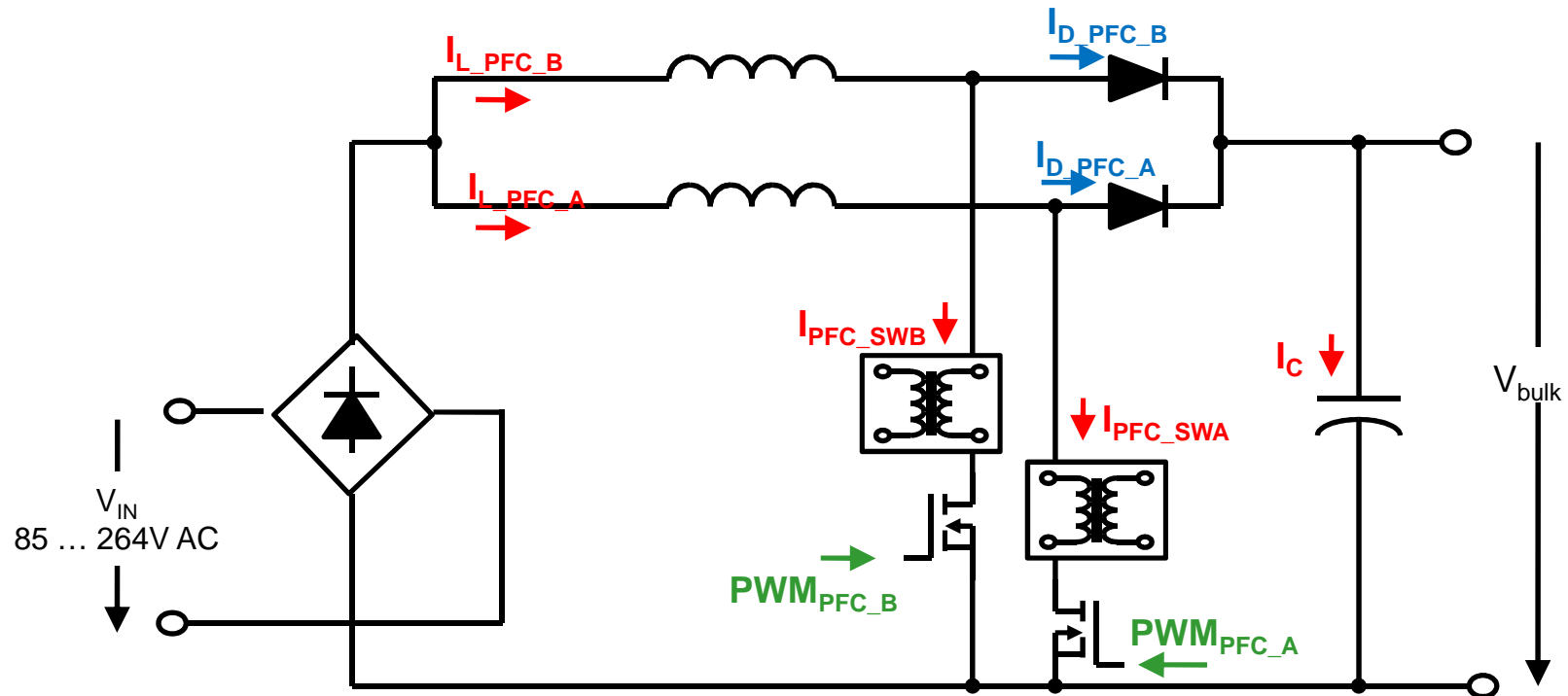
- Two independent boost converters connected in parallel operating 180° out of phase
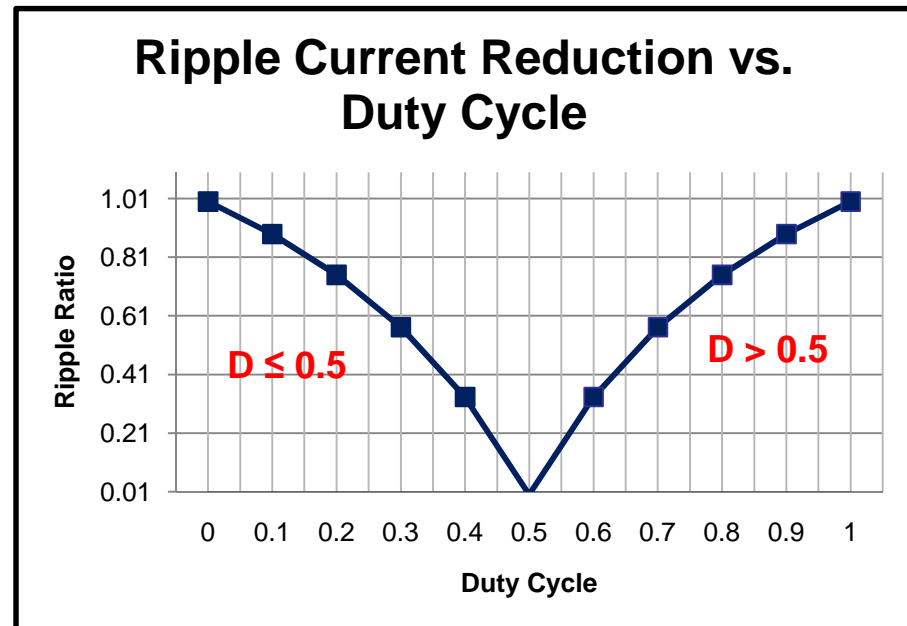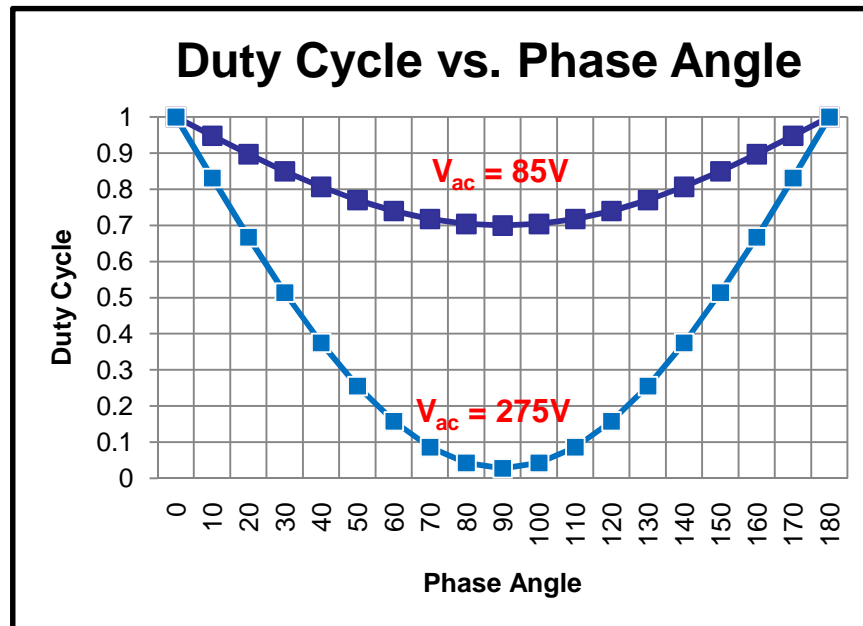- Great for high power applications with size constraints
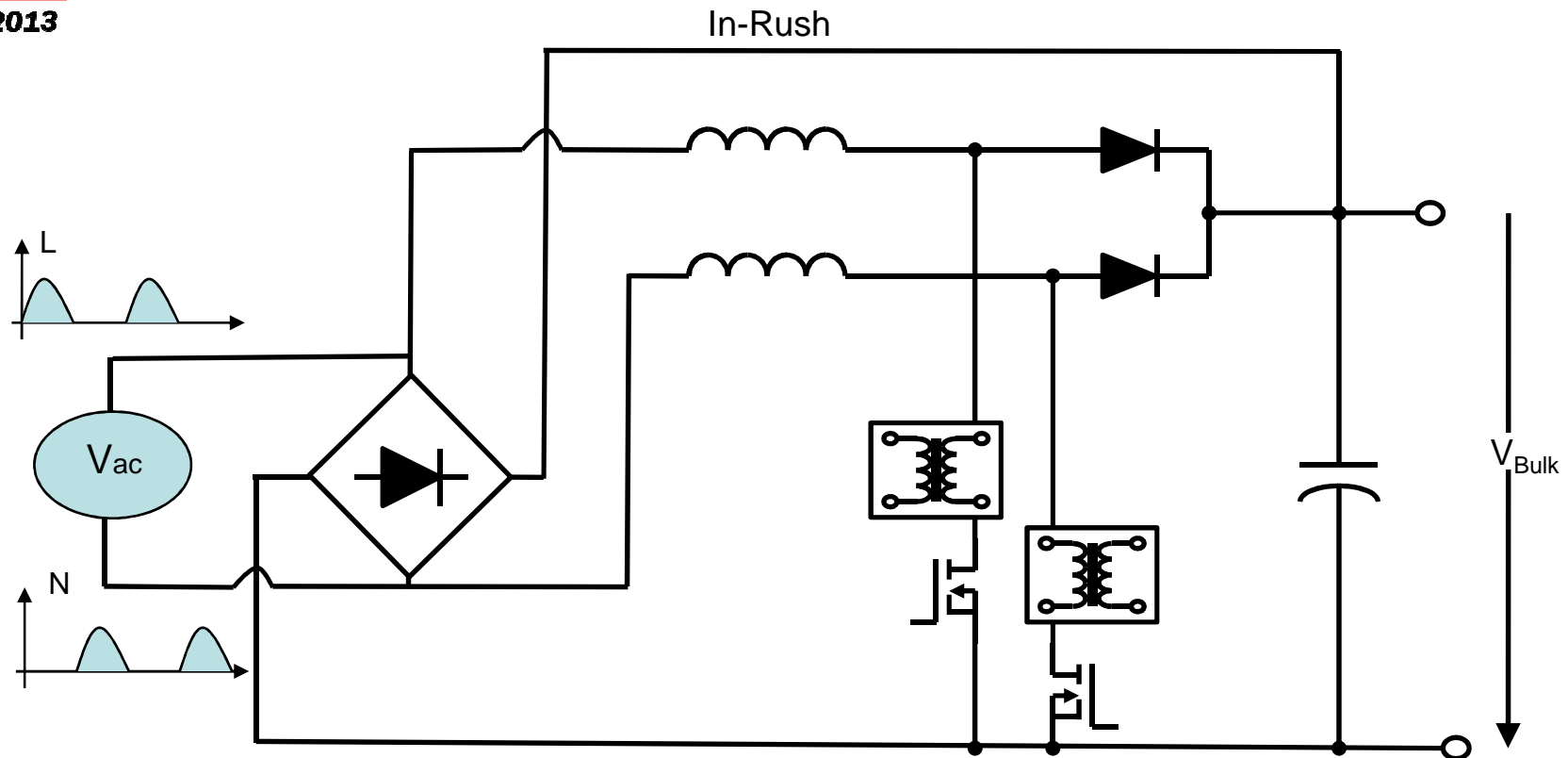
Benefits of IPFC
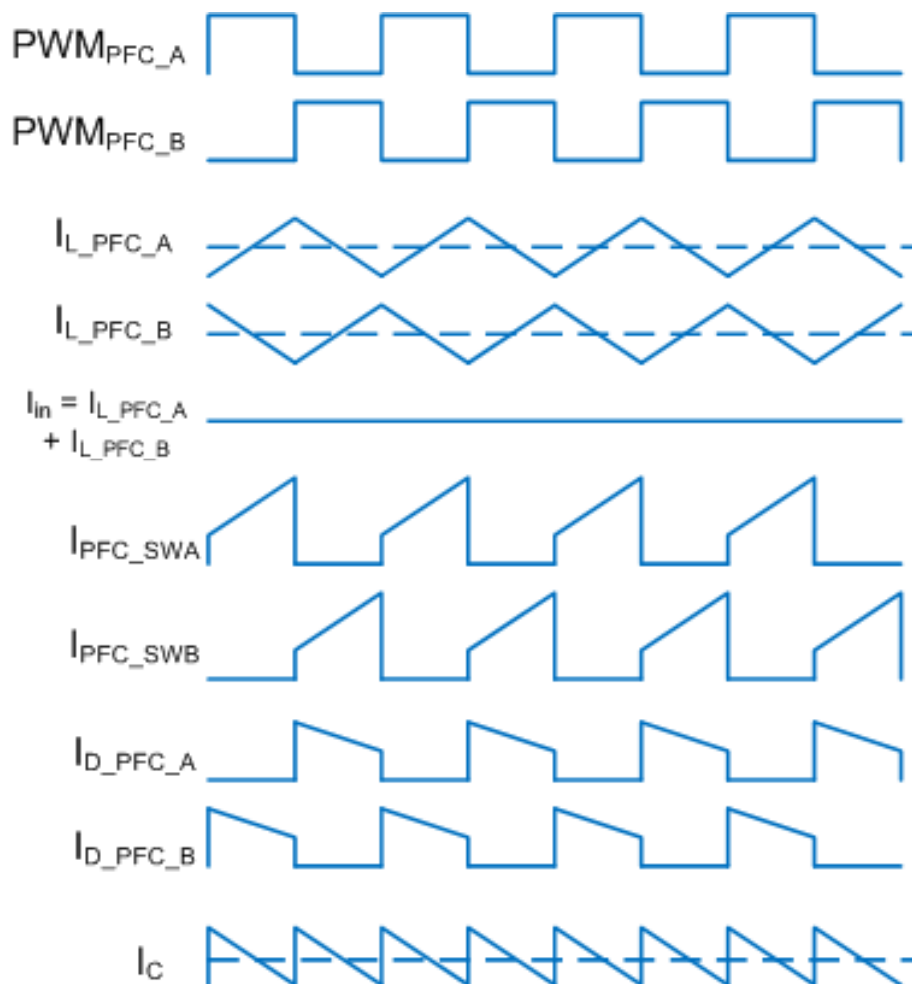
- Inductor ripple currents are out of phase and tend to cancel each other out. Best current ripple cancellation occurs at 50% duty cycle.

- Inductors stored energy requirement is ½ that of single phase PFC (reduction in magnetic volume)

- Interleaving also reduces the output capacitor ripple current

- Higher efficiency

IPFC Ripple Cancellation

- Maximum ripple current will occur at the peak of the minimum input voltage (85V_{ac}).
    - Duty Cycle of ~70% yields an input current ripple that is ~60% of the inductor ripple current

Duty Cycle vs. Phase Angle

$V_{ac} = 85V$

$V_{ac} = 275V$

Ripple Current Reduction vs. Duty Cycle

D ≤ 0.5   D > 0.5

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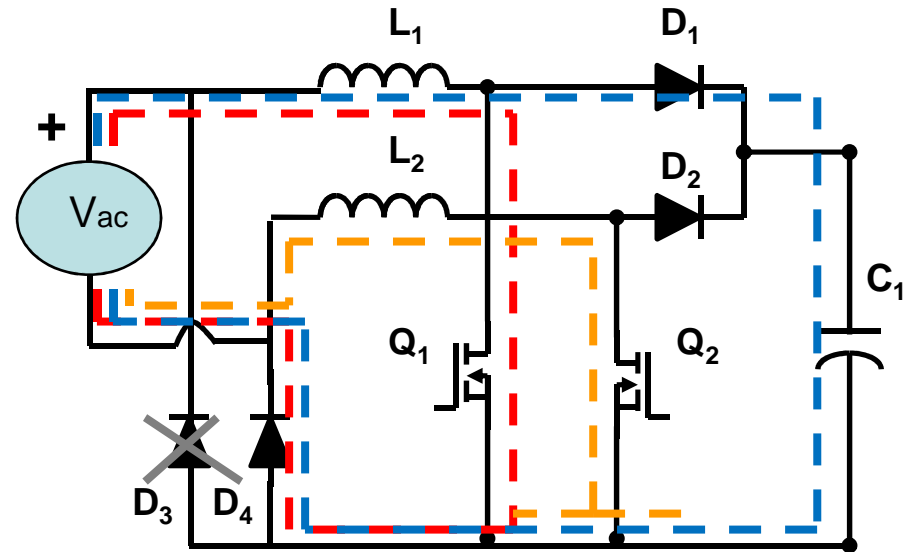
Semi-Bridgeless PFC

- **Also known as two/dual phase PFC**
- **AC input directly connected to Boost Inductors**
- **Two diodes in bridge rectifier used for In-Rush Current protection at Start-up. Other two diodes link PFC ground to input line**
- **Both phases can be driven simultaneously or in the case of digital control and to improve efficiency each phase is active when L/N is active**
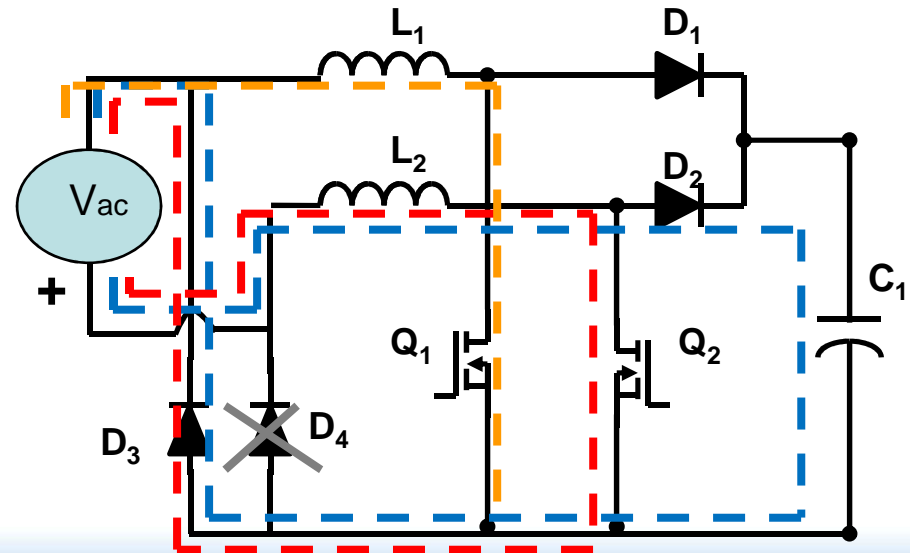
Semi-Bridgeless PFC

Case 1: Line Positive

- MOSFET Q1 switches
- Diode D3 Reversed Biased
- Current returns through D4 **and** through body diode Q2 and L2 (introduces new MOSFET losses)

Case 2: Neutral Positive

- MOSFET Q2 switches
- Diode D4 Reversed Biased
- Current returns through D3 **and** through body diode Q1 and L1

Semi-Bridgeless PFC Efficiency Improvements

- For universal input voltage range the peak current through the diode bridge occurs at 85V$_{ac}$.

- The total bridge consumes ~2% of the input power at low line and about 1% at high line.

- If we eliminate one diode then we could gain ~1% efficiency at low line.
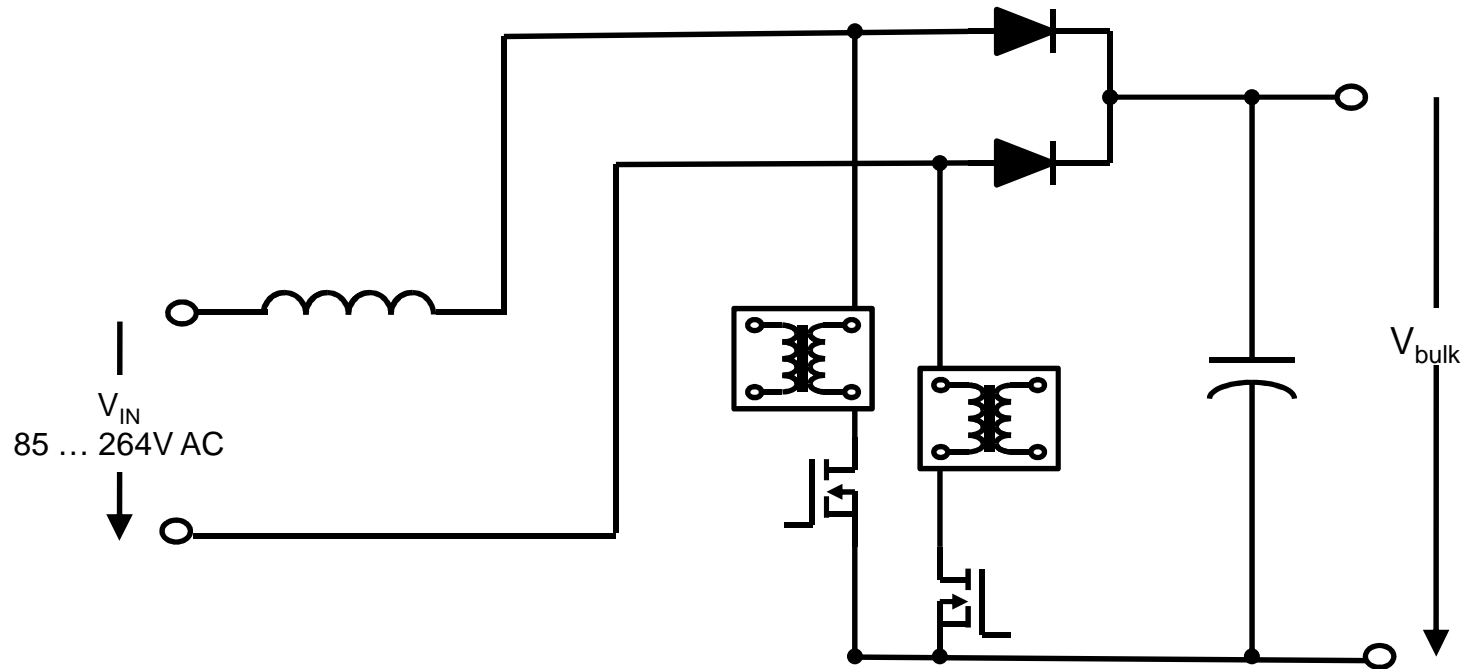
$$I_{D\_avg} = \frac{2}{\pi}\sqrt{2} * I_{line\_rms}$$

$$P_D = \frac{4\sqrt{2} * V_f * P_{out}}{\pi * \eta * V_{line\_rms}}$$

$$I_{line\_rms} = \frac{P_{out}}{\eta * V_{line\_rms}}$$

$$P_D = 2.1\% * \frac{P_{out}}{\eta}$$

Bridgeless PFC

- **Efficiency is improved as the diode bridge is completely eliminated but MOSFET losses will increase**

- **Line is floating compared to PFC ground so simple circuitry (resistor divider network) to sense the input voltage can not be used. Instead an opto-coupler based circuit or low frequency transformer has to be used.**

- **EMI is difficult to reduce as more parasitic capacitance contribute to common mode noise.**
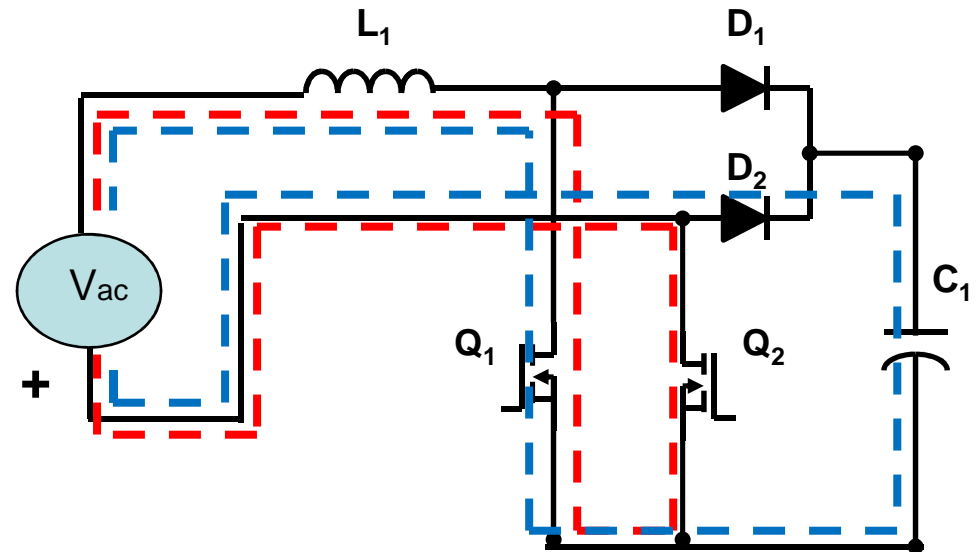
Bridgeless PFC

Case 1: Line Positive
- MOSFET Q1 switches
- Current returns through Q2
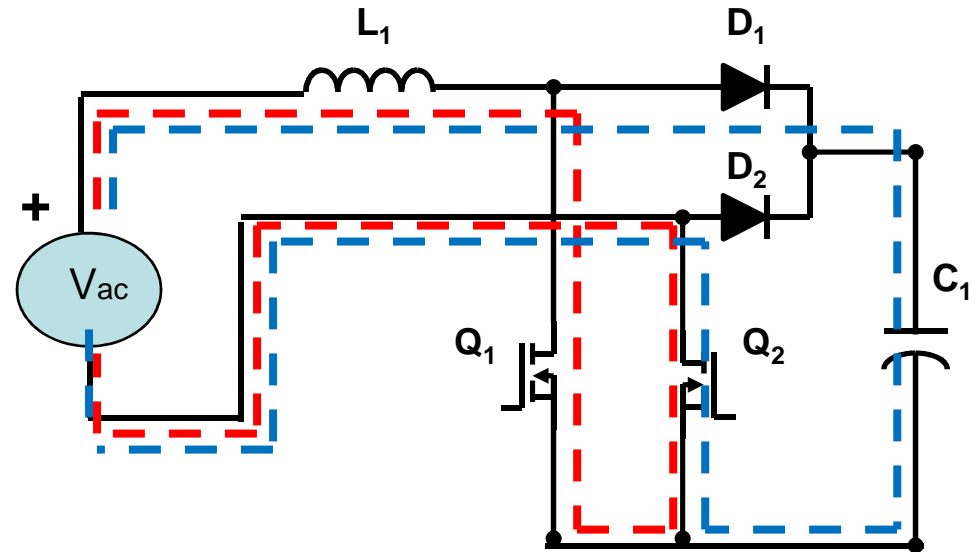
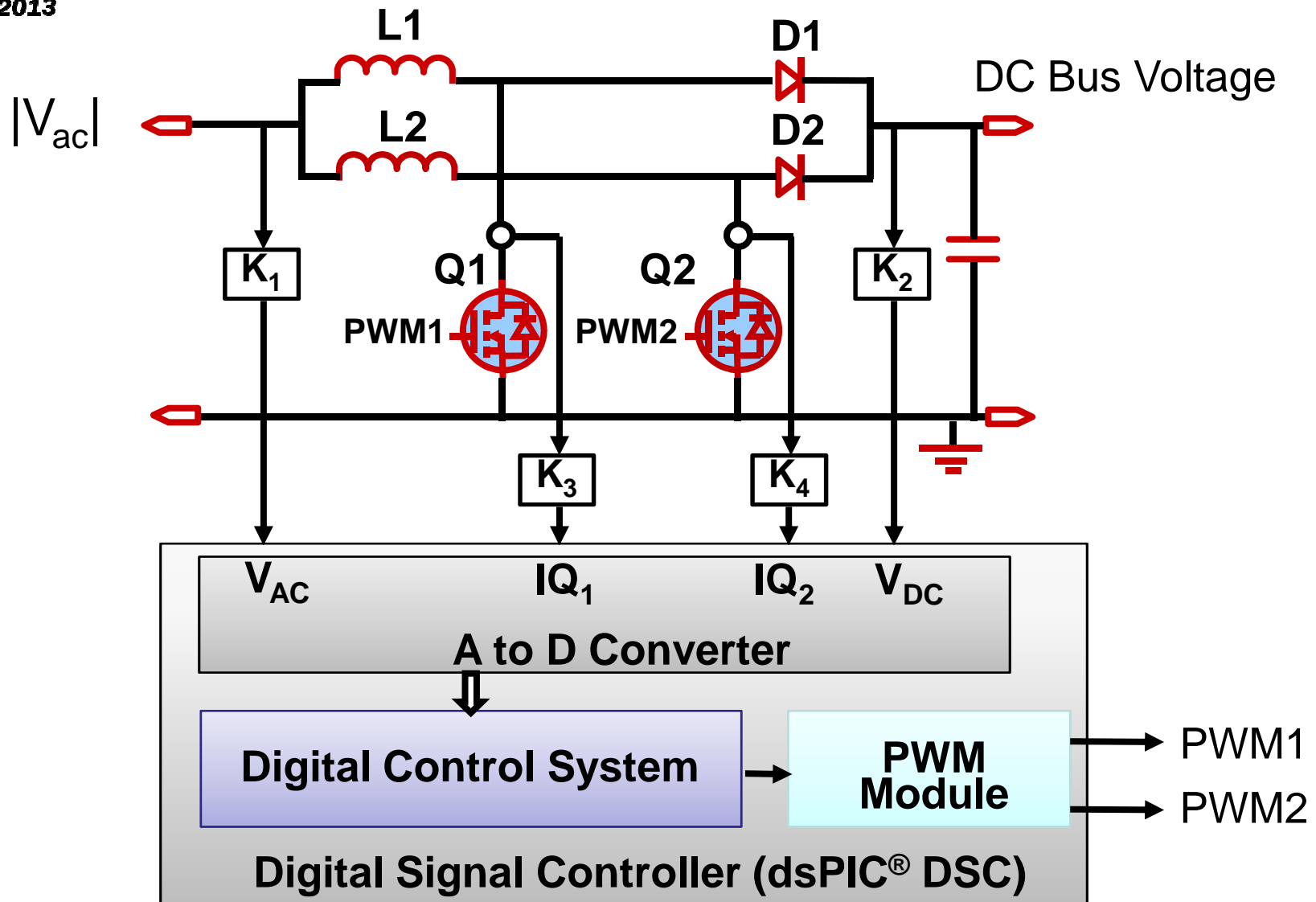**Case 2: Neutral Positive**
- MOSFET Q2 switches
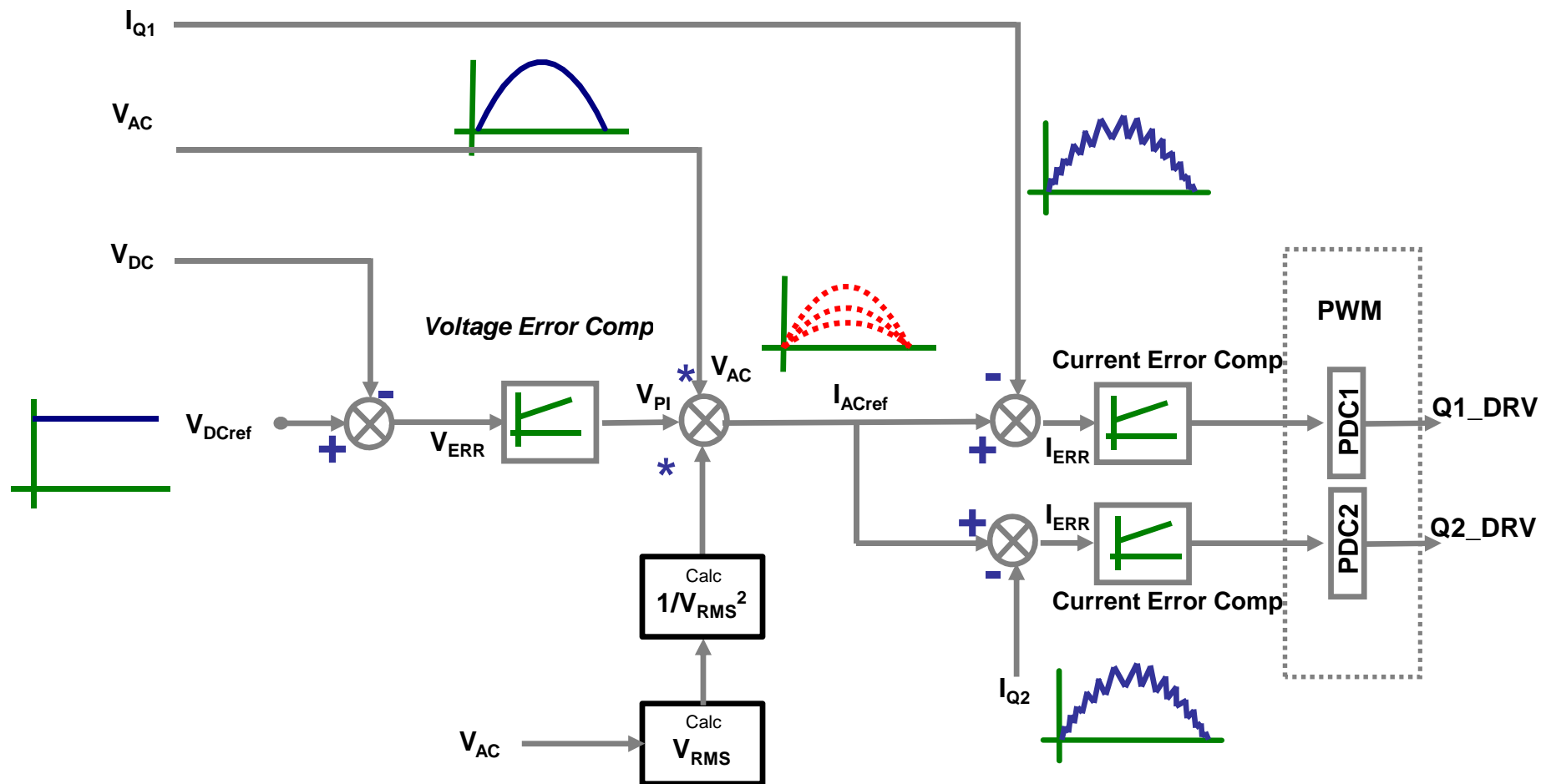- Current returns through Q1

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Digital Implementation - IPFC

IPFC Control Scheme

Voltage Compensator

PI Compensator

$$k_p * V_{ERR}$$

$$k_i \int V_{ERR}(n)$$

$V_{DCref} = 805$ V_{ERR} **x32** V_{ERR} (Q15)   **+**   U(n)

Clamp to 0

U(n) < 0

V_{PI}

+   **-**

V_{DC_sense}
(10-Bit)

Kp and Ki are Q15

$V_{DC} = 400V$

470kΩ

470kΩ

470kΩ

120kΩ

V_{DC_sense}

10kΩ
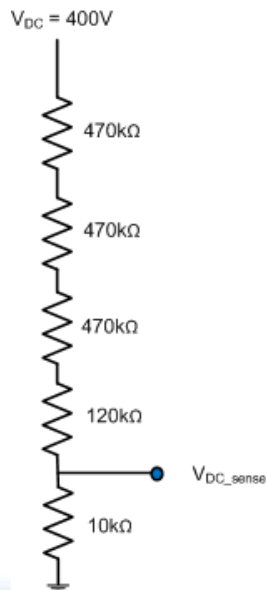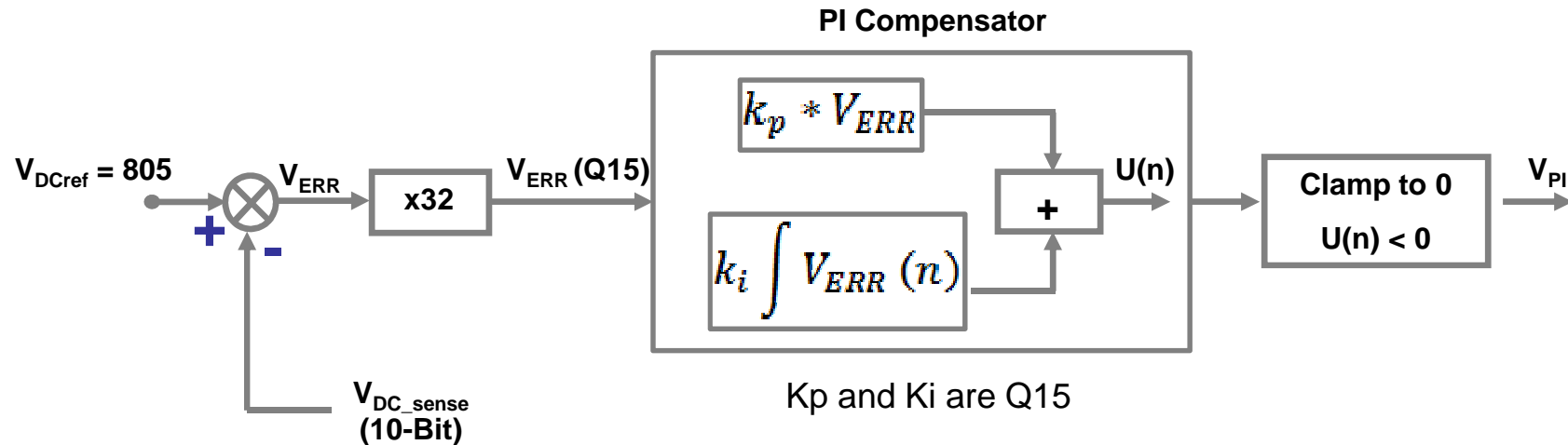
Find V_{DCref} by determining the base voltage that gives 3.3V on the ADC pin

$$V_{base} = \frac{V_{ADC\_MAX}}{G_{R\_DIV}} = \frac{3.3V}{\frac{10}{1540}} = 508.2V$$
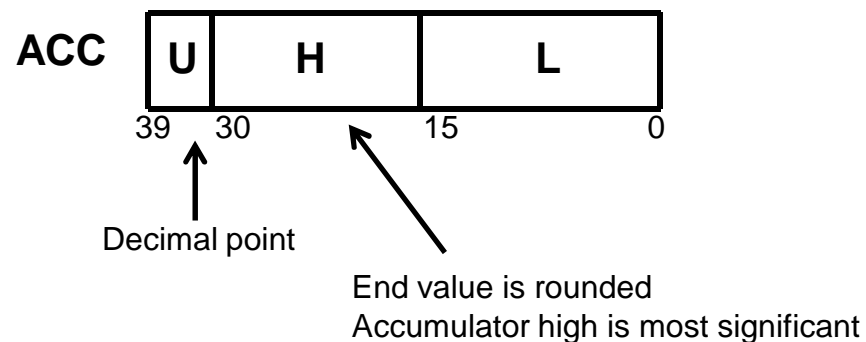
$$V_{DCref} = \frac{V_{DC}}{V_{base}} * 2^{10} = 805$$

Voltage Compensator Cont.

```
typedef struct {
    int Ki;
    long sum; // integrator sum
    int Kp;
    int psc;  // output postscaler
    int out; // unscaled output
} tPI32;
```

MAC = Multiply and accumulate

Accumulator += (Q15 * Q15)

Q15 * Q15 = 2.30

ACC

U	H	L
39 30	15	0

Decimal point

End value is rounded
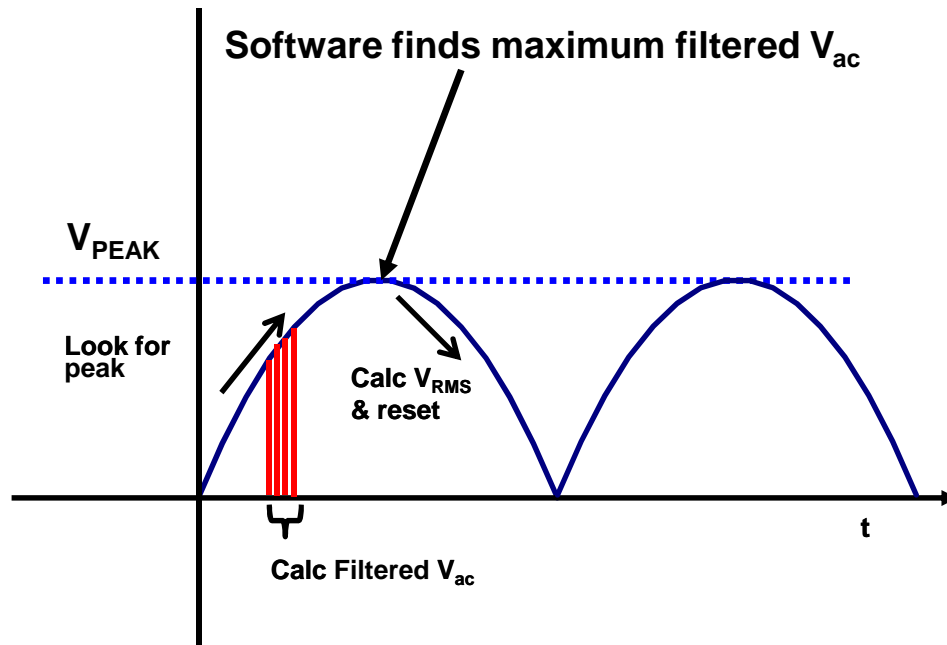Accumulator high is most significant

```
_PI32:
; Input:
;   w0 = address of tPI32 data structure
;   w1 = reference value
;   w2 = control input
;
;   Return:
;   w0 = control output

;save working registers
push    w8
push    CORCON          ;prepare CORCON for fractional computation
fractsetup      w8

sub.w   w1, w2, w4      ;w4 = error
sl      w4, #5, w4      ;error *= 32
mov     w0, w8          ;w8 = &PI
disi    #11             ;disable interrupts for next 11 cycles
clr     b, [w8]+=4, w5  ;w5 = Ki, w8 = &sum_hi
lac     [w8--], b       ;b = sum_hi, w8 = &sum_lo
mov     [w8], w0        ;w0 = sum_lo
mov     w0, ACCBL       ;accbl = w0 = sum_lo
mac     w4*w5, b        ;b += Ki*error
mov     ACCBL, w0       ;w0 = accbl
mov     w0, [w8++]      ;sum_lo = w0 = accbl, w8 = &sum_hi
sac     b, [w8++]       ;sum_hi = b, w8=&Kp
clr     a, [w8]+=2, w5  ;w5 = Kp, w8 = &psc
mac     w4*w5,b         ;b += Kp*error
sac.r   b, w0           ;w0 = result
btsc    w0, #15         ;skip next instruction if w0>=0
mov     #0, w0          ;clear result if negative

pop     CORCON          ;restore CORCON.
pop     w8              ;restore working registers.
return
```

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Input Voltage RMS

Software finds maximum filtered V_{ac}

V_{PEAK}

Look for peak

Calc V_{RMS} & reset

Calc Filtered V_{ac}

t

RMS Voltage : $V_{RMS} = V_{pk} * 0.707$

Measure V_{ac}: 19.2kHz
Filtered V_{ac}: 4.8kHz (~50 samples per half wave)

```
if((uin_filter_input > uin_filter_max) && (peakDetectFlag == 1))
{
    uin_filter_max = uin_filter_input;
}

if(uin_filter_input > uin_filter_input_last)
{
  upcnt++;
  downcnt = 0;

  if((upcnt >= 5) && (peakDetectFlag == 0))
  {
    peakDetectFlag = 1;
  }
}
else if(uin_filter_input < uin_filter_input_last)
{
  upcnt = 0;
  downcnt++;

  if((downcnt >= 5) && (peakDetectFlag == 1))
  {
    peakDetectFlag = 0;
    uin_filtered_peak =
            MUL16SX16FU(uin_filter_max, 46341u)>>2;
    uin_filter_max = 0;
  }
}

uin_filter_input_last = uin_filter_input;
```
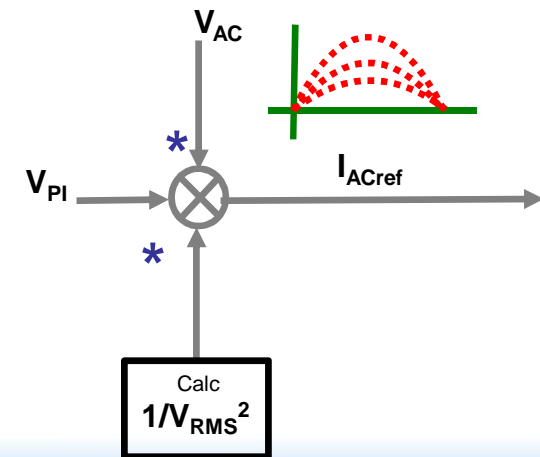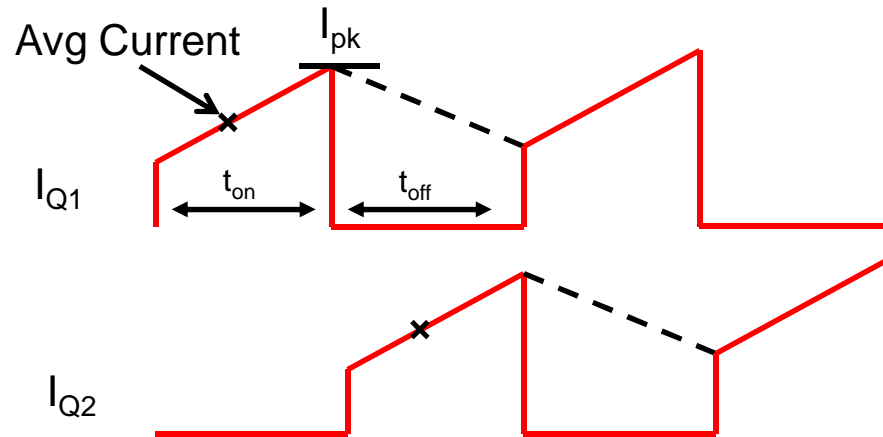
Determine Current Reference

- Current reference is calculated and scaled to a number between 0 and 1023 [10 bits] as current feedback is in this range.

- V_{rms}^2 = (uin_filtered_peak>>2) * (uin_filtered_peak>>2)

    = 8bits * 8bits = 16bits

- Multiply V_{AC} * V_{PI} = pfcInputVoltage * u_out

    = 10bits * 15bits = 25bits

- Divide (32/16), (V_{AC}* V_{PI})/ V_{rms}^2 = 25bits/16bits = 9Bits

- Shift left one bit (x2) for 10-bit scale

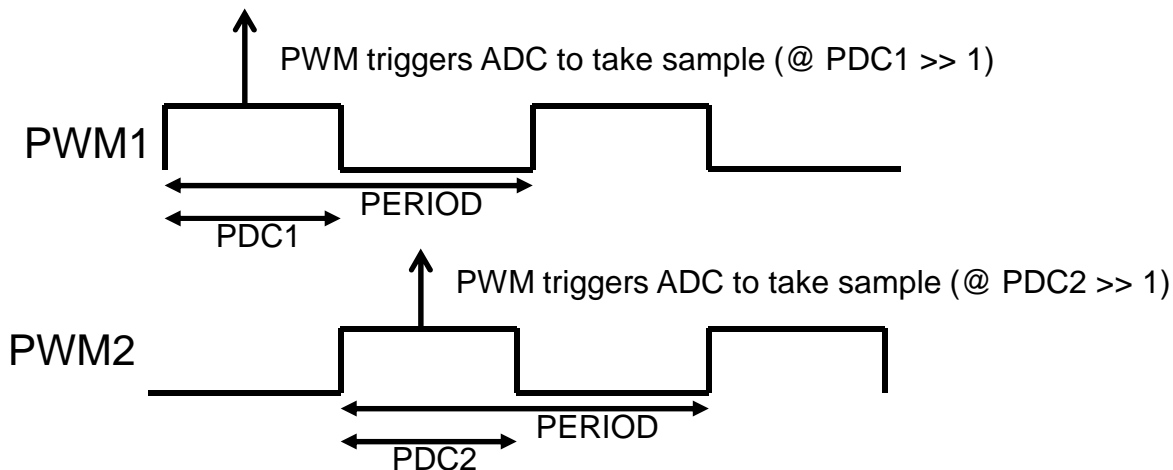$$I_{AC\_REF} = (\frac{V_{PI} * V_{AC}}{V_{RMS}^2} \ll 1)$$

Average Inductor Current

Avg Current

I_{pk}

I_{Q1}

t_{on} t_{off}

I_{Q2}

$$i_{L\_avg} = \frac{1}{T_s}\int_0^{T_s} i_L(t)\,dt$$

$$i_{L\_avg} = \frac{1}{2T_s} i_{L_{pk}}(t_{on}+t_{off}) = \frac{1}{2} i_{L_{pk}}$$

PWM triggers ADC to take sample (@ PDC1 >> 1)

PWM1

PERIOD

PDC1

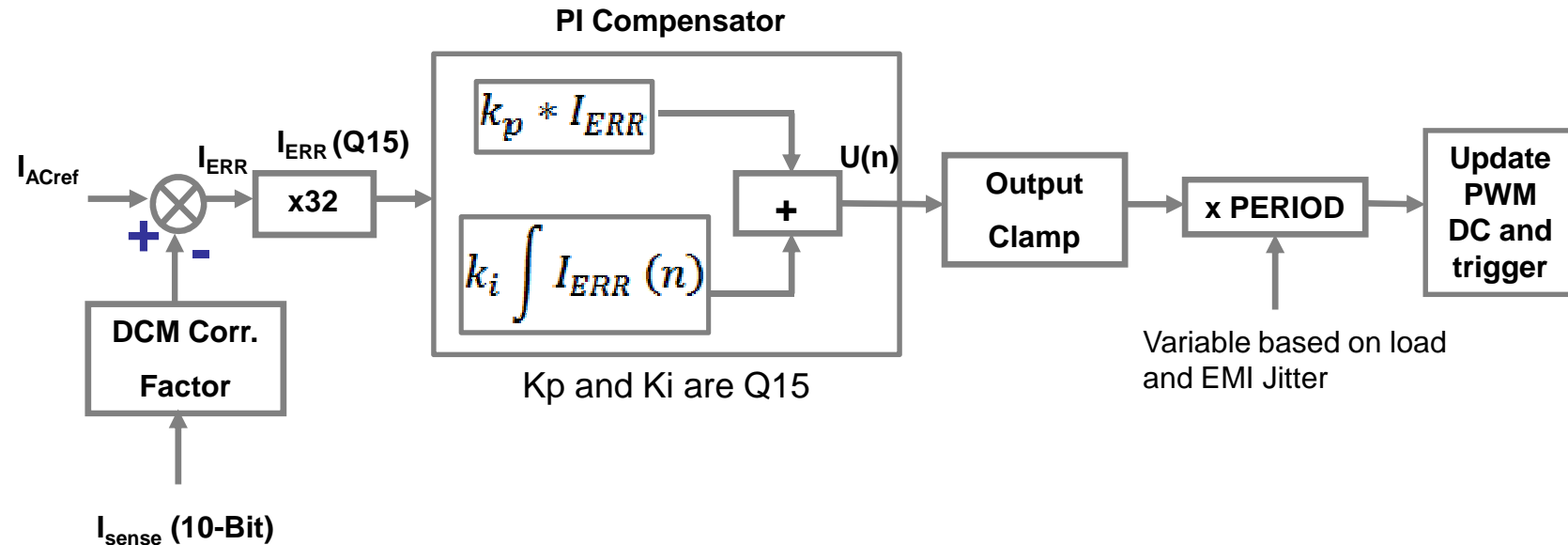PWM triggers ADC to take sample (@ PDC2 >> 1)

PWM2

PERIOD

PDC2

Software updates duty cycle and trigger event every PWM cycle

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Current Sense

- It is important that the current feedback be on dedicated S&H circuits to measure the average current accurately

- PWM module triggers the ADC directly no software intervention

- ADC generates interrupt when conversion is complete. Current compensator called in ADC ISR.

- Current comp. called every PWM cycle so it is important to minimize # of instructions to reduce overall MIPS


Dedicated S&H

I_{Q1}

I_{Q2}

ADC Conv.

Dedicated S&H

Shared S&H

Current Compensator

PI Compensator

$$k_p * I_{ERR}$$

$$k_i \int I_{ERR}(n)$$

Kp and Ki are Q15

I_{ACref}

I_{ERR} I_{ERR} (Q15)

x32

+   -

DCM Corr. Factor

I_{sense} (10-Bit)

+   U(n)

Output Clamp

x PERIOD

Update PWM DC and trigger
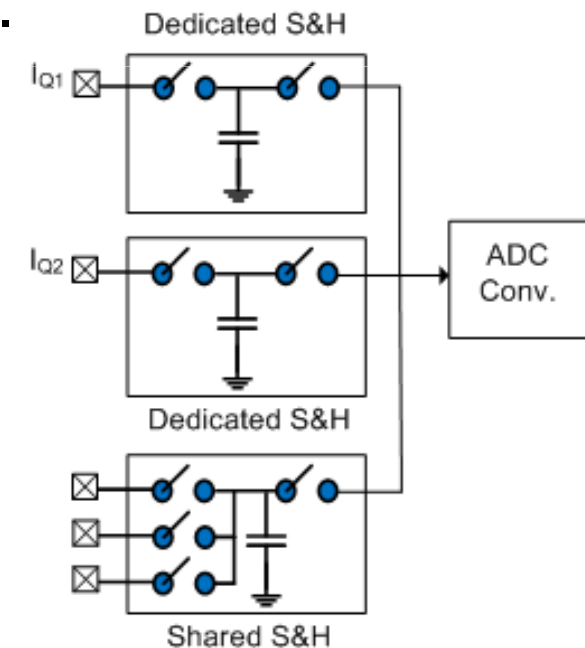
Variable based on load and EMI Jitter

- PI Output range (U(n)): -32768 to 32767
- Output Clamp: 0 < U(n) < 30145 (92%)
- Total output = Output Clamp * PERIOD
  = 0 to 92% of PWM period

Implementing Jitter

- Vary PWM switching frequency by +/- 10%
- PWM Period varies with load so algorithm needs to account for this

Step size of ~1.5%
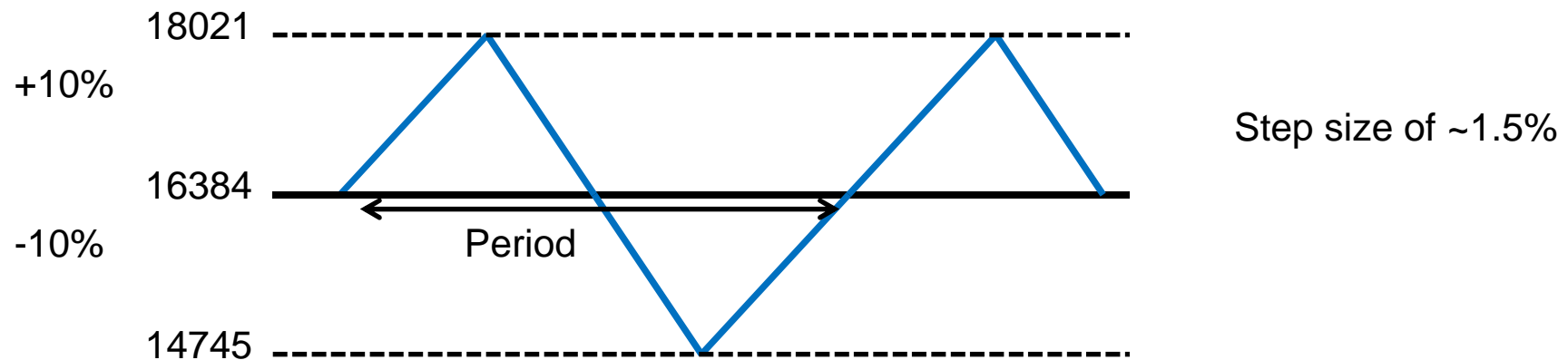
$$totalPeriod = [(workingPeriod * jitterFactor) << 1]$$
$$= signed\ int * fract * 2$$

At any operating period the Jitter algorithm will add +/- 10%
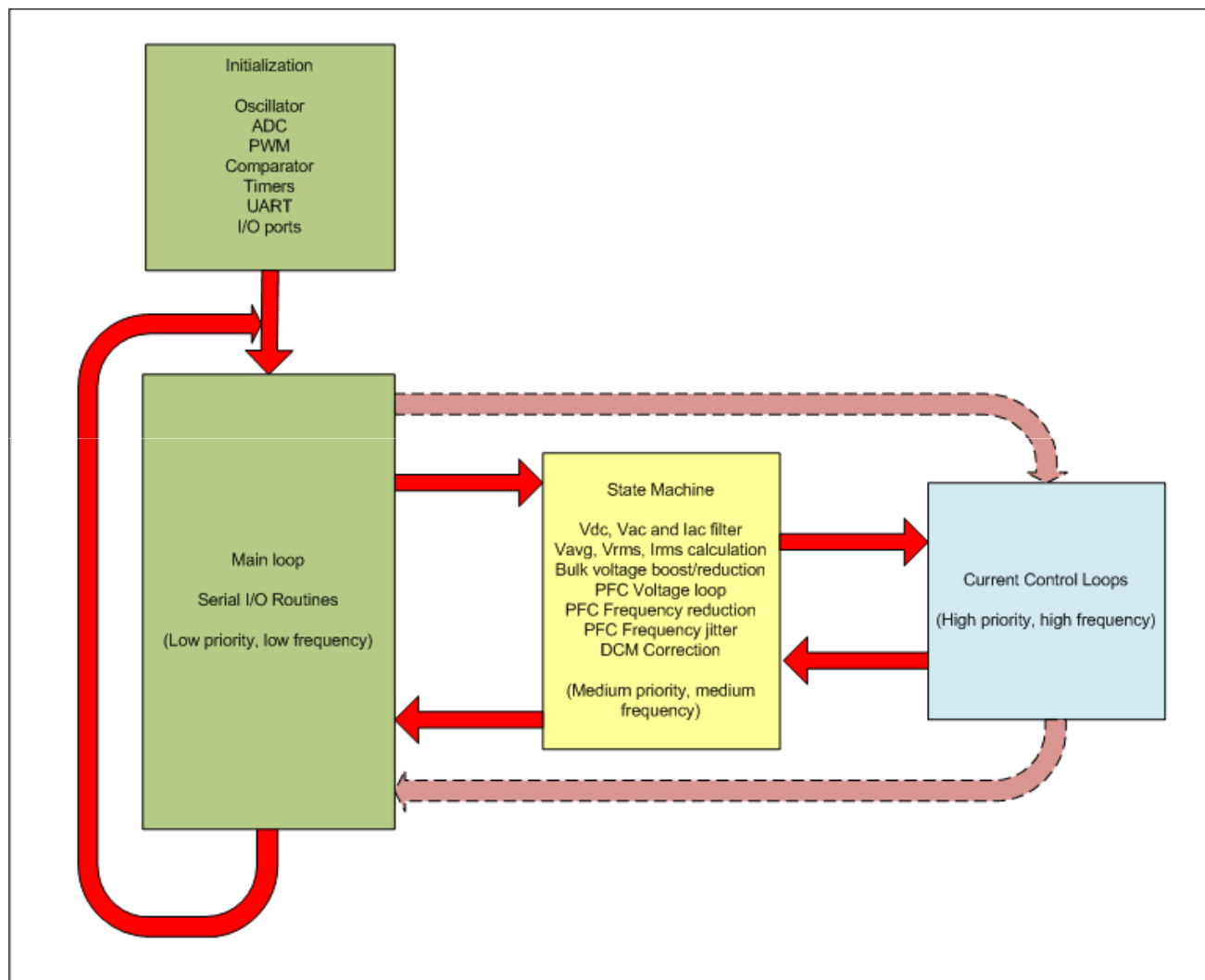
Software Overview

Interrupt based priority scheme:

- High priority – Critical Control algorithms
- Medium priority – Advanced algorithms
- Low priority – Communications
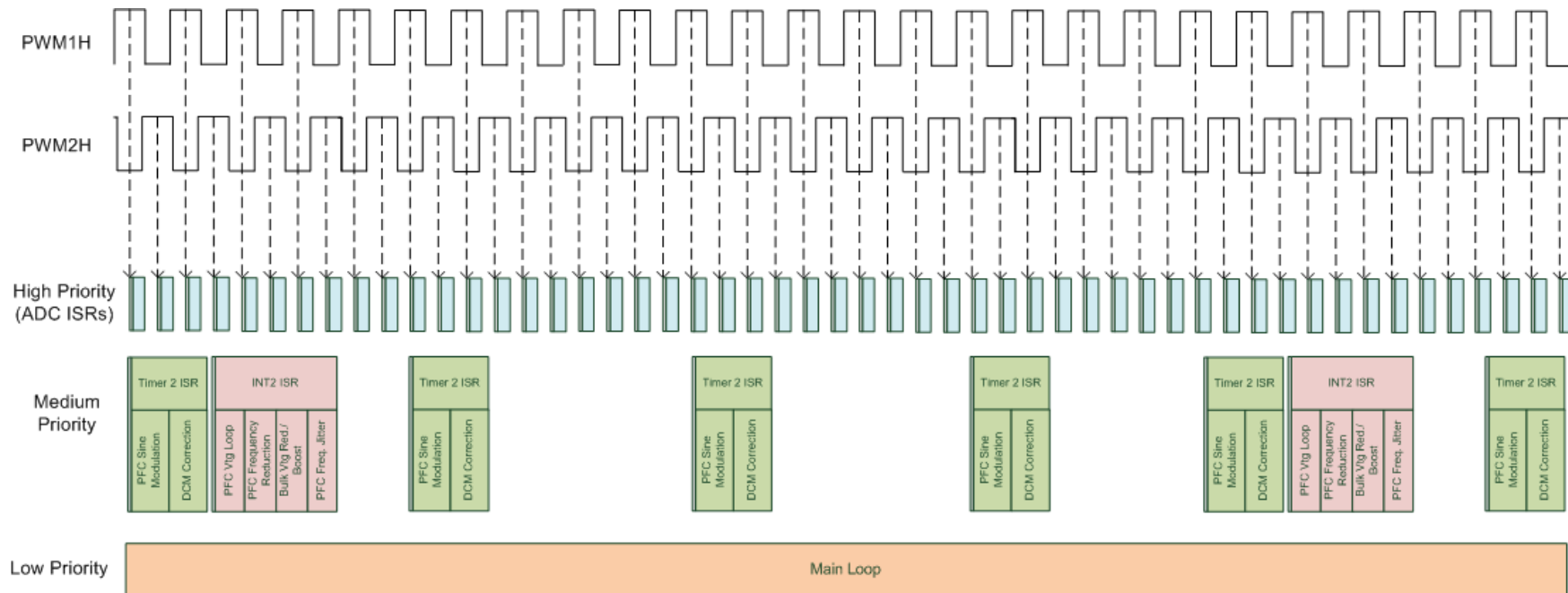
Note: Timing diagrams are drawn showing relative trigger events. Block size does not represent actual algorithm duration.

Software Structure

Agenda

- **Power Factor and its Significance**

- **How to Achieve Power Factor Correction**

- **Overview of Different Boost Type PFC Designs**

- **Digital PFC Using the dsPIC® DSC**

- **Advanced PFC Techniques**

- **Overview of 720W AC-DC Reference Design**

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Advanced PFC Techniques

- **New Regulations require higher efficiency, higher Power Factor and lower THD**

- **Unavoidable factors limit performance of system at light loads**
  - EMI Filter
  - Discontinuous Conduction mode

- **Fixed minimum power losses limit maximum theoretical efficiency at light loads**

Problem: Discontinuous Conduction Mode (DCM)

V_{AC}

ωt

i_{AC}

ωt

0

π

Transition between CCM and DCM modes
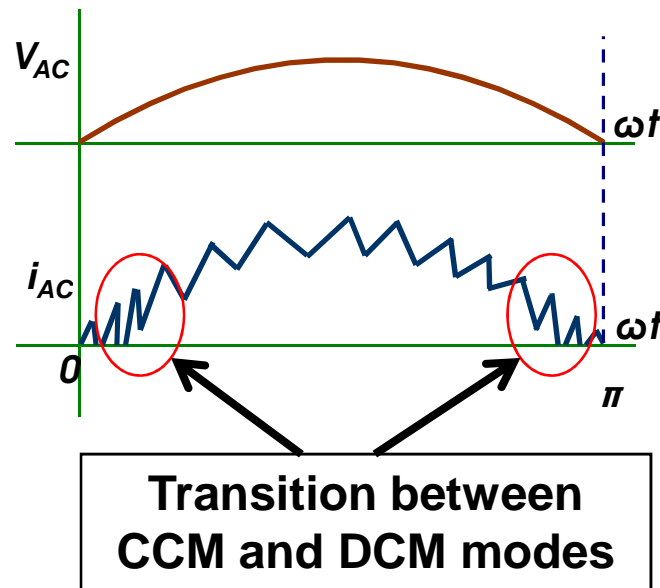
- V_{AC} varies from 0V to $V_{AC(PK)}$ on every sine wave cycle causing boost converter to operate in DCM (occurs near zero crossings and depends on load)

- The Boost Converter will operate in DCM when:

$$i_{AC} < \frac{\left(V_{AC} \cdot D \cdot T_S\right)}{2L}$$

DCM Correction

- When inductor current becomes discontinuous the current sampling point (PDC/2) is no longer the average inductor current

- With the CT in series with boost MOSFET, we only see t_{on} current. Additional circuitry is needed to see when inductor current reaches zero to determine t_{off}.
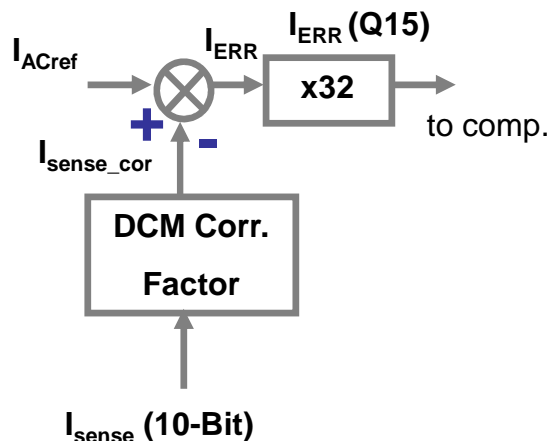
No longer the average
Inductor current

I_Q
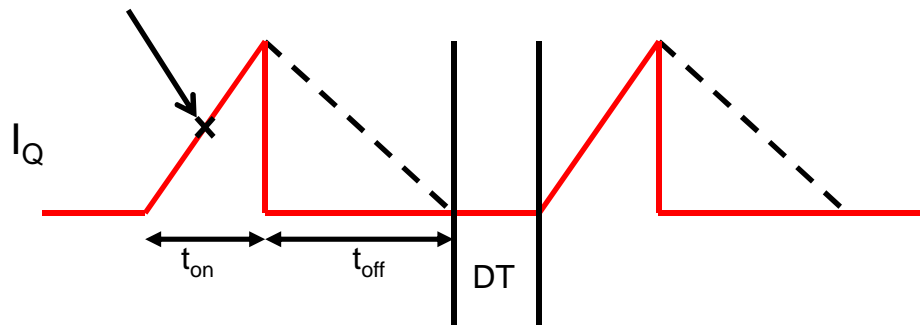
t_{on} t_{off} DT

$$I_{Q\_avg} = \frac{I_{Q\_pk}}{2} * (t_{on} + t_{off})f_s$$

DCM Correction

- Add a correction factor in the current control algorithm to account for the measured inductor current not being the average.

- Proposed solution is to modify the sense current (I_{sense}) with respect to the V_{ac}, V_{out}, and compensator output.
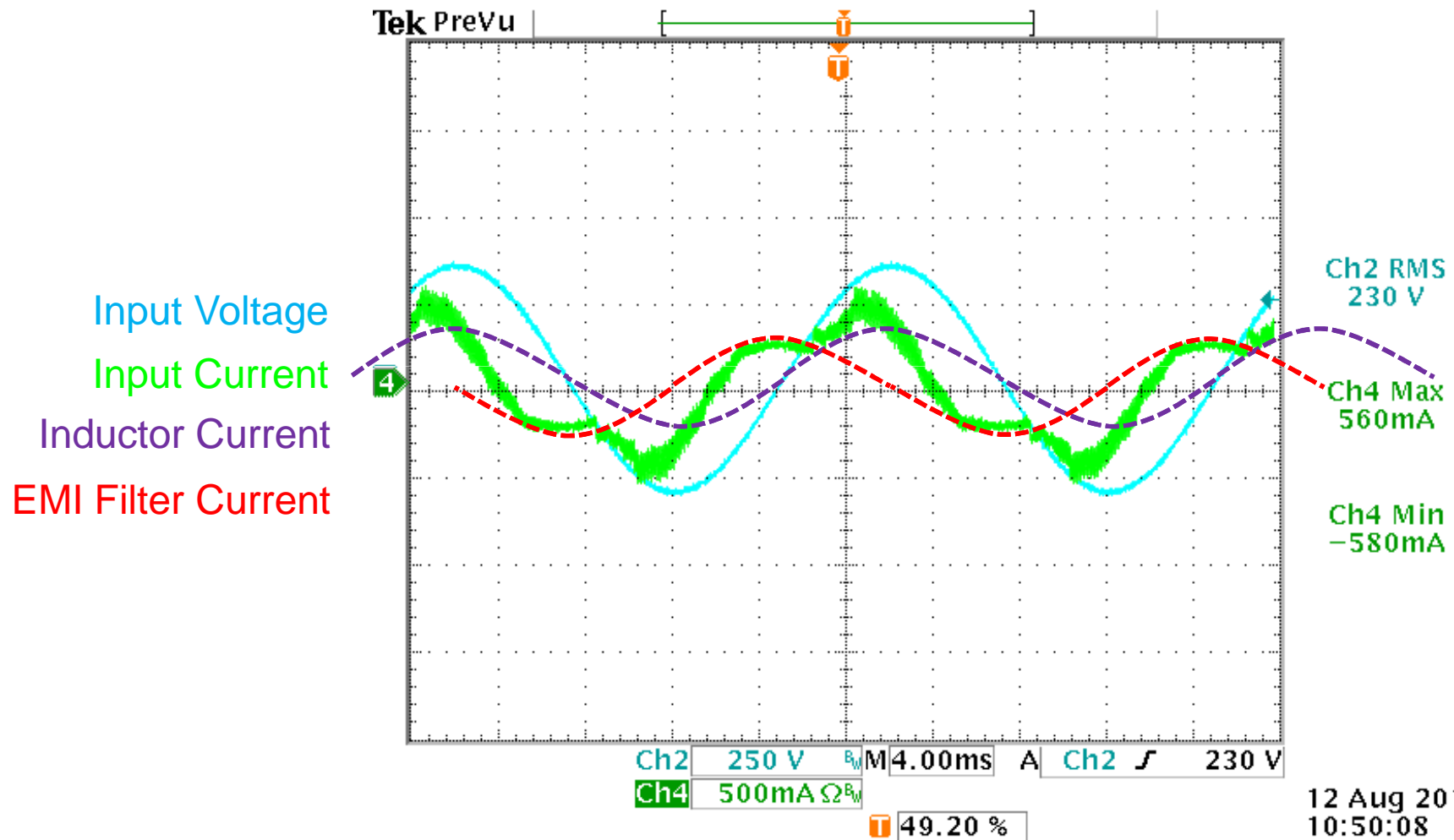
$$I_{sense\_cor} = \frac{V_{out}}{V_{out} - V_{AC}} * Comp_{out} * I_{sense}$$

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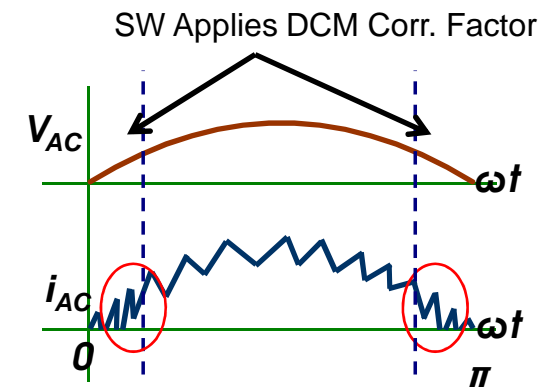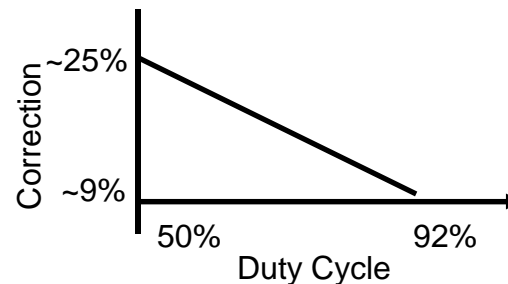
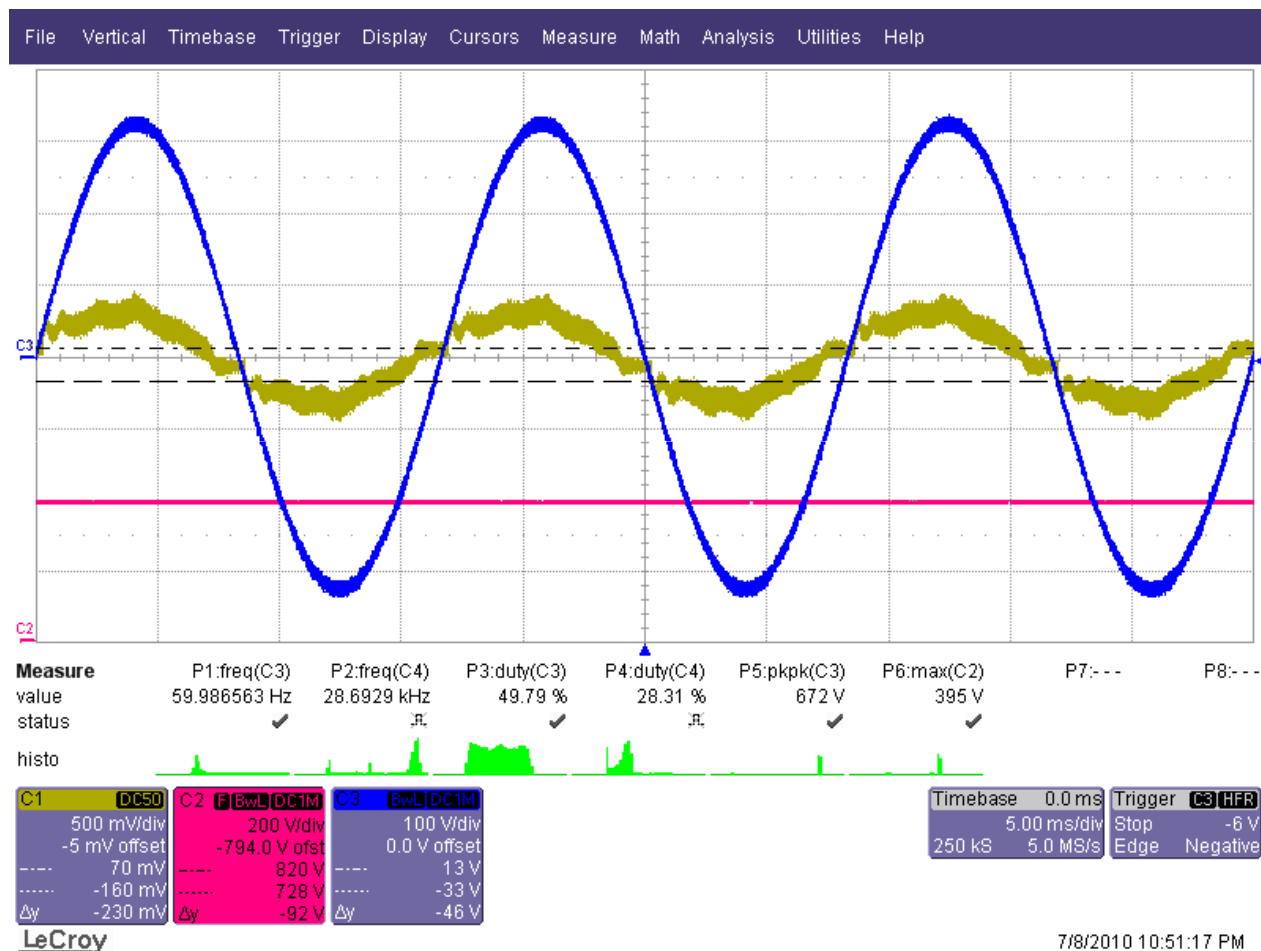# Problem: How to Improve Efficiency @ light load

- Design system with lower switching frequency
  - Results in larger component sizes
  - May impact performance

- Utilize other control schemes like boundary conduction mode
  - Higher peak currents may impact EMI
  - Efficiency will be impacted at higher load currents

- Implement advanced software algorithms
  - PFC Output Bulk voltage reduction
  - Switching Frequency reduction
  - Phase-shedding (interleaved PFC)

How to Improve PF at Light Load? (230Vrms@50W)

Input Voltage
Input Current
Inductor Current
EMI Filter Current

Tek PreVu

Ch2 RMS 230 V

Ch4 Max 560mA

Ch4 Min −580mA

Ch2   250 V   M4.00ms   A   Ch2   230 V
Ch4   500mA Ω
49.20 %

12 Aug 2011
10:50:08

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How to Improve PF at Light Load? (230Vrms@50W)

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Bulk Voltage Reduction

- At light loads the bulk voltage is reduced to improve efficiency by reducing the switching losses

- Output bulk voltage increases as soon as a load transient is detected to maintain good response

- For large load transients, bulk voltage "boost" is added to improve transient response – control loop coefficients are modified

Bulk Voltage vs. Load
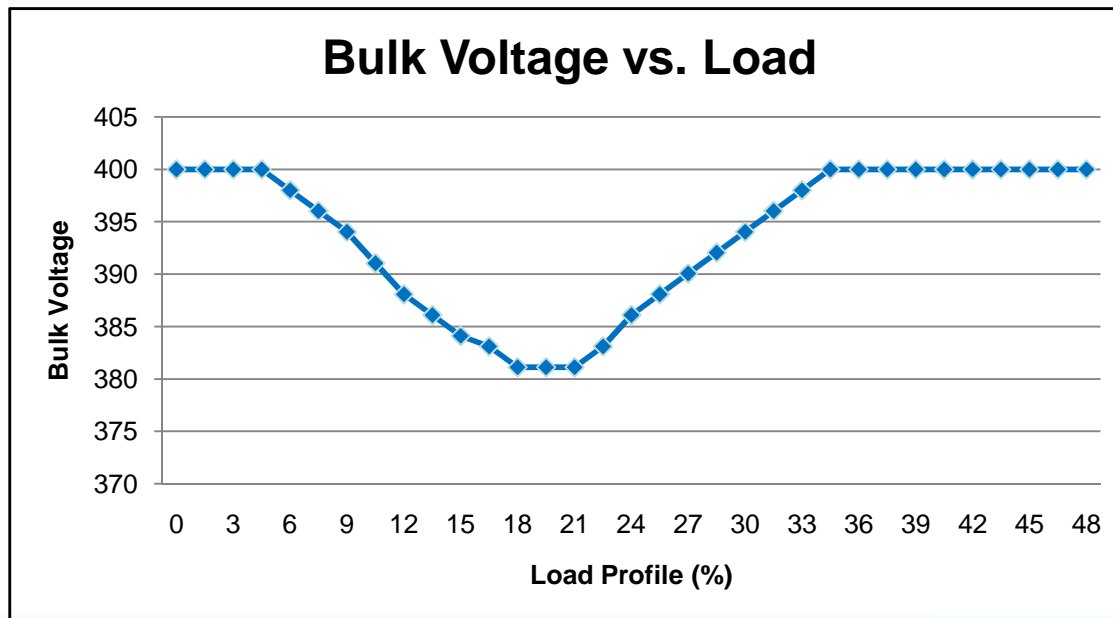
- Software has 32 element lookup table and interpolates between two data points based on secondary load current

Frequency Reduction

- At low load conditions, the frequency is reduced gradually in steps of 4ns until optimum frequency is reached

- When a load transient is detected, frequency is instantly increased to required frequency to maintain good response

- Control loop output scaling and coefficients are modified based on the calculated operating frequency

Switching Freq vs. Load
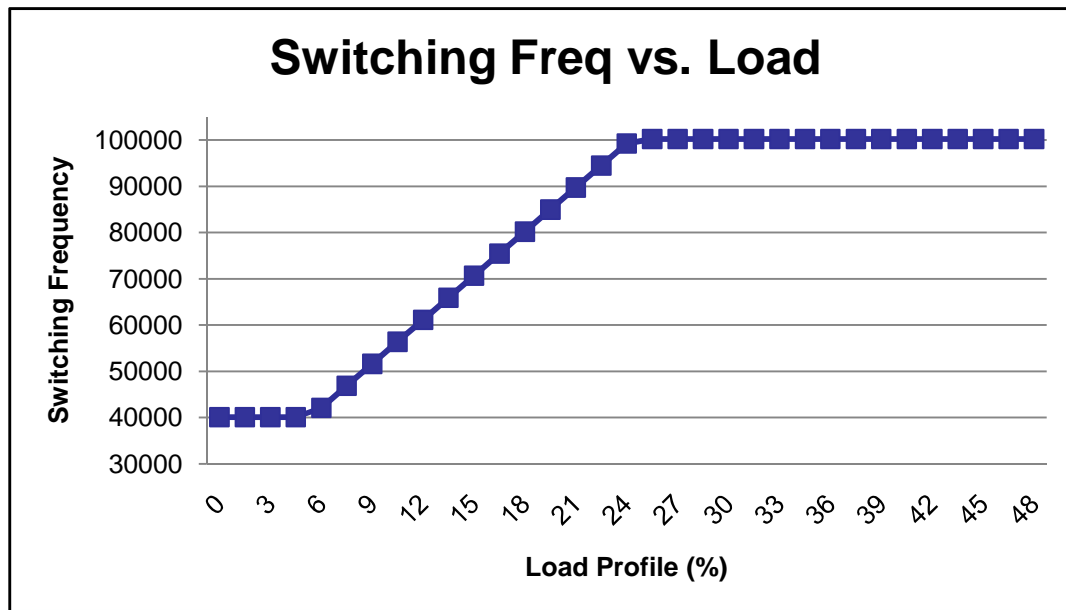
- Software has 32 element lookup table and interpolates between two data points based on load

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Agenda

- Power Factor and its Significance
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- Advanced PFC Techniques
- **Overview of 720W AC-DC Reference Design**

Platinum-Rated AC/DC Reference Design

- **Input / Output:**
  - 85~264 V_{AC} 45-65 Hz
  - Active PFC (PF up to 0.99)
  - 12V DC / 60A (720W max)
  - Load Regulation: ± 1.5%

- **Efficiency:**
  - Up to 94.1%
  - Meets ENERGY STAR CSCI Platinum Level

- **Special Features:**
  - Full digital control
  - Enhanced system monitoring & fault handling
  - Load share bus for N+1 Redundancy

- **Dynamic efficiency optimization**
  - Switching Frequency Adaption
  - Dynamic Bulk Voltage Adjustment
  - Enhanced Sync Rectifier Control

High Level Block Diagram
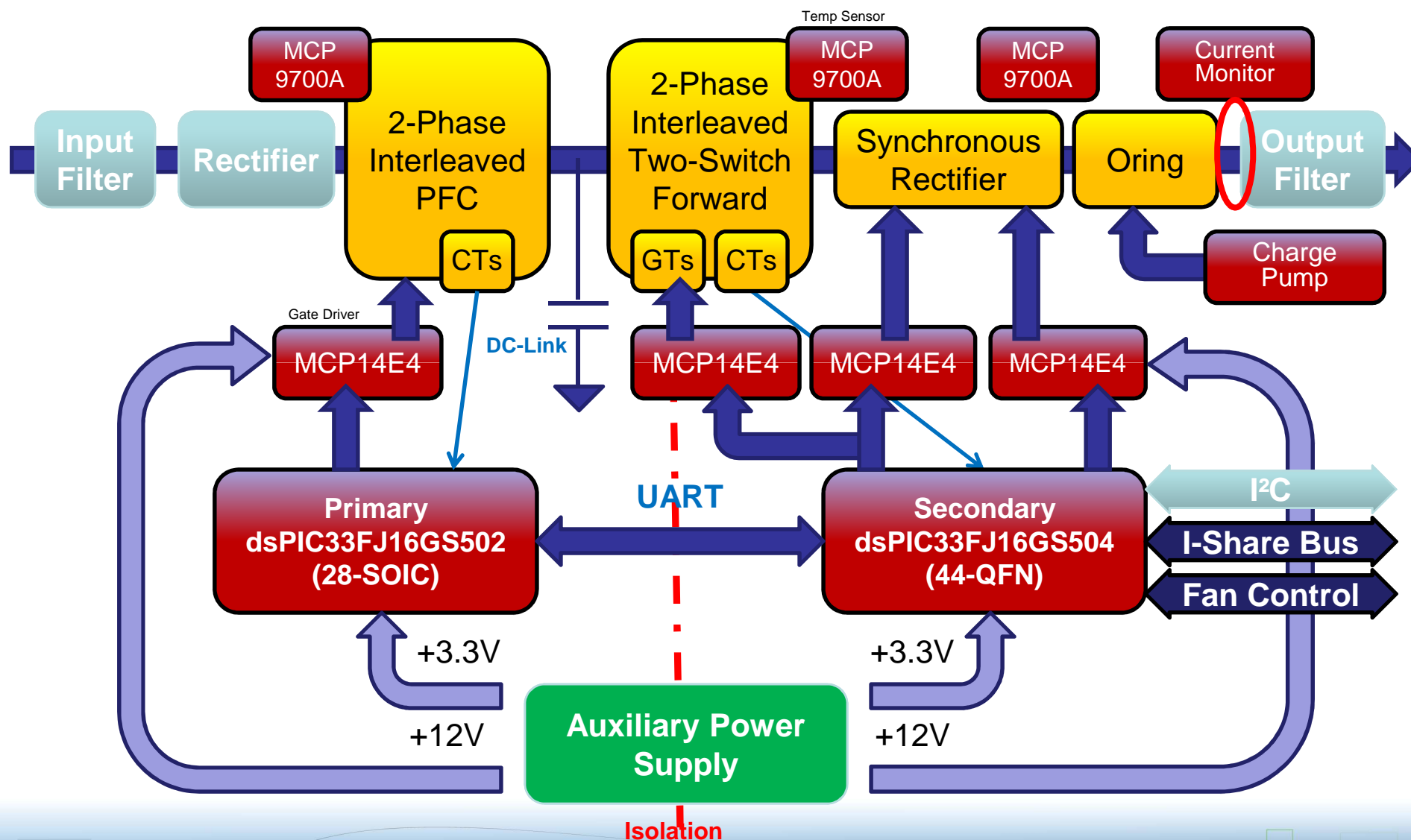
Power Factor Results

Power Factor vs. Load
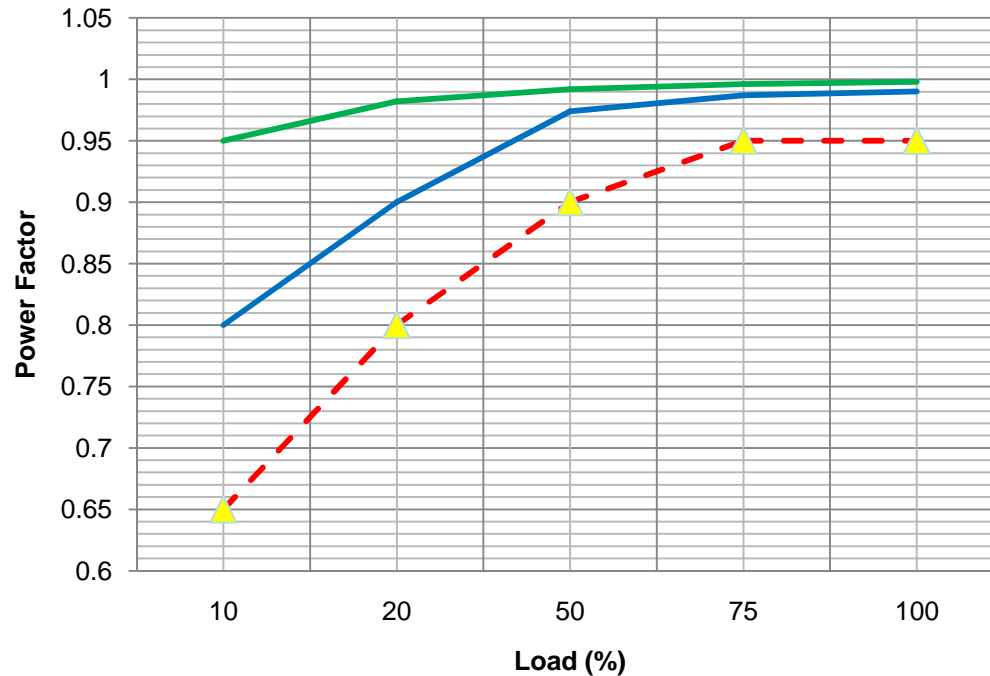
Red:
CSCI Minimum Required Power Factor

Blue:
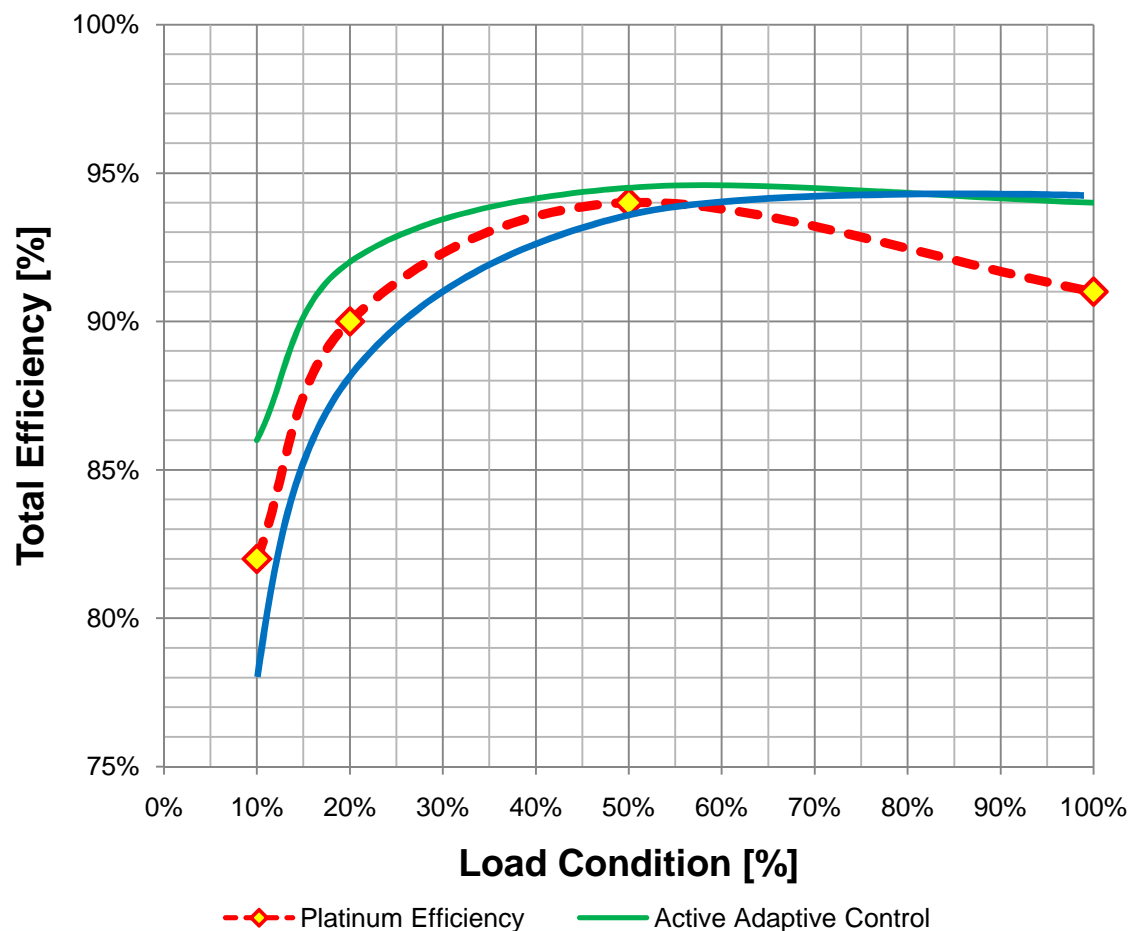Measured Power Factor 230Vac

Green:
Measured Power Factor 120Vac

Recent push for even better PF performance:
- **0.85 at 5% load**
- **0.9 at 10% load**
- **0.95 at 20% load**
- **0.99 >50% load**

Efficiency Analysis

Efficiency Level Optimization

Test Conditions:
 230Vac / 50Hz Input

Red:
   CSCI Platinum Efficiency with given Reference Points

Blue:
   Efficiency with no enhanced features enabled

Green:
   Efficiency with enhanced features enabled

Summary

- **Power Factor Correction reduces energy losses and overall costs and is required on most switch mode power supplies**

- **Implementing active PFC especially digital PFC, is quite complex but can achieve high PF, low iTHD, and work with universal mains.**

- **The dsPIC$^{©}$ DSC enables advanced PFC techniques for improved system performance**
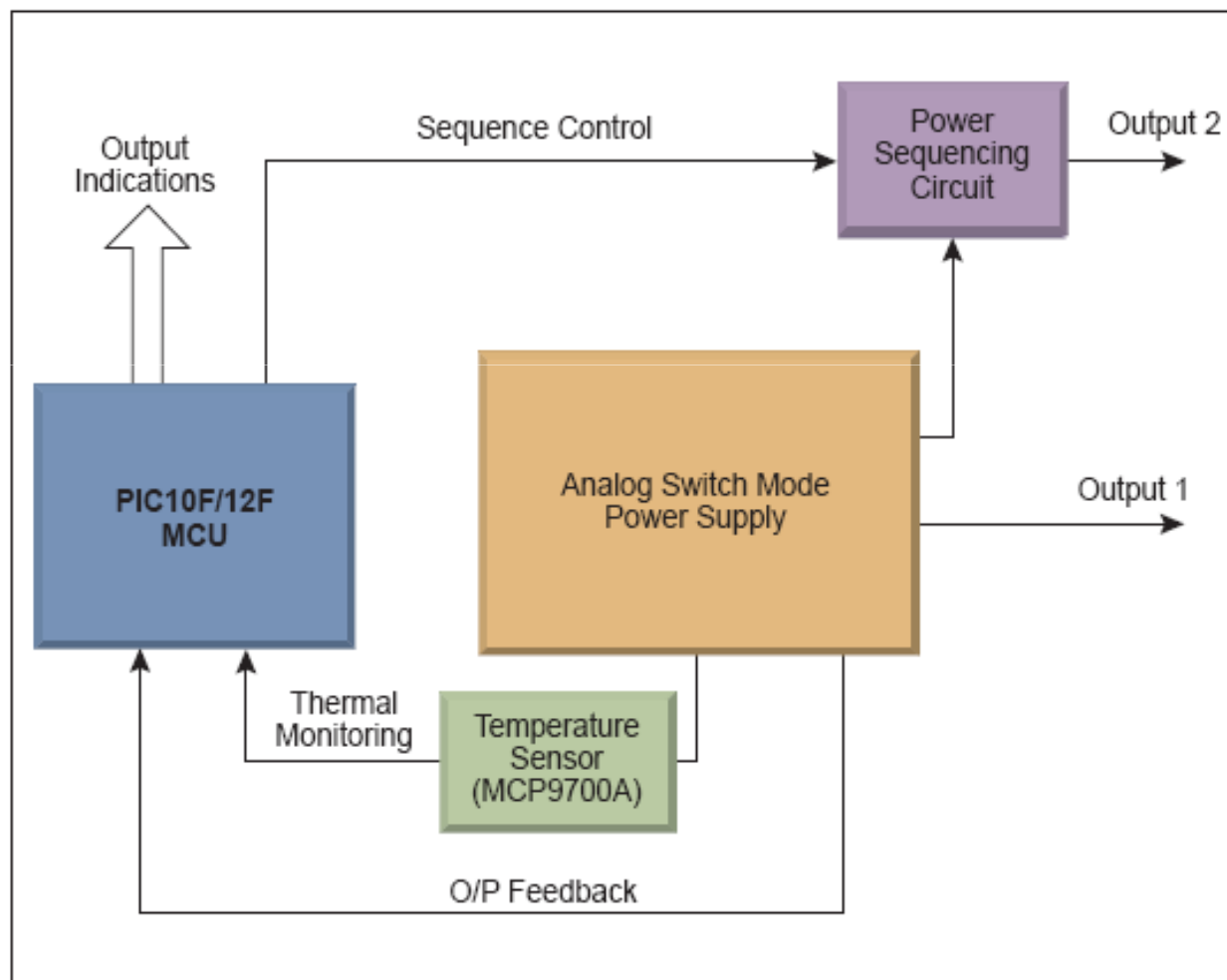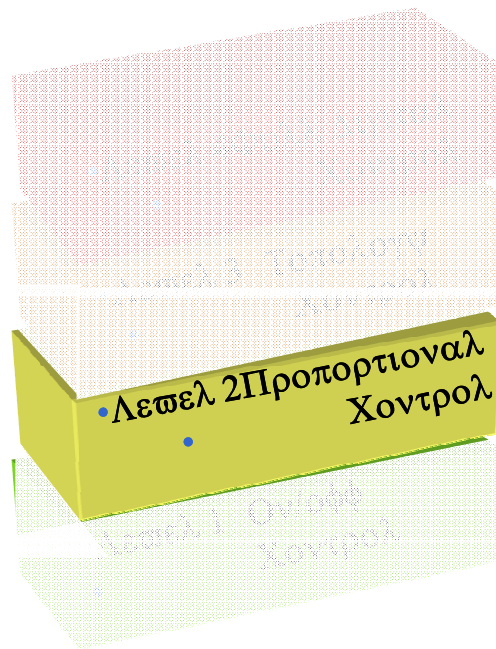
Four Digital Power Level
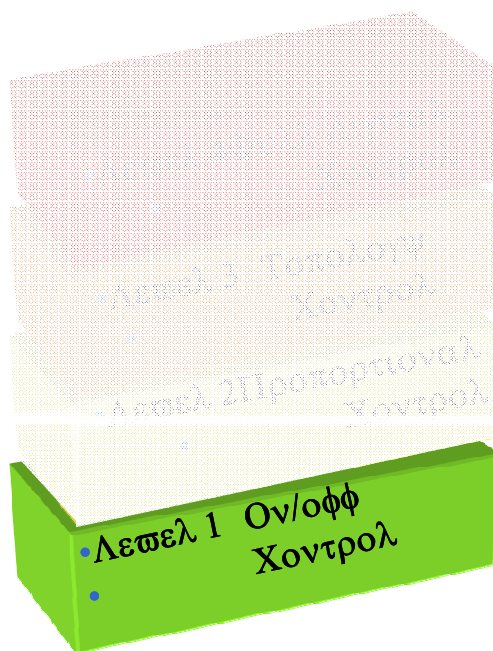
Technical Functions

– **Low-power standby**

– **Programmable soft start**

– **Power up sequencing**

– **Primary/secondary**

communication bridge

•Λεωελ 1 Ον/οφφ Χοντρολ

Simple Control and Monitoring

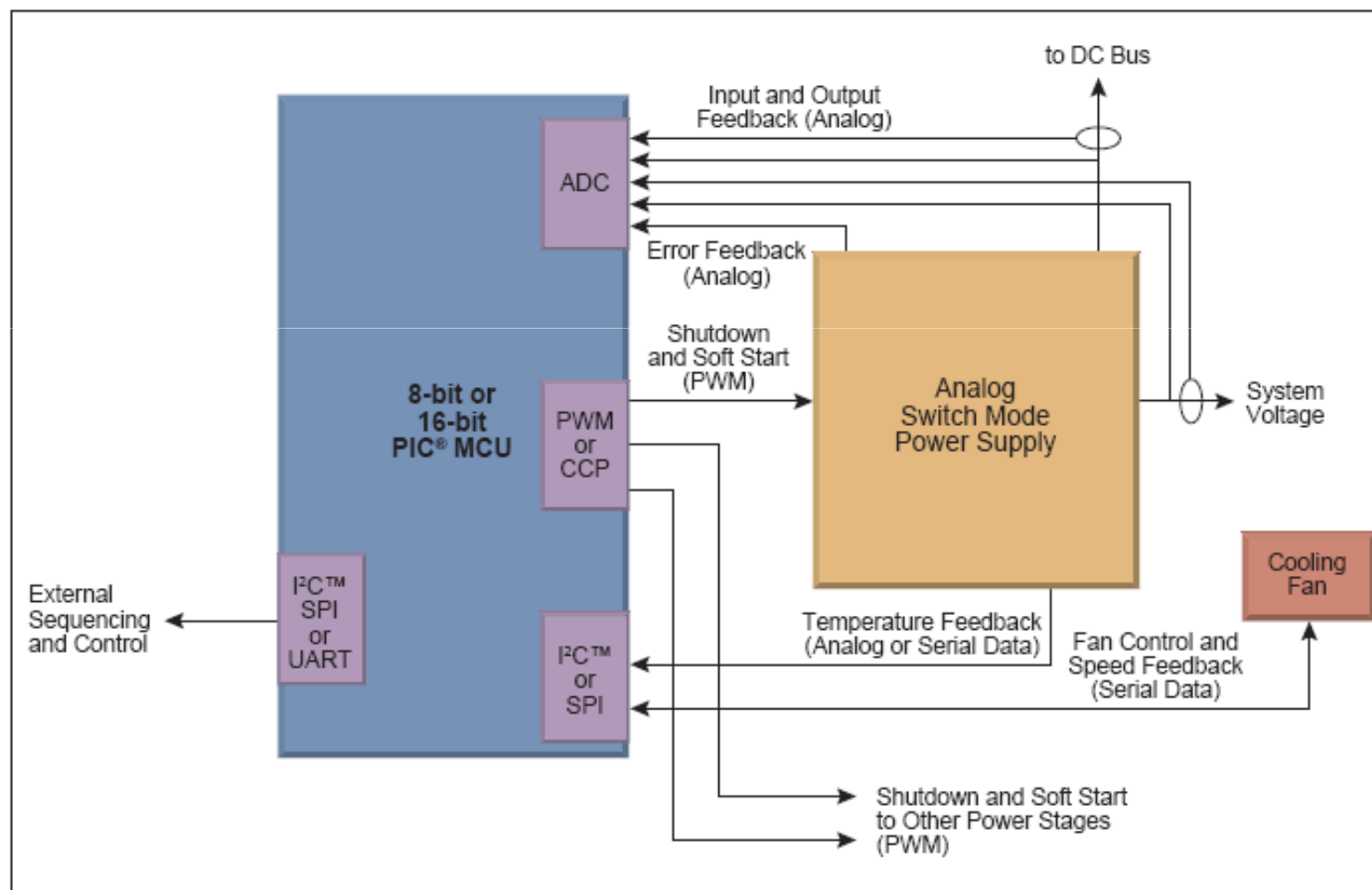# Four Digital Power Level

·Λεωελ 2Προπορτιοναλ Χοντρολ

Technical Functions
– Output voltage margining – Load sharing and balancing – History logging – Primary/secondary communication bridge

Four Digital Power Level
Level 2

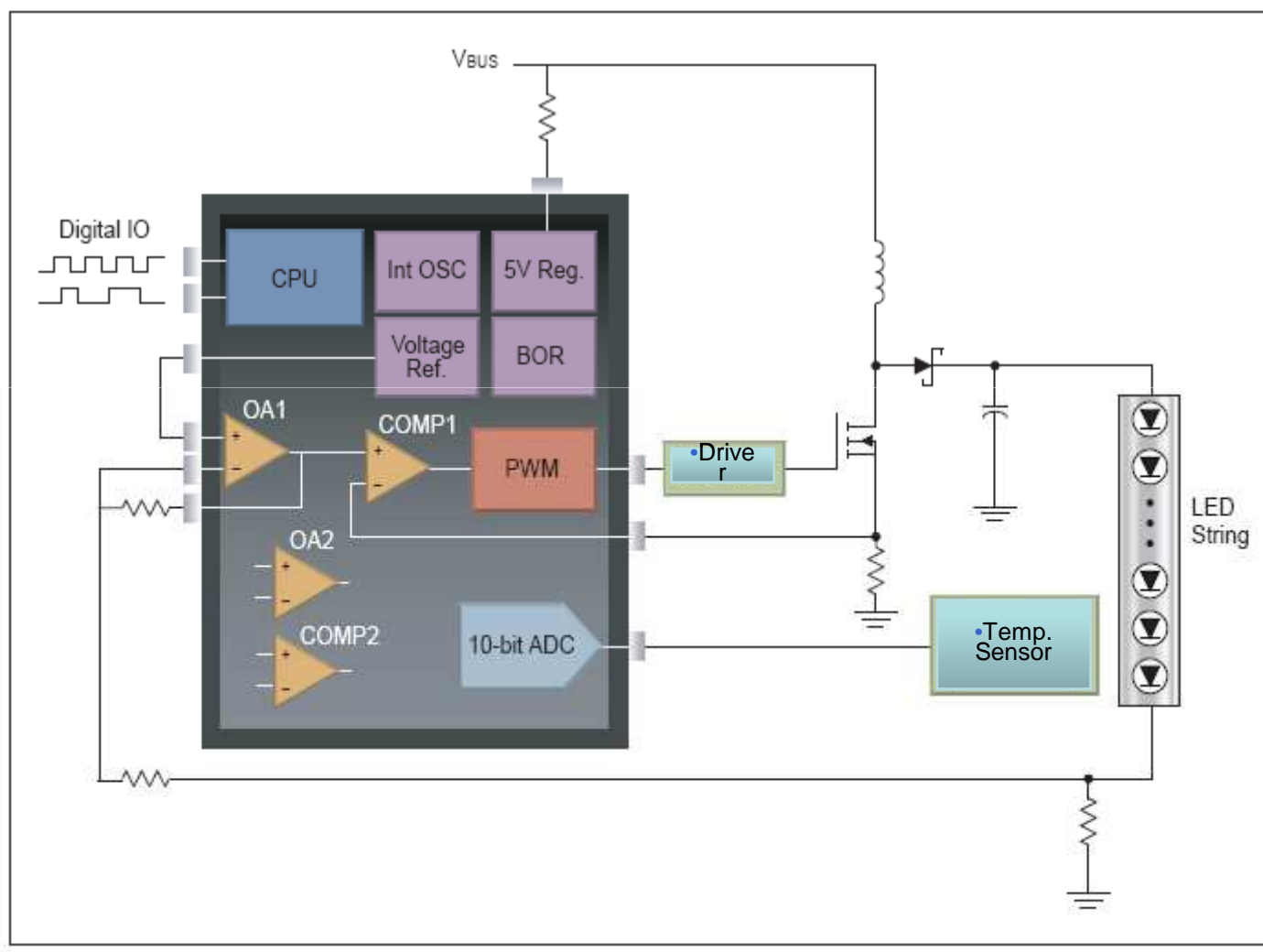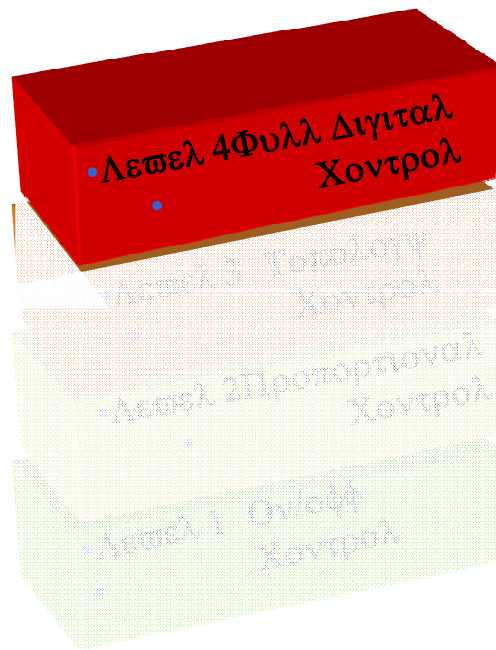Digital Monitoring to Analog Power Supply

Four Digital Power Level

•Λεωελ 3 Τοπολογψ
Χοντρολ

Technical Functions
– Optimize control loop for load changes **– Enable common platform for multiple applications** **– Operational flexibility for different power levels**

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Four Digital Power Level Level 3

Four Digital Power Level
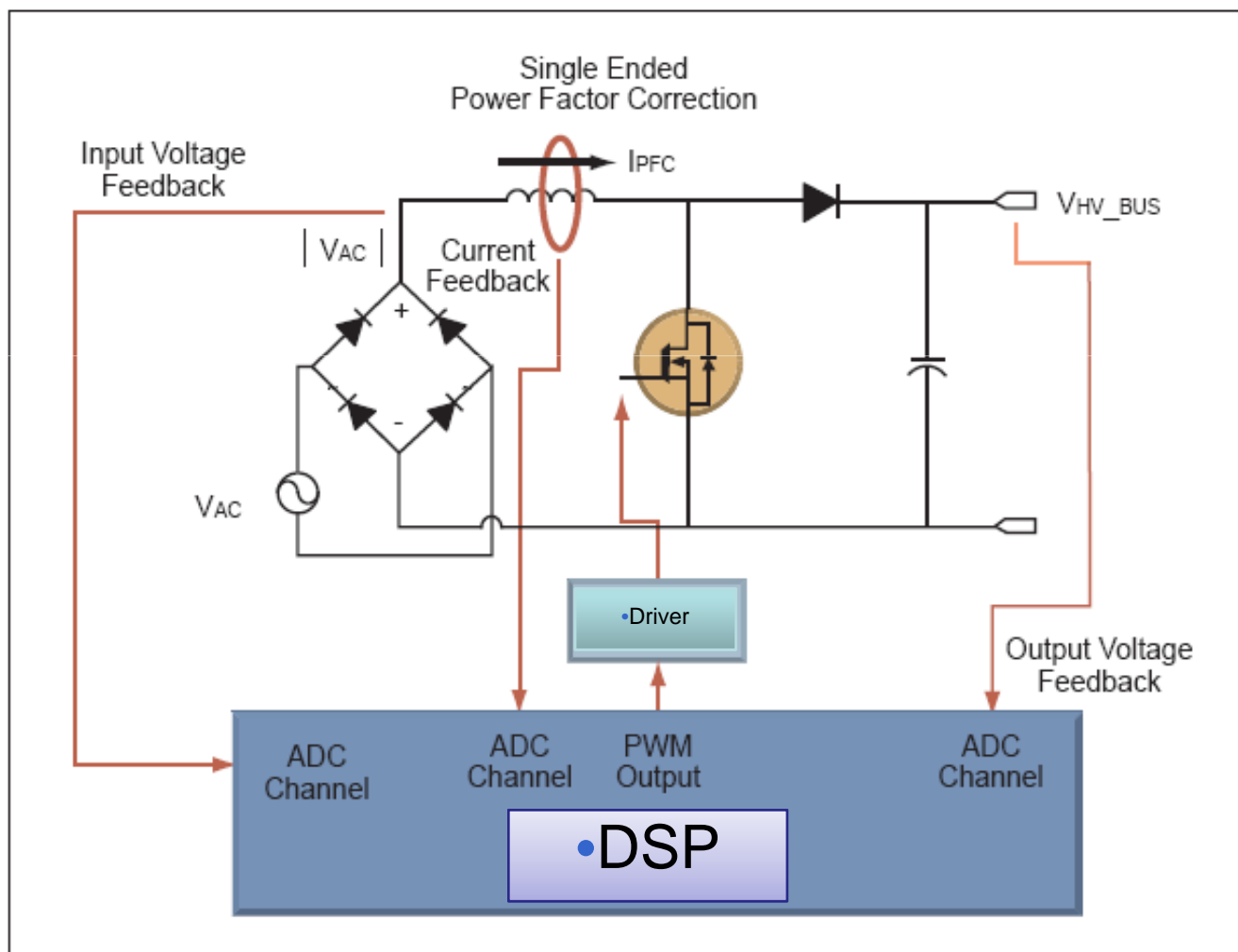
•Λεωελ 4Φυλλ Διγιταλ Χοντρολ

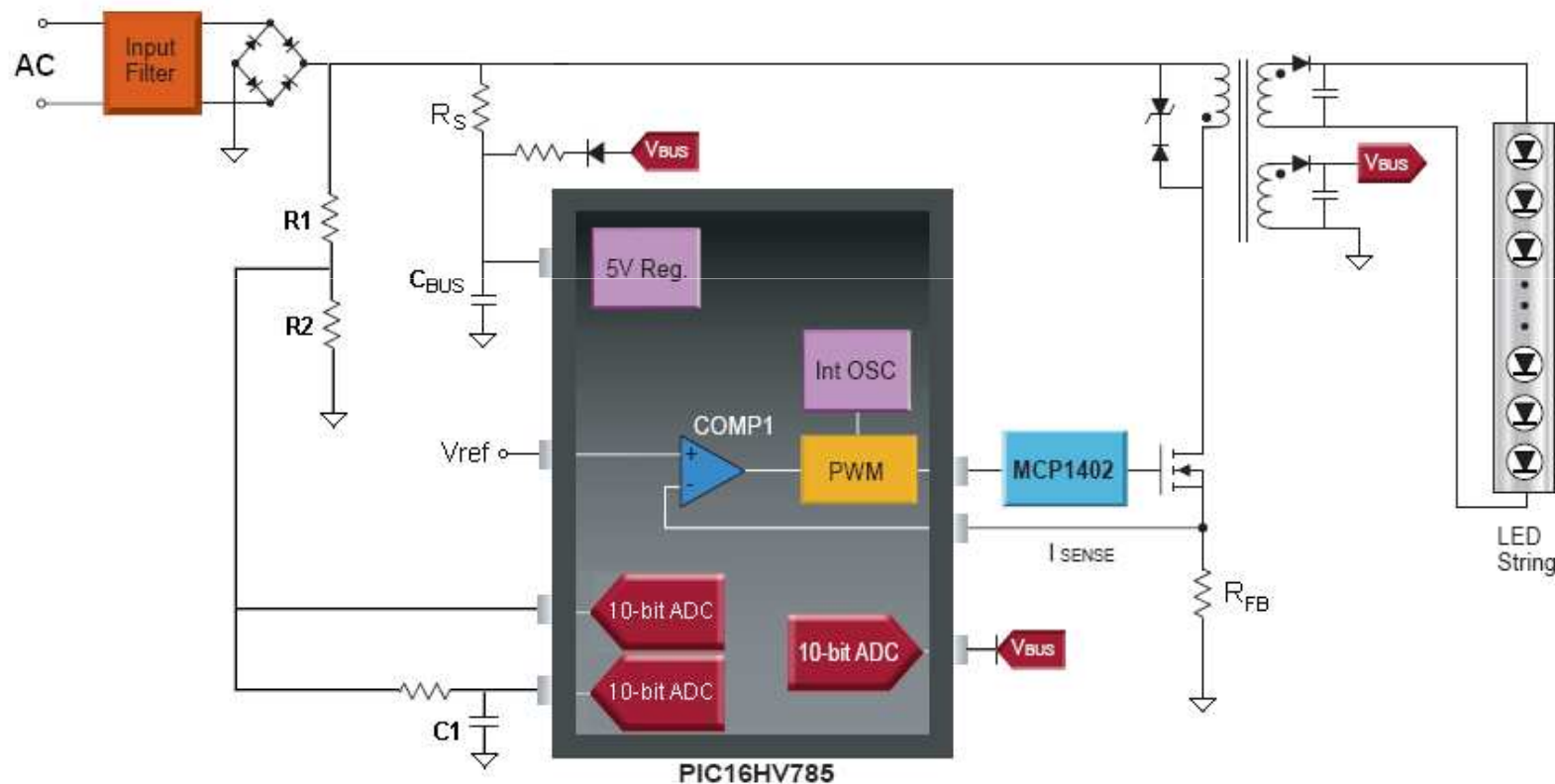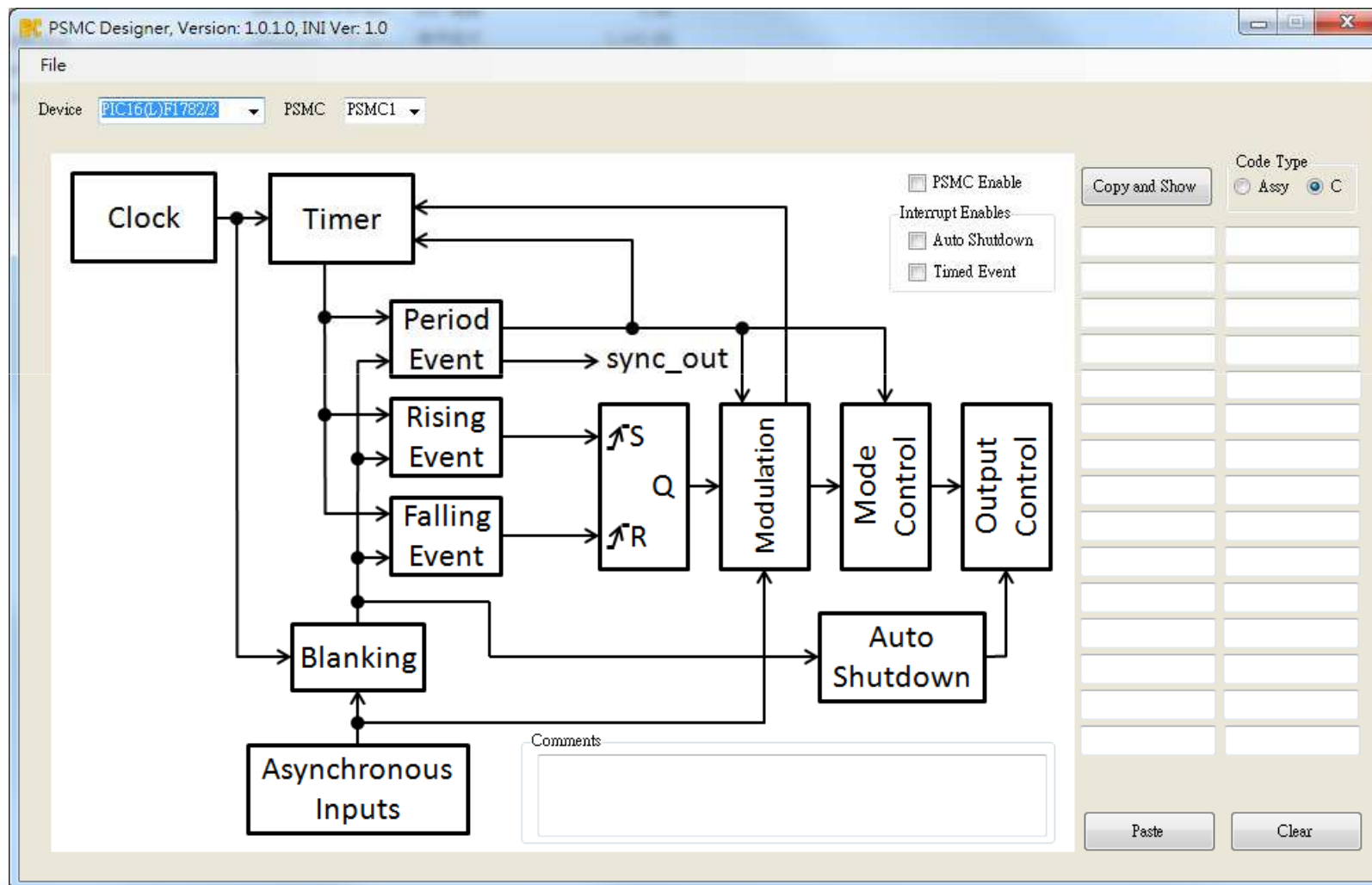| Technical Functions |
|---|
| **– Dynamic control loop adjustment**
 – Predictive control loop algorithms
 – Operational flexibility for different power levels |

PFC with Advanced Digital Control

Flyback Converter
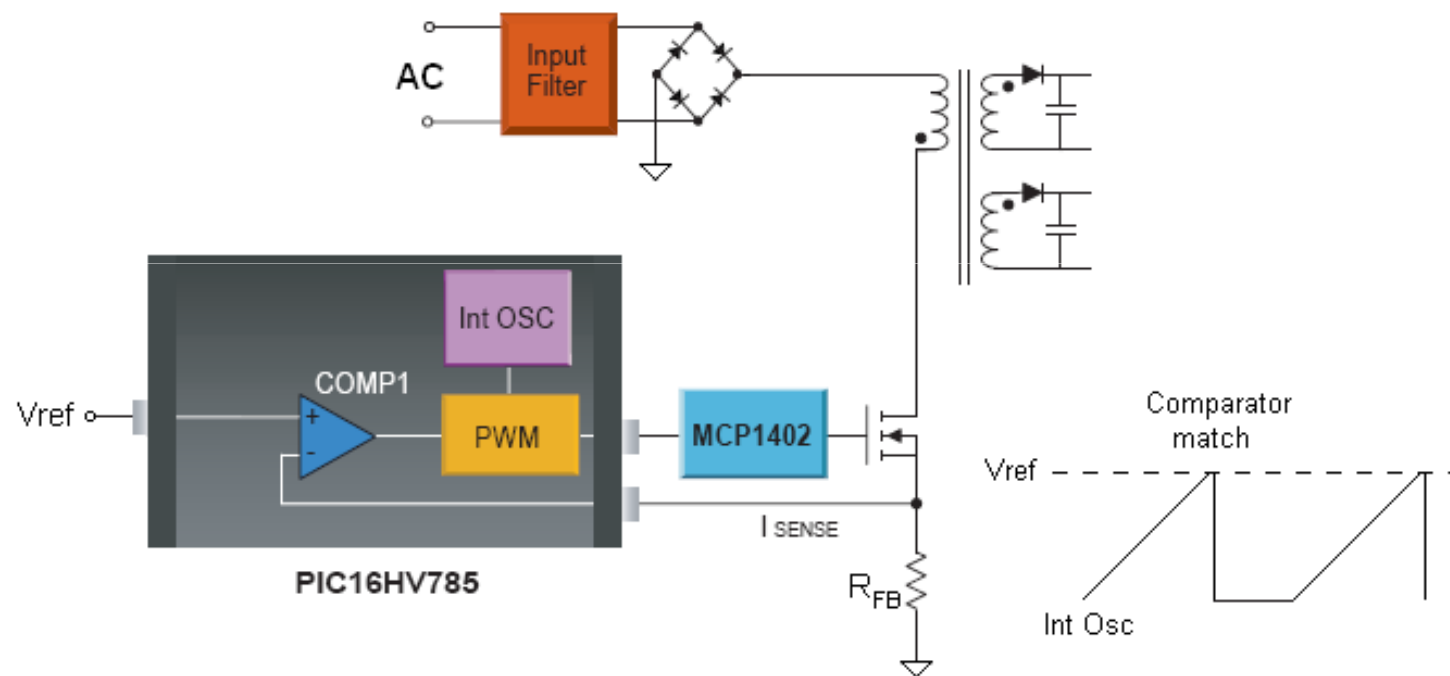
Basic Schematic
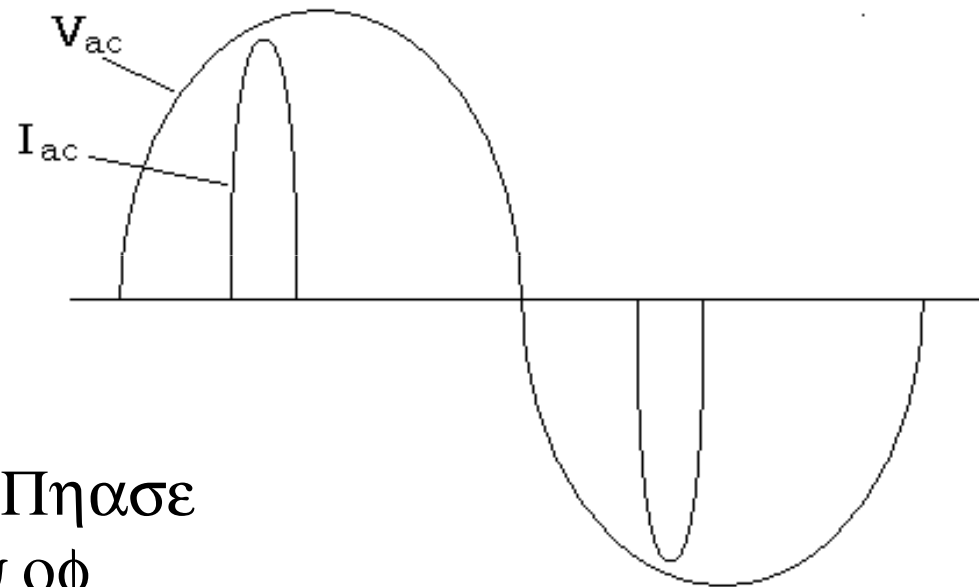
PSMC GUI

Flyback Converter

Basic Operation

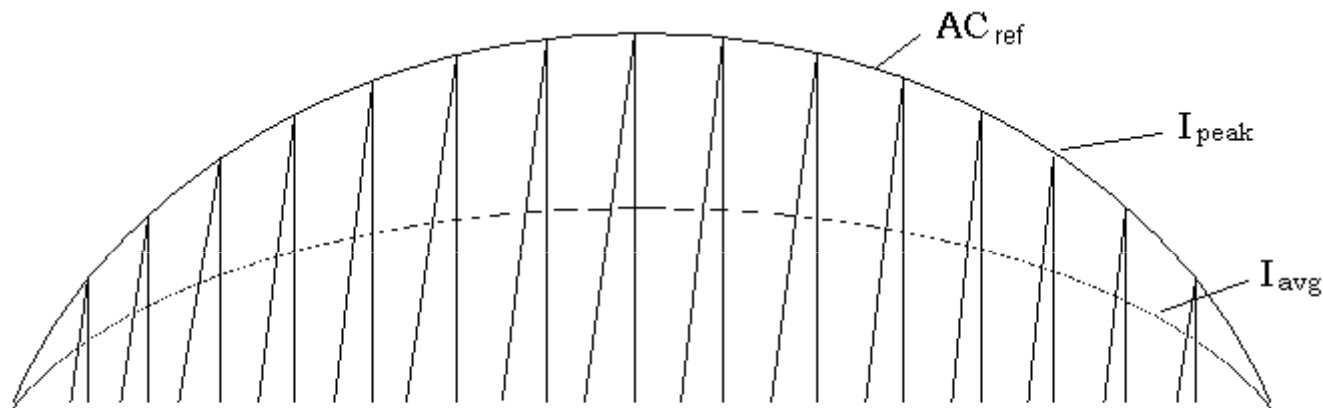- Νο φιρμωαρε νεεδεδ φορ οπερατιον!

Flyback Converter

Power Factor Correction

- Ουτ οφ Πηασε
- Πλεντψ οφ Ηαρμονιχσ

Flyback Converter
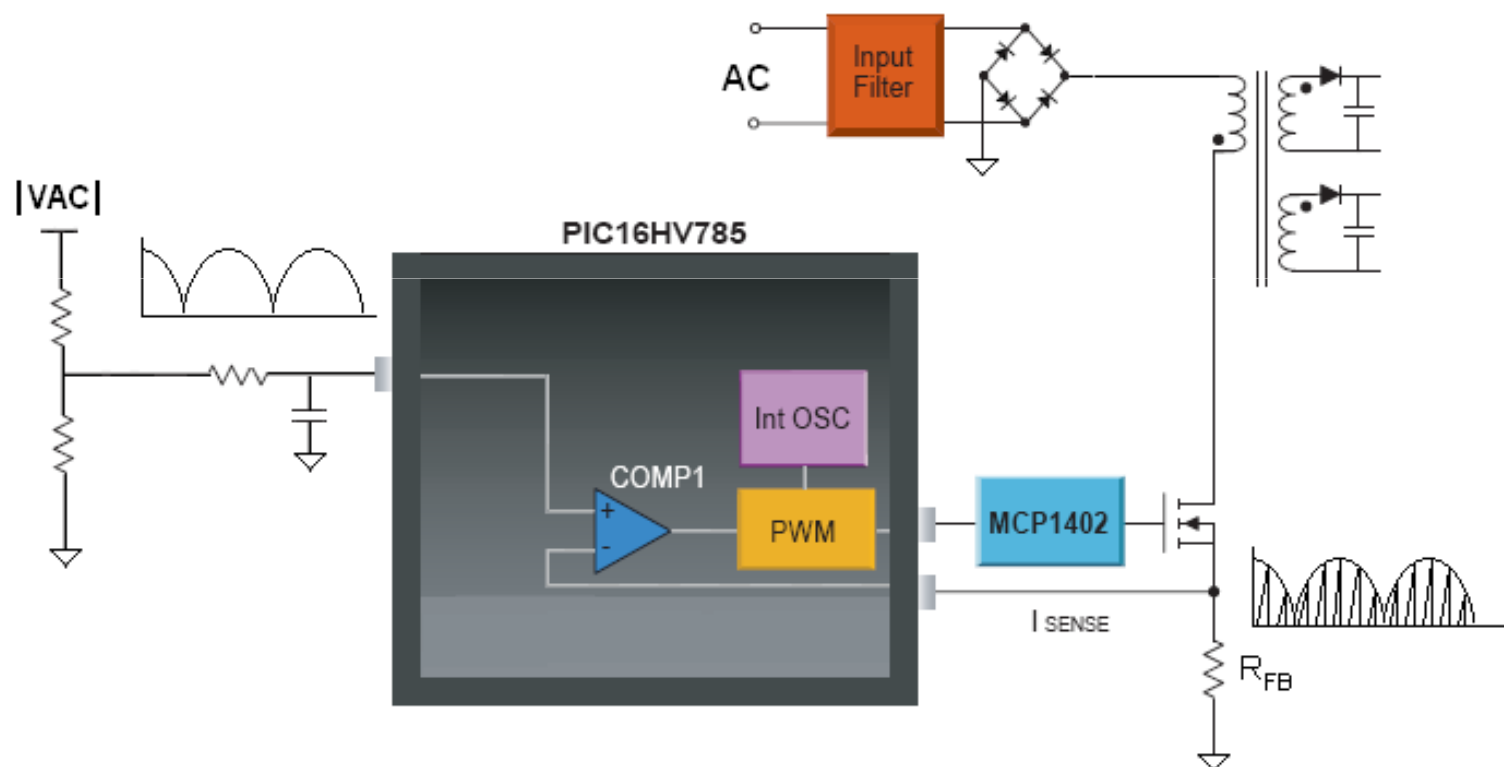
Power Factor Correction

Current, I_{peak} , as a function of the AC reference voltage.

- Ινπυτ χυρρεντ μυστ φολλοω τηε ινπυτ ϖολταγε.

Flyback Converter

Implementing PFC

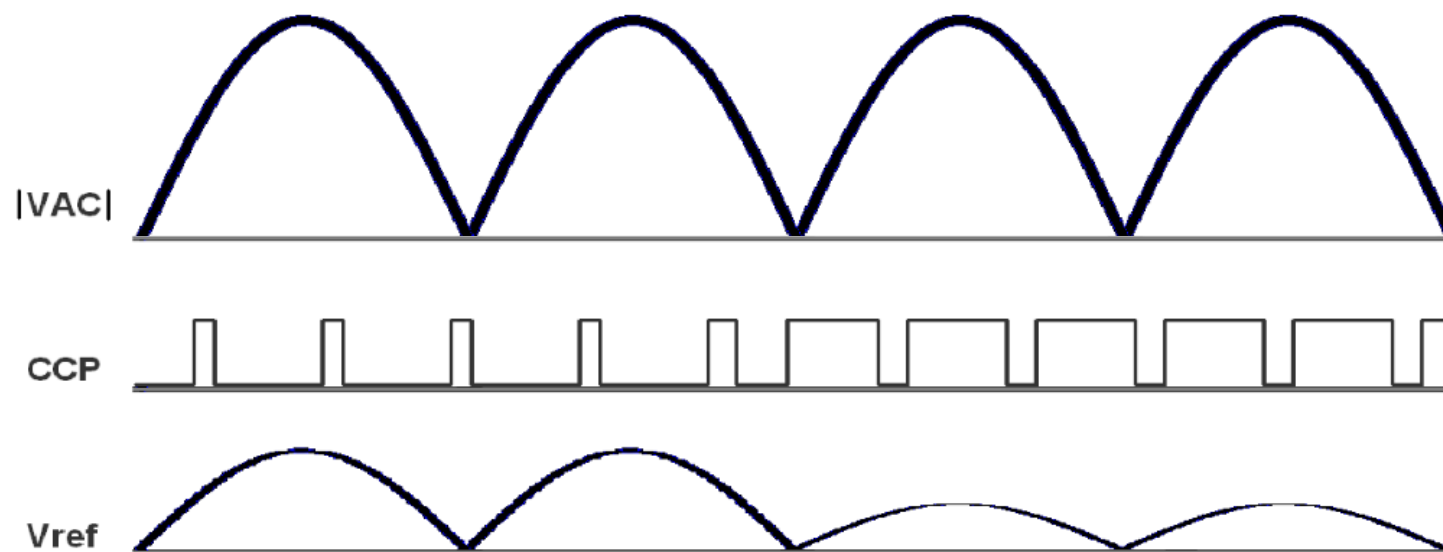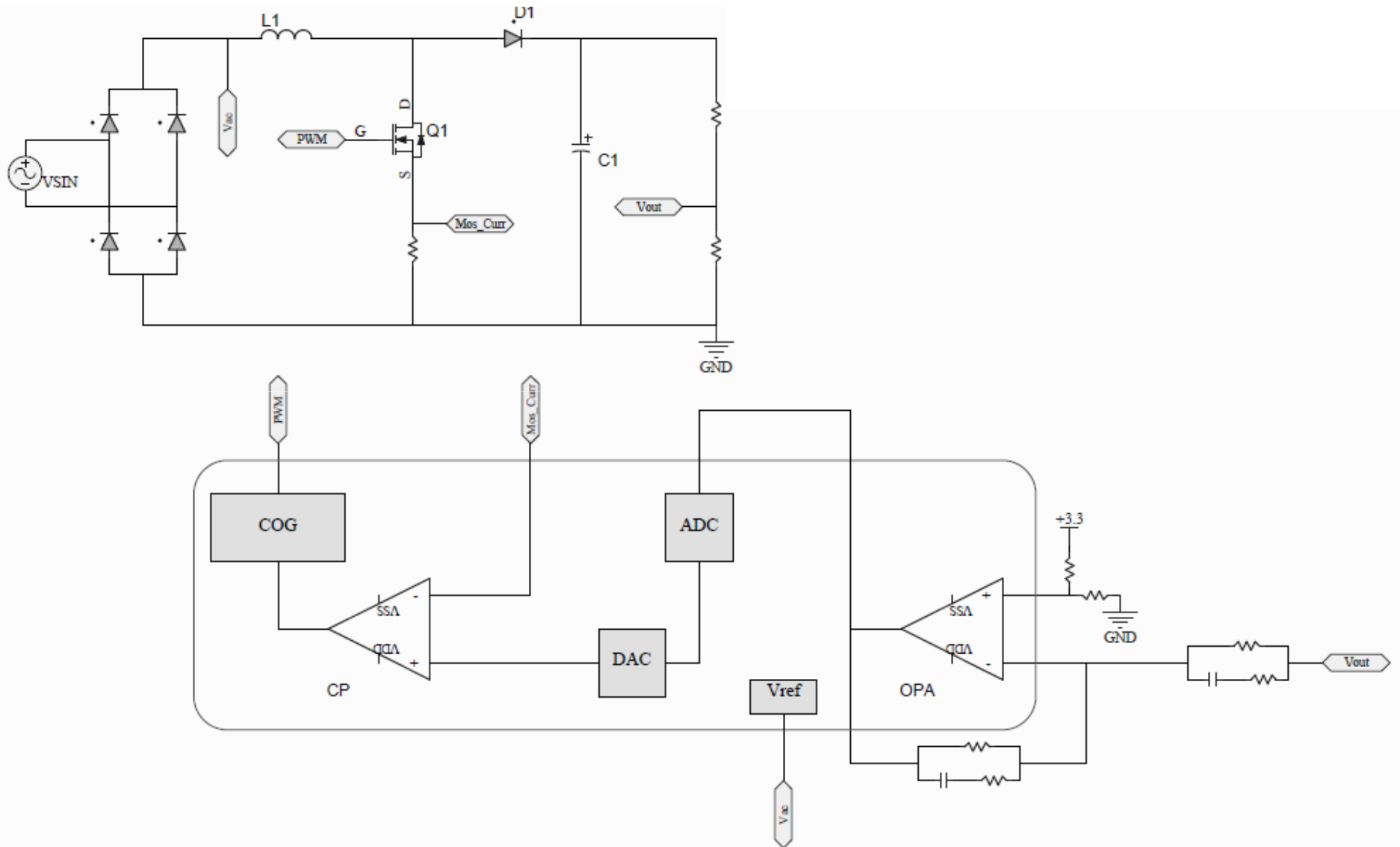# Flyback Converter

Dimming Control

PWM Dimming Control W/ PFC
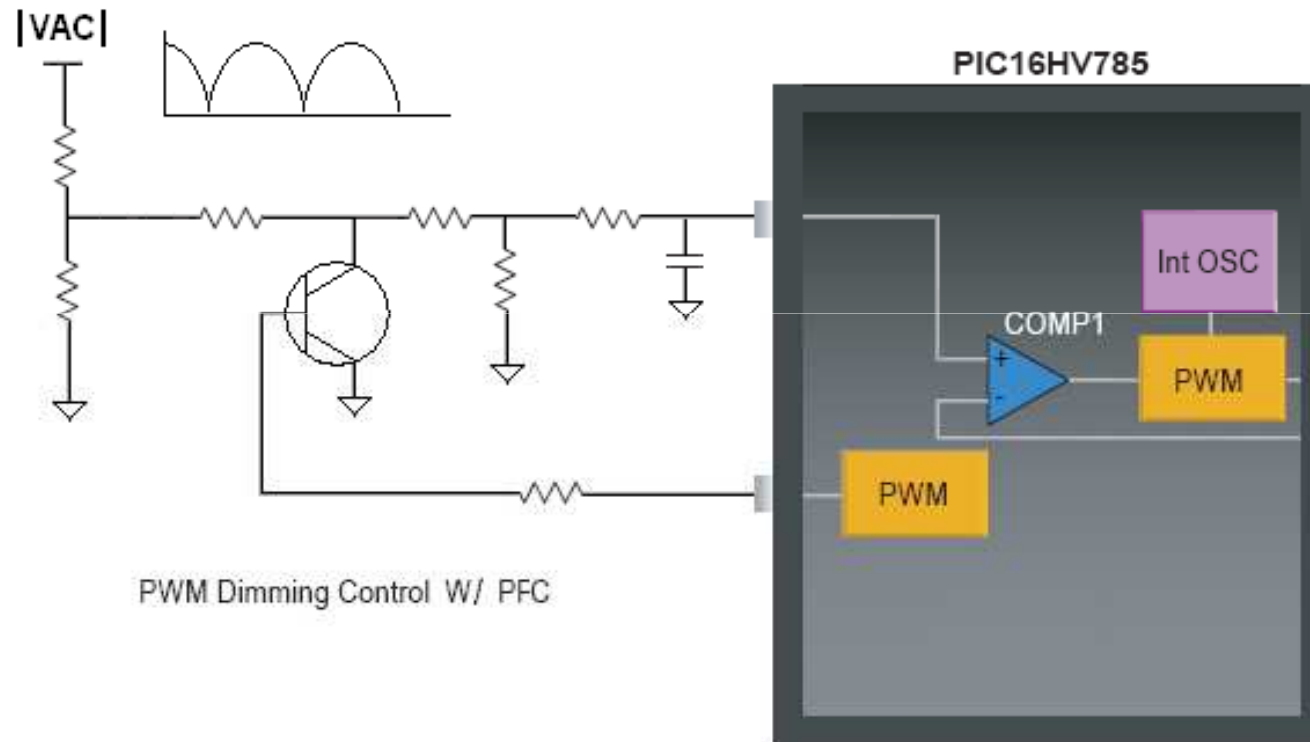
- ΧΧΠ ισ υσεδ το χοντρολ ςρεφ ανδ τηε ουτπυτ ποωερ.

17091 PS2   Slide   71

Flyback Converter

Combining PFC and Dimming

One more.....CIP Module

Thank You

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References

- www.microchip.com/smps

- Platinum-Rated AC/DC Reference Design Using the dsPIC© DSC Application Note AN1421

- Interleaved Power Factor Correction (IPFC) Using the dsPIC © DSC Application Note AN1278

- H.Z. Azazi, E.E. El-Kholy, S.A. Mahmoud and S.S. Shokralla, "Review of Passive and Active Circuits for Power Factor Correction in Single Phase, Low Power AC-DC Converters" MEPCON'10, Cairo Egypt, Paper ID 154.

- Michael O'Loughlin, "An Interleaving PFC Pre-Regulator for High Power Converters" Texas Instruments, Topic 5.

- http://www.cps.fi/Library/Power_Factor_C.pdf

- Joel Turchi, "A High-Efficiency, 300W Bridgeless PFC Stage" On Semiconductor, AND8481/D

- Joel Turchi, "A 800W Bridgeless PFC Stage" On Semiconductor, AND8392/D

- Laszlo Huber, Yungtaek Jang, and Milan M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers", Delta Products Corporation

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