

Jikai Wang

<https://happywjw.github.io/> (607) 319-2699 · jw2777@cornell.edu

EDUCATION

Cornell University

M.Eng in Electrical and Computer engineering

Relevant Coursework: Computer Architecture; Intro to Digital (VLSI) Design; Complex Digital ASIC Design

Ithaca, US

Expected Dec 2025

The University of Manchester

BSc (Hons) in Physics GPA 3.91/4.0

Relevant Coursework: Quantum Computing; Condensed Matter Physics; Semiconductor Quantum Structures; Electrodynamics(M)

Manchester, UK

Sept 2020 - June 2023

WORK EXPERIENCE

High-Level Synthesis for Machine Learning Accelerators (Allo & Xilinx Vivado/Vitis)

Research assistant under Prof. Christopher Batten

Sept 2024 - Now

- Designed FPGA accelerators using Allo, a new Python-based domain-specific language developed by Cornell Computer Systems Laboratory, targeting high-performance workloads in machine learning, genomics, and robotics.
- Rewrote PyTorch MNIST models in Allo, achieving performance parity with original models, and conducted comprehensive resource analysis.
- Accelerated HLS MNIST MLP models by **224x** using Allo HLS, optimizing layer architecture and resolving loop dependencies on different layers.
- Synthesized FPGA designs on Alveo U250, applying **pipeline, unroll, and partition** techniques to achieve single-cycle pipeline interval on computation layers.
- Optimizations led to a large increase in BRAM usage (from 1% to 19%) and higher FF and LUT utilization (from ~0% to 1%), trading area for significant performance gains.
- Currently porting CycleGAN models to Allo, targeting FPGA deployment to balance performance, area, and resource efficiency.

PROJECT EXPERIENCE

Pipelined Processor and Multi-Core System Design

Sept – Dec 2024

- Designed and implemented a **four-core multi-core system** with private instruction caches and a shared banked data cache, supporting TinyRV2 ISA.
- Developed a **five-stage pipelined processor** with bypassing, squashing, and stalling mechanisms to mitigate hazards (data, control, structural).
- Built ring-network interconnects for **cache-coherent memory** communication across cores.
- Created a **unit and full-system testing framework** using pytest, incorporating directed and random test generation for core components.
- Evaluated performance through CPI, throughput, and memory latency analysis for sorting benchmarks (single/multi-threaded).

GAN-Based Image Transformation System on Raspberry Pi

Nov – Dec 2024

- Built a real-time GAN-based image transformation system using Raspberry Pi 4, Pi camera, and PiTFT touchscreen.
- Deployed Pix2Pix (U-Net architecture) for day-to-night transformations and artistic style transfers, leveraging encoder-decoder layers with skip connections.
- Trained the model on 18,000 paired images over 400 epochs using multi-GPU and tqdm progress tracking.
- Integrated CycleGAN to generate images based on command labels.
- Developed a touchscreen Python interface enabling one-tap image capture and transformation selection directly on the PiTFT.

SKILL

Programming Language: C, python, Verilog, PyMTL3.

Technical Tools: PyTorch, Xilinx Vivado, Vitis, High-Level Synthesis (HLS), GitHub, Vscode.

Hardware: FPGA (Alveo U250), Raspberry Pi