Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Title:	Electronic Circuits I
Course Section:	ELE404
Semester/Year (e.g. F2017)	W2024

Instructor	Dr. Fei Yuan

Assignment/Lab Number:	N/A
Assignment/Lab Title:	Design Project

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Table Of Contents

Circuit Description

Constraints
- $V_{cc} = 10V$
- $I_c \leq 10mA$
- $|A_{vo}| = 50 \pm 5$
- $|A_v| \geq (0.9)(|A_{vo}|)$
- $R_{in} \geq 20k\Omega$

Assumptions
- $\beta = 150$
- $R_{out,ce} \approx 10k\Omega$
- $R_{out} \approx 1k\Omega$
- For biasing current stability set $V_E = 3V_{BE}$: $V_E = 2.1V$
- For good output swing set $V_c = \frac{1}{2}(V_{cc} + V_E + 0.3)$: $V_c = 6.2V$

Givens
- $R_s = 600\Omega$
- $R_L = 1k\Omega$

- Based on the desired $|A_{vol}|$, R_{in}, and $R_{o,ce}$ the CE amplifier will be best to achieve these values.
- Furthermore to achieve the R_o the CC amplifier will be the second stage due to it's signal buffering properties.
- Using capacitor values from LAB 7. $C_1 = 10\mu F$, $C_2 = C_3 = 100\mu F$

Setup:

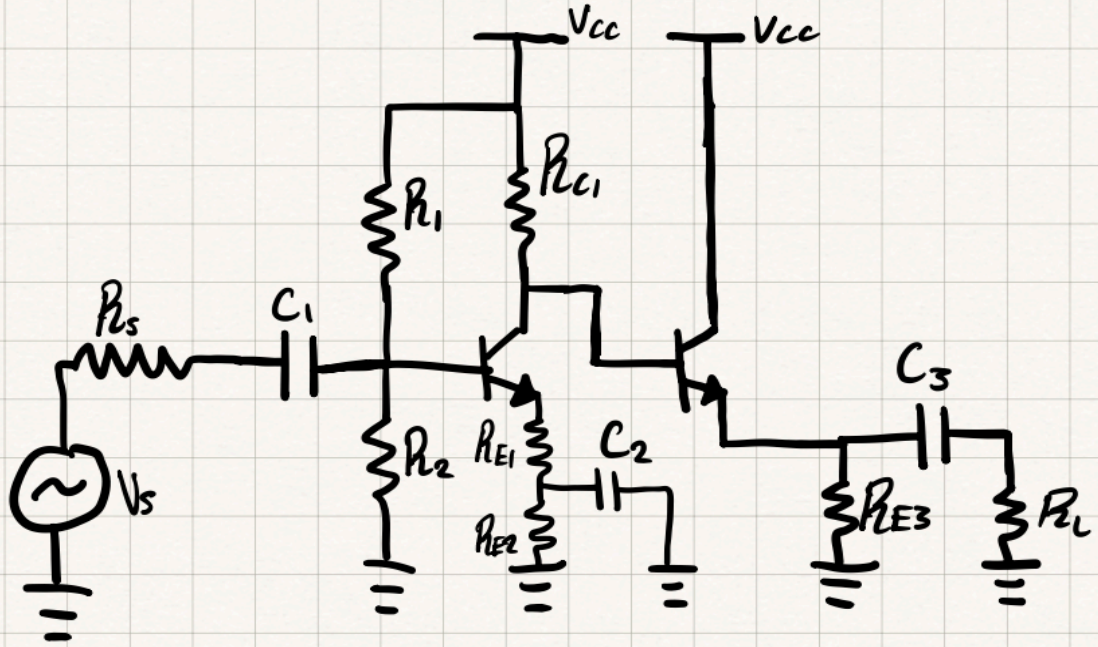


Figure 1. CE amplifier that cascades to a CC amplifier.

Calculations

$I_c = \frac{V_{cc} - V_c}{R_c}$ - since CE → $R_{o,CE} \approx R_c = 10k\Omega$

$I_c = \frac{10 - 6.2}{10k} = 0.38mA$

$I_c \approx I_E = 0.38mA$

$g_m = 26 I_C \rightarrow g_m = 9.88mS$

$R_{E1} + R_{E2} = \frac{V_E}{I_E} = \frac{2.1\,V}{0.38mA} = 5.47k\Omega$

$|A_{V0}| = \left| \frac{-g_m \cdot R_c}{1 + g_m \cdot R_{E1}} \right| = 50$

$50 = \frac{(9.88)(10)}{1 + (9.88)(R_{E1})} \rightarrow R_{E1} = 0.0987k\Omega$

$R_{E2} = 5.37k\Omega$

$R_i \geq 20k\Omega$

$(R_1 \| R_2 \| R_i') \geq 20k\Omega$

$\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_i'} \geq \frac{1}{20}$

$R_i' = r_\pi + (\beta + 1) R_{E1}$

$R_i' = \frac{\beta}{g_m} + (\beta + 1) R_{E1}$

$R_i' \approx 30k\Omega$

$R_1 \| R_2 \geq \left(\frac{1}{20} - \frac{1}{30} \right)^{-1}$

$R_1 \| R_2 \geq 60k\Omega$

$R_1 \| R_2 = 60k\Omega$

$V_B = V_{cc} \cdot \frac{R_2}{R_1 + R_2}$

$2.8 = 10 \cdot \frac{R_2}{R_1 + R_2}$

$\frac{R_1 \cdot R_2}{R_1 + R_2} = 60$ ①

$\frac{R_1 + R_2}{R_2} = 3.57$ ②

Solving eqn ① & ② → $R_1 = 214.2k\Omega$

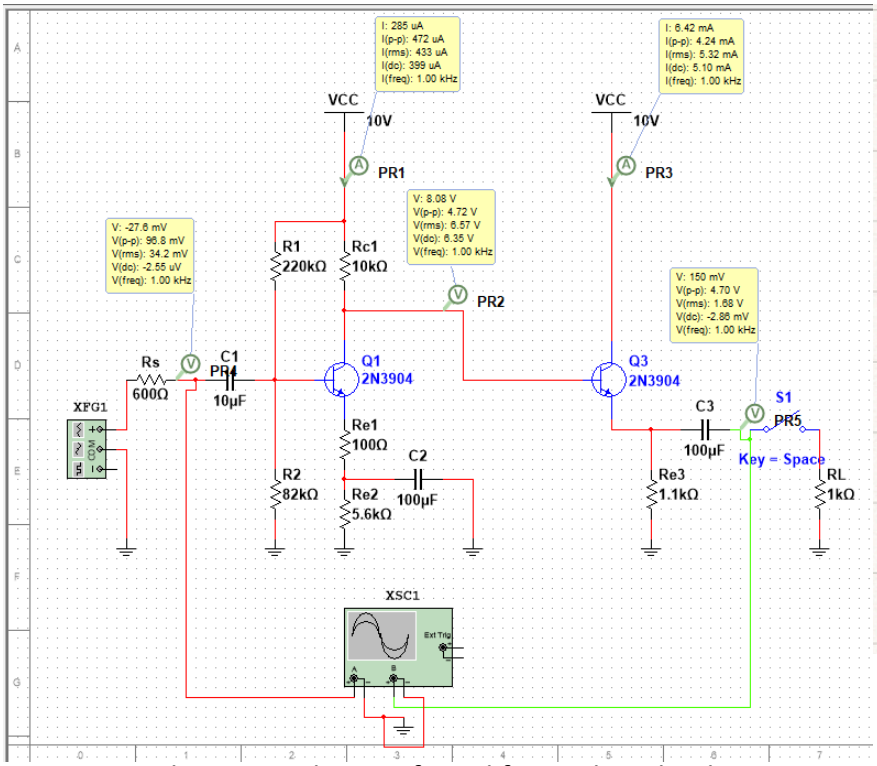
$R_2 = 83.34k\Omega$

$R_o = R_{E3} \| R_{o,CE}$

$1k\Omega = \frac{R_{E3} \cdot (10k\Omega)}{R_{E3} + 10k\Omega} \rightarrow R_{E3} = 1.11k\Omega$

Due to resistor constraints: $R_c = 10k\Omega$, $R_{E1} = 0.1k\Omega$, $R_{E2} = 5.6k\Omega$, $R_1 = 220k\Omega$, and $R_2 = 82k\Omega$, $R_{E3} = 1.1k\Omega$

Simulations and Verification



$I_c = I_{c1} + I_{c2}$

$= 0.285mA + 6.42mA$

$= 6.705mA \leq 10mA$ ✓

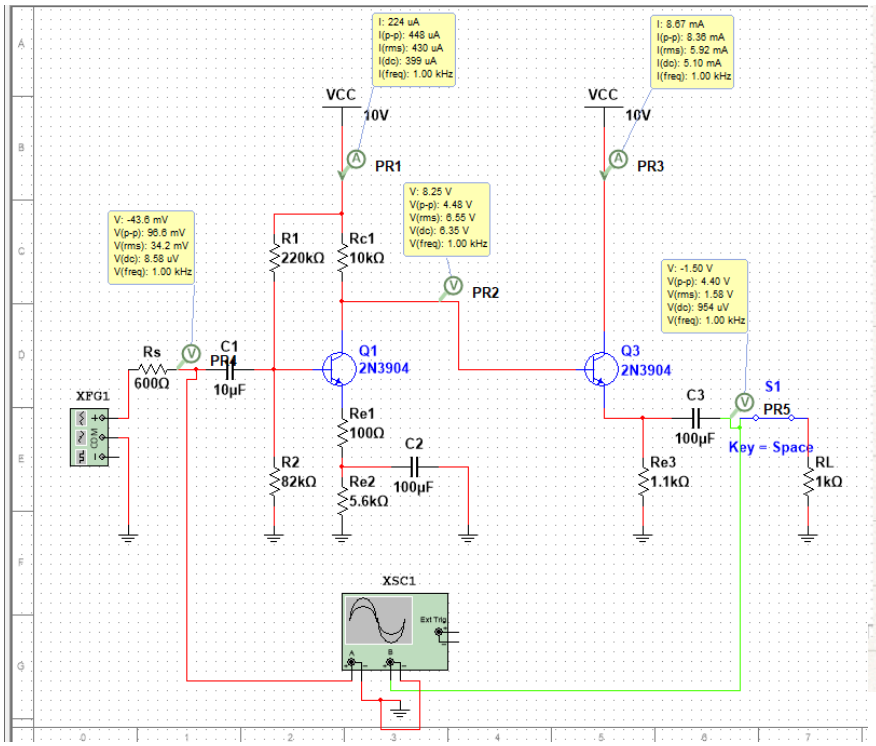
$|A_{vo}| = \frac{V_o}{V_i} = \frac{4.70}{0.0968} = 48.6$

$|A_{vo}| = 50 \pm 5 \rightarrow 45 \leq |A_{vo}| \leq 55$

$45 \leq 48.6 \leq 55$ ✓

*Both values within spec *

Figure 2. MultiSim simulation of amplifier with no load.



$I_c = I_{c1} + I_{c2}$

$= 0.224mA + 8.67mA$

$= 8.894mA \leq 10mA$ ✓

$|A_v| = \frac{V_o}{V_i} = \frac{4.40}{0.0966} = 45.5$

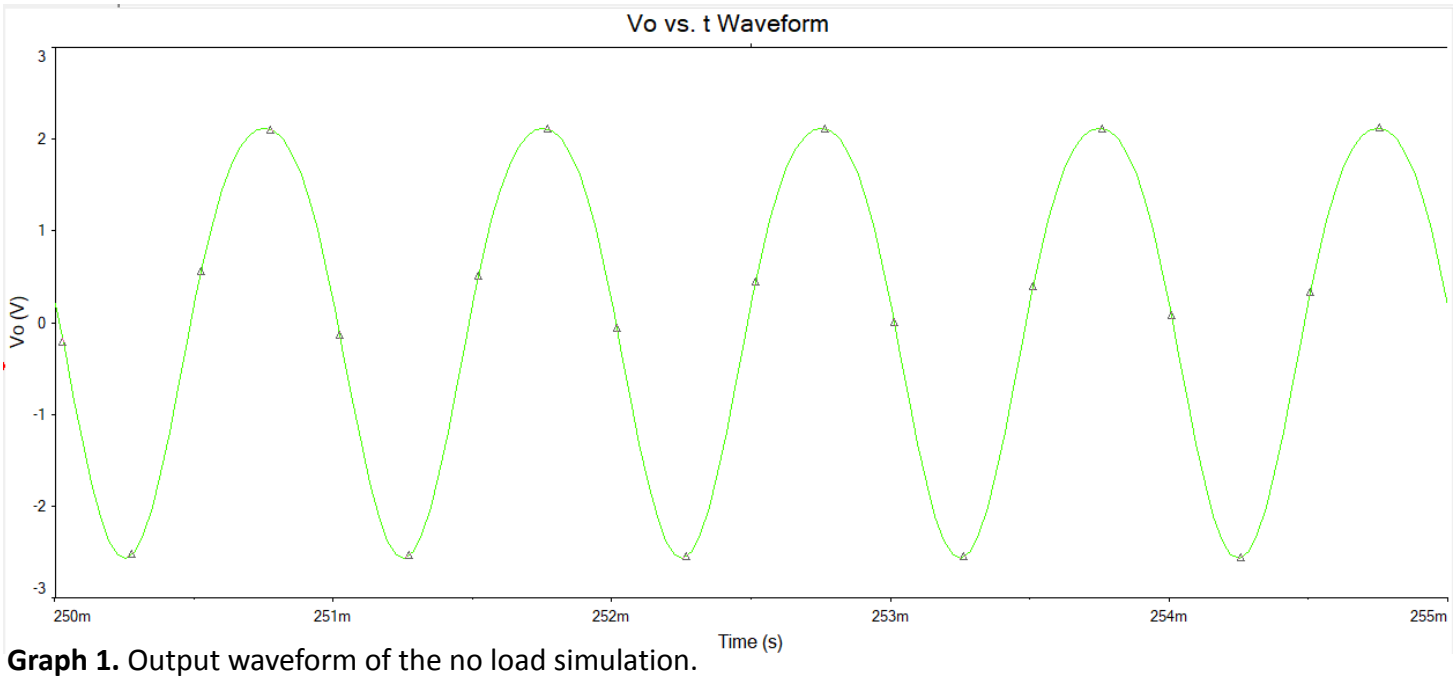
$|A_{vo}|(0.9) = (48.6)(0.9)$

$= 43.7$

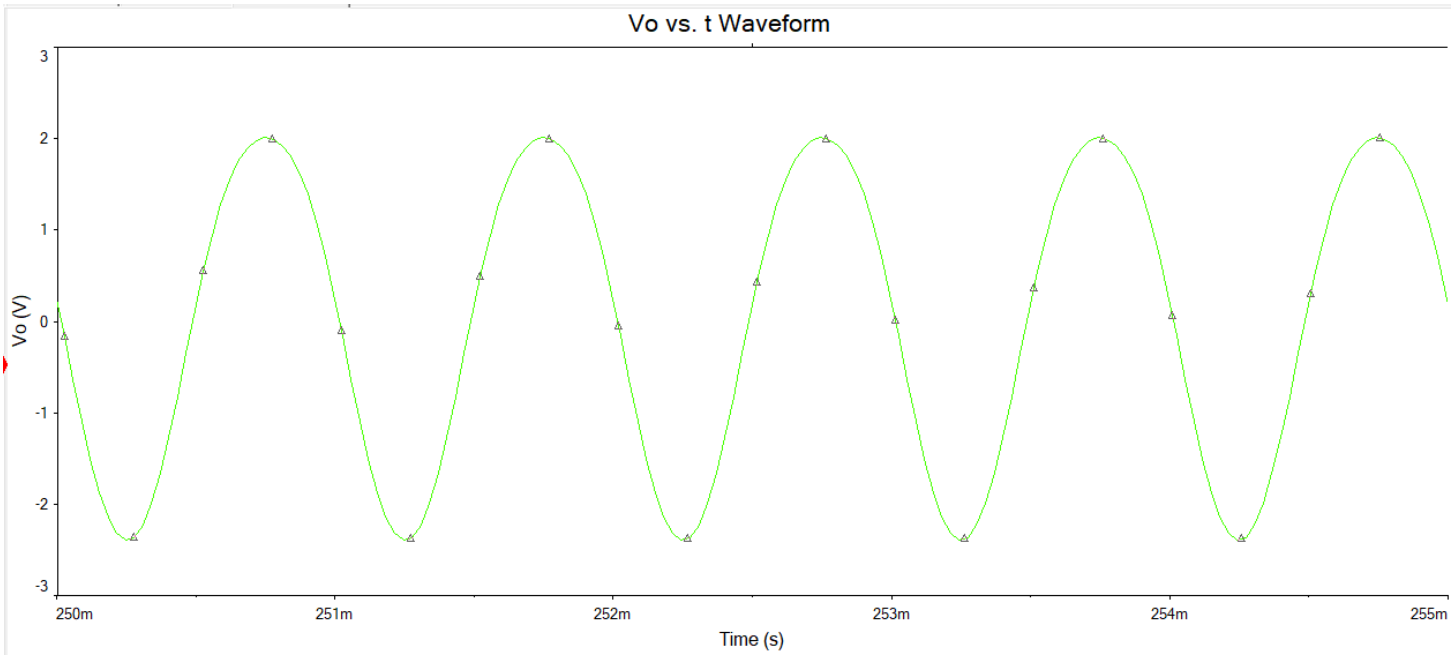
$45.5 \geq 43.7$ ✓

*Both values within spec *

Figure 3. MultiSim simulation of amplifier with load.



Graph 1. Output waveform of the no load simulation.



Graph 2. Output waveform of the loaded simulation.

Discrepancies/Notes

- The slight differences can most likely be attributed to the approximations made whilst doing initial calculations.
- Another reason for slight discrepancies was that whilst selecting the final resistance values, all of the values that were calculated had to be altered to meet the E24 constraints.

References

Lab 7 - Common-Collector (CC) Amplifier. (2024). Toronto Metropolitan University.

Yuan, Fei. (2024). *Module 3: BJT Voltage Amplifiers.* D2L Brightspace.

Kaler, Sandeep. (2023). *Lecture 9A.* Metropolitan Undergraduate Engineering Society