

Problem 1)

I was not able to get state transitions to work but I do know that it is possible for the criteria to be met if the instruction set starts at either Neo or Smith. An example of this process for starting at Neo is provided.

Initial -> Neo -> Bus1 -> Oracle -> Bus2 -> Neo -> Bus3 -> Smith -> Bus4 -> Oracle -> Bus5 -> Architect -> Bus6 -> Smith -> Terminal

Problem 2)

Again, as I was not able to get state transitions to work I cannot properly complete this question. However, I do know that there is no solution to this model as there is no path from any of the cores that will allow an instruction set to pass through all buses only once. I do not know how to prove this other than that I traced through each path by hand.