LTC3350

High Current Supercapacitor Backup Controller and System Monitor

FEATURES

- **High Efficiency Synchronous Step-Down CC/CV Charging of One to Four Series Supercapacitors**
- **Step-Up Mode in Backup Provides Greater Utilization of Stored Energy in Supercapacitors**
- **14-Bit ADC for Monitoring System Voltages/Currents, Capacitance and ESR**
- **Active Overvoltage Protection Shunts**
- **Internal Active Balancers—No Balance Resistors**
- V_{IN}: 4.5V to 35V, $V_{CAP(n)}$: Up to 5V per Capacitor, Charge/Backup Current: 10+A
- Programmable Input Current Limit Prioritizes System Load Over Capacitor Charge Current
- Dual Ideal Diode PowerPath™ Controller
- All N-FET Charger Controller and PowerPath Controller
- Compact 38-Lead 5mm × 7mm QFN Package

APPLICATIONS

- High Current 12V Ride-Through UPS
- Servers/Mass Storage/High Availability Systems

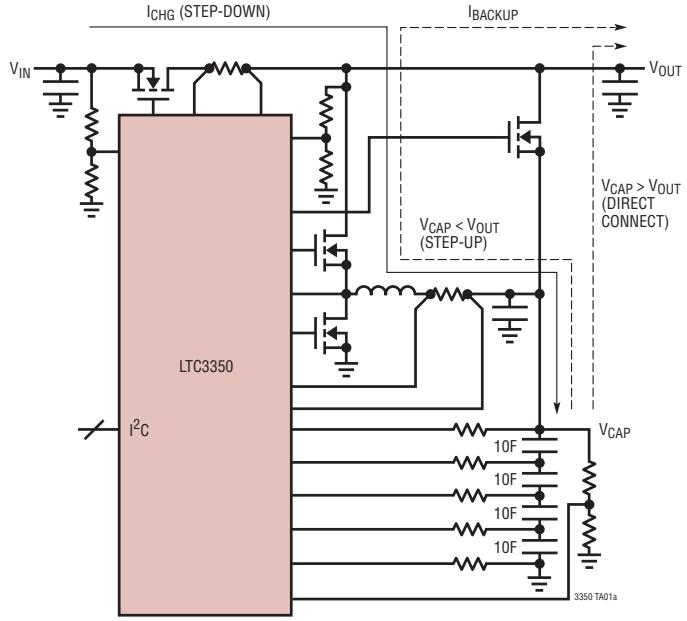
DESCRIPTION

The LTC®3350 is a backup power controller that can charge and monitor a series stack of one to four supercapacitors. The LTC3350's synchronous step-down controller drives N-channel MOSFETs for constant current/constant voltage charging with programmable input current limit. In addition, the step-down converter can run in reverse as a step-up converter to deliver power from the supercapacitor stack to the backup supply rail. Internal balancers eliminate the need for external balance resistors and each capacitor has a shunt regulator for overvoltage protection.

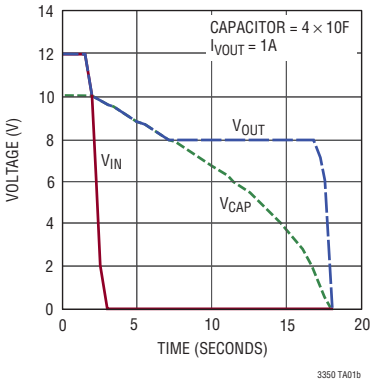
The LTC3350 monitors system voltages, currents, stack capacitance and stack ESR which can all be read over the I²C/SMBus. The dual ideal diode controller uses N-channel MOSFETs for low loss power paths from the input and supercapacitors to the backup system supply. The LTC3350 is available in a low profile 38-lead 5mm × 7mm × 0.75mm QFN surface mount package.

TYPICAL APPLICATION

High Current Supercapacitor Charger and Backup Supply



Backup Operation



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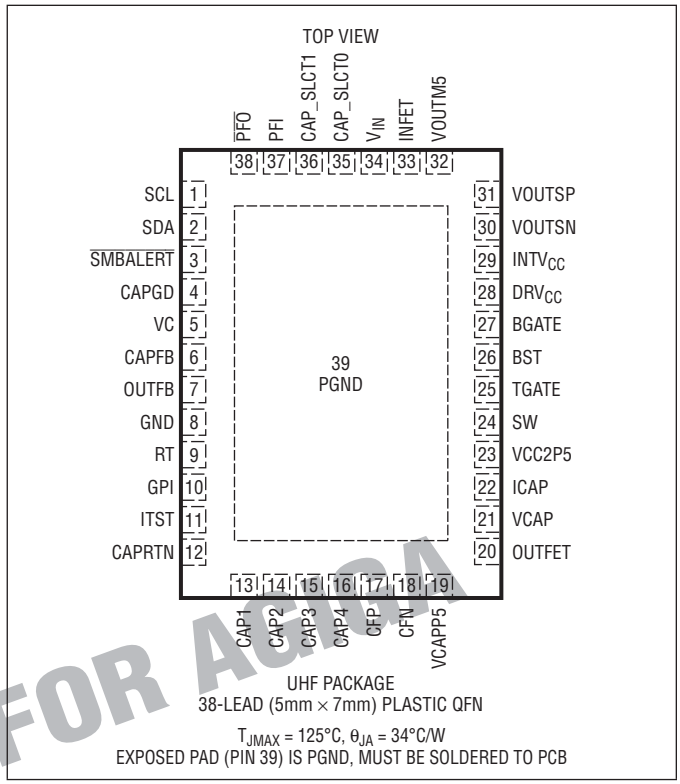
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, VOUTSP, VOUTSN ..... –0.3V to 40V
VCAP ..... –0.3V to 22V
CAP4-CAP3, CAP3-CAP2, CAP2-CAP1,
CAP1-CAPRTN ..... –0.3V to 5.5V
DRV_{CC}, OUTFB, CAPFB, $\overline{SMBALERT}$, CAPGD,
$\overline{PFO}$, GPI, SDA, SCL ..... –0.3V to 5.5V
BST to GND ..... –0.3V to 45.5V
PFI ..... –0.3V to 20V
CAP_SLCT0, CAP_SLCT1 ..... –0.3 to 3V
BST to SW ..... –0.3V to 5.5V
VOUTSP to VOUTSN, ICAP to VCAP ..... –0.3V to 0.3V
I_{INTVCC} 100mA
$I_{CAP(1,2,3,4)}$, I_{CAPRTN} 600mA
I_{CAPGD}, $I_{\overline{PFO}}$, $I_{\overline{SMBALERT}}$ 10mA
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3350EUHF#PBF	LTC3350EUHF#TRPBF	3350	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3350IUHF#PBF	LTC3350IUHF#TRPBF	3350	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator							
V_{IN}	Input Supply Voltage		●	4.5		35	V
I_Q	Input Quiescent Current (Note 4)				4		mA
$V_{CAPFBHI}$	Maximum Regulated V_{CAP} Feedback Voltage	V_{CAPDAC} Full Scale (1111b)	 ●	1.194 1.19	1.200 1.200	1.206 1.21	V V
$V_{CAPFBLO}$	Minimum Regulated V_{CAP} Feedback Voltage	V_{CAPDAC} Zero Scale (0000b)		0.631	0.638	0.644	V
I_{CAPFB}	CAPFB Input Leakage Current	V_{CAPFB} = 1.2V	●	–50		50	nA
V_{OUTFB}	Regulated V_{OUT} Feedback Voltage		 ●	1.188 1.176	1.200 1.200	1.212 1.224	V V
I_{OUTFB}	OUTFB Input Leakage Current	V_{OUTFB} = 1.2V	●	–50		50	nA
V_{OUTBST}	V_{OUT} Boost Voltage	V_{IN} = 0V	●	4.5		35	V
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.9	4.3 4	4.4	V V
$V_{DRVUVLO}$	DRV_{CC} Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.8	4.2 3.9	4.3	V V
V_{DUVLO}	V_{IN} – V_{CAP} Differential Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	TBD TBD	200 100	TBD TBD	V V
V_{OVLO}	V_{IN} Overvoltage Lockout	Rising Threshold Falling Threshold	● ●	37.7 36.3	38.6 37.2	39.5 38.1	V V
V_{VCAPP5}	Charge Pump Output Voltage	Relative to V_{CAP}, 0V ≤ V_{CAP} ≤ 20V			5		V
Input Current Sense Amplifier							
V_{SNSI}	Regulated Input Current Sense Voltage (VOUTSP – VOUTSN)		 ●	31.68 31.36	32.00 32.00	32.32 32.64	mV mV
V_{CMI}	Common Mode Range (VOUTSP, VOUTSN)			4.5		35	V
Charge Current Sense Amplifier							
V_{SNSC}	Regulated Charge Current Sense Voltage (ICAP – VCAP)	0V ≤ V_{CAP} ≤ 20V	 ●	31.68 31.36	32.00 32	32.32 32.64	mV mV
V_{CMC}	Common Mode Range (ICAP, VCAP)			0		20	V
V_{PEAK}	Peak Inductor Current Sense Voltage	I_{PEAK} = V_{PEAK}/R_{SNSC}	●	49	52	55	mV
V_{REV}	Reverse Inductor Current Sense Voltage	I_{REV} = V_{REV}/R_{SNSC}	●	3.867	4.167	4.467	mV
I_{ICAP}	ICAP Pin Current	Step-Down Mode, V_{SNSC} = 32mV Step-Up Mode, V_{SNSC} = 32mV			30 135		µA µA
Error Amplifier							
g_{MV}	V_{CAP} Voltage Loop Transconductance				1.2		mmho
g_{MC}	Charge Current Loop Transconductance				64		µmho
g_{MI}	Input Current Loop Transconductance				64		µmho
g_{MO}	V_{OUT} Voltage Loop Transconductance				400		µmho
Oscillator							
f_{OSC}	Switching Frequency	R_T = 107k	●	495	500	505	kHz
	Maximum Programmable Frequency	R_T = 53.6k			1		MHz
	Minimum Programmable Frequency	R_T = 267k			200		kHz
DC_{MAX}	Maximum Duty Cycle	Step-Down Mode Step-Up Mode		97 90	98 94	100	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers							
R_{UP-TG}	TGATE Pull-Up On-Resistance				1.5		Ω
$R_{DOWN-TG}$	TGATE Pull-Down On-Resistance				0.6		Ω
R_{UP-BG}	BGATE Pull-Up On-Resistance				1.5		Ω
$R_{DOWN-BG}$	TGATE Pull-Down On-Resistance				0.6		Ω
t_{r-TG}	TGATE 10% to 90% Rise Time	C_{LOAD} = 3.3nF			12	25	ns
t_{f-TG}	TGATE 10% to 90% Fall Time	C_{LOAD} = 3.3nF			6	15	ns
t_{r-BG}	BGATE 10% to 90% Rise Time	C_{LOAD} = 3.3nF			12	25	ns
t_{f-BG}	BGATE 10% to 90% Fall Time	C_{LOAD} = 3.3nF			6	15	ns
t_{NO}	Non-Overlap Time				30		ns
$t_{ON(MIN)}$					80		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	5.2V ≤ V_{IN} ≤ 35V			5		V
ΔV_{INTVCC}	Load Regulation	I_{INTVCC} = 50mA			–1	–2	%
PowerPath/Ideal Diodes							
V_{FTO}	Forward Turn-On Voltage				45		mV
V_{FR}	Forward Regulation				15		mV
V_{RTO}	Reverse Turn Off				–30		mV
$t_{IF(ON)}$	INFET Rise Time	INFET – V_{IN} > 3V, C_{INFET} = 3.3nF			500		µs
$t_{IF(OFF)}$	INFET Fall Time	INFET – V_{IN} < 1V, C_{INFET} = 3.3nF			2.0		µs
$t_{OF(ON)}$	OUTFET Rise Time	OUTFET – V_{CAP} > 3V, C_{OUTFET} = 3.3nF			1		µs
$t_{OF(OFF)}$	OUTFET Fall Time	OUTFET – V_{CAP} < 1V, C_{OUTFET} = 3.3nF			0.75		µs
Power-Fail Comparator							
$V_{PFI(TH)}$	PFI Input Threshold (Falling Edge)		●	1.162	1.17	1.178	V
$V_{PFI(HYS)}$	PFI Hysteresis				30		mV
I_{PFI}	PFI Input Leakage Current	V_{PFI} = 0.5V	●	–50		50	nA
$V_{\overline{PFO}}$	$\overline{PFO}$ Output Low Voltage	I_{SINK} = 5mA			200		mV
$I_{\overline{PFO}}$	$\overline{PFO}$ High-Z Leakage Current	$V_{\overline{PFO}}$ = 5V	●			1	µA
	PFI Falling to $\overline{PFO}$ Low Delay	20mV of Overdrive on PFI			0.5		µs
	PFI Rising to $\overline{PFO}$ High Delay	20mV of Overdrive on PFI			1		µs
CAPGD							
$V_{CAPFB(TH)}$	CAPFB Input Threshold (Rising Edge)	V_{CAPDAC} Full Scale (1111b)	●	1.095	1.105	1.115	V
$V_{CAPFB(HYS)}$	CAPFB Hysteresis				15		mV
V_{CAPGD}	CAPGD Output Low Voltage	I_{SINK} = 5mA			200		mV
I_{CAPGD}	CAPGD High-Z Leakage Current	V_{CAPGD} = 5V	●			1	µA
Analog-to-Digital Converter							
V_{RES}	Measurement Resolution				14		Bits
V_{LSB}	Measurement LSB	Measuring V_{CAP1-4} or GPI			732		µV
V_{GPI}	General Purpose Input Voltage Range	Unbuffered Buffered		0 0		5 3.5	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{GPI}	General Purpose Input Pin Leakage Current	Buffered Input				1	µA
R_{GPI}	GPI Pin Resistance	Buffer Disabled			1		MΩ
Measurement System Error							
V_{ERR}	Measurement Error (Note 5)	V_{IN} = 10V V_{IN} = 30V			TBD		mV mV
		V_{OUTSP} = 10V V_{OUTSP} = 30V					mV mV
		V_{CAP} = 2V V_{CAP} = 10V					mV mV
		V_{GPI} = 1V V_{GPI} = 3.5V					mV mV
		V_{CAP1} = 100mV V_{CAP1} = 2V					mV mV
		V_{CAP2} = 100mV V_{CAP2} = 2V					mV mV
		V_{CAP3} = 100mV V_{CAP3} = 2V					mV mV
		V_{CAP4} = 100mV V_{CAP4} = 2V					mV mV
		V_{SNSI} = 32mV V_{SNSI} = 1mV					µV µV
		V_{SNSC} = 32mV V_{SNSC} = 1mV					µV µV
CAP1 to CAP4							
DV_{CAP}	CAP(N) – CAP(N-1) Voltage Range, N = 2-4			–0.7		5.3	V
R_{SHNT}	Shunt Resistance				0.5		Ω
DV_{CAPMAX}	Maximum Capacitor Voltage with Shunts Enabled	2 or More Capacitors in Stack				3.6	V
Programming Pins							
V_{ITST}	ITST Voltage				1.2		V
I_{ITST}	ITST Pin Current	R_{TST} = 121Ω			9.92		mA
I^2C/SMBus – SDA, SCL, $\overline{SMBALERT}$							
V_{IH}	Input High Threshold			1.5			V
V_{IL}	Input Low Threshold					0.8	V
f_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	Low Period of SCL Clock			1.3			µs
t_{HIGH}	High Period of SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Start and Stop Conditions			1.3			µs
$t_{HD,STA}$	Hold Time, After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Setup Time After a Repeated Start Condition			0.6			µs
$t_{SU,STO}$	Stop Condition Set-Up Time			0.6			µs
$t_{HD,DATO}$	Output Data Hold Time			0		900	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{HD,DATI}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Set-Up Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
$V_{\overline{SMBALERT}}$	$\overline{SMBALERT}$ Output Low Voltage	I_{SINK} = 1mA			200		mV
$I_{\overline{SMBALERT}}$	$\overline{SMBALERT}$ High-Z Leakage Current	$V_{\overline{SMBALERT}}$ = 5V	●			1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3350 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3350E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3350I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 34°C/W for the UHF package.

Note 3: The LTC3350 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

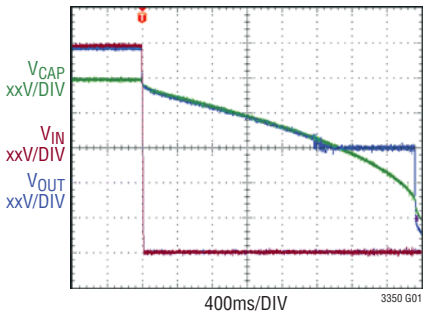
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 5: Measurement error is the difference between the actual measured code and the ideal code for an input value, referred to the input. V_{SNSI} is the voltage between VOUTSP and VOUTSN, simulating input current. V_{SNSC} is the voltage between ICAP and VCAP, simulating charge current. Error for V_{SNSI} and V_{SNSC} is expressed in µV, a conversion to an equivalent current may be made by dividing by the respective sense resistors, R_{SNSI} and R_{SNSC}, respectively.

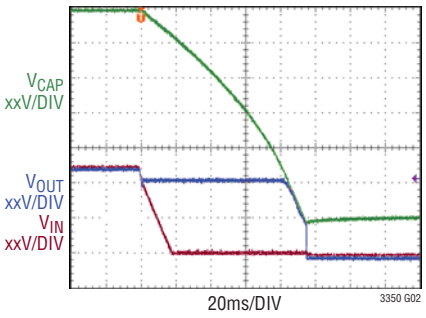
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

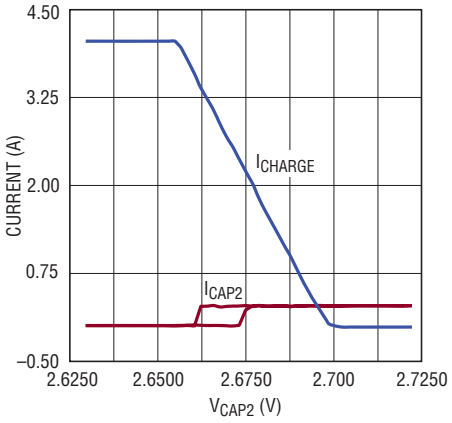
Supercapacitor Power Failure



HV Electrolytic Power Failure



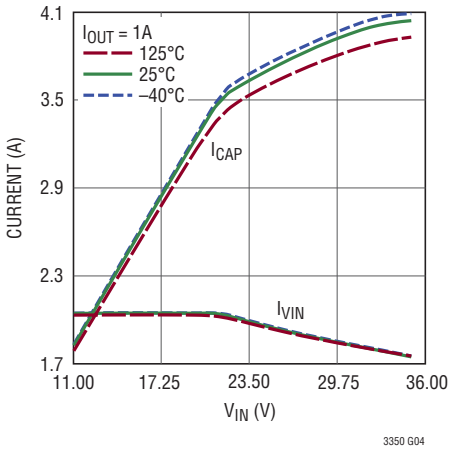
Shunt Operation Using V_{CAP2}



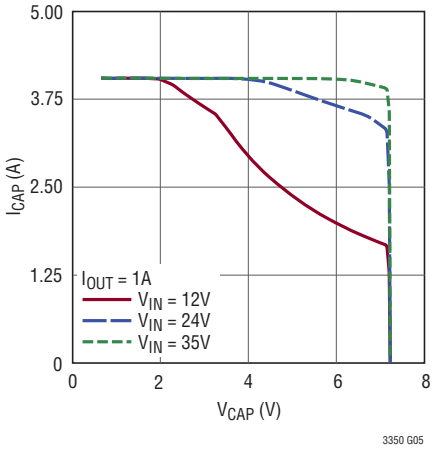
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

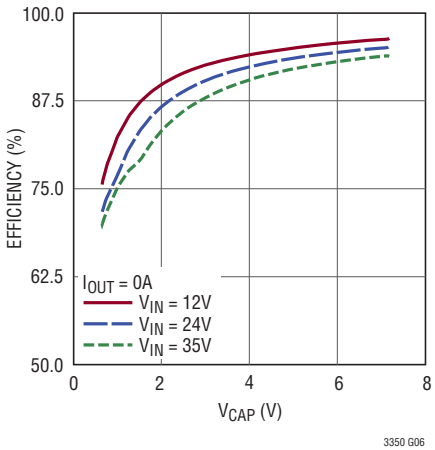
I_{VIN} and I_{CHARGE} vs V_{IN}



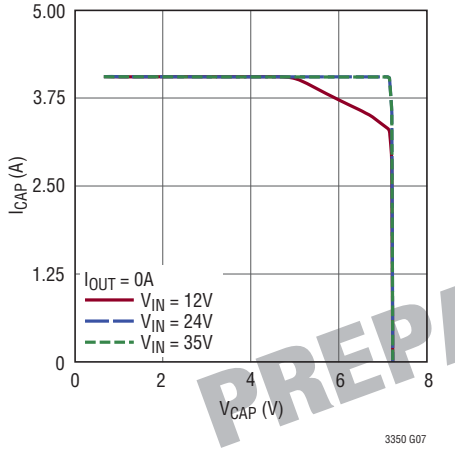
I_{CAP} vs V_{CAP}



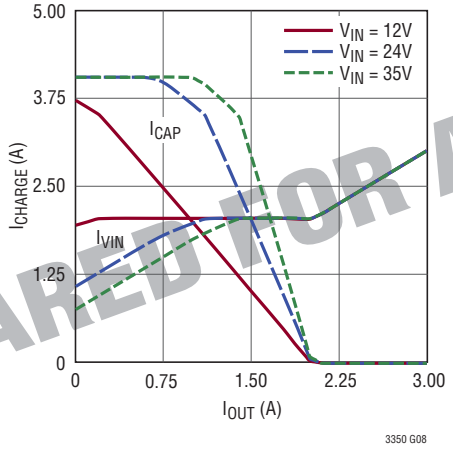
Charger Efficiency vs V_{CAP}



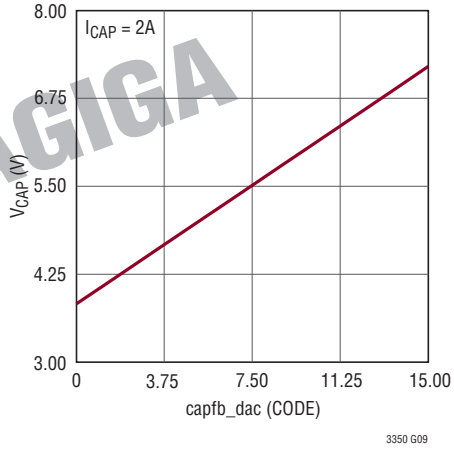
I_{CAP} vs V_{CAP}



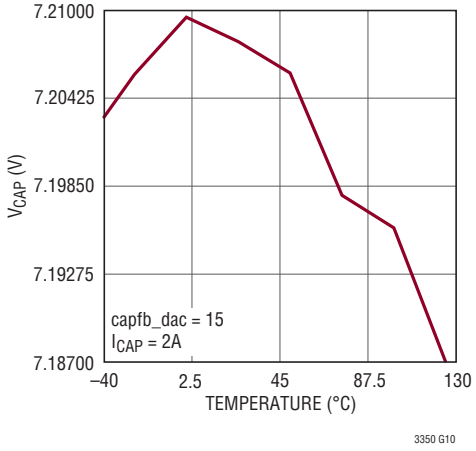
I_{CHARGE} vs I_{OUT}



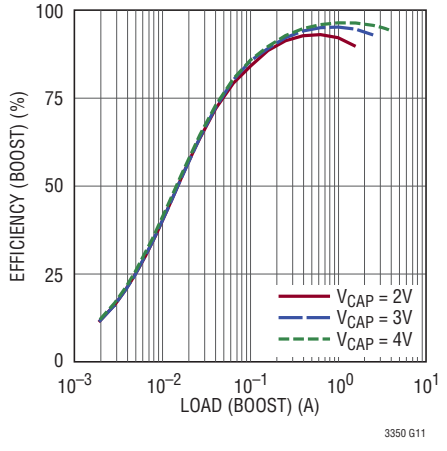
V_{CAP} vs capfb_dac



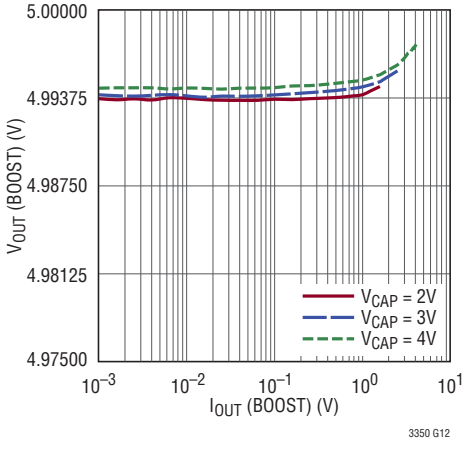
V_{CAP} vs Temperature



Efficiency in Boost



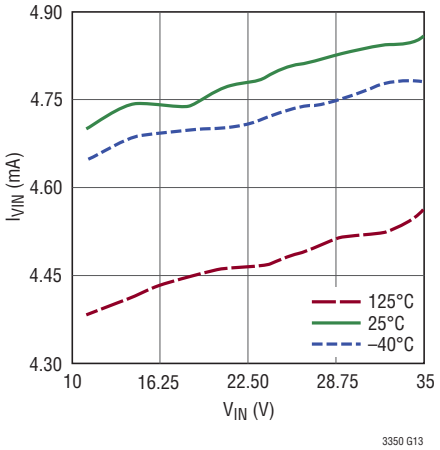
Load Regulation in Boost



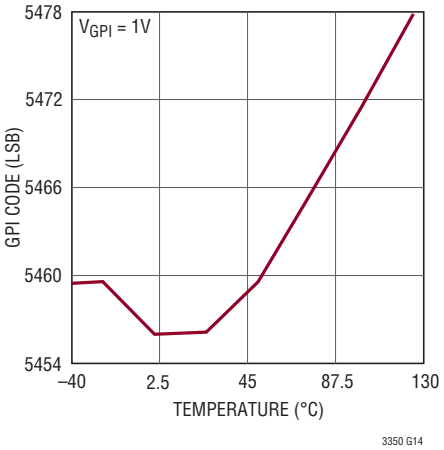
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

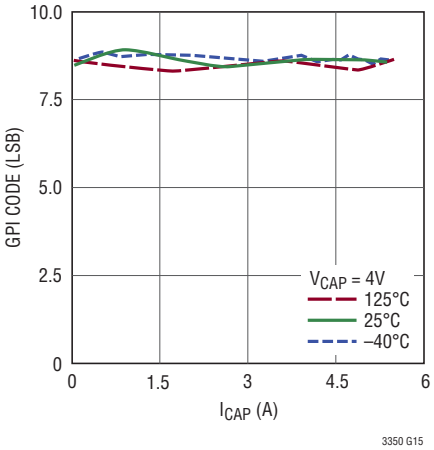
I_Q vs V_{IN}, Pulse Skipping



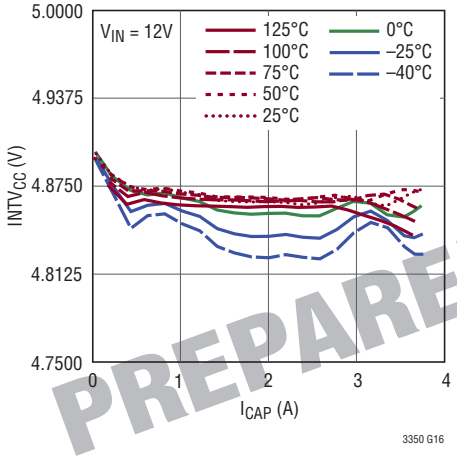
GPI Code vs Temperature



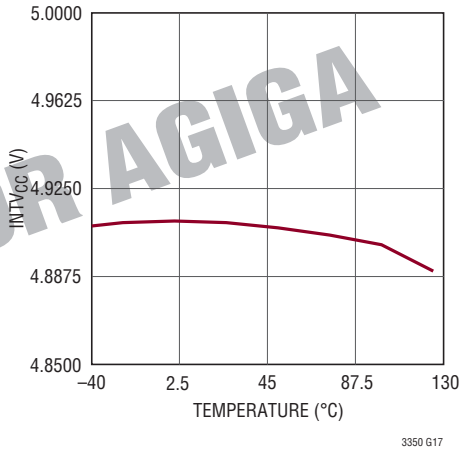
DRV_{CC} Current vs Boost Current



$INTV_{CC}$ vs Charge Current



$INTV_{CC}$ vs Temperature



PIN FUNCTIONS

SCL (Pin 1): Clock Pin for the I^2C/SMBus Serial Port.

SDA (Pin 2): Bidirectional Data Pin for the I^2C/SMBus Serial Port.

$\overline{\text{SMBALERT}}$ (Pin 3): Interrupt Output. This open-drain output is pulled low when an alarm threshold is exceeded, and will remain low until the acknowledgement of the part's response to an SMBus ARA.

CAPGD (Pin 4): Capacitor Power Good. This open-drain output is pulled low when there is insufficient voltage on the supercapacitor stack to power the backup supply rail.

VC (PIN 5): Control Voltage Pin. This is the compensation node for the charge current, input current, supercapacitor stack voltage and output voltage control loops. An RC network is connected between VC and GND. Nominal voltage range for this pin is 1V to 3V.

CAPFB (Pin 6): Capacitor Stack Feedback Pin. This pin closes the feedback loop for constant voltage regulation. An external resistor divider between VCAP and GND with the center tap connected to CAPFB programs the final supercapacitor stack voltage. This pin is nominally equal to the output of the V_{CAP} DAC when the synchronous controller is in constant voltage mode.

OUTFB (Pin 7): Step-Up Mode Feedback Pin. This pin closes the feedback loop for voltage regulation of V_{OUT} during input power failure using the synchronous controller in step-up mode. An external resistor divider between V_{OUT} and GND with the center tap connected to OUTFB

PIN FUNCTIONS

programs the backup supply rail voltage when input power is unavailable. This pin is nominally 1.2V when the synchronous controller is not in current limit. To disable step-up mode tie OUTFB to $INTV_{CC}$.

GND (Pin 8): Signal Ground. All small-signal and compensation components should be connected to this pin, which in turn connects to PGND at one point. This pin should also Kelvin to the bottom plate of the capacitor stack.

RT (Pin 9): Timing Resistor. The switching frequency of the synchronous controller is set by placing a resistor, R_T, to GND. This resistor is always required. If not present the synchronous controller will not start.

GPI (Pin 10): General Purpose Input. The voltage on this pin is digitized directly by the ADC. For high impedance inputs an internal buffer can be selected and used to drive the ADC. The GPI pin can be connected to a negative temperature coefficient (NTC) thermistor to monitor the temperature of the supercapacitor stack. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to GND if not used. The digitized voltage on this pin may be read in the meas_gpi register.

ITST (Pin 11): Programming Pin for Capacitance Test Current. This current is used to partially discharge the capacitor stack at a precise rate for capacitance measurement. This pin servos to 1.2V during a capacitor measurement. A resistor, R_{TST}, from this pin to ground programs the test current. R_{TST} is typically 121Ω.

CAPRTN (Pin 12): Capacitor Stack Shunt Return Pin. This pin is connected to the grounded bottom plate of the first super capacitor in the stack through a shunt resistor.

CAP1 (Pin 13): First Supercapacitor Pin. The top plate of the first supercapacitor and the bottom plate of the second supercapacitor are connected to this pin through a shunt resistor. CAP1 and CAPRTN are used to measure the voltage across the first super capacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. The voltage between this pin and CAPRTN is digitized and may be read in the meas_vcap1 register.

CAP2 (Pin 14): Second Supercapacitor Pin. The top plate of the second supercapacitor and the bottom plate of the third supercapacitor are connected to this pin through a shunt resistor. CAP2 and CAP1 are used to measure the voltage across the second supercapacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. If not used this pin should be shorted to CAP1. The voltage between this pin and CAP1 is digitized and may be read in the meas_vcap2 register.

CAP3 (Pin 15): Third Supercapacitor Pin. The top plate of the third supercapacitor and the bottom plate of the fourth supercapacitor are connected to this pin through a shunt resistor. CAP3 and CAP2 are used to measure the voltage across the third supercapacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. If not used this pin should be shorted to CAP2. The voltage between this pin and CAP2 is digitized and may be read in the meas_vcap3 register.

CAP4 (Pin 16): Fourth Supercapacitor Pin. The top plate of the fourth supercapacitor is connected to this pin through a shunt resistor. CAP4 and CAP3 are used to measure the voltage on the capacitor and to shunt current around the supercapacitor to provide balancing and to limit capacitor voltage. If not used this pin should be shorted to CAP3. The voltage between this pin and CAP3 is digitized and may be read in the meas_vcap4 register.

CFP (Pin 17): VCAPP5 Charge Pump Flying Capacitor Positive Terminal. Place a 0.1µF between CFP and CFN.

CFN (Pin 18): VCAPP5 Charge Pump Flying Capacitor Negative Terminal. Place a 0.1µF between CFP and CFN.

VCAPP5 (Pin 19): Charge Pump Output. The internal charge pump drives this pin to VCAP + $INTV_{CC}$ which is used as the high side rail for the OUTFET gate drive and charge current sense amplifier. Connect a 0.1µF capacitor from VCAPP5 to VCAP.

OUTFET (Pin 20): Output Ideal Diode Gate Drive Output. This pin controls the gate of an external N-channel MOSFET used as an ideal diode between V_{OUT} and V_{CAP}. The gate drive receives power from the internal charge pump output VCAPP5. The source of the N-channel MOSFET should be connected to VCAP and the drain should be connected to VOUTSN. If the output ideal diode MOSFET is not used, OUTFET should be left floating.

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VCAP (Pin 21): Supercapacitor Stack Voltage and Charge Current Sense Amplifier Negative Input. Connect this pin to the top of the supercapacitor stack. The voltage at this pin is digitized and may be read in the meas_vcap register.

ICAP (Pin 22): Charge Current Sense Amplifier Positive Input. The ICAP and VCAP pins measure the voltage across the sense resistor, R_{SNSC}, to provide instantaneous current signals for the control loops and ESR measurement system. The maximum charge current is $32mV/R_{SNSC}$.

VCC2P5 (Pin 23): Internal 2.5V Regulator Output. This regulator provides power to the internal logic circuitry. Decouple this pin to GND with a minimum 1µF low ESR tantalum or ceramic capacitor.

SW (Pin 24): Switch Node Connection to the Inductor. The negative terminal of the boot-strap capacitor, C_B, is connected to this pin. The voltage on this pin is also used as the source reference for the top side N-channel MOSFET gate drive. In step-down mode, the voltage swing on this pin is from a diode (external) forward voltage below GND to V_{OUT}. In step-up mode the voltage swing is from GND to a diode forward voltage above V_{OUT}.

TGATE (Pin 25): Top Gate Driver Output. This pin is the output of a floating gate driver for the top external N-channel MOSFET. The voltage swing at this pin is GND to V_{OUT} + DRV_{CC}.

BST (Pin 26): TGATE Driver Supply Input. The positive terminal of the boot-strap capacitor, C_B, is connected to this pin. This pin swings from a diode voltage drop below DRV_{CC} up to V_{OUT} + DRV_{CC}.

BGATE (Pin 27): Bottom Gate Driver Output. This pin drives the bottom external N-channel MOSFET between GND and DRV_{CC}.

DRV_{CC} (Pin 28): Power Rail for Bottom Gate Driver. Connect to $INTV_{CC}$ through a 1Ω resistor or to an external supply. Decouple this pin to GND with a minimum 2.2µF low ESR tantalum or ceramic capacitor. Do not exceed 5.5V on this pin.

$INTV_{CC}$ (Pin 29): Internal 5V Regulator Output. The control circuits are powered from this supply. Decouple this pin to GND with a minimum 1µF low ESR tantalum or ceramic capacitor.

VOUTSN (Pin 30): Input Current Limiting Amplifier Negative Input. A sense resistor, R_{SNSI}, between VOUTSP and VOUTSN sets the input current limit. The maximum input current is $32mV/R_{SNSI}$. An RC network across the sense resistor can be used to modify loop compensation. To disable input current limit, connect this pin to VOUTSP.

VOUTSP (Pin 31): Backup System Supply Voltage and Input Current Limiting Amplifier Positive Input. The voltage across the VOUTSP and VOUTSN pins are used to regulate input current. This pin also serves as the power supply for the IC. The voltage at this pin is digitized and may be read in the meas_vout register.

VOUTM5 (Pin 32): V_{OUT} – 5V Regulator. This pin is regulated to 5V below V_{OUT} or to ground if V_{OUT} < 5V. This rail provides power to the input current sense amplifier. Decouple this pin with at least 1µF to V_{OUT}.

INFET (Pin 33): Input Ideal Diode Gate Drive Output. This pin controls the gate of an external N-channel MOSFET used as an ideal diode between V_{IN} and V_{OUT}. The gate drive receives power from an internal charge pump. The source of the N-channel MOSFET should be connected to V_{IN} and the drain should be connected to VOUTSP. If the input ideal diode MOSFET is not used, INFET should be left floating.

V_{IN} (Pin 34): External DC Power Source Input. Decouple this pin with at least 0.1µF to GND. The voltage at this pin is digitized and may be read in the meas_vin register.

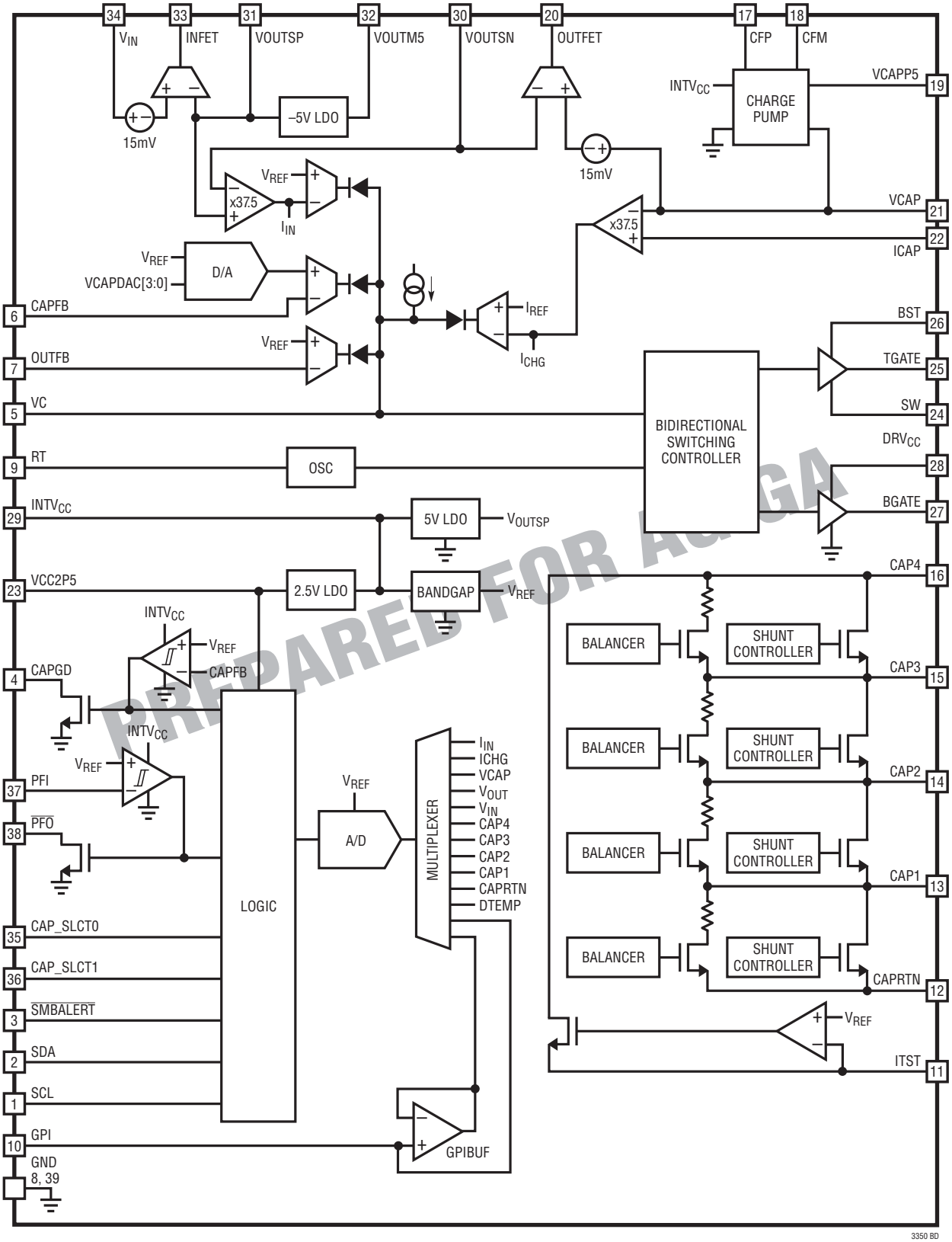
CAP_SLCT0, CAP_SLCT1 (Pins 35, 36): CAP_SLCT0 and CAP_SLCT1 set the number of super-capacitors used. Refer to Table 1.

PFI (Pin 37): Power-Fail Comparator Input. When the voltage at this pin drops below 1.185V, $\overline{PFO}$ is pulled low and step-up mode is enabled.

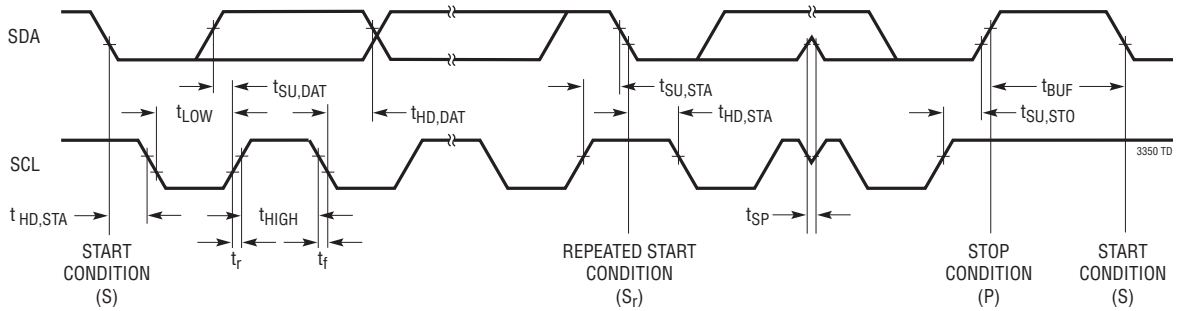
$\overline{PFO}$ (Pin 38): Power-Fail Status Output. This open-drain output is pulled low when a power fault has occurred.

PGND (Exposed Pad Pin 39): Power Ground. The exposed pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3350 and be tied to the GND pin.

BLOCK DIAGRAM



TIMING DIAGRAM



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Introduction

The LTC3350 is a highly integrated backup power controller and system monitor. It features a bidirectional switching controller, input and output ideal diodes, supercapacitor shunts/balancers, a power-fail comparator, a 14-bit ADC and I^2C/SMBus programmability and status reporting.

If V_{IN} is above an externally programmable PFI threshold voltage, the synchronous controller operates in step-down mode and charges a stack of supercapacitors. A programmable input current limit ensures that the supercapacitors will automatically be charged at the highest possible charge current that the input can support. If V_{IN} is below the PFI threshold, then the synchronous controller will run in reverse as a step-up converter to deliver power from the supercapacitor stack to V_{OUT}.

The two ideal diode controllers drive external MOSFETs to provide low loss power paths from V_{IN} and V_{CAP} to V_{OUT}. The ideal diodes work seamlessly with the bidirectional controller to provide power from the supercapacitors to V_{OUT} without backdriving V_{IN}.

The LTC3350 provides balancing and overvoltage protection to a series stack of one to four supercapacitors. The internal capacitor voltage balancers eliminate the need for external balance resistors. Overvoltage protection is provided by shunt regulators that use an internal switch and an external resistor across each supercapacitor.

The LTC3350 monitors system voltages, currents, and die temperature. A general purpose input (GPI) pin is provided to measure an additional system parameter or implement a thermistor measurement. In addition, the LTC3350 can measure the capacitance and resistance of the supercapacitor stack. This provides indication of the health of the supercapacitors and, along with the V_{CAP} voltage measurement, provides information on the total energy stored and the maximum power that can be delivered.

Bidirectional Switching Controller—Step-Down Mode

The bidirectional switching controller is designed to charge a series stack of supercapacitors (Figure 1). Charging proceeds at a constant current until the supercapacitors reach their maximum charge voltage determined by the CAPFB servo voltage and the resistor divider between V_{CAP} and CAPFB. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, used in series with the inductor. The charge current loop servos the voltage across the sense resistor to 32mV. When charging is enabled, an internal soft-start ramp will increase the charge current from zero to full current in 2ms. The V_{CAP} voltage and charge current can be read from the meas_vcap and meas_ichrg registers, respectively.

OPERATION

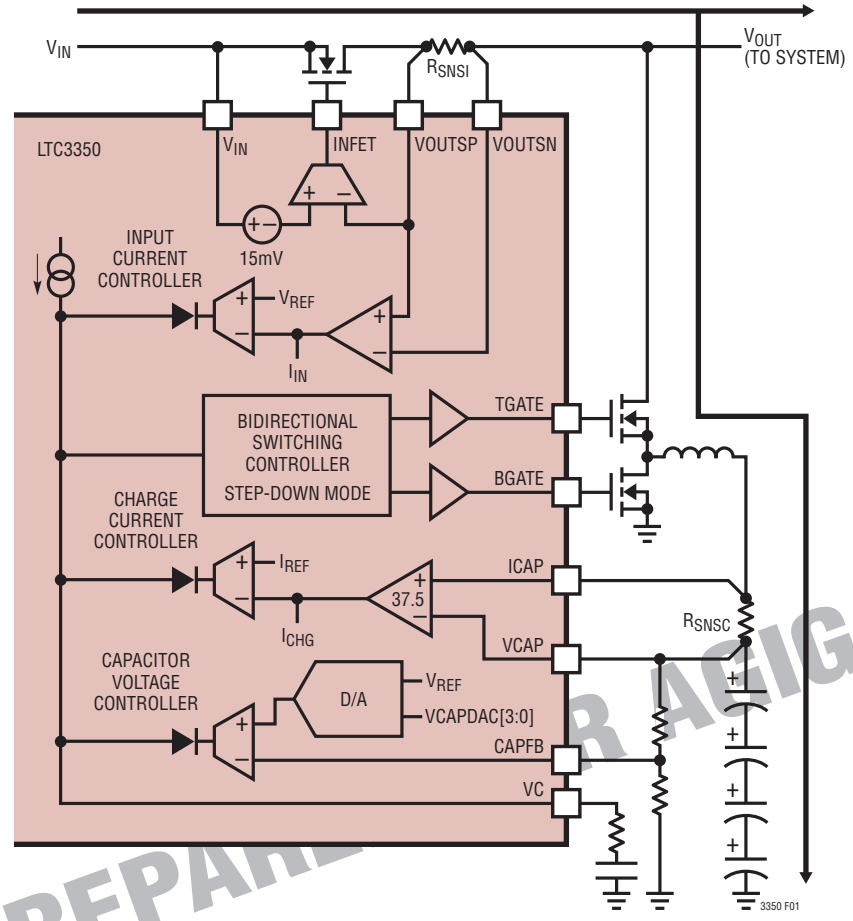

Figure 1. Power Path Block Diagram—Power Available from V_{IN}

The LTC3350 provides constant power charging (for a fixed V_{IN}) by limiting the input current drawn by the switching controller in step-down mode. The input current limit will reduce charge current to limit the voltage across the input sense resistor, R_{SNSI}, to 32mV. If the combined system load plus supercapacitor charge current is large enough to cause the switching controller to reach the programmed input current limit, the input current limit loop will reduce the charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the charge current is programmed to exceed the allowable input current, the input current will not be violated; the supercapacitor charger will reduce its current as needed. Note that the part's quiescent and gate drive currents are not included in the input current measurement.The input current can be read from the meas_iin register.

Bidirectional Switching Controller—Step-Up Mode

The bidirectional switching controller acts as a step-up converter to provide power from the supercapacitors to V_{OUT} when input power is unavailable (Figure 2). The PFI comparator enables step-up mode. V_{OUT} regulation is set by a resistor divider between V_{OUT} and OUTFB. To disable step-up mode tie OUTFB to $INTV_{CC}$.

Step-up mode can be used in conjunction with the output ideal diode. The V_{OUT} regulation can be set below the capacitor stack voltage. Upon removal of input power, power to V_{OUT} will be provided from the supercapacitor stack via the output ideal diode. When the supercapacitor voltage falls to just above the level set by the V_{OUT} resistor divider, the output ideal diode shuts off and the switching controller takes over and holds up V_{OUT} while the supercapacitors discharge to ground.

OPERATION

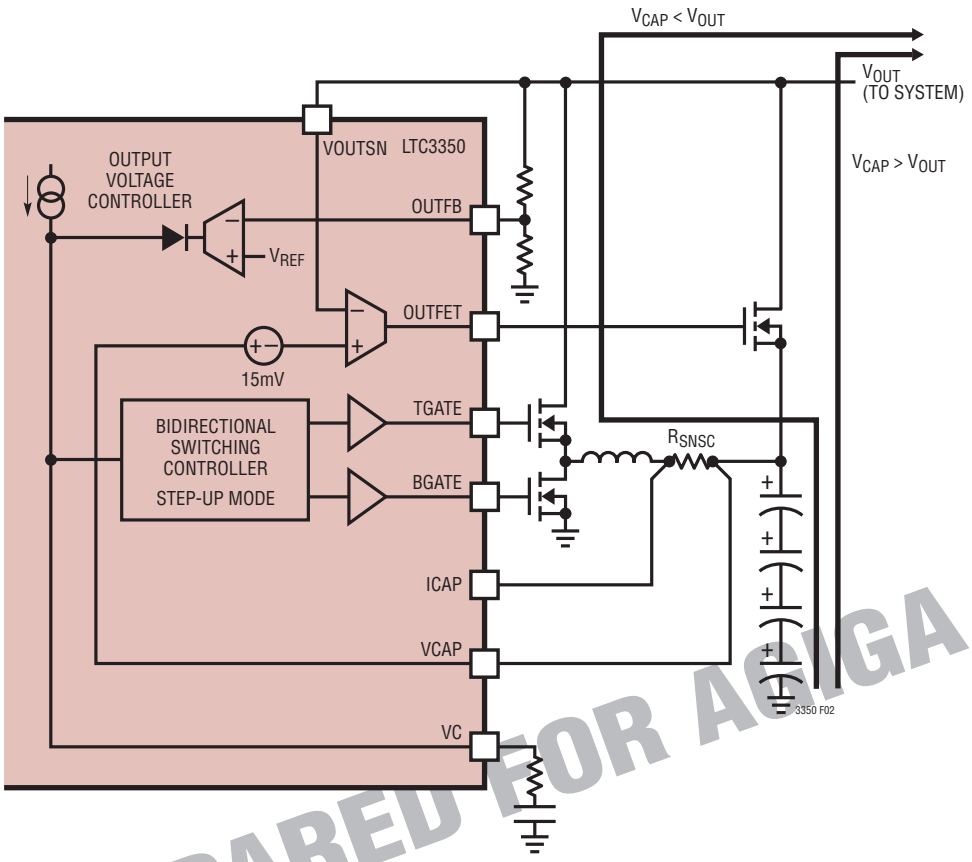

Figure 2. Power Path Block Diagram—Power Back-Up

Ideal Diodes

The LTC3350 has two ideal diode controllers that drive external N-channel MOSFETs. The ideal diodes consist of a precision amplifier that drives the gates of N-channel MOSFETs whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at V_{IN} or V_{CAP}. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFETs will be in full conduction.

The input ideal diode prevents the supercapacitors from back driving V_{IN} during backup mode. A Fast-Off comparator shuts off the N-channel MOSFET if V_{IN} falls 30mV below V_{OUT}. The PFI comparator also shuts off the MOSFET during power failure.

The output ideal diode provides a path for the supercapacitors to power V_{OUT} when V_{IN} is unavailable. In addition to a Fast-Off comparator, the output ideal diode also has a Fast-On comparator that turns on the external MOSFET when V_{OUT} drops 45mV below V_{CAP}. The output ideal diode will shut off when OUTFB is just above regulation allowing the synchronous controller to power V_{OUT} in step-up mode.

Gate Drive Supply (DRV_{CC})

The bottom gate driver is powered from the DRV_{CC} pin. It is normally connected to the $INTV_{CC}$ pin. An RC filter can be placed between the DRV_{CC} and $INTV_{CC}$ pins to provide additional filtering. An external LDO can also be used to power the gate drivers to minimize power dissipation inside the IC. See the Applications Information section for details.

Undervoltage Lockout (UVLO)

Internal undervoltage lockout circuits monitor both the $INTV_{CC}$ and DRV_{CC} pins. The switching controller is kept off until $INTV_{CC}$ rises above 4.3V and DRV_{CC} rises above

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4.2V. Hysteresis on the UVLOs turn off the controller if either $INTV_{CC}$ falls below 4V or DRV_{CC} falls below 3.9V.

Charging is not enabled until V_{IN} is 200mV above the supercapacitor voltage and above the PFI threshold. Charging is disabled when V_{IN} falls to within 50mV of the supercapacitor voltage or V_{IN} is below the PFI threshold.

RT Oscillator and Switching Frequency

The RT pin is used to program the switching frequency. A resistor, R_T, from this pin to ground sets the switching frequency according to:

$$f_{OSC}(MHz) = \frac{53.5}{R_T(k\Omega)}$$

R_T also sets the scale factor for the capacitor measurement value reported in the meas_cap register, described in the Capacitance and ESR Measurement section of this data sheet.

Input Overvoltage Protection

The LTC3350 has overvoltage protection on its input. If V_{IN} exceeds 38.6V, the switching controller will hold both switches off. The controller will resume switching if V_{IN} falls below 37.2V.

V_{CAP} DAC

The feedback reference for the CAPFB servo point can be programmed using an internal 4-bit digital-to-analog converter (DAC). The reference voltage can be programmed from 0.6375V to 1.2V in 37.5mV increments. The DAC defaults to full scale (1.2V) and is programmed via the vcapfb_dac register.

Supercapacitors lose capacitance as they age. By initially setting the V_{CAP} DAC to a low setting, the final charge voltage on the supercapacitors can be increased as they age to maintain a constant level of stored backup energy throughout the lifetime of the supercapacitors.

Power-Fail (PF) Comparator

The LTC3350 contains a fast power-fail (PF) comparator which switches the part from charging to backup mode in the event the input voltage, V_{IN}, falls below an externally programmed threshold voltage. In backup mode, the input ideal diode shuts off and the supercapacitors power the load either directly through the output ideal diode or through the synchronous controller in step-up mode.

The PF comparator threshold voltage is programmed by an external resistor divider via the PFI pin. The output of the PF comparator also drives the gate of an open-drain NMOS to report the status via the $\overline{PFO}$ pin. When input power is available the $\overline{PFO}$ pin is high impedance. When V_{IN} falls below the PF comparator threshold, $\overline{PFO}$ is pulled down to ground.

The output of the PF comparator may also be read from the chrg_pfo bit in the chrg_status register.

Charge Status Indication

The LTC3350 includes a comparator to report the status of the supercapacitors via an open-drain NMOS transistor on the CAPGD pin. This pin is pulled to ground until the CAPFB pin voltage rises to within 8% of the V_{CAP} DAC setting. Once the CAPFB pin is above this threshold, the CAPGD pin goes high impedance.

The output of this comparator may also be read from the chrg_cappg bit in the chrg_status register.

Capacitor Voltage Balancer

The LTC3350 has an integrated active stack balancer. This balancer slowly balances all of the capacitor voltages to within about 10mV of each other. This maximizes the life of the supercapacitors by keeping the voltage on each as low as possible to achieve the needed total stack voltage. When the difference between any two capacitor voltages exceeds about 10mV, the capacitor with the largest voltage is discharged with a resistive balancer at about 10mA until all capacitor voltages are within 10mV.

Capacitor Shunt Regulators

In addition to balancing, there is a need to protect each capacitor from overvoltage during charging. The capacitors in the stack will not have exactly the same capacitance due to manufacturing tolerances or uneven aging. This will cause the capacitor voltages to increase at different rates with the same charge current. If this mismatch is

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severe enough or if the capacitors are being charged to near their maximum voltage, it becomes necessary to limit the voltage increase on some capacitors while still charging the other capacitors. Up to 500mA of current may be shunted around a capacitor whose voltage is approaching the programmable shunt voltage. This shunt current reduces the charge rate of that capacitor relative to the other capacitors. If a capacitor continues to approach its shunt voltage, the charge current is reduced. This protects the capacitor from overvoltage while still charging the other capacitors, although at a reduced rate of charge. The shunt voltage is programmable in the vshunt register. Shunt voltages up to 3.6V may be programmed in 183µV increments. The shunt regulators can be disabled by programming vshunt to zero (0x0000).

I²C/SMBus and $\overline{\text{SMBALERT}}$

The LTC3350 contains an I²C/SMBus port. This port allows communication with the LTC3350 for configuration and reading back telemetry data. The port supports two SMBus formats, read word and write word. Refer to the SMBus specification for details of these formats. The registers accessible via this port are organized on an 8-bit address bus and each register is 16 bits wide. The "command code" (or sub-address) of the SMBus read/write word formats is the 8-bit address of each of these registers. The address of the LTC3350 is 0b0001001.

The $\overline{\text{SMBALERT}}$ pin is asserted (pulled low) whenever an enabled limit is exceeded or when an enabled status event happens (see Limit Check and Alarms and Monitor Status Register). The LTC3350 will deassert the $\overline{\text{SMBALERT}}$ pin only after responding to an SMBus alert response address (ARA), an SMBus protocol used to respond to a SMBALERT. The host will read from the ARA (0b0001100) and each part asserting SMBALERT will begin to respond with its address. The responding parts arbitrate in such a way that only the part with the lowest address responds. Only when a part has responded with its address does it release the SMBALERT signal. If multiple parts are asserting the SMBALERT signal then multiple reads from the ARA are needed. For more information refer to the SMBus specification.

Details on the registers accessible through this interface are available in the Register Map and Register Descriptions sections of this data sheet.

Analog-to-Digital Converter

The LTC3350 has an integrated 14-bit sigma-delta analog-to-digital converter (ADC). This converter is automatically multiplexed between all of the measured channels and its results are stored to registers accessible via the I²C/SMBus port. There are 11 channels measured by the ADC, each of which takes approximately 820µs to measure. In addition to providing status information about the system voltages and currents, some of these measurements are used by the LTC3350 to balance, protect, and measure the capacitors in the stack.

The result of the analog-to-digital conversion is stored in a 16-bit register as a signed, two's complement, number. The lower two bits of this number are sub-bits. These bits are ADC outputs which are too noisy to be reliably used on any single conversion, however, they may be included if multiple samples are averaged.

The measurements from the ADC are directly stored in the meas_vcap1, meas_vcap2, meas_vcap3, meas_vcap4, meas_gpi, meas_vin, meas_vcap, meas_vout, meas_iin, and meas_ichg registers.

Capacitance and ESR Measurement

The LTC3350 has the ability to measure the capacitance and equivalent series resistance (ESR) of its supercapacitor stack. This measurement is performed with minimal impact to the system, and can be done while the supercapacitor backup system is online. This measurement discharges the capacitors by a small amount. If input power fails during this test, the part will go into backup mode and the test will terminate.

The capacitance test is performed only once the supercapacitors have finished charging. The test temporarily disables the charger, then discharges the supercapacitors by 200mV with a precision current. The discharge time is measured and used to calculate the capacitance with the result of this measurement stored in

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the meas_cap register. The number reported is proportional to the combined capacitance of the stack. Two different scales can be set using the ctl_cap_scale bit in the ctl_reg register. If ctl_cap_scale is set to 0, use the following equation to convert the meas_cap value to Farads:

$$C_{STACK} = \frac{R_T}{R_{TST}} \bullet 330\mu F \bullet meas\_cap$$

If ctl_cap_scale is set to 1, use the following equation to convert the meas_cap value to Farads:

$$C_{STACK} = \frac{R_T}{R_{TST}} \bullet 3.3\mu F \bullet meas\_cap$$

In the two previous equations R_T is the resistor on the RT pin and R_{TST} is the resistor on the ITST pin.

The ESR test is performed immediately following the capacitance test. The switching controller is switched on and off several times. The changes in charge current and stack voltage are measured. These measurements are used to calculate the ESR relative to the charge current sense resistor. The result of this measurement is stored in the meas_esr register. The value reported in meas_esr can be converted to ohms using the following equation:

$$R_{ESR} = \frac{R_{SNSC}}{64} \bullet meas\_esr$$

where R_{SNSC} is the charge current sense resistor in series with the inductor.

The capacitance and capacitor ESR measurements do not automatically run as the other measurements do. They must be initiated by setting the ctl_strt_capesr bit in the ctl_reg register. This bit will automatically clear once the measurement begins. If the cap_esr_per register is set to a non-zero value, the meas-urement will be repeated after the time programmed in the cap_esr_per register. Each LSB in the cap_esr_per register represents one second.

The capacitance and ESR measurements may fail to complete for several reasons, in which case the respective mon_cap_failed or mon_esr_failed bit will be set. The capacitance test may fail due to a power failure or if the 200mV discharge trips the CAPGD comparator. The ESR test will also fail if the capacitance test fails. The ESR test uses the charger to supply a current and then measures the supercapacitor stack voltage with and without that current. If the ESR is greater than 1024 times R_{SNSC}, the ESR measurement will fail. If the full charge current times the ESR is unable to generate enough voltage, then the mon_esr_low_qor bit will be set. This is a warning that the measurement has completed, but the accuracy of the measurement is likely to be low. The ESR measurement is adaptive; it uses knowledge of the ESR from previous measurements to program the test current. The capacitance and ESR tests should initially be run several times when first powering up to get the most accuracy out of the system. It is possible for the first few measurements to give low quality results or fail to complete and after running several times will complete with a quality result.

Monitor Status Register

The LTC3350 has a monitor status register (mon_status) which contains status bits regarding the state of the capacitance and ESR monitoring system. These bits are set and cleared by the capacitor monitor upon certain events during a capacitor and ESR measurement, as described in the Capacitance and ESR Measurement section.

There is a corresponding msk_mon_status register. Writing a one to any of these bits will cause the $\overline{\text{SMBALERT}}$ pin to pull low when the corresponding bit in the msk_mon_status register has a rising edge. This allows reduced polling of the LTC3350 when waiting for a capacitance or ESR measurement to complete.

Details of the mon_status and msk_mon_status registers can be found in the Register Descriptions section of this data sheet.

Charge Status Register

The LTC3350 has a charger status register (chrg_status). This register contains data about the state of the charger, switcher, shunts, and balancers. Details of this register may be found in the Register Description sections of this data sheet.

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Limit Checking and Alarms

The LTC3350 has a limit checking function that will check each measured value against I²C/SMBus programmable limits. This feature is optional, and all the limits are disabled by default. The limit checking is designed to simplify system monitoring, eliminating the need to continuously poll the LTC3350 for measurement data.

If a measured parameter goes outside of the programmed level of an enabled limit, the associated bit in the alarm_reg is set high and the $\overline{\text{SMBALERT}}$ pin is pulled low. This informs the I²C/SMBus host a limit has been exceeded. The alarms register may then be read to determine exactly which programmed limits have been exceeded.

A single ADC is shared between the 11 channels with about 9ms between consecutive measurements of the same channel. It is possible, in a transient condition, for these parameters to exceed their programmed levels in between consecutive ADC measurements without setting the alarm.

Once the LTC3350 has responded to an SMBus ARA the $\overline{\text{SMBALERT}}$ pin is released. The part will not pull the pin low again until another limit is exceeded. To reset a limit that has been exceeded, it must be cleared by writing a one to the clr_alarms register.

A number of the LTC3350's registers are used for limit checking. Individual limits are enabled or disabled in the msk_alarms registers. Once an enabled alarm's measured value exceeds the programmed level for that alarm the alarm is set. That alarm may only be cleared by writing a one to the clr_alarms register. All alarms that have been set and have not yet been cleared may be read in the alarm_reg register.

All of the individual measured voltages have a corresponding undervoltage (uv) and overvoltage (ov) alarm level. All of the individual capacitor voltages are compared to the same alarm levels, set in the cap_ov_lvl and cap_uv_lvl registers. The input current measurement has an overcurrent (oc) alarm programmed in the iin_oc_lvl register. The charge current has an undercurrent alarm programmed in the ichg_uc_lvl register.

Die Temperature Sensor

The LTC3350 has an integrated die temperature sensor monitored by the ADC and digitized to the meas_dtemp register. An alarm may be set on die temperature by setting the dtemp_cold_lvl and/or dtemp_hot_lvl registers and enabling their respective alarms in the msk_alarms register. To convert the code in the meas_dtemp register to degrees Celsius use the following:

$$T_{DIE}\ (°C) = 0.028 \bullet \text{meas\_dtemp} - 251.4$$

General Purpose Input

The general purpose input (GPI) pin can be used to measure an additional system parameter. The voltage on this pin is directly digitized by the ADC. For high impedance inputs an internal buffer may be selected and used to drive the ADC. This buffer is enabled by setting the ctl_gpi_buffer_en bit in the ctl_reg register. With this buffer, the input range is limited from 0V to 3.5V. If this buffer is not used, the range is from –0.3V to 5.5V, however, the input stage of the ADC will draw about 1µA per volt from this pin. The ADC input is a switched capacitor amplifier running at about 2MHz, so this current draw will be at that frequency. This current can be eliminated at the cost of reduced range and increased offset by enabling the buffer.

Alarms are available for this pin voltage with levels programmed using the gpi_uv_lvl and gpi_ov_lvl registers. These alarms are enabled using the msk_gpi_uv and msk_gpi_ov bits in the msk_alarms register.

The GPI pin can be connected to a negative temperature coefficient (NTC) thermistor to monitor the temperature of the supercapacitor stack. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to GND if not used.

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Digital Configuration

Although the LTC3350 has extensive digital features, only a few are required for basic use. The shunt voltage should be programmed via the vshunt register if a value other than the default 2.7V is required. The capacitor voltage feedback reference defaults to 1.2V; it may be changed in the vcapfb_dac register.

All other digital features are optional and used for monitoring. The ADC automatically runs and stores conversions to registers (e.g., meas_vcap). Capacitance and ESR measurements only run if requested, however, they may be scheduled to repeat if desired (ctl_strt_capesr and cap_esr_per). Each measured parameter has programmable limits (e.g., vcap_uv_lvl and vcap_ov_lvl) which may trigger an alarm and SMBAlert when enabled. These alarms are disabled by default.

Capacitor Configuration

The LTC3350 may be used with one to four supercapacitors. If less than four capacitors are used, the capacitors must be populated from CAPRTN to CAP4, and the unused CAP pins must be tied to the highest used CAP pin. For example, if three capacitors are used, CAP4 should be tied to CAP3. If only two capacitors are used, both CAP4 and CAP3 should be tied to CAP2. The number of capacitors used must be programmed on the CAP_SLCT0 and CAP_SLCT1 pins by tying the pins to VCC2P5 for a one and GND for a zero as shown in Table 1. The value programmed on these pins may be read back from the num_caps register via I²C/SMBus.

Table 1

CAP_SLCT1	CAP_SLCT0	num_caps REGISTER VALUE	NUMBER OF CAPACITORS
0	0	0	1
0	1	1	2
1	0	2	3
1	1	3	4

Capacitor Shunt Regulator Programming

V_{SHUNT} is programmed via the I²C/SMBus interface and defaults to 2.7V at initial power-up. V_{SHUNT} serves to limit the voltage on any individual capacitor by turning on a bypass shunt around that capacitor as the voltage approaches V_{SHUNT}. CAPRTN, CAP1, CAP2, CAP3 and CAP4 must be connected to the supercapacitors through resistors which serve as ballasts for the internal shunts. The shunt current is approximately V_{SHUNT} divided by twice the shunt resistance value. For a V_{SHUNT} of 2.7V, 2.7Ω resistors should be used for 500mA of shunt current. The shunts have a duty cycle of up to 75%. The power dissipated in a single shunt resistor is approximately:

$$P_{SHUNT} \approx \frac{3V_{SHUNT}^2}{16R_{SHUNT}}$$

and the resistors should be sized accordingly.

Since the shunt current is less than what the switcher can supply, the on-chip logic will automatically reduce the charging current to allow the shunt to protect the capacitor. This greatly reduces the charge rate once any one shunt is activated. For this reason, V_{SHUNT} should be programmed as high as possible to reduce the likelihood of it activating during a charge cycle. Ideally, V_{SHUNT} would be set high enough so that any likely capacitor mismatches would not cause the shunts to turn on. This keeps the charger operating at the highest possible charge current and reduces the charge time. If the shunts never turn on, the charge cycle completes quickly and the balancers eventually equalize the voltage on the capacitors. The shunt setting may also be used to discharge the capacitors for testing, storage or other purposes.

Setting Input and Charge Currents

The maximum input current is determined by the resistance across the VOUTSP and VOUTSN pins, R_{SNSI}. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, used in series with the inductor. The input and charge current loops servo the voltage across their respective sense resistor to 32mV. Therefore, the maximum input and charge currents are:

$$I_{IN(MAX)} = \frac{32mV}{R_{SNSI}}$$

$$I_{CHG(MAX)} = \frac{32mV}{R_{SNSC}}$$

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The peak inductor current limit, I_{PEAK}, is 80% higher than the maximum charge current and is equal to:

$$I_{PEAK} = \frac{58mV}{R_{SNSC}}$$

Note that the input current limit does not include the part's quiescent and gate drive currents. The total current drawn by the part will be $I_{IN(MAX)} + I_Q + I_G$, where I_Q is the non-switching quiescent current and I_G is the gate drive current.

Low Current Charging and High Current Backup

The LTC3350 can accommodate applications requiring low charge currents and high backup currents. In these applications, program the desired charge current using R_{SNSI}. The higher current needed during backup can be set using R_{SNSC}. The input current limit will override the charge current limit when the supercapacitors are charging while the charge current limit provides sufficient current capability for backup operation.

The charge current will be limited to $I_{CHG(MAX)}$ at low V_{CAP} (i.e., low duty cycles). As V_{CAP} rises, the switching controller's input current will increase until it reaches $I_{IN(MAX)}$. The input current will be maintained at $I_{IN(MAX)}$ and the charge current will decrease as V_{CAP} rises further.

Some applications may want to use only a portion of the input current limit to charge the supercapacitors. Two input current sense resistors placed in series can be used to accomplish this as shown in Figure 3. VOUTSP is kelvin connected to the positive terminal of R_{SNSI1} and VOUTSN is kelvin connected to the negative terminal of R_{SNSI2}. The load current is pulled across R_{SNSI1} while the input current to the charger is pulled across R_{SNSI1} and R_{SNSI2}. The input current limit is:

$$32mV = R_{SNSI1} \bullet I_{LOAD} + (R_{SNSI1} + R_{SNSI2}) \bullet I_{INCHG}$$

For example, suppose that only 2A of input current is desired to charge the supercapacitors but the system load and charger combined can pull a total of 4A from the supply. Setting $R_{SNSI1} = R_{SNSI2} = 8m\Omega$ will set a 4A current limit for the load + charger while setting a 2A limit for the charger. With no system load, the charger can pull up to 2A of input current. As the load pulls 0A to 4A of current the charger's input current will reduce from 2A down to 0A. The following equation can be used to determine charging input current as a function of system load current:

$$I_{INCHG} = \frac{32mV}{R_{SNSI1}+R_{SNSI2}} - \frac{R_{SNSI1}}{R_{SNSI1}+R_{SNSI2}} \bullet I_{LOAD}$$

The contact resistance of the negative terminal of R_{SNSI1} and the positive terminal of R_{SNSI2} as well as the resistance of the trace connecting them will cause variability in the input current limit. To minimize the error, place both sense input current sense resistors close together with a large PCB pad area between them as the system load current is pulled from the trace connecting the two sense resistors.

Note that the discharge current will flow through R_{SNSI2} in backup mode. The R_{SNSI2} package should be sized to handle the power dissipation due the discharge current in backup mode.

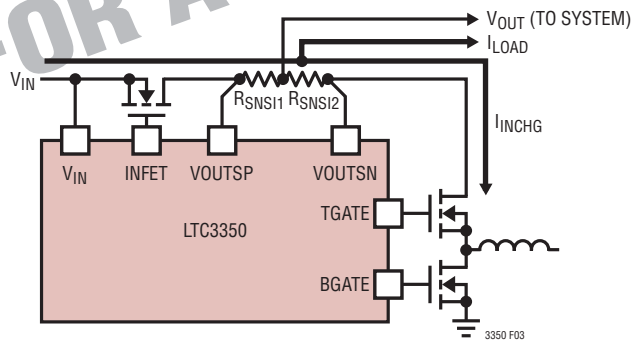

Figure 3

Setting V_{CAP} Voltage

The LTC3350 V_{CAP} voltage is set by an external feedback resistor divider, as shown in Figure 4. The regulated output voltage is determined by:

$$V_{CAP} = \left(1 + \frac{R_{FBC1}}{R_{FBC2}}\right) CAPFBREF$$

where CAPFBREF is the output of the V_{CAP} DAC, programmed in the vcapfb_dac register. Great care should be taken to route the CAPFB line away from noise sources, such as the SW line.

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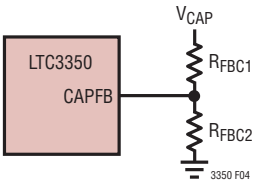

Figure 4. V_{CAP} Voltage Feedback Divider

Power-Fail Comparator Input Voltage Threshold

The input voltage threshold below which the power-fail status pin, $\overline{PFO}$, indicates a power-fail condition and the LTC3350 bidirectional controller switches to step-up mode is programmed using a resistor divider from the V_{IN} pin to GND via the PFI pin such that:

$$V_{IN} = \left(1 + \frac{R_{PF1}}{R_{PF2}}\right) V_{PFI(TH)}$$

where $V_{PFI(TH)}$ is 1.185V. Typical values for R_{PF1} and R_{PF2} are in the range of 40k to 1M. See Figure 5.

The input voltage above which the power-fail status pin $\overline{PFO}$ is high impedance and the bidirectional controller switches to step-down mode is:

$$V_{IN} = \left(1 + \frac{R_{PF1}}{R_{PF2}}\right)\left(V_{PFI(TH)} + V_{PFI(HYS)}\right)$$

where $V_{PFI(HYS)}$ is the hysteresis of the PFI comparator and is equal to 30mV.

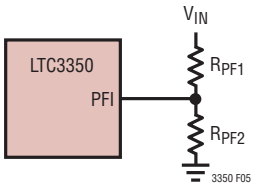

Figure 5. PFI Threshold Voltage Divider

Setting V_{OUT} Voltage in Backup Mode

The output voltage for the controller in step-up mode is set by an external feedback resistor divider, as shown in Figure 6. The regulated output voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R_{FBO1}}{R_{FBO2}}\right) 1.2V$$

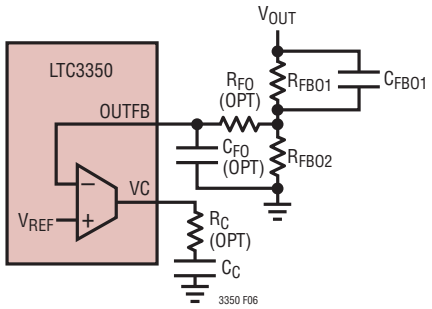

Figure 6. V_{OUT} Voltage Divider and Compensation Network

Great care should be taken to route the OUTFB line away from noise sources, such as the SW line.

Minimum V_{CAP} Voltage in Backup Mode

In backup mode, power is provided to the output from the supercapacitors either through the output ideal diode or the synchronous controller operating in step-up mode.

The output ideal diode provides a low loss power path from the supercapacitors to V_{OUT}. The minimum supercapacitor voltage will be equal to the minimum V_{OUT} necessary for the system to operate plus the voltage drops from the output ideal diode and supercapacitor ESR.

Example: System needs 5V to run and draws 1A during backup. There are four supercapacitors in the stack, each with an ESR of 45mΩ. The output ideal diode forward regulation voltage is 15mV (OUTFET $R_{DS(ON)}$ < 15mΩ). The minimum supercapacitor voltage is:

$$V_{CAP(MIN)} = 5V + 0.015V + (1A \bullet 4.45m\Omega) = 5.195V$$

Using the synchronous controller in step-up mode allows the supercapacitors to be discharged to a voltage much lower than the minimum V_{OUT} needed to run the system. The amount of power that the supercapacitor stack can deliver at its minimum voltage should be greater than what is needed to power the output and the step-up converter:

$$P_{CAP(MIN)} = \frac{V_{CAP(MIN)}^2}{4 \bullet \eta \bullet R_{SC}} > \frac{P_{BACKUP}}{\eta}$$

In the equation above η is the efficiency of the synchronous controller in step-up mode and η is the number of supercapacitors in the stack.

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Example: System needs 5V to run and draws 1A during backup. There are four supercapacitors in the stack, each with an ESR of 45mΩ. The converter efficiency is 90%. The minimum supercapacitor voltage is:

$$V_{CAP(MIN)} = \sqrt{\frac{4 \bullet 45m\Omega \bullet 5V \bullet 1A}{0.9}} = 2.0V$$

Note the minimum V_{CAP} voltage can also be limited by the peak inductor current limit (180% of maximum charge current) and the maximum duty cycle in step-up mode (~90%).

Optimizing Supercapacitor Energy Storage Capacity

In most systems the supercapacitors will provide backup power to one or more DC/DC converters. A DC/DC converter presents a constant power load to the supercapacitor. When the supercapacitors are near their maximum voltage, the loads will draw little current. As the capacitors discharge, the current drawn from supercapacitors will increase to maintain constant power to the load. The amount of energy required in back up mode is the product of this constant backup power, P_{BACKUP}, and the backup time, t_{BACKUP}.

The energy stored in a stack of n supercapacitors available for back up is:

$$\frac{1}{2} nC_{SC}\left(V^2_{CELL(MAX)} - V^2_{CELL(MIN)}\right)$$

where C_{SC}, $V_{CELL(MAX)}$ and $V_{CELL(MIN)}$ are the capacitance, maximum voltage and minimum voltage of a single capacitor in the stack, respectively. The maximum voltage on the stack is $V_{CAP(MAX)} = n \bullet V_{CELL(MAX)}$. The minimum voltage on the stack is $V_{CAP(MIN)} = n \bullet V_{CELL(MIN)}$.

Some of this energy will be dissipated as conduction loss in the ESR of the supercapacitor stack. A higher backup power requirement leads to a higher conduction loss for a given stack ESR.

The amount of capacitance needed can be found by solving the following equation for C_{SC}:

$$P_{BACKUP} \bullet t_{BACKUP} = \frac{1}{4} nC_{SC}\left[\gamma_{MAX} \bullet V^2_{CELL(MAX)} - \gamma_{MIN} \bullet V^2_{CELL(MIN)} - \frac{4R_{SC} \bullet P_{BACKUP}}{n} \ln\left(\frac{\gamma_{MAX} \bullet V_{CELL(MAX}}{\gamma_{MIN} \bullet V_{CELL(MIN)}}\right)\right]$$

where:

$$\gamma_{MAX} = 1 + \sqrt{1 - \frac{4R_{SC} \bullet P_{BACKUP}}{nV^2_{CELL(MAX)}}} \text{ and,}$$

$$\gamma_{Min} = 1 + \sqrt{1 - \frac{4R_{SC} \bullet P_{BACKUP}}{nV^2_{CELL(MIN)}}}$$

R_{SC} is the equivalent series resistance (ESR) of a single supercapacitor in the stack. Note that the maximum power transfer rule limits the minimum cell voltage to:

$$V_{CELL(MIN)} = \frac{V_{CAP(MIN)}}{n} \geq \sqrt{\frac{4R_{SC} \bullet P_{BACKUP}}{n}}$$

To minimize the size of the capacitance for a given amount of backup energy, the maximum voltage on the stack, $V_{CELL(MAX)}$, can be increased. However, the voltage is limited to a maximum of 2.7V and this may lead to an unacceptably low capacitor lifetime.

An alternative option would be to keep $V_{CELL(MAX)}$ at a voltage that leads to reasonably long lifetime and increase the capacitor utilization ratio of the supercapacitor stack. The capacitor utilization ratio, α_B, can be defined as:

$$\alpha_B = \frac{V^2_{CELL(MAX)} - V^2_{CELL(MIN)}}{V^2_{CELL(MAX)}}$$

If the boost converter is used then the supercapacitors can be run down to a voltage set by the maximum power transfer rule to maximize the utilization ratio. The minimum voltage is this case is:

$$V_{CELL(MIN)} = \sqrt{\frac{4R_{SC} \bullet P_{BACKUP}}{n\eta}}$$

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where η is the efficiency of the boost converter (~90% to 96%). In that case the energy needed for backup is governed by the following equation:

$$\frac{P_{BACKUP}}{\eta} t_{BACKUP} \leq \frac{1}{2} nC_{SC} \bullet V_{CELL(MAX)}^2 \bullet \left[\frac{\alpha_B + \sqrt{\alpha_B}}{2} - \frac{1-\alpha_B}{2} \ln\left(\frac{1+\sqrt{\alpha_B}}{\sqrt{1-\alpha_B}} \right) \right]$$

Once a capacitance is found using the above equation the maximum ESR allowed needs to be checked:

$$R_{SC} \leq \frac{\eta(1-\alpha_B) nV_{CELL(MAX)}^2}{4P_{BACKUP}}$$

Capacitor Selection Procedure:

1. Determine backup requirements P_{BACKUP} and t_{BACKUP}.
2. Determine maximum cell voltage that provides acceptable capacitor lifetime.
3. Choose number of capacitors in the stack.
4. Choose a desired utilization ratio, α_B, for the supercapacitor (e.g., 80%)
5. Solve for capacitance, C_{SC}:

$$C_{SC} \geq \frac{2P_{BACKUP} \bullet t_{BACKUP}}{n\eta V_{CELL(MAX)}^2} \bullet \left[\frac{\alpha_B + \sqrt{\alpha_B}}{2} - \frac{1-\alpha_B}{2} \ln\left(\frac{\left(1+\sqrt{\alpha_B}\right)}{\sqrt{1-\alpha_B}} \right) \right]^{-1}$$

6. Find supercapacitor with sufficient capacitance C_{SC} and minimum R_{SC}:

$$R_{SC} \leq \frac{\eta(1-\alpha_B) nV_{CELL(MAX)}^2}{4P_{BACKUP}}$$

7. If a suitable capacitor is not available, iterate by choosing more capacitance, a higher cell voltage, more capacitors in the stack and/or a lower utilization ratio.
8. Make sure to account for lifetime degradation of ESR and capacitance.

Compensation

The input current, charge current, V_{CAP} voltage, and V_{OUT} voltage loops all require a 1.2nF to 10nF capacitor from the VC node to ground.

In addition to the VC node capacitor, the V_{OUT} voltage loop requires a phase-lead capacitor, C_{FBO1}, for stability and improved transient response during input power failure (Figure 6). The product of the top divider resistor and the phase-lead capacitor should be used to create a 2kHz zero:

$$R_{FBO1} \bullet C_{FBO1} = \frac{1}{2\pi(2kHz)}$$

Choose an R_{FBO1} such that C_{FBO1} is > 100pF to minimize the effects of parasitic pin capacitance. Because the phase-lead capacitor introduces a larger ripple at the input of the V_{OUT} transconductance amplifier, an additional RC lowpass filter from the V_{OUT} divider to the OUTFB pin may be needed to eliminate voltage ripple spikes. The filter time constant should be located at the switching frequency of the synchronous controller:

$$R_{FO} \bullet C_{FO} = \frac{1}{2\pi f_{SW}}$$

with C_{FO} > 10pF to minimize the effects of parasitic pin capacitance. For back up applications where the V_{OUT} regulation voltage is low (~5V to 6V), an additional 1k to 3k resistor, R_C, in series with the VC capacitor can improve stability.

Inductor Selection

The operating frequency and inductor selection are interrelated. Higher operating frequencies allow the use of smaller inductor and capacitor values, but generally results in lower efficiency due to MOSFET switching and gate charge losses. In addition, the effect of inductor value on ripple current must also be considered. The inductor ripple current decreases with higher inductance or higher frequency and increases with higher V_{IN}. Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

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For the LTC3350, the best overall performance will be attained if the inductor is chosen to be:

$$L = \frac{V_{IN(MAX)}}{I_{CHG(MAX)} \bullet f_{SW}}$$

for $V_{IN(MAX)} \leq 2V_{CAP}$ and:

$$L = \left(1 - \frac{V_{CAP}}{V_{IN(MAX)}}\right) \frac{V_{CAP}}{0.25 \bullet I_{CHG(MAX)} \bullet f_{SW}}$$

for $V_{IN(MAX)} \geq 2V_{CAP}$, where V_{CAP} is the final supercapacitor stack voltage, $V_{IN(MAX)}$ is the maximum input voltage, $I_{CHG(MAX)}$ is the maximum regulated charge current, and f_{SW} is the switching frequency. Using these equations, the inductor ripple will be at most 25% of $I_{CHG(MAX)}$.

Using the above equation, the inductor may be too large to provide a fast enough transient response to hold up V_{OUT} when input power goes away. This occurs in cases where the maximum V_{IN} can be high (e.g. 35V) and the backup voltage low (e.g. 5V). In these situations it would be best to choose an inductor that is smaller resulting in maximum peak-to-peak ripple as high as 40% of $I_{CHG(MAX)}$.

Once the value for L is known, the type of inductor core must be selected. Ferrite cores are recommended for their very low core loss. Selection criteria should concentrate on minimizing copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This causes an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate! The saturation current for the inductor should be at least 80% higher than the maximum regulated current, $I_{CHG(MAX)}$.

C_{OUT} and C_{CAP} Capacitance

V_{OUT} serves as the input to the synchronous controller in step-down mode and as the output in step-up (backup) mode. If backup mode is used, place 100µF of bulk (aluminum electrolytic, OS-CON, POSCAP) capacitance for every 2A of backup current desired. In addition, a certain amount of high frequency bypass capacitance is needed to minimize voltage ripple. The voltage ripple in backup mode is:

$$\Delta V_{OUT} = \left[\left(1 - \frac{V_{CAP}}{V_{OUT}}\right) \frac{1}{C_{OUT} \bullet f_{SW}} + \frac{V_{OUT}}{V_{CAP}} \bullet R_{ESR}\right] I_{OUT(BACKUP)}$$

Maximum ripple occurs at the lowest V_{CAP} that can supply $I_{OUT(BACKUP)}$. Multilayer ceramics are recommended for high frequency filtering.

If backup mode is unused, then the specification for C_{OUT} will be determined by the desired ripple voltage in step down mode:

$$\Delta V_{OUT} = \frac{V_{CAP}}{V_{OUT}} \left(1 - \frac{V_{CAP}}{V_{OUT}}\right) \frac{I_{CHG(MAX)}}{C_{OUT} \bullet f_{SW}} + I_{CHG(MAX)} \bullet R_{ESR}$$

In continuous conduction mode, the source current of the top MOSFET is a square wave of duty cycle V_{CAP}/V_{OUT}. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{CHG(MAX)} \frac{V_{CAP}}{V_{OUT}} \sqrt{\frac{V_{CAP}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{OUT} = 2V_{CAP}$, where $I_{RMS} = I_{CHG(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON, and switcher-rated electrolytic capacitors can be used as input capacitors. Sanyo OS-CON SVP, SVPD series, Sanyo POSCAP TQC series, or aluminum electrolytic capacitors from Panasonic WA series or Cornel Dublilier SPV series in parallel with a couple of high performance ceramic capacitors can be used as an effective means of achieving low ESR and high bulk capacitance.

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V_{CAP} serves as the input to the controller in step-up mode and as the output in step-down mode. The purpose of the V_{CAP} capacitor is to filter the inductor current ripple. The V_{CAP} ripple (ΔV_{CAP}) is approximated by:

$$\Delta V_{CAP} \approx \Delta I_{PP}\left(\frac{1}{8C_{CAP} \bullet f_{SW}} + R_{ESR}\right)$$

where f_{SW} is the operating frequency, C_{CAP} is the capacitance on V_{CAP} and ΔI_{PP} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{PP} increases with input voltage.

Because supercapacitors have low series resistance, it is important that C_{CAP} be sized properly so that the bulk of the inductor current ripple flows through the filter capacitor and not the supercapacitor. It is recommended that:

$$\left(\frac{I_{CHG(MAX)}}{8C_{CAP} \bullet f_{SW}} + R_{ESR}\right) \leq \frac{\eta \bullet R_{SC}}{5}$$

where η is the number of supercapacitors in the stack and R_{SC} is the ESR of each supercapacitor. The capacitance on VCAP can be a combination of bulk and high frequency capacitors. Aluminum electrolytic, OS-CON and POSCAP capacitors are suitable for bulk capacitance while multilayer ceramics are recommended for high frequency filtering.

Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC3350's synchronous controller: one N-channel MOSFET for the top switch and one N-channel MOSFET for the bottom switch. The selection criteria of the external N-channel power MOSFETs include maximum drain-source voltage (V_{DSS}), threshold voltage, on-resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), total gate charge (Q_G), and maximum continuous drain current.

V_{DSS} of both MOSFETs should be selected to be higher than the maximum input supply voltage (including transient). The peak-to-peak drive levels are set by the DRV_{CC} voltage. Logic-level threshold MOSFETs should be used because DRV_{CC} is powered from either $INTV_{CC}$ (5V) or an external LDO whose output voltage must be less than 5.5V.

MOSFET power losses are determined by $R_{DS(ON)}$, C_{RSS} and Q_G. The conduction loss at maximum charge current for the top and bottom MOSFET switches are:

$$P_{COND(TOP)} = \frac{V_{CAP}}{V_{OUT}} I_{CHG(MAX)}{}^2 \bullet R_{DS(ON)}(1+\delta\Delta T)$$

$$P_{COND(BOT)} = \left(1-\frac{V_{CAP}}{V_{OUT}}\right) I_{CHG(MAX)}{}^2 \bullet R_{DS(ON)}(1+\delta\Delta T)$$

The term $(1+\delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

Both MOSFET switches have conduction loss. However, transition loss occurs only in the top MOSFET in step-down mode and only in the bottom MOSFET in step-up mode. These losses are proportional to $V_{OUT}{}^2$ and can be considerably large in high voltage applications (V_{OUT} > 20V). The maximum transition is:

$$P_{TRAN} \approx \frac{k}{2} V_{OUT}{}^2 \bullet I_{CHG(MAX)} \bullet C_{RSS} \bullet f_{SW}$$

where k is related to the drive current during the Miller plateau and is approximately equal to one.

The synchronous controller can operate in both step-down and step-up mode with different voltages on V_{OUT} in each mode. If V_{OUT} is 12V in step-down mode (input power available) and 10V in step-up mode (backup mode) then both MOSFETs can be sized to minimize conduction loss. If V_{OUT} can be as high as 35V while charging and V_{OUT} is held to 5V in backup mode, then the MOSFETs should be sized to minimize losses during backup mode. This may lead to choosing a high side MOSFET with significant transition loss which may be tolerable when input power is available so long as thermal issues do not become a limiting factor. The bottom MOSFET can be chosen to minimize conduction loss. If step-up mode is unused, then choosing a high side MOSFET that that has a higher $R_{DS(ON)}$ device and lower C_{RSS} would minimize overall losses.

Another power loss related to switching MOSFET selection is the power lost to driving the gates. The total gate charge, Q_G, must be charged and discharged each switching cycle.

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The power is lost to the internal LDO and gate drivers within the LTC3350. The power lost due to charging the gates is:

$$P_G \approx (Q_{GTOP} + Q_{GBOT}) \bullet f_{SW} \bullet V_{OUT}$$

where Q_{GTOP} is the top MOSFET gate charge and Q_{GBOT} is the bottom MOSFET gate charge. Whenever possible, utilize MOSFET switches that minimize the total gate charge to limit the internal power dissipation of the LTC3350.

Schottky Diode Selection

Optional Schottky diodes can be placed in parallel with the top and bottom MOSFET switches. These diodes clamp SW during the non-overlap times between conduction of the top and bottom MOSFET switches. This prevents the body diodes of the MOSFET switches from turning on, storing charge during the non-overlap time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. One or both diodes can be omitted if the efficiency loss can be tolerated. The diode can be rated for about one-third to one-fifth of the full load current since it is on for only a fraction of the duty cycle. Larger diodes result in additional switching losses due to their larger junction capacitance. In order for the diodes to be effective, the inductance between them and the top and bottom MOSFETs must be as small as possible. This mandates that these components be placed next to each other on the same layer of the PC board.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BST pin supplies the gate drive voltage for the top MOSFET. Capacitor C_B, in Figure 7, is charged though external diode, D_B, from DRV_{CC} when the SW pin is low. The value of the bootstrap capacitor, C_B, needs to be 20 times that of the total input capacitance of the top MOSFET.

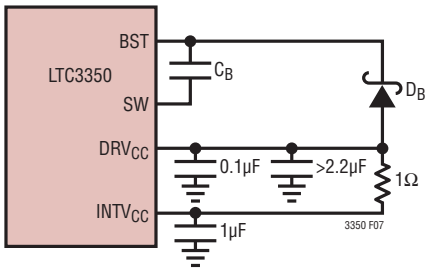


Figure 7. Bootstrap Capacitor/Diode and DRV_{CC} Connections

With the top MOSFET on, the BST voltage is above the system supply rail:

$$V_{BST} = V_{OUT} + V_{DRVCC}$$

The reverse break down of the external Schottky diode, D_B, must be greater than $V_{OUT(MAX)} + V_{DRVCC(MAX)}$.

$INTV_{CC}/DRV_{CC}$ and IC Power Dissipation

The LTC3350 features a low dropout linear regulator (LDO) that supplies power to $INTV_{CC}$ from the V_{OUT} supply. $INTV_{CC}$ powers the gate drivers (when connected to DRV_{CC}) and much of the LTC3350's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5V. The LDO can supply a maximum current of 50mA and must be bypassed to GND with a minimum of 1µF. It should be connected to DRV_{CC} through a 1Ω resistor, as shown in Figure 6. DRV_{CC} should have at least a 2.2µF ceramic or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used on DRV_{CC}, an additional 0.1µF ceramic capacitor placed directly adjacent to the DRV_{CC} pin and GND is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3350 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, is supplied by the 5V LDO.

Power dissipation for the IC in this case is highest and is approximately equal to $(V_{OUT}) \bullet (I_Q + I_G)$, where I_Q is the non-switching quiescent current of ~4mA and I_G is gate charge current. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the I_G supplied by the $INTV_{CC}$ LDO is limited to less than 42mA from a 35V supply in the QFN package at a 70°C ambient temperature:

$$T_J = 70°C + (35V)(4mA + 42mA)(34°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the $INTV_{CC}$ LDO current must be checked while operating in continuous conduction mode at maximum V_{OUT}.

APPLICATIONS INFORMATION

The power dissipation in the IC is drastically reduced if DRV_{CC} is powered from an external LDO. In this case the power dissipation in the IC is equal to power dissipation due to I_Q and the power dissipated in the gate drivers, $(V_{DRVCC}) \bullet (I_G)$. Assuming the external DRV_{CC} LDO output is 5V and is supplying 42mA to the gate drivers, the junction temperature rises to only 82°C:

$T_J = 70°C + [(35V)(4mA)+(5V)(42mA)](34°C/W) = 82°C$

The external LDO should be powered from V_{OUT} and its output must be less than 5.5V. $INTV_{CC}$ should no longer be tied to DRV_{CC} through a 1Ω resistor.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3350 is capable of turning on the top MOSFET in step-down mode. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. The minimum on-time for the LTC3350 is approximately 80ns. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{CAP}}{V_{OUT} \bullet f_{SW}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The charge current and V_{CAP} voltage will continue to be regulated, but the ripple voltage and current will increase.

Ideal Diode MOSFET Selection

An external N-channel MOSFET is required for the input and output ideal diodes. Important parameters for the selection of these MOSFETs are the maximum drain-source voltage, V_{DSS}, gate threshold voltage and on-resistance ($R_{DS(ON)}$).

When the input is grounded, the supercapacitor stack voltage is applied across the input ideal diode MOSFET. When the supercapacitors are at 0V, the input voltage is applied across the output ideal diode MOSFET. Therefore, the V_{DSS} of the input ideal diode MOSFET must withstand the maximum voltage on V_{CAP} while the V_{DSS} of output ideal diode MOSFET must withstand the highest voltage on V_{IN}.

The gate drive for both ideal diodes is 5V. This allows the use of logic-level threshold N-channel MOSFETs.

As a general rule, select MOSFETs with a low enough $R_{DS(ON)}$ to obtain the desired V_{DS} while operating at full load current. The LTC3350 will regulate the forward voltage drop across the input and output ideal diode MOSFETs to 15mV if $R_{DS(ON)}$ is low enough. The required $R_{DS(ON)}$ can be calculated by dividing 0.015V by the load current in amps.

Achieving forward regulation will minimize power loss and heat dissipation, but it is not a necessity. If a forward voltage drop of more than 15mV is acceptable, then a smaller MOSFET can be used but must be sized compatible with the higher power dissipation. Care should be taken to ensure that the power dissipated is never allowed to rise above the manufacturer's recommended maximum level.

PCB Layout Considerations

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the IC. Check the following in your layout:

1. Keep M1, M2, D1, D2 and C_{OUT} close together. The high di/dt loop formed by the MOSFETs, Schottky diodes and the V_{OUT} capacitance, shown in Figure 8, should have short, wide traces to minimize high frequency noise and voltage stress from inductive ringing. Surface mount components are preferred to reduce parasitic inductances from component leads. Connect the drain of the top MOSFET and cathode of the top diode directly to the positive terminal of C_{OUT}. Connect the source of the bottom MOSFET and anode of the bottom diode directly to the negative terminal of C_{OUT}. This capacitor provides the AC current to the MOSFETs.
2. GND is referenced to the negative terminal of the V_{CAP} decoupling capacitor in step-down mode and to the negative terminal of the V_{OUT} decoupling capacitor in step-up mode. The negative terminal of C_{OUT} should be as close as possible to the negative terminal of C_{CAP} by placing the capacitors next to each other and away from the switching loop described above. The combined IC GND pin/paddle and the ground returns of C_{INTVCC} and C_{DRVCC} must return to the combined negative terminal of C_{OUT} and C_{CAP}.

APPLICATIONS INFORMATION

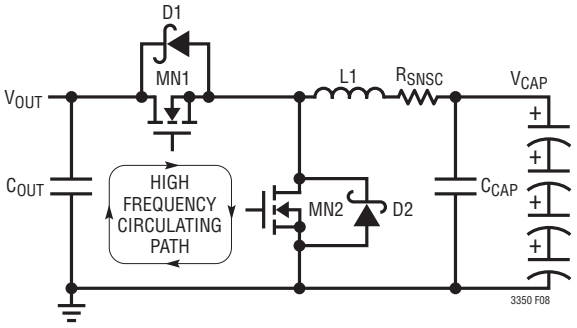


Figure 8. High Speed Switching Path

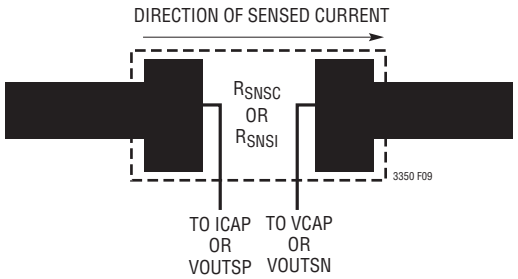


Figure 9. Kelvin Current Sensing

3. Effective grounding techniques are critical for successful DC/DC converter layouts. Orient power components such that switching current paths in the ground plane do not cross through the GND pin and exposed pad on the backside of the LTC3350 IC. Switching path currents can be controlled by orienting the MOSFET switches, Schottky diodes, the inductor, and V_{OUT} and V_{CAP} decoupling capacitors in close proximity to each other.

4. Locate V_{CAP} and V_{OUT} dividers near the part and away from switching components. Kelvin the top of resistor dividers to the positive terminals of C_{CAP} and C_{OUT}, respectively. The bottom of the resistive dividers should go back to the GND pin. The feedback resistor connections should not be along the high current feeds from the C_{OUT} capacitor.

5. Route ICAP and VCAP sense lines together, keep them short. Same with VOUTSP and VOUTSN. Filter components should be placed near the part and not near sense resistor. Ensure accurate current sensing with Kelvin connections at the sense resistors. See Figure 9.

6. The trace from the positive terminal of the input current sense resistor, R_{SNSI}, to the VOUTSP pin carries the part's quiescent and gate drive currents. To maintain accurate measurement of the input current keep this trace short by placing R_{SNSI} near the part.

7. Locate the DRV_{CC} and BST decoupling capacitors in close proximity to the IC. These capacitors carry the MOSFET drivers' high peak currents. An additional 0.1µF ceramic capacitor placed immediately next to the DRV_{CC} pin can help improve noise performance substantially.

8. Locate the small-signal components away from high frequency switching nodes (BST, SW, TG, and BG). All of these nodes have very large and fast moving signals and should be kept on the output side of the LTC3350.

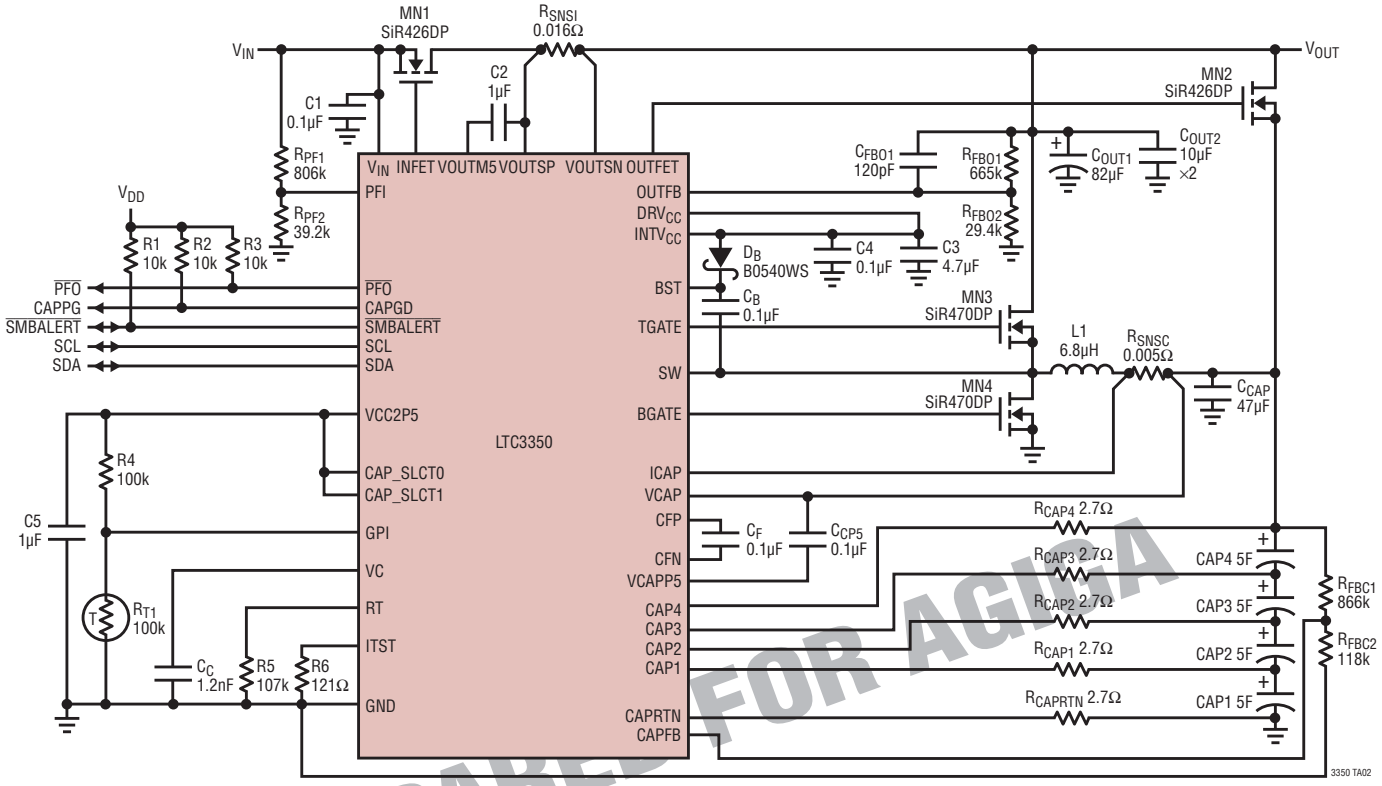
9. The input ideal diode senses the voltage between V_{IN} and VOUTSP. V_{IN} should be connected near the source of the input ideal diode MOSFET. VOUTSP is used for Kelvin sensing the input current. Place the input current sense resistor, R_{SNSI}, near the input ideal diode MOSFET with a short, wide trace to minimize resistance between the drain of the ideal diode MOSFET and R_{SNSI}.

10. The output ideal diode senses the voltage between VOUTSN and VCAP. VCAP is used for Kelvin sensing the charge current. Place the output ideal diode near the charge current sense resistor, R_{SNSC}, with a short, wide trace to minimize resistance between the source of the ideal diode MOSFET and R_{SNSC}.

11. The INFET and OUTFET pins for the external ideal diode controllers have extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from these pins will introduce an additional offset to the ideal diodes of approximately 10mV. To minimize leakage, the INFET trace can be guarded on the PC board by surrounding it with VOUT connected metal. Similarly, the OUTFET trace should be guarded by surrounding it with VCAP connected metal.

TYPICAL APPLICATIONS

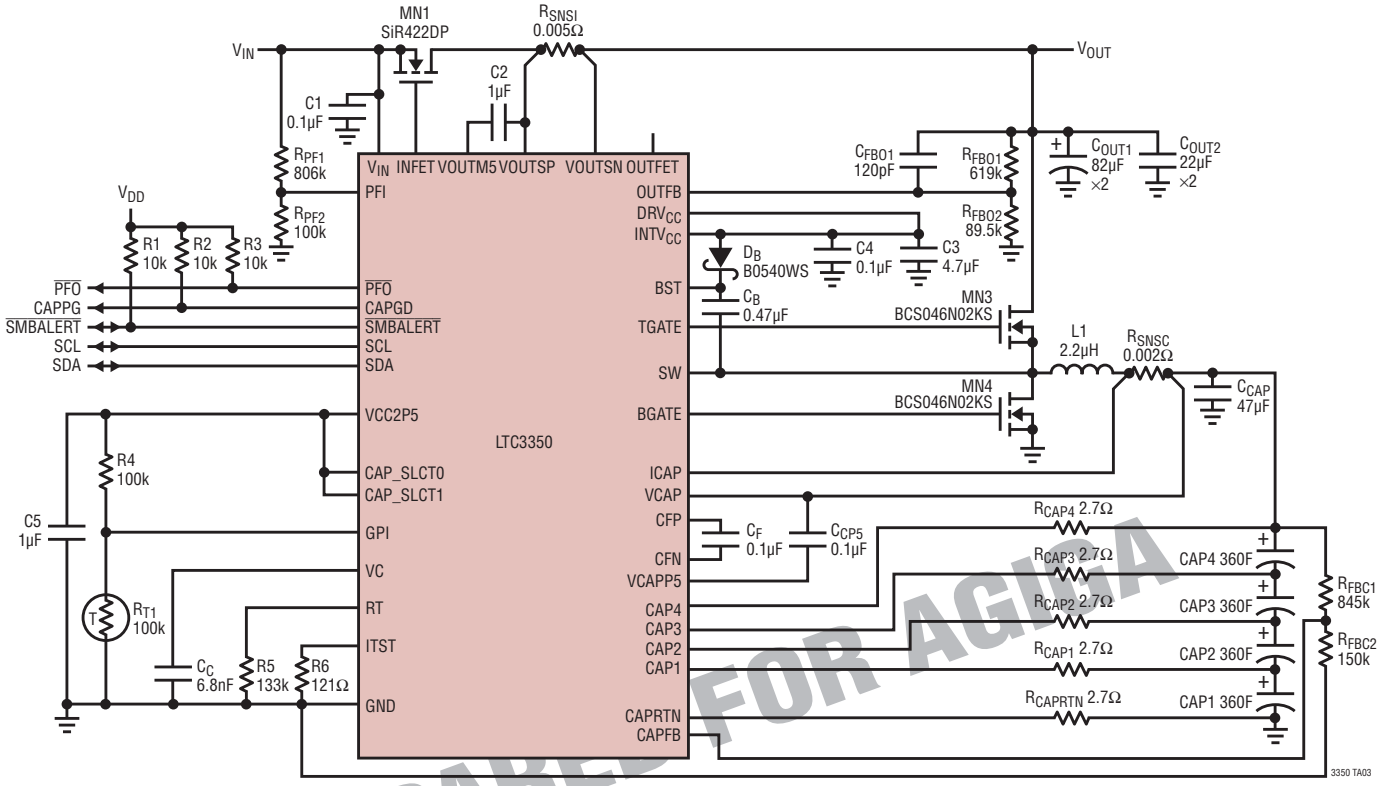
28V, 6.4A Supercapacitor Charger with 2A Input Current Limit and 28V, 50W Backup Mode



CAP1-4: NESSCAP ESHSR-0005C0-002R7

TYPICAL APPLICATIONS

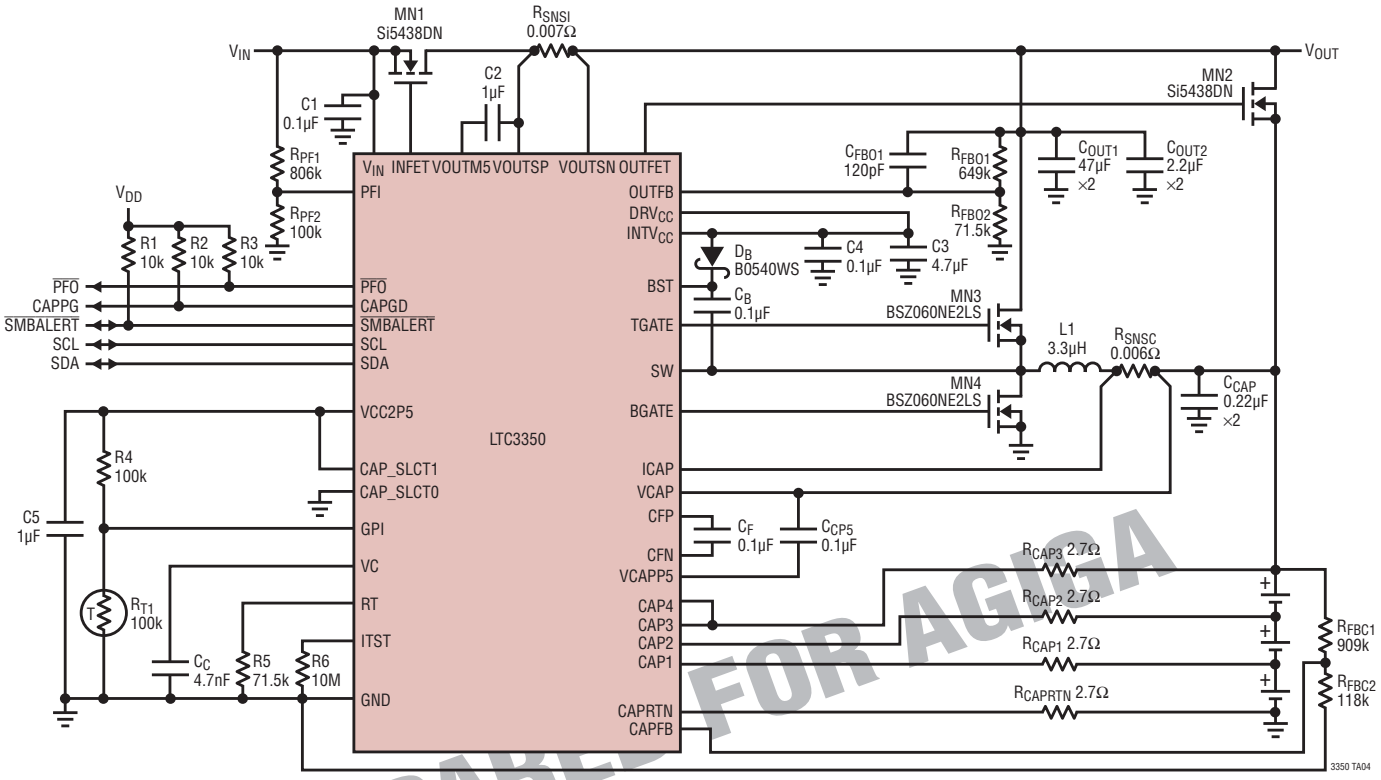
12V, 16A Supercapacitor Charger with 6.4A Input Current Limit and 10V, 60W Backup Mode



CAP1-4: NESSCAP FSHSR-0360CO-002R7

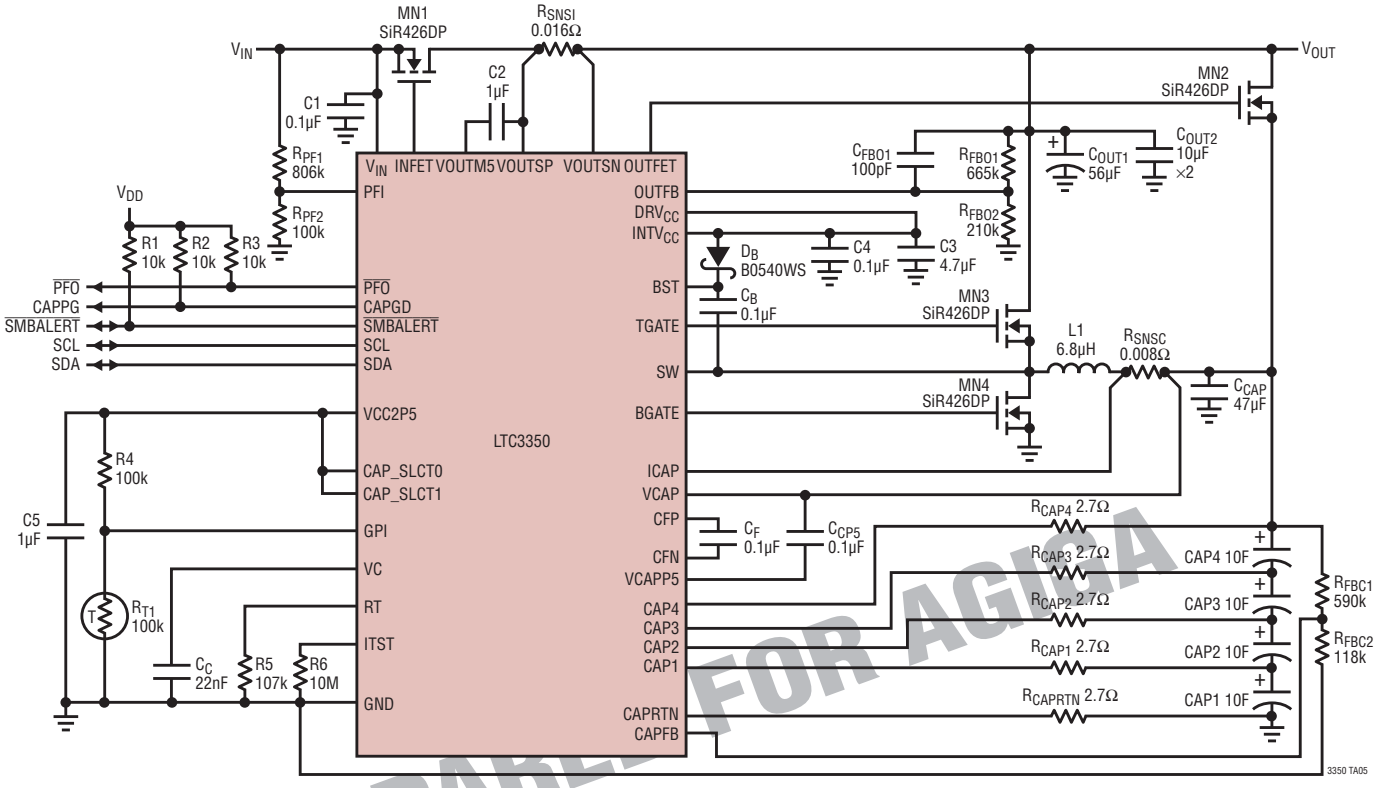
TYPICAL APPLICATIONS

12V, 5A LiFePo Battery Charger with 4.6A Input Current Limit and 12V, 48W Backup Mode



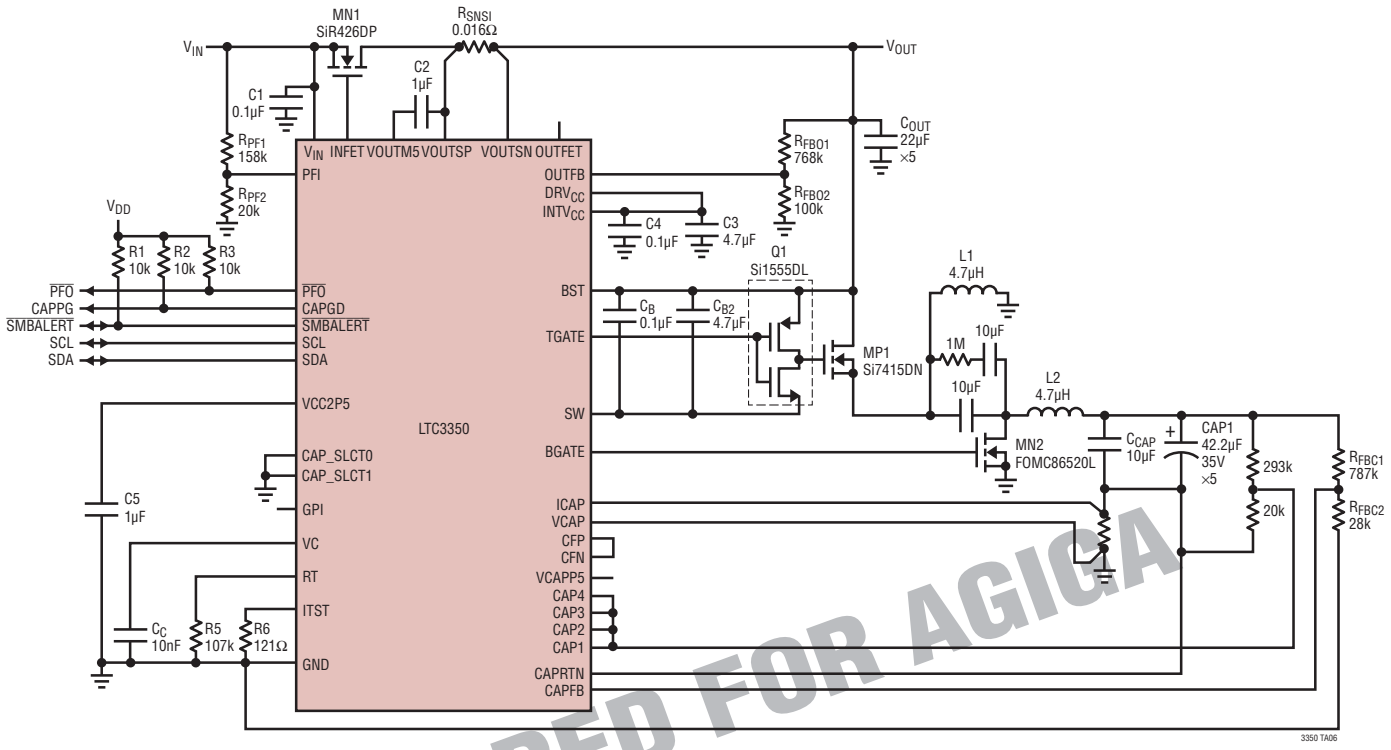
TYPICAL APPLICATIONS

35V, 4A Supercapacitor Charger with 2A Input Current Limit and 5V, 1A Backup Mode



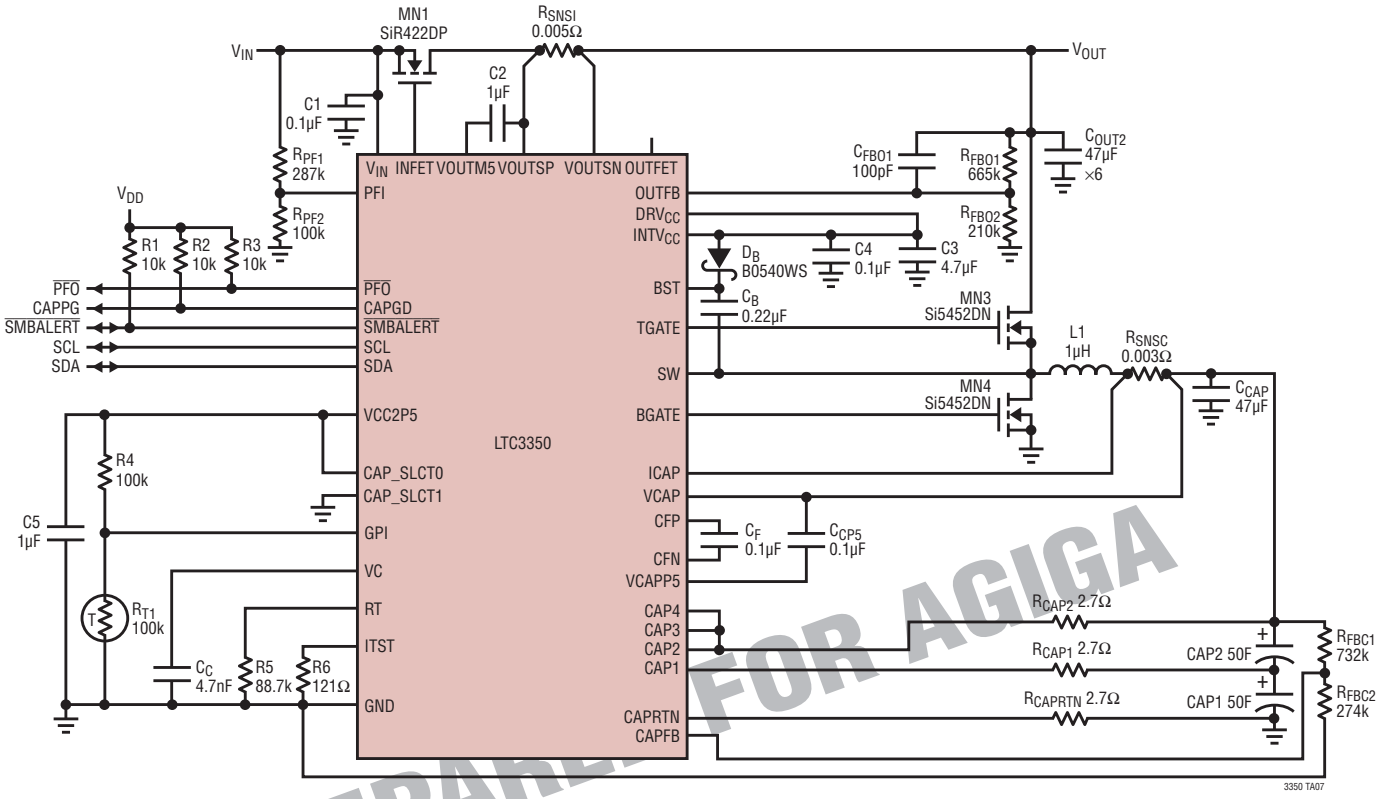
TYPICAL APPLICATIONS

12V, 2A ZETA-SEPIC High Voltage Capacitor Charger with 4.6A Input Current Limit and 10V, 25W Backup Mode



TYPICAL APPLICATIONS

5V, 10A Supercapacitor Charger with 6.4A Input Current Limit and 5V, 30W Backup Mode



REGISTER MAP

REGISTER	SUB ADDR	R/W	BITS	DESCRIPTION	DEFAULT	PAGE
clr_alarms	0x00	R/W	15:0	Clear alarms register	0x0000	xx
msk_alarms	0x01	R/W	15:0	Enable/mask alarms register	0x0000	xx
msk_mon_status	0x02	R/W	9:0	Enable/mask monitor status alerts	0x0000	xx
–	0x03	R/W	15:0	Unused register	-	xx
cap_esr_per	0x04	R/W	15:0	Capacitance/ESR measurement period	0x0000	xx
vcapfb_dac	0x05	R/W	3:0	V_{CAP} voltage reference DAC setting	0x0	xx
vshunt	0x06	R/W	15:0	Capacitor shunt voltage setting	0x3998	xx
cap_uv_lvl	0x07	R/W	15:0	Capacitor undervoltage alarm level	0x0000	xx
cap_ov_lvl	0x08	R/W	15:0	Capacitor overvoltage alarm level	0x0000	xx
gpi_uv_lvl	0x09	R/W	15:0	GPI undervoltage alarm level	0x0000	xx
gpi_ov_lvl	0x0A	R/W	15:0	GPI overvoltage alarm level	0x0000	xx
vin_uv_lvl	0x0B	R/W	15:0	V_{IN} undervoltage alarm level	0x0000	xx
vin_ov_lvl	0x0C	R/W	15:0	V_{IN} overvoltage alarm level	0x0000	xx
vcap_uv_lvl	0x0D	R/W	15:0	V_{CAP} undervoltage alarm level	0x0000	xx
vcap_ov_lvl	0x0E	R/W	15:0	V_{CAP} overvoltage alarm level	0x0000	xx
vout_uv_lvl	0x0F	R/W	15:0	V_{OUT} undervoltage alarm level	0x0000	xx
vout_ov_lvl	0x10	R/W	15:0	V_{OUT} overvoltage alarm level	0x0000	xx
iin_oc_lvl	0x11	R/W	15:0	I_{IN} undercurrent alarm level	0x0000	xx
ichg_uc_lvl	0x12	R/W	15:0	I_{CHG} undercurrent alarm level	0x0000	xx
dtemp_cold_lvl	0x13	R/W	15:0	Die temperature cold alarm level	0x0000	xx
dtemp_hot_lvl	0x14	R/W	15:0	Die temperature hot alarm level	0x0000	xx
esr_hi_lvl	0x15	R/W	15:0	ESR high alarm level	0x0000	xx
cap_lo_lvl	0x16	R/W	15:0	Capacitance low alarm level	0x0000	xx
ctl_reg	0x17	R/W	3:0	Control register	0b0000	xx
num_caps	0x1A	R	1:0	Number of capacitors configured	–	xx
chrg_status	0x1B	R	11:0	Charger status register	–	xx
mon_status	0x1C	R	9:0	Monitor status register	–	xx
alarm_reg	0x1D	R	15:0	Active alarms register	0x0000	xx
meas_cap	0x1E	R	15:0	Measured capacitance value	–	xx
meas_esr	0x1F	R	15:0	Measured ESR value	–	xx
meas_vcap1	0x20	R	15:0	Measured capacitor one voltage	–	xx
meas_vcap2	0x21	R	15:0	Measured capacitor two voltage	–	xx
meas_vcap3	0x22	R	15:0	Measured capacitor three voltage	–	xx
meas_vcap4	0x23	R	15:0	Measured capacitor four voltage	–	xx
meas_gpi	0x24	R	15:0	Measured GPI pin voltage	–	xx
meas_vin	0x25	R	15:0	Measured V_{IN} voltage	–	xx
meas_vcap	0x26	R	15:0	Measured V_{CAP} voltage	–	xx
meas_vout	0x27	R	15:0	Measured V_{OUT} voltage	–	xx
meas_iin	0x28	R	15:0	Measured I_{IN} current	–	xx
meas_ichg	0x29	R	15:0	Measured I_{CHG} current	–	xx
meas_dtemp	0x2A	R	15:0	Measured die temperature	–	xx

REGISTER DESCRIPTIONS

clr_alarms (0x00)

Clear Alarms Register: This register is used to clear alarms caused by exceeding a programmed limit. Writing a one to any bit in this register will cause its respective alarm to be cleared. The one written to this register is automatically cleared when its respective alarm is cleared.

BIT(S)	BIT NAME	DESCRIPTION
0	clr_cap_uv	Clear capacitor undervoltage alarm
1	clr_cap_ov	Clear capacitor overvoltage alarm
2	clr_gpi_uv	Clear GPI undervoltage alarm
3	clr_gpi_ov	Clear GPI overvoltage alarm
4	clr_vin_uv	Clear V_{IN} undervoltage alarm
5	clr_vin_ov	Clear V_{IN} overvoltage alarm
6	clr_vcap_uv	Clear V_{CAP} undervoltage alarm
7	clr_vcap_ov	Clear V_{CAP} overvoltage alarm
8	clr_vout_uv	Clear V_{OUT} undervoltage alarm
9	clr_vout_ov	Clear V_{OUT} overvoltage alarm
10	clr_iin_oc	Clear input overcurrent alarm
11	clr_ichg_uc	Clear charge undercurrent alarm
12	clr_dtemp_cold	Clear die temperature cold alarm
13	clr_dtemp_hot	Clear die temperature hot alarm
14	clr_esr_hi	Clear ESR high alarm
15	clr_cap_lo	Clear capacitance low alarm

msk_alarms (0x01)

Mask Alarms Register: Writing a one to any bit in the Mask Alarms Register enables its respective alarm to trigger an SMBALERT.

BIT(S)	BIT NAME	DESCRIPTION
0	msk_cap_uv	Enable capacitor undervoltage alarm
1	msk_cap_ov	Enable capacitor overvoltage alarm
2	msk_gpi_uv	Enable GPI undervoltage alarm
3	msk_gpi_ov	Enable GPI overvoltage alarm
4	msk_vin_uv	Enable V_{IN} undervoltage alarm
5	msk_vin_ov	Enable V_{IN} overvoltage alarm
6	msk_vcap_uv	Enable V_{CAP} undervoltage alarm
7	msk_vcap_ov	Enable V_{CAP} overvoltage alarm
8	msk_vout_uv	Enable V_{OUT} undervoltage alarm
9	msk_vout_ov	Enable V_{OUT} overvoltage alarm
10	msk_iin_oc	Enable input overcurrent alarm
11	msk_ichg_uc	Enable charge undercurrent alarm
12	msk_dtemp_cold	Enable die temperature cold alarm
13	msk_dtemp_hot	Enable die temperature hot alarm
14	msk_esr_hi	Enable ESR high alarm
15	msk_cap_lo	Enable capacitance low alarm

REGISTER DESCRIPTIONS

msk_mon_status (0x02)

Mask Monitor Status Register: Writing a one to any bit in this register enables a rising edge of its respective bit in the mon_status register to trigger an SMBALERT.

BIT(S)	BIT NAME	DESCRIPTION
0	msk_mon_capesr_active	Set the SMBALERT when there is a rising edge on mon_capesr_active
1	msk_mon_capesr_scheduled	Set the SMBALERT when there is a rising edge on mon_capesr_scheduled
2	msk_mon_capesr_pending	Set the SMBALERT when there is a rising edge on mon_capesr_pending
3	msk_mon_cap_done	Set the SMBALERT when there is a rising edge on mon_cap_done
4	msk_mon_esr_done	Set the SMBALERT when there is a rising edge on mon_esr_done
5	msk_mon_cap_failed	Set the SMBALERT when there is a rising edge on mon_cap_failed
6	msk_mon_esr_failed	Set the SMBALERT when there is a rising edge on mon_esr_failed
7	msk_mon_esr_low_qor	Set the SMBALERT when there is a rising edge on mon_low_qor
8	msk_mon_power_failed	Set the SMBALERT when there is a rising edge on mon_power_failed
9	msk_mon_power_returned	Set the SMBALERT when there is a rising edge on mon_power_returned
15:10		reserved

cap_esr_per (0x04)

Capacitance and ESR Measurement Period: This register sets the period of repeated capacitance and ESR measurements. Each LSB represents 1 second. Capacitance and ESR measurements will not repeat if this register is zero. This register is set to zero by default.

vcapfb_dac (0x05) CAPFBREF = 187.5mV • vcapfb_dac + 618.75mV

V_{CAP} Regulation Reference: This register is used to program the capacitor voltage feedback loop's reference. Only bits 3:0 are active.

vshunt (0x06) 183µV per LSB

Shunt Voltage Register: This register programs the shunt voltage for each capacitor in the stack. The charger will limit current and the active shunts will shunt current to prevent this voltage from being exceeded. As a capacitor voltage nears this level, the charge current will be reduced. This should be programmed higher than the intended final balanced individual capacitor voltage. Setting this register to 0x0000 disables the shunt.

cap_uv_lvl (0x07) 183µV per LSB

Capacitor Undervoltage Level: This is an alarm threshold for each individual capacitor voltage in the stack. If enabled, any capacitor voltage falling below this level will trigger an alarm and an SMBALERT.

cap_ov_lvl (0x08) 183µV per LSB

Capacitor Overvoltage Level: This is an alarm threshold for each individual capacitor in the stack. If enabled, any capacitor voltage rising above this level will trigger an alarm and an SMBALERT.

gpi_uv_lvl (0x09) 183µV per LSB

General Purpose Input Undervoltage Level: This is an alarm threshold for the GPI pin. If enabled, the voltage falling below this level will trigger an alarm and an SMBALERT.

gpi_ov_lvl (0x0A) 183µV per LSB

General Purpose Input Overvoltage Level: This is an alarm threshold for the GPI pin. If enabled, the voltage rising above this level will trigger an alarm and an SMBALERT.

REGISTER DESCRIPTIONS

vin_uv_lvl (0x0B) 2.2mV per LSB

V_{IN} Undervoltage Level: This is an alarm threshold for the V_{IN} voltage. If enabled, the voltage falling below this level will trigger an alarm and an SMBALERT.

vin_ov_lvl (0x0C) 2.2mV per LSB

V_{IN} Overvoltage Level: This is an alarm threshold for the input voltage. If enabled, the voltage rising above this level will trigger an alarm and an SMBALERT.

vcap_uv_lvl (0x0D) 1.465mV per LSB

V_{CAP} Undervoltage Level: This is an alarm threshold for the capacitor stack voltage. If enabled, the voltage falling below this level will trigger an alarm and an SMBALERT.

vcap_ov_lvl (0x0E) 1.465mV per LSB

V_{CAP} Overvoltage Level: This is an alarm threshold for the capacitor stack voltage. If enabled, the voltage rising above this level will trigger an alarm and an SMBALERT.

vout_uv_lvl (0x0F) 2.2mV per LSB

V_{OUT} Undervoltage Level: This is an alarm threshold for the output voltage. If enabled, the voltage falling below this level will trigger an alarm and an SMBALERT.

vout_ov_lvl (0x10) 2.2mV per LSB

V_{OUT} Overvoltage Level: This is an alarm threshold for the output voltage. If enabled, the voltage rising above this level will trigger an alarm and an SMBALERT.

iin_oc_lvl (0x11) $1.953\mu V/R_{SNSI}$ per LSB

Input Overcurrent Level: This is an alarm threshold for the input current. If enabled, the current rising above this level will trigger an alarm and an SMBALERT.

ichg_uc_lvl (0x12) $1.953\mu V/R_{SNSC}$ per LSB

Charge Undercurrent Level: This is an alarm threshold for the charge current. If enabled, the current falling below this level will trigger an alarm and an SMBALERT.

dtemp_cold_lvl (0x13) Temperature = 0.028°C per LSB – 251.4°C

Die Temperature Cold Level: This is an alarm threshold for the die temperature. If enabled, the die temperature falling below this level will trigger an alarm and an SMBALERT.

dtemp_hot_lvl (0x14) Temperature = 0.028°C per LSB – 251.4°C

Die Temperature Hot Level: This is an alarm threshold for the die temperature. If enabled, the die temperature rising above this level will trigger an alarm and an SMBALERT.

esr_hi_lvl (0x15) $R_{SNSC}/64$ per LSB

ESR High Level: This is an alarm threshold for the measured stack ESR. If enabled, a measurement of stack ESR exceeding this level will trigger an alarm and an SMBALERT.

cap_lo_lvl (0x16) $33.7\mu F \bullet R_{TST}/R_T$ per LSB

Capacitance Low Level: This is an alarm threshold for the measured stack capacitance. If enabled, if the measured stack capacitance is less than this level it will trigger an alarm and an SMBALERT.

REGISTER DESCRIPTIONS

ctl_reg (0x17)

Control Register: Several Control Functions are grouped into this register.

BIT(S)	BIT NAME	DESCRIPTION
0	ctl_strt_capesr	Begin a capacitance and ESR measurement when possible; this bit clears itself once a cycle begins.
1	ctl_gpi_buffer_en	A one in this bit location enables the input buffer on the GPI pin. With a zero in this location the GPI pin is measured without the buffer.
2	ctl_stop_sapesr	Steps an active capacitance/?? measurement.
3	ctl_cap_scale	Increases capacitor measurement resolution by 100x, this is used when measuring smaller capacitors.

num_caps (0x1A)

Number of Capacitors: This register shows the state of the CAP_SLCT1, CAP_SLCT0 pins. The value read in this register is the number of capacitors programmed minus one.

VALUE	CAPACITORS	
0b00	1 Capacitor Selected	
0b01	2 Capacitors Selected	
0b10	3 Capacitors Selected	
0b11	4 Capacitors Selected	

chrg_status (0x1B)

Charger Status Register: This register provides real time status information about the state of the charger system. Each bit is active high.

BIT(S)	BIT NAME	DESCRIPTION
0	**chrg_stepdown**	The synchronous controller is in step-down mode (charging)
1	**chrg_stepup**	The synchronous controller is in step-up mode (backup)
2	**chrg_cv**	The charger is in constant voltage mode
3	**chrg_uvlo**	The charger is in undervoltage lockout
4	**chrg_input_ilim**	The charger is in input current limit
5	**chrg_cappg**	The capacitor voltage is above power good threshold
6	**chrg_shnt**	The capacitor manager is shunting
7	**chrg_bal**	The capacitor manager is balancing
8	**chrg_dis**	The charger is temporarily disabled for capacitance measurement
9	**chrg_ci**	The charger is in constant current mode
10	**Reserved**	
11	**chrg_pfo**	Input voltage is below PFI level

REGISTER DESCRIPTIONS

mon_status (0x1C)

Monitor Status: This register provides real time status information about the state of the monitoring system. Each bit is active high.

BIT(S)	BIT NAME	DESCRIPTION
0	**mon_capesr_active**	Capacitance/ESR measurement is in progress
1	**mon_capesr_scheduled**	Waiting programmed time to begin a capacitance/ESR measurement
2	**mon_capesr_pending**	Waiting for satisfactory conditions to begin a capacitance/ESR measurement
3	**mon_cap_done**	Capacitance measurement has completed
4	**mon_esr_done**	ESR Measurement has completed
5	**mon_cap_failed**	The last attempted capacitance and ESR measurement was unable to complete
6	**mon_esr_failed**	The last attempted ESR measurement was unable to complete
7	**mon_esr_low_qual**	Insufficient signal for quality ESR measurement, result may still be usable
8	**mon_power_failed**	This bit is set when V_{IN} falls below the PFI threshold or the charger is unable to charge. It is cleared only when power returns and the charger is able to charge.
9	**mon_power_returned**	This bit is set when the input is above the PFI threshold and the charger is able to charge. It is cleared only when mon_power_failed is set.

alarm_reg (0x1D)

Alarms Register: A one in any bit in the register indicates its respective alarm has triggered. All bits are active high.

BIT(S)	BIT NAME	DESCRIPTION
0	**alarm_cap_uv**	Capacitor undervoltage alarm
1	**alarm_cap_ov**	Capacitor overvoltage alarm
2	**alarm_gpi_uv**	GPI undervoltage alarm
3	**alarm_gpi_ov**	GPI overvoltage alarm
4	**alarm_vin_uv**	V_{IN} undervoltage alarm
5	**alarm_vin_ov**	V_{IN} overvoltage alarm
6	**alarm_vcap_uv**	V_{CAP} undervoltage alarm
7	**alarm_vcap_ov**	V_{CAP} overvoltage alarm
8	**alarm_vout_uv**	V_{OUT} undervoltage alarm
9	**alarm_vout_ov**	V_{OUT} overvoltage alarm
10	**alarm_iin_oc**	Input overcurrent alarm
11	**alarm_ichg_uc**	Charge undercurrent alarm
12	**alarm_dtemp_cold**	Die temperature cold alarm
13	**alarm_dtemp_hot**	Die temperature hot alarm
14	**alarm_esr_hi**	ESR high alarm
15	**alarm_cap_lo**	Capacitance low alarm

REGISTER DESCRIPTIONS

meas_cap (0x1E) — 337µF • R_{TST}/R_T per LSB

Measured capacitor stack capacitance value. When ctl_cap_scale is set the constant is 3.37µF R_{TST}/R_T.

meas_esr (0x1F) — $R_{SNSC}/64$ per LSB

Measured capacitor stack equivalent series resistance (ESR) value

meas_vcap1 (0x20) — 183µV per LSB

Measured voltage between the CAP1 and CAPRTN pins.

meas_vcap2 (0x21) — 183µV per LSB

Measured voltage between the CAP2 and CAP1 pins.

meas_vcap3 (0x22) — 183µV per LSB

Measured voltage between the CAP3 and CAP2 pins.

meas_vcap4 (0x23) — 183µV per LSB

Measured voltage between the CAP4 and CAP3.

meas_gpi (0x24) — 183µV per LSB

Measurement of GPI pin voltage.

meas_vin (0x25) — 2.2mV per LSB

Measured Input Voltage.

meas_vcap (0x26) — 1.465µV per LSB

Measured Capacitor Stack Voltage.

meas_vout (0x27) — 2.2mV per LSB

Measured Output Voltage.

meas_iin (0x28) — 1.953µV/R_{SNSI} per LSB

Measured Input Current.

meas_ichg (0x29) — 1.953µV/R_{SNSC} per LSB

Measured Charge Current.

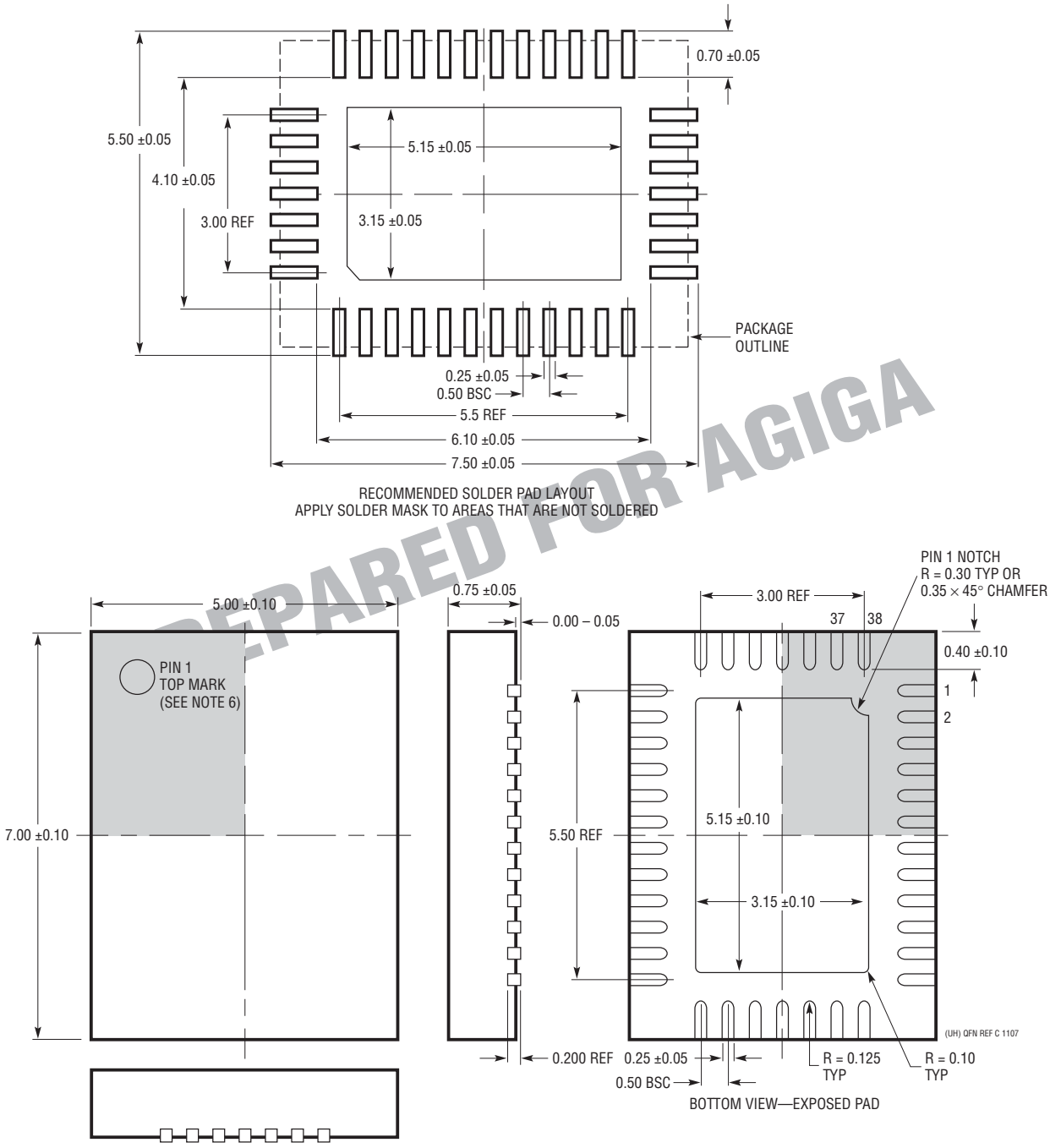
meas_dtemp (0x2A) — Temperature = 0.028°C per LSB – 251.4°C

Measured die temperature.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

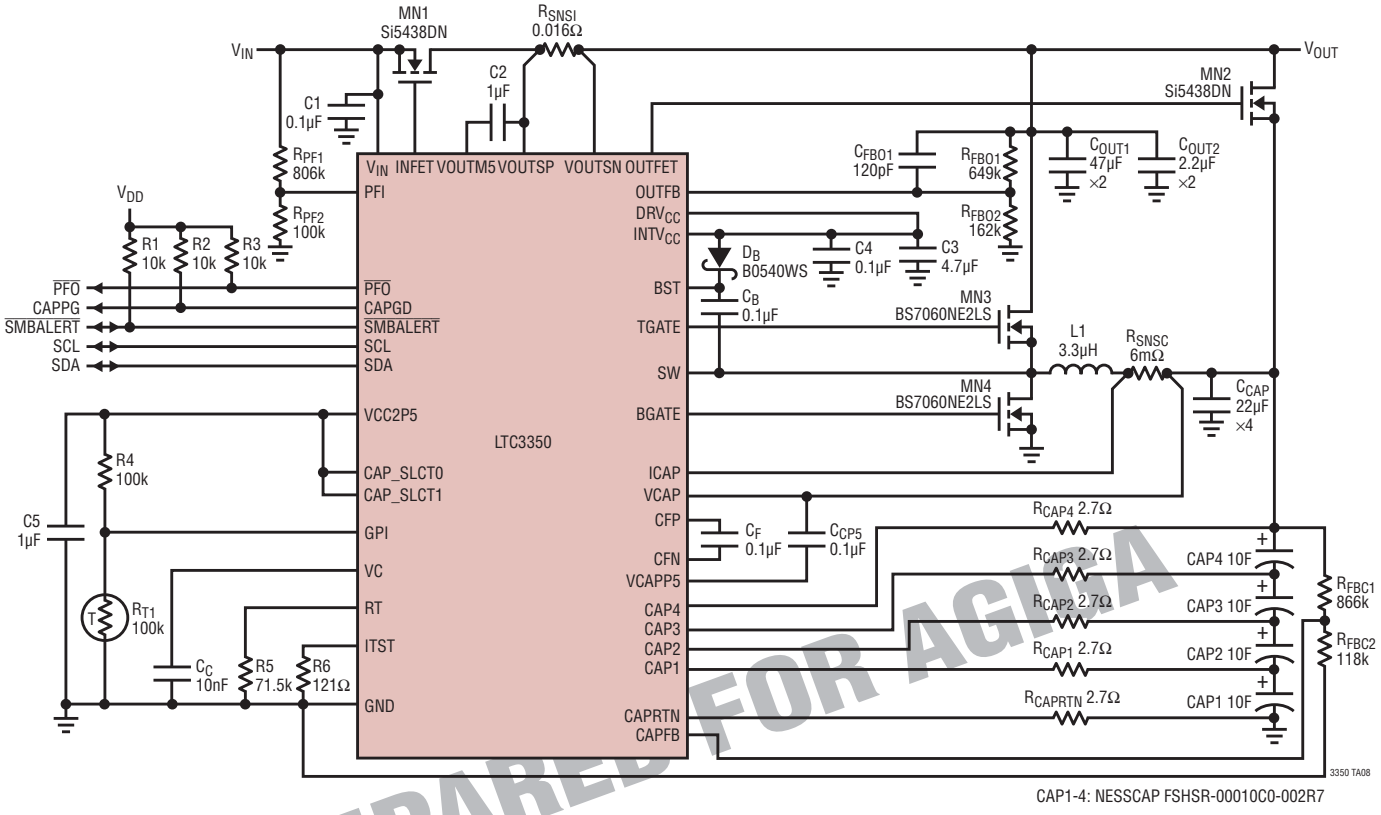
UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

12V, 5A Supercapacitor Charger with 2A Input Current Limit and 6V, 25W Backup Mode



CAP1-4: NESSCAP FSHSR-00010C0-002R7

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Power Management		
LTC3226	2-Cell Supercapacitor Charger with Backup PowerPath Controller	1x/2x Multimode Charge Pump Supercapacitor Charger, Automatic Cell Balancing, PowerPath, 2A LDO Backup Supply, Automatic Main/Backup Switchover, 2.5V to 5.5V, Programmable Charge Voltage, Programmable Input Current, 16-Lead 3mm × 3mm QFN Package
LTC3625	1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing	High Efficiency Step-Up/Step-Down Charging of Two Series Supercapacitors. Automatic Cell Balancing. Programmable Charging Current to 500mA (Single Inductor), 1A (Dual Inductor). V_{IN} = 2.7V to 5.5V, Selectable 2.4V/2.65V Regulation per Cell (LTC3625). Low No-Load Quiescent Current: 23µA. 12-Lead 3mm × 4mm DFN Package
LT3741	High Power, Constant Current, Constant Voltage, Step-Down Controller	6V to 36V Input Range, Wide Output Range, Average Current Mode Control, <1µA Shutdown Current, 4mm × 4mm QFN Package, 20-Lead FE Package
LTC4425	Linear SuperCap Charger with Current-Limited Ideal Diode and V/I Monitor	Constant-Current/Constant-Voltage Linear Charger for 2-Cell Series Supercapacitor Stack. V_{IN}: Li-Ion/Polymer Battery, a USB Port, or a 2.7V to 5.5V Current-Limited Supply. 2A Charge Current, Automatic Cell Balancing, 20µA Quiescent Current, Shutdown Current <2µA. Low Profile 12-Pin 3mm × 3mm DFN or a 12-Lead MSOP Package

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