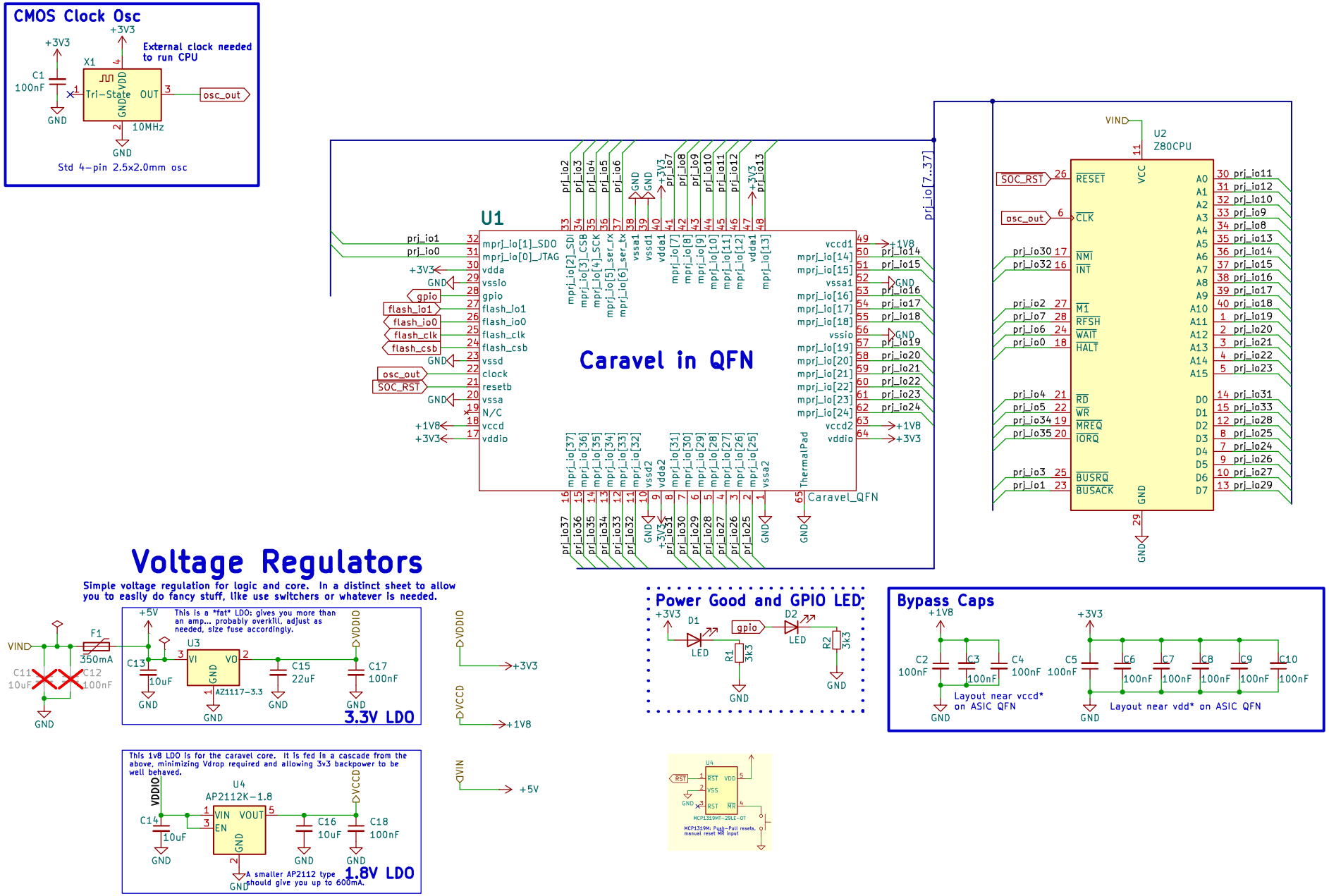
CMOS Clock Osc
External clock needed to run CPU
X1
Tri-State
VDD
GND
OUT
10MHz
C1 100nF
+3V3
osc_out
Std 4-pin 2.5x2.0mm osc
U1
Caravel in QFN
Caravel_QFN
mprj_io[1]_SDO
mprj_io[0]_JTAG
vdda
vssio
gpio
flash_io1
flash_io0
flash_clk
flash_csb
vssd
clock
resetb
vssa
N/C
vccd
vddio
SOC_RST
prj_io[7..37]
U2
Z80CPU
VIND
RESET
CLK
NMI
INT
M1
RFSH
WAIT
HALT
RD
WR
MREQ
IORQ
BUSRQ
BUSACK
VCC
GND
Voltage Regulators
Simple voltage regulation for logic and core. In a distinct sheet to allow you to easily do fancy stuff, like use switchers or whatever is needed.
F1 350mA
C11 10uF
C12 100nF
This is a *fat* LDO: gives you more than an amp... probably overkill, adjust as needed, size fuse accordingly.
U3
AZ1117-3.3
C13 10uF
C15 22uF
C17 100nF
VDDIO
3.3V LDO
VCCD
This 1v8 LDO is for the caravel core. It is fed in a cascade from the above, minimizing Vdrop required and allowing 3v3 backpower to be well behaved.
U4
AP2112K-1.8
VIN
VOUT
EN
C14 10uF
C16 10uF
C18 100nF
A smaller AP2112 type should give you up to 600mA.
1.8V LDO
Power Good and GPIO LED
D1 LED
D2 LED
R1 3k3
R2 3k3
Bypass Caps
C2 100nF
C3 100nF
C4 100nF
C5 100nF
C6 100nF
C7 100nF
C8 100nF
C9 100nF
C10 100nF
Layout near vccd* on ASIC QFN
Layout near vdd* on ASIC QFN
MCP1319MT-29LE-OT
MCP1319M: Push-Pull resets, manual reset MR input