EE 214: Digital Circuits Lab

Homework-1 Submission

Roll No. 200070054

Q.1. This zip file contains all the needed files.

Gates.vhdl

add_sub.vhdl

Full_Adder.vhdl

DUT.vhdl

Testbench.vhdl

TRACEFILE.txt

Q.2. Effect of different values of M on the functionality of a given circuit:

1. For M=1, the circuit behaves like a 4-bit ripple carry subtractor

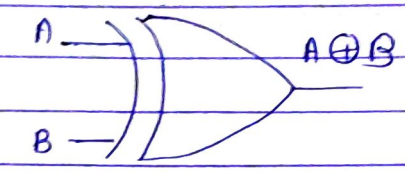
2. For M=0, the circuit behaves like a 4-bit ripple carry adder.

Q.3. The simulation folder in this zip file contains the output file generated after RTL and Gate Level Simulation.

Explanation of part-B

→ Truth table of a XOR gate,

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0



→ now in our problem we are giving B_0, B_1, B_2 and B_3 with M as a input to XOR gate & its output to full adder with A_0, A_1, A_2 and A_3

so $$M \oplus B_i = \begin{cases} B_i, & \text{if } M = 0 \\ \overline{B_i}, & \text{if } M = 1 \end{cases}$$

⇒ so the input to full adder will be A_i & B_i when $M = 0$
& A_i & $\overline{B_i}$ when $M = 1$

⇒ so this circuit will add A_i & B_i for $M=0$ & subtract for $M = 1$.

→ conclusion: This four bit ripple carry adder will behave like a subtracter when $M=1$ & a adder when $M = 0$.