Combinational Circuit 1

Wadhwani Electronics Lab, IIT Bombay
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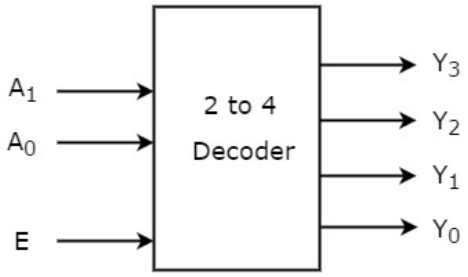
Use structural modelling for this experiment; means instantiate components and use port map to connect those components

Part-A: 2 to 4 decoder

(i) Design [3 Marks]

Design a 2 to 4 decoder with enable input as shown in figure below. Use only 2 or 3 input AND / NAND gate and inverters. (Assume enable as active high input)



INFO

Decoders are combinational circuit which takes in binary information in the form of N input lines and change the binary information into 2^N output lines.

Hint: See Tracefile to understand the functionality of decoder

(ii) VHDL description [5 Marks]

Describe a 2 to 4 decoder with enable input in VHDL.

(iii) Simulation [5 Marks]

Simulate the decoder using the generic testbench to confirm the correctness of your description.

NOTE

To do this, you need to use the given tracefile and modify the testbench given to you appropriately.

Tracefile format<A1 A0><E> <Y3 Y2 Y1 Y0> 1111Tracefile

Part-B: 3 to 8 decoder

(i) Design **[3 Marks]**

Design a 3 to 8 decoder with enable input using 2 to 4 decoder designed in part A

> **INFO**
>
> 3 data input
> 1 enable input
> $2^3 = 8$ output lines

(ii) VHDL description **[5 Marks]**

Describe a 3 to 8 decoder with enable input in VHDL.

(iii) Simulation **[5 Marks]**

Simulate the decoder using the generic testbench to confirm the correctness of your description.

> **NOTE**
>
> To do this, you need to use the given tracefile and modify the testbench given to you appropriately.

Tracefile format<A2 A1 A0><E> <Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0> 11111111Tracefile

Part-C: Full adder using 3 to 8 decoder

(i) Design **[3 Marks]**

Design full adder using 3 to 8 decoder designed in part B

(ii) VHDL description **[5 Marks]**

Describe full adder using 3 to 8 decoder in VHDL.

(iii) Simulation **[5 Marks]**

Simulate this full adder using the generic testbench to confirm the correctness of your description.

> **NOTE**
>
> To do this, use the given tracefile (from full adder demo resources) and modify the testbench given to you appropriately.

Tracefile format<A B Cin> <S Cout> 11