Hardik Panchal

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Research Interests

Digital VLSI Design, Machine Learning, Communication Networks, Computer Architecture

Education

Indian Institute of Technology Bombay *2020-24*
B.Tech. with Honours in Electrical Engineering CGPA: 9.02
Minor Degree in Computer Science and Engineering

Scholastic Achievements

- Achieved a perfect **10 SPI** during the 7th and 8th semester at IIT Bombay with 54 credits *(2024)*
- Secured **99.84** percentile in Joint Entrance Examination (JEE) Main among **1.1 million** candidates *(2020)*
- Achieved **98.97** percentile in *IIT-JEE Advanced* examination among **0.15 million** candidates across India *(2020)*
- Ranked in the **Top 24** out of **0.12 million** candidates in the Intermediate level board examination by **GSEB** *(2020)*

Professional Experience

Hardware Engineer Associate | Qualcomm *Jul 24-present*

– Working in an ML-based tool development project to assist Physical Design Enginners

Hardware Engineer Intern | Qualcomm *May-Jul 23*

– Implemented **Q-learning**-based **macro placer** algorithm to get optimal placement in a 2D grid for same-sized macros
– Collected data using the Cadence **Innovus placer** tool and trained a model to predict the feedback for given placement
– Integrated the **Congestion** and **wire length** based feedback with the RL pipeline to provide a **reward** at each iteration
– Executed the entire Physical Design(PD) flow on a small netlist, including floorplan, CTS, and routing in **Innovus**
– Ranked in **top 10** teams in **IdeaQuest** competition for proposing an innovative idea using ML and 5G for smart cities

Computer Vision and AI Intern | Assert AI *Jun-Jul 22*

– Estimated **33** key landmarks of the human body using the **Mediapipe** pipeline by Google and predicted **7+** use-cases with different poses, activities, and counters by manipulating them, resulting in lightweight and **fast live tracking**
– Utilized **Face Mesh** tool from Mediapipe to predict **emotions** from **468 3D** face landmarks with **84.72%** accuracy
– Deployed **custom YOLO models** for classification and object detection in surveillance tasks, with RTSP and multi-stream capability on **Deepstream SDK** using **NVIDIA Jetson series** GPU accelerator

Research Projects

Wi-Fi 6 Performance Analysis and Scheduling Optimization *Aug '23-May '24*

BTP | Research Project | Prof. Jayakrishnan Nair, Prof. Nikhil Karamchandani, IIT Bombay

– Worked on validation and enhancement of **OFDMA** in Wi-Fi 6 networks using **ns-3** network simulator in C++
– Enhanced simulator codebase to provide more features and flexibility and modeled scenarios involving **haptic** devices
– Implemented better scheduling schemes and used **online learning** techniques to improve uplink flow latency values

True Random Number Generator(TRNG) using Ring Oscillators in FPGA *Jan-May '24*

RnD | Research Project | Prof. Udayan Ganguly, IIT Bombay

– Utilised **clock jitter** as a physical entropy source to generate True Random Numbers in **Genesys2** FPGA
– TRNG operates at **3 Mbit/sec** with a power consumption of **20 fJ/bit**, which is very low for an FPGA based TRNG
– TRNG custom IP interacts with the **MicroBlaze** softcore microprocessor via **AXI** interface in FPGA

Technical Projects

Unsupervised Representational Learning with DCGAN *Mar-Apr '23*

Introduction to Machine Learning | Course Project | Prof. Amit Sethi, IIT Bombay

– Implemented the **DCGAN** architecture from scratch for unsupervised representational learning and feature extraction
– Trained DCGAN models in **Tensorflow** on LSUN, CIFAR-10, SVHN, Human Faces, and Tiny ImageNet datasets
– Utilized the trained model as a **feature extractor** for classification on above datasets with **84%** of average accuracy

Reinforcement Learning *Aug-Nov '22*

Foundations of Intelligent and Learning Agents | Course Project | Prof. Shivaram Kalyanakrishnan, IIT Bombay

– Implemented and compared ϵ-greedy, **UCB**, **KL-UCB**, and Thompson Sampling for stochastic **multi-armed bandits**
– Modelled a situation in cricket as an **MDP** and derived optimal policy using **policy iteration** and **linear programming**

– Navigated a vehicle through obstacles via an algorithm based on action-value **function approximation** methods

Superscalar Processor Design *Nov-Dec '22*

Advanced Computer Architecture | *Course Project* | *Prof. Virendra Singh, IIT Bombay*

– Created a six-stage, **2-way fetch**, an **out-of-order**, superscalar, 16-bit microprocessor for a 15-instruction **RISC** ISA
– Employed instruction fetch, decode, dispatch, execute, and write-back stages with **branch prediction** techniques
– Collaborated in a team of 4 and implemented blocks of the register file, memory banks, reservation station, and reorder buffer and integrated and tested them using custom testbenches in **VHDL** using Intel **Quartus Prime**

Autonomous Driving: Car Detection *Dec '21*

Winter in Data Science(WiDS) | *Analytics Club, IIT Bombay*

– Implemented **Non-Max Suppression** and Intersection Over Union(**IOU**) parameters to process the YOLO encoder output for predicting accurate bounding boxes and class probabilities with a **mAP** score of **0.56** on the drive.ai dataset
– Applied **Transfer Learning** on YOLO to **fine-tune** the pre-trained CNN model for the Vehicles-OpenImages dataset

Flash ADC Design in Cadence Virtuoso *Jan-Apr '23*

Mixed Signal VLSI Design | *Course Project* | *Prof. Rajesh Zele, IIT Bombay*

– Designed and simulated **bootstrapped** switch-based **sample and hold** circuit with **9+** ENOB and performed **FFT**
– Constructed a **Strong-Arm** latched comparator having 3σ offset of **2.5 mV** and performed layout in Cadence Virtuoso
– Integrated 6-bit design operates at **1 GHz**, having ENOB of **5.28** and **SFDR** of **42 dB**, and max **DNL** as **0.6 LSB**

Gadget for Solar Cell Characterization *Jan-Apr '23*

Electronic Design Lab | *Prof. Joseph John, IIT Bombay*

– Invented a compact, modular, battery-operated, rechargeable device to characterize a 10W solar panel **automatically**
– Programmed an **ATXMEGA128 MCU** to vary the gate voltage of a **power MOSFET** to make variable load for panel
– Developed a Python-based **CLI program** to save and plot the data received on PC from the device via **USART**

Low Noise Amplifier(LNA) Design *Mar-Apr '23*

RF Microelectronics Chip Design | *Course Project* | *Prof. Jayanta Mukherjee, IIT Bombay*

– Designed a **single-ended cascoded** common source Low Noise Amplifier (CS-LNA) on UMC 180nm CMOS technology
– Achieved a **Noise Figure** of less than **3 dB** across the frequency range of 880 MHZ to 915 MHz in Cadence Virtuoso

8051 Microcontroller Programming *Jan-Apr '22*

Microprocessors Lab | *Course Project* | *Prof. S. Vijayakumaran, IIT Bombay*

– Interfaced a speaker with the **AT89C5131** development board using a MOSFET in the common emitter mode
– Developed the program in embedded C to make an **interactive ATM emulator** having password authentication and taking inputs from a computer terminal using **UART** and displaying outputs and instructions on **onboard LCD**

Technical Skills

Languages	C++, Python, MATLAB, VHDL/Verilog, Embedded C, Assembly, LaTeX, SageMath
Software & Packages	Cadence Virtuoso and Innovus, Quartus Prime, Vivado, Keil μVision, Flip, Eagle, NGSpice, Git/GitHub
Python Libraries	PyTorch, TensorFlow, NumPy, pandas, OpenCV, Matplotlib, scikit-learn

Positions of Responsibility

Department Academic Mentor | Department of Electrical Engineering | IIT Bombay *Jun '22 - May '23*

– Part of **46**-member DAMP team selected from **100+ applicants** on the basis of extensive **interview** and **peer reviews**
– Mentored **12 sophomores** to help them with academics, time management, and extra-curricular endeavors
– Attended **mentor training programs** organized by professional mentors from Student Wellness Center

Winter In Data Science(WiDS) Mentor | Analytics Club | IIT Bombay *Dec '22*

– Mentored **10 students** for a Data Science and Computer Vision project of **Sudoku Solver** in (**WiDS**)
– Articulated beginner-friendly roadmap for learning basics of Deep Learning and CV with hands-on practice assignments

Key Courses Undertaken

CS and Math	Advanced Topics in Machine Learning | Computer Programming (C++) | Linear Algebra | Probability and Random Processes | Image Processing | Medical Image Computing
Electrical	VLSI Design | Embedded Systems Design | Microprocessors | Computer Architecture | Testing and Verification of VLSI Circuits | Digital Systems | Control Systems | Electronic Devices | Digital Signal Processing | Communication Systems | CMOS Analog IC Design

Extra Curricular Activities

- Completed a year-long training course in **National Cadet Corps**, IIT Bombay (2021)
- Completed a **fROSty Winter** workshop conducted by **E**lectronics and **R**obotics **C**lub covering basics of ROS (2021)