Hardik Dhansukhbhai Panchal | **200070054**
Electrical Engineering | **B.Tech.**
Indian Institute of Technology Bombay | **Gender: Male**
DOB: 03/07/2003

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2024	8.68
Intermediate	GSEB	Shree Vasishtha Vidhyalaya, Vav	2020	93.00%
Matriculation	GSEB	The Mandvi High School, Mandvi	2018	96.50%

Pursuing a **Minor** degree in the Department of **Computer Science & Engineering**

Scholastic Achievements

- Secured **98.97** percentile in **JEE Advanced** examination among **0.15 million** aspirants across India [2020]
- Achieved **99.84** percentile in **JEE Main** examination among **1.14 million** candidates across India [2020]
- Ranked in the **Top 24** out of **0.12 million** candidates in the Intermediate level board examination by **GSEB** [2020]
- Achieved **99.92** percentile in **GUJ-CET** entrance examination among **0.12 million** candidates [2020]

Professional Experience

Chip Placement using Reinforcement Learning | Qualcomm | Hardware Intern [May-July '23]

Developed an RL-based framework to automatically generate optimal macro placement

- Implemented the **Q-learning**-based **macro placer** algorithm to get optimal placement in a 2D grid for same-sized macros
- Collected data using the Cadence **Innovus placer** tool and trained a model to predict the feedback for the given placement
- Integrated the **Congestion** and **wire length** based feedback with the RL pipeline to provide a **reward** at each iteration
- Executed the entire Physical Design(PD) flow on a small netlist, including floorplan, CTS, and routing in **Innovus**
- Ranked in the **top 10** teams in **IdeaQuest** competition for proposing an innovative idea using ML and 5G for smart cities

Human Pose and Activity Estimation | Assert AI | Computer Vision and AI Intern [May-July '22]

Developed an ML model to predict emotions from face landmarks

- Estimated **33** key landmarks of the human body using the **Mediapipe** pipeline by Google and predicted **7+** use-cases with different poses, activities, and counters by manipulating them, resulting in lightweight and **fast live tracking**
- Utilized **Face Mesh** tool from Mediapipe to predict **emotions** from **468 3D** face landmarks with **84.72%** accuracy
- Deployed **custom YOLO models** for classification and object detection in surveillance tasks, with RTSP and multi-stream capability on **Deepstream SDK** using **NVIDIA Jetson series** GPU accelerator

Key Projects

Reinforcement Learning [Aug-Nov '22]

Foundations of Intelligent and Learning Agents | Course Project | Prof. Shivaram Kalyanakrishnan, IIT Bombay

- Implemented and compared ϵ-greedy, **UCB**, **KL-UCB**, and Thompson Sampling for stochastic **multi-armed bandit** framework
- Modelled a situation in cricket as an **MDP** and derived optimal policy using **policy iteration** and **linear programming**
- Navigated a vehicle through obstacles via an algorithm based on action-value **function approximation** methods

Unsupervised Representational Learning with DCGAN [Mar-Apr '23]

Introduction to Machine Learning | Course Project | Prof. Amit Sethi, IIT Bombay

- Implemented the **DCGAN** architecture from scratch for unsupervised representational learning and feature extraction
- Trained DCGAN models in **Tensorflow** on LSUN, CIFAR-10, SVHN, Human Faces, and Tiny ImageNet datasets
- Utilized the trained model as a **feature extractor** for classification on above datasets with **84%** of average accuracy

Autonomous Driving: Car Detection [Dec '21]

Winter in Data Science(WiDS) | Analytics Club, IIT Bombay

- Implemented **Non-Max Suppression** and Intersection Over Union(**IOU**) parameters to process the YOLO encoder output for predicting accurate bounding boxes and class probabilities with a **mAP** score of **0.56** on the drive.ai dataset
- Applied **Transfer Learning** on YOLO to **fine-tune** the pre-trained CNN model for the Vehicles-OpenImages dataset

Superscalar Processor Design [Nov-Dec '22]

Advanced Computer Architecture | Course Project | Prof. Virendra Singh, IIT Bombay

- Created a six-stage, **2-way fetch**, an **out-of-order**, superscalar, 16-bit microprocessor for a 15-instruction **RISC** ISA
- Employed instruction fetch, decode, dispatch, execute, and write-back stages with **branch prediction** techniques
- Collaborated in a team of 4 and implemented blocks of the register file, memory banks, reservation station, and reorder buffer and integrated and tested them using custom testbenches in **VHDL** using Intel **Quartus Prime**

Other Projects

A Deep Dive into CNNs [Mar-Jun '21]

Seasons Of Code | Web and Coding Club, IIT Bombay

- Studied and implemented CNN architectures of **AlexNet**, **VGGNet**, **ResNet**, and **GoogleNet** in Pytorch framework
- Trained and tested models of these architectures on MNIST, Fashion-MNIST, and CIFAR-10 datasets
- Implemented the concept of **Transfer Learning** using a pre-trained model of CNN in PyTorch

Gadget for Solar Cell Characterization [Jan-Apr '23]

Electronic Design Lab | Course Project | Prof. Joseph John, IIT Bombay

- Invented a compact, modular, battery-operated, rechargeable device to characterize a 10W solar panel **automatically**
- Programmed an **ATXMEGA128 MCU** to vary the gate voltage of a **power MOSFET** to create a variable load for panel
- Developed a Python-based **CLI program** to save and plot the data received on PC from the device via **USART**

Neural Style Transfer and Image Segmentation [May '22]

Self Project | Deep Learning

- Merged content image with a style image using **VGG-19** neural network following the Neural Style Transfer paper
- Implemented semantic segmentation using **U-Net** paper based architecture on the **CARLA** self-driving car dataset
- Applied sparse **categorical cross-entropy** loss function for pixel-wise prediction and achieved **79.26%** accuracy

8051 Microcontroller Programming [Jan-Apr '22]

Microprocessors Lab | Course Project | Prof. S. Vijayakumaran, IIT Bombay

- Interfaced a speaker with the **AT89C5131** development board using a MOSFET in the common emitter mode
- Developed the program in embedded C to make an **interactive ATM emulator** having password authentication and taking inputs from a computer terminal using **UART** and displaying outputs and instructions on **onboard LCD**

Flash ADC Design in Cadence Virtuoso [Jan-Apr '23]

Mixed Signal VLSI Design | Course Project | Prof. Rajesh Zele, IIT Bombay

- Designed and simulated **bootstrapped** switch-based **sample and hold** circuit with **9+** ENOB and performed **FFT** analysis
- Constructed a **Strong-Arm** latched comparator having 3σ offset of **2.5 mV** and performed layout in Cadence Virtuoso

Probability of Correct Local inversion of a map [Mar-Apr '23]

Topics in Cryptology | Course Project | Prof. Virendra Sule, IIT Bombay

- Analysed Linear Complexity (**LC**) profiles of the bit multisequences with Quadratic Residue and Exponential Map
- Utilized **SageMath** to get probability of local inversion of a map using the minimal polynomial of a recursive sequence

Positions Of Responsibility

Department Academic Mentor | *Department of Electrical Engineering* [Jun '22 - May '23]

- Part of **46**-member DAMP team selected from **100+ applicants** on the basis of extensive **interview** and **peer reviews**
- Mentored **12 sophomores** to help them with academics, time management, and extra-curricular endeavors
- Attended **mentor training programs** organized by professional mentors from Student Wellness Center

Winter In Data Science(WiDS) Mentor | *Analytics Club* [Dec '22]

- Mentored **10 students** for a Data Science and Computer Vision project **Sudoku Solver** in Winter in Data Science(**WiDS**)
- Articulated beginner-friendly roadmap for learning basics of Deep Learning and CV, including hands-on practice assignments

Technical Skills

Languages	C++, Python, Java, MATLAB, VHDL, Embedded C, Assembly, LaTeX, SageMath
Softwares/Packages	Cadence Virtuoso and Innovus, Quartus Prime, Keil μVision, Flip, Eagle, NGSpice, Git/GitHub
Python Libraries	PyTorch, TensorFlow, NumPy, pandas, OpenCV, Matplotlib, scikit-learn

Key Courses Undertaken

Electrical	Mixed Signal VLSI Design, RF Chip Design, Advanced Computer Architecture, Topics in Cryptology, Information Theory & Coding, Communication Networks, VLSI Design*
CSE	Data Structures and Algorithms, Design and Analysis of Algorithms, Intro to ML, Computer Networks, Foundations of Intelligent and Learning Agents, Advanced ML*, Logic for CS*
MOOC's	Coursera Deep Learning Specialization

Extra Curricular Activities

**To be completed by November 2023*

- Completed a year-long training course in **National Cadet Corps**, IIT Bombay [2021]
- Completed a **fROSty Winter** workshop conducted by **E**lectronics and **R**obotics **C**lub covering basics of ROS [2021]
- Represented Shree Vasishtha Vidhyalaya at the **National Science Day** competition at **PRL**, Ahmedabad [2019]