ESC201: Introduction to Electronics **End-semester Exam** **18 Nov 2023**

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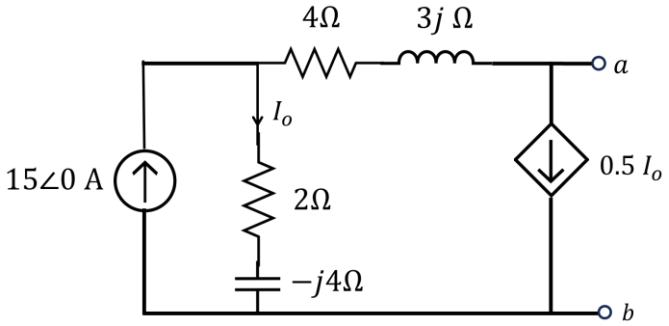
37 marks

Instructions:

1. Provide justification/steps for each solution. Answers without reasoning will be awarded 0 marks.
2. Answer questions in order. Answer all parts of a question at one place. Answers written in different order will not be graded.
3. Label x,y axis and other significant parameters in any plot you draw.
4. Feel free to make appropriate approximations in your calculations or assumptions in your analysis. But be sure to mention them clearly in your answer paper.

Question 1a **3 marks**

Compute Thevenin equivalent of this circuit as seen from the terminals a-b



Solutions

To compute open circuit voltage, let a-b are open. Then $V_{ab} = v_{th}$.

Applying KCL we get

$$15 = \mathbf{I}_o + 0.5\mathbf{I}_o \quad \Rightarrow \quad \mathbf{I}_o = 10 \text{ A}$$

Applying KVL to the loop on the right-hand side), we obtain

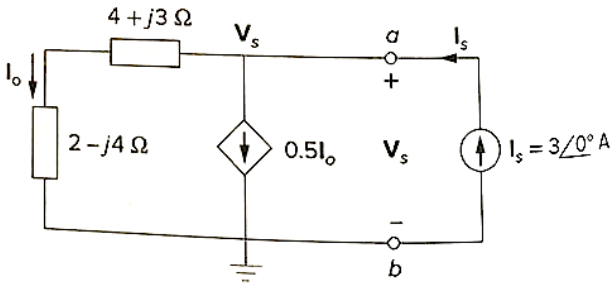
$$-\mathbf{I}_o(2 - j4) + 0.5\mathbf{I}_o(4 + j3) + \mathbf{V}_{\text{Th}} = 0$$

or

$$\mathbf{V}_{\text{Th}} = 10(2 - j4) - 5(4 + j3) = -j55$$

Thus, the Thevenin voltage is

$$\mathbf{V}_{\text{Th}} = 55\underline{/-90^\circ} \text{ V}$$



To obtain $\mathbf{Z}_{Th}$, we remove the independent source. Due to the presence of the dependent current source, we connect a 3-A current source (3 is an arbitrary value chosen for convenience here, a number divisible by the sum of currents leaving the node) to terminals a-b as shown in Fig. 10.26(b). At the node, KCL gives

$$3 = \mathbf{I}_o + 0.5\mathbf{I}_o \qquad \Rightarrow \qquad \mathbf{I}_o = 2\text{A}$$

Applying KVL to the outer loop in Fig. 10.26(b) gives

$$\mathbf{V}_s = \mathbf{I}_o(4 + j3 + 2 - j4) = 2(6 - j)$$

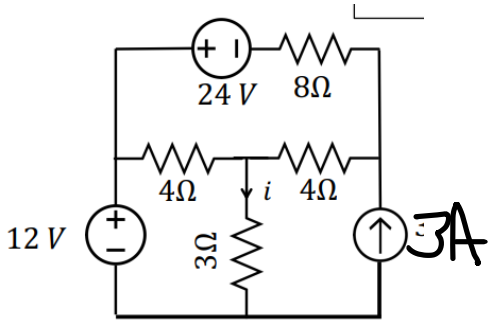
The Thevenin impedance is

$$\mathbf{Z}_{\text{Th}} = \frac{\mathbf{V}_s}{\mathbf{I}_s} = \frac{2(6-j)}{3} = 4 - j0.6667\ \Omega$$

Note that any other current source can be added. Or some one can use Is current and compute Vs in terms of Is.

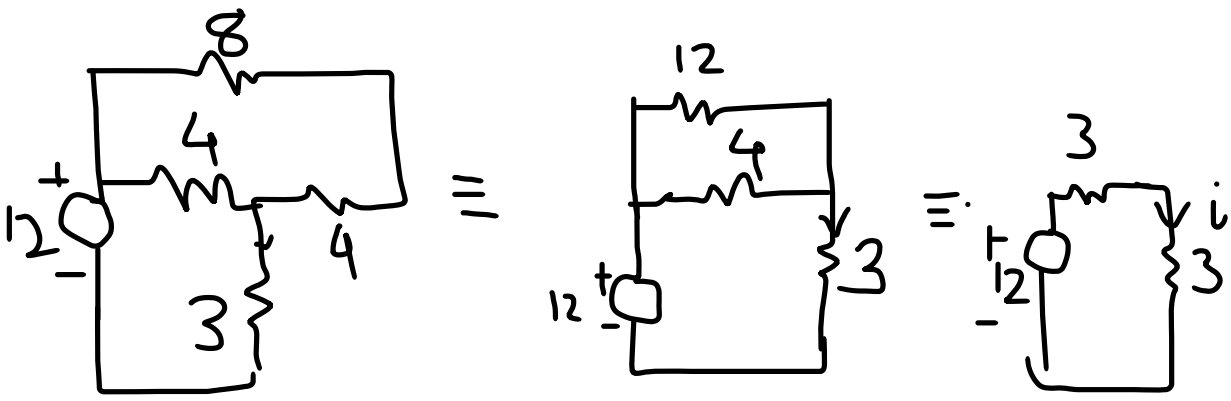
Question 1b **3 marks**

Use the superposition theorem to find i in the circuit given on the right.



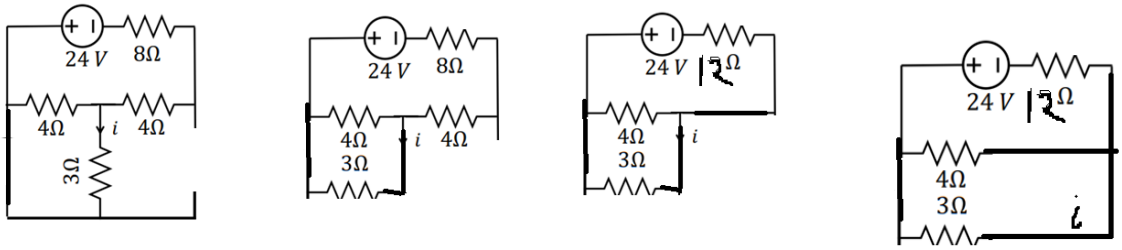
Solution

For 12 V source, keep 24V short and 3A open to get



So i=2

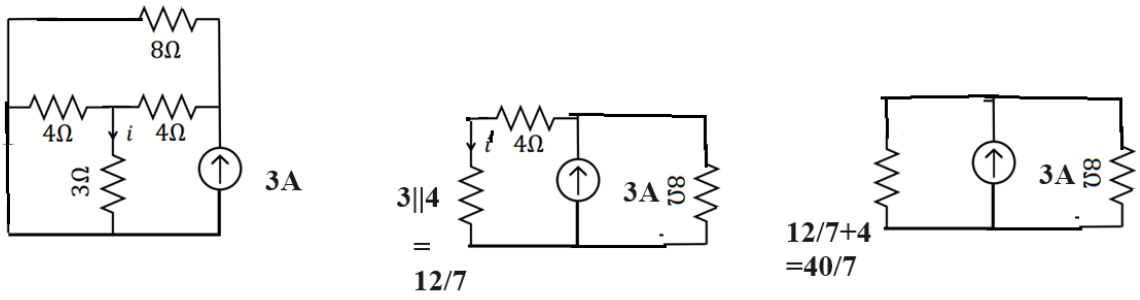
For 24 V



current is 24/(12+4||3)=24/(12+12/7)=2/(8/7)=7/4A

hence from current division, i=-7/4*4/(3+4) =-1A

For 3 A



From current division

i'=3* 8/(8+40/7)=3*(1+5/7)=3*7/12

again from current division

i=i'*4/7

i=3*7/12*4/7=1A

from superposition, total current i= 2-1+1=2A

Question 2a

Determine the voltage across the resistor in the circuit shown below. Assume that cut-in voltage of both diode and Zener diode is 0.7V and that Zener voltage is 3V.

2 marks

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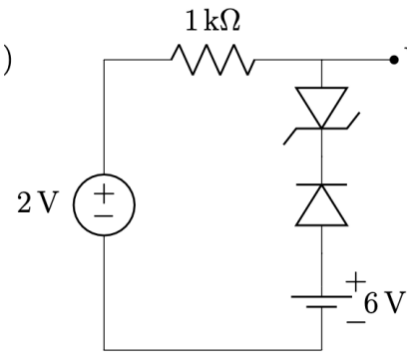


Solution

Let us assume that Diode D2 is forward biased. Assume Zener is like a 3V battery. The circuit can be written as

Let us calculate the current to check our assumption

$$-6+0.7+3+i\times10^{3}+2=0\Rightarrow i=0.3mA$$

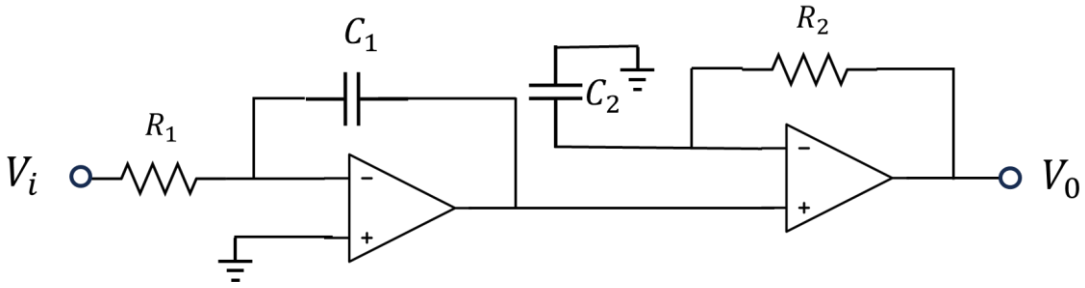
$$-6+0.7+3+v_o=0\Rightarrow v_o=2.3V$$

Hence, the assumption is correct.

The voltage across the resistor is 0.3V.

Question 2b **4 marks**

Write down the impedance model of the following circuit.



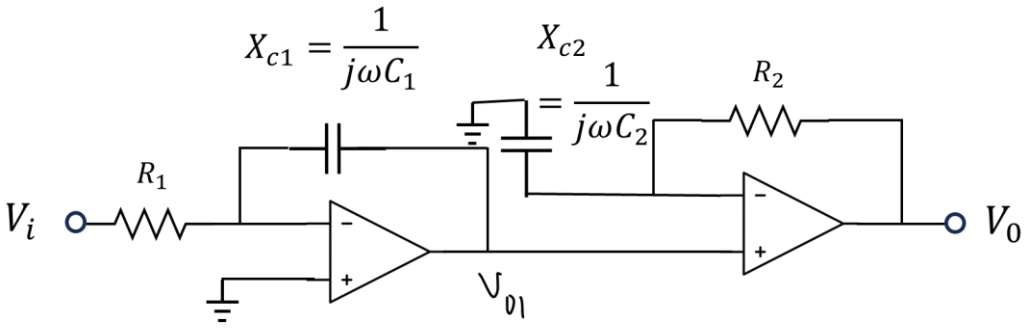
Using the impedance model, compute the frequency response of the circuit *ie* $\frac{V_o(\omega)}{V_i(\omega)}$.

Sketch its bode plot for $R_1C_1 = 10$ and $R_2C_2 = .01$. Mark all labels, slopes and axes.

Hint: The frequency response or the transfer function of a system is the ratio between output and input complex phasors.

Solution

Impedance model is



After first part

$$V_{o1} = -V_i\frac{X_{c1}}{R_1}$$

After second part

$$V_o = V_{o1}\left(1+\frac{R_2}{X_{c2}}\right)$$

Total

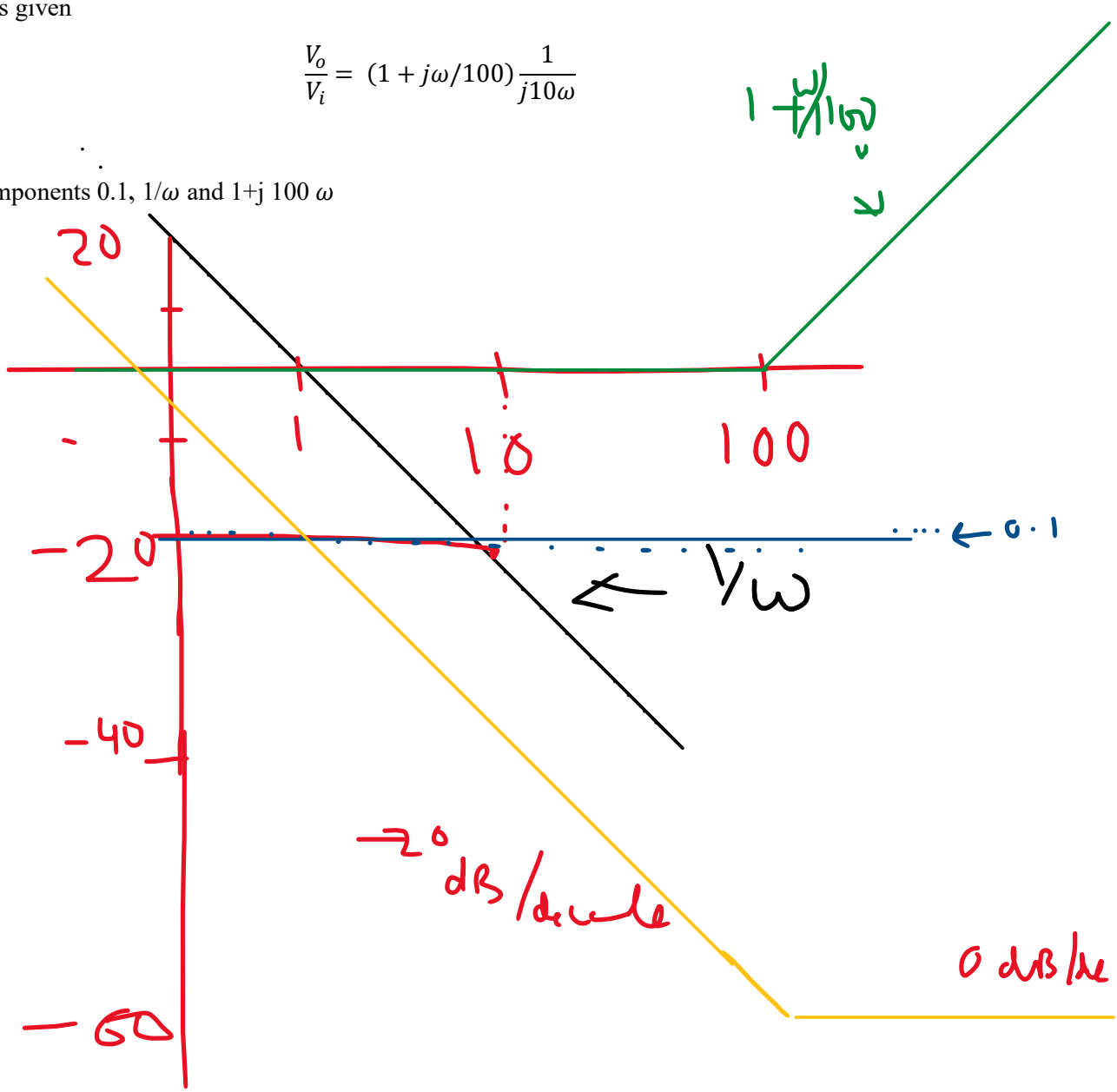
$$V_o = -V_i \left(1 + \frac{R_2}{X_{c2}}\right)\frac{X_{c1}}{R_1}$$

$$\frac{V_o}{V_i} = -\left(1 + \frac{R_2}{X_{c2}}\right)\frac{X_{c1}}{R_1} = -(1 + j\omega R_2 C_2)\frac{1}{j\omega C_1 R_1}$$

For values given

$$\frac{V_o}{V_i} = (1 + j\omega/100)\frac{1}{j10\omega}$$

Three components 0.1, 1/ω and 1+j 100 ω



Question 3a **4 marks**

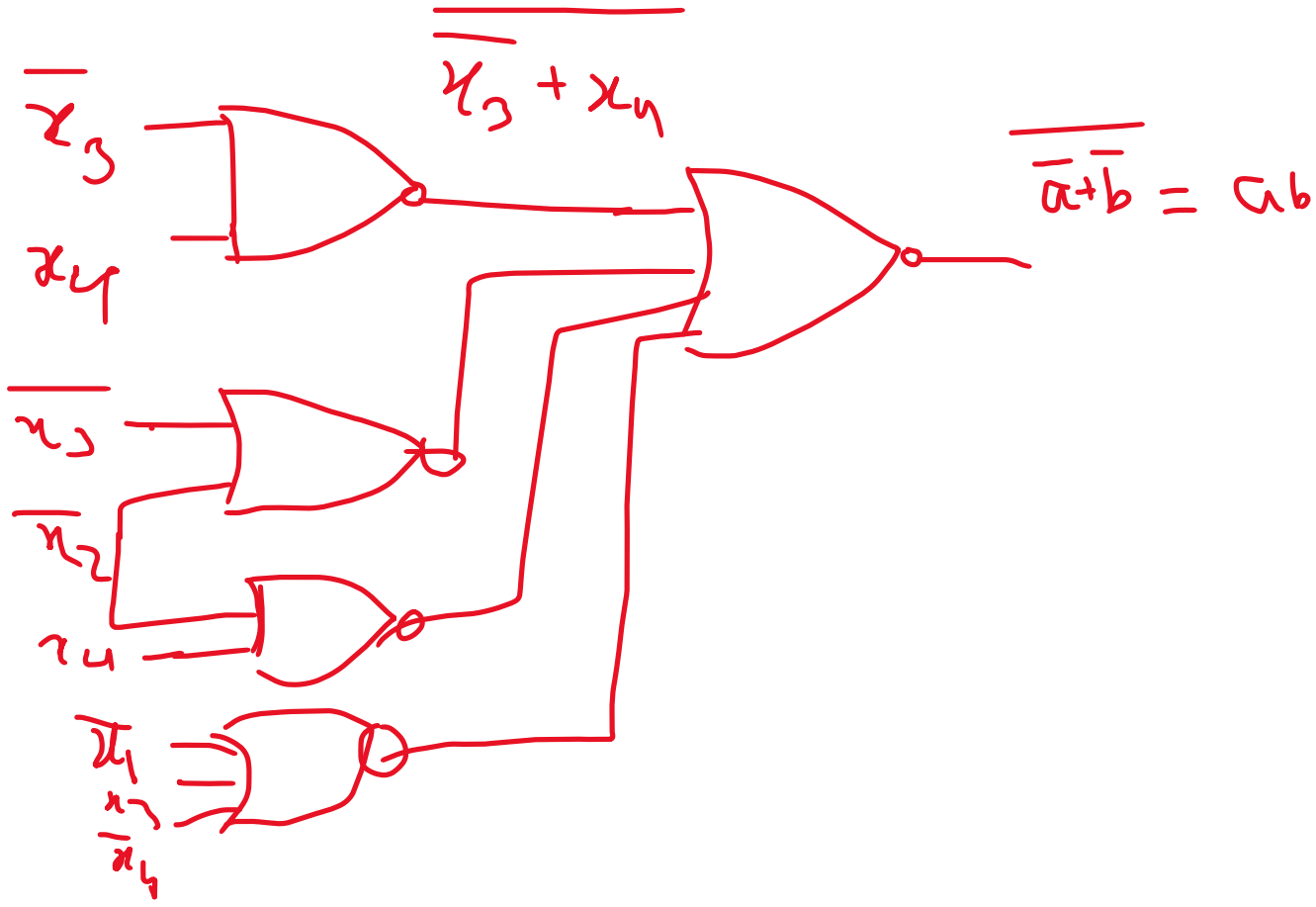
Determine the minimized product of sum (**PoS**) expression for the K-map shown below. Implement this expression using only NOR gates. Assume that complements of input variables are also available and need not be generated using gates.

x_1x_2 \ x_3x_4	00	01	11	10
00	1	1	1	0
01	0	1	0	0
11	0	0	0	0
10	1	0	1	0

Solution

x_1x_2 \ x_3x_4	00	01	11	10
00	1	1	1	0
01	0	1	0	0
11	0	0	0	0
10	1	0	1	0

$$F = (\overline{x_3} + x_4).(\overline{x_3} + \overline{x_2}).(x_4 + \overline{x_2}).(\overline{x_1} + x_3 + \overline{x_4})$$



4 marks

Question 3b

In this question, we will make a digital circuit which extract kth bit of a given n-bit number

Consider a 3-bit number A.

Consider a 2-bit number S which represents decimal number k (from 0 to 3).

Output Y is the kth bit of A, if k>0, otherwise Y=0.

Write down the truth table of Y for all possible values of S.

Find out the SOP Boolean expression of Y.

Implement the expression using 4x1 Multiplexer

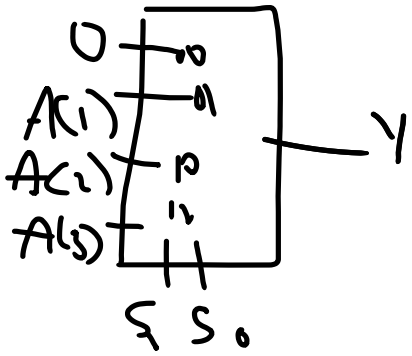
Solutions:

The truth table is

S_1	S_0	Y
0	0	0
0	1	A[1]
1	0	A[2]
1	1	A[3]

The Boolean Expression is

$$Y = A[1]\,\overline{S_1}S_0 + A[2]\,\overline{S_0}S_1 + A[3]\;\;S_0S_1$$



4 marks

Question 4a)

Design a counter using 3 T flip-flops such that it generates the following sequences of state $Q_AQ_BQ_C$ (010,110,001,011,010). Consider all unused states as "Don't care". Clearly mention the flip-flops, show different components of the design, the simplified expressions for the T inputs of the flip flops.

Previous State			Next state			TA	TB	TC
A	B	C	A	B	C			
0	1	0	1	1	0	1	0	0
1	1	0	0	0	1	1	1	1
0	0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	0	1

Using KMaps

1. TA

BC\A	0	1
00	x	x
01	0	x
11	0	x
10	1	1

TA= $\bar{C}$

2. TB

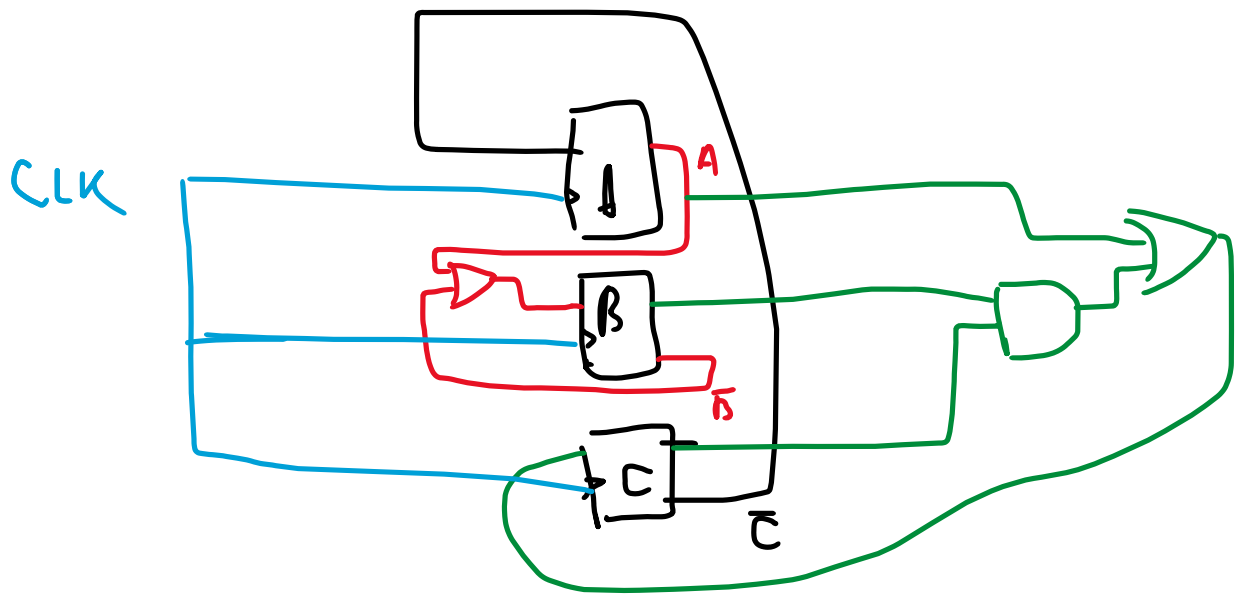
BC\A	0	1
00	x	x
01	1	x
11	0	x
10	0	1

TB= $\bar{B} + A$

3. TC

4. BC\A	0	1
00	x	x
01	0	x
11	1	x
10	0	1

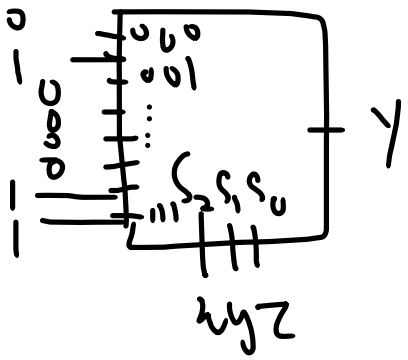
TC= $BC + A$



Question 4b **3 marks**

Implement the following logic using 8x1 multiplexer with x,y,z as the control inputs.

$$u = xy + \bar{x}\,\bar{y}\,z$$



Question 5a **4 marks**

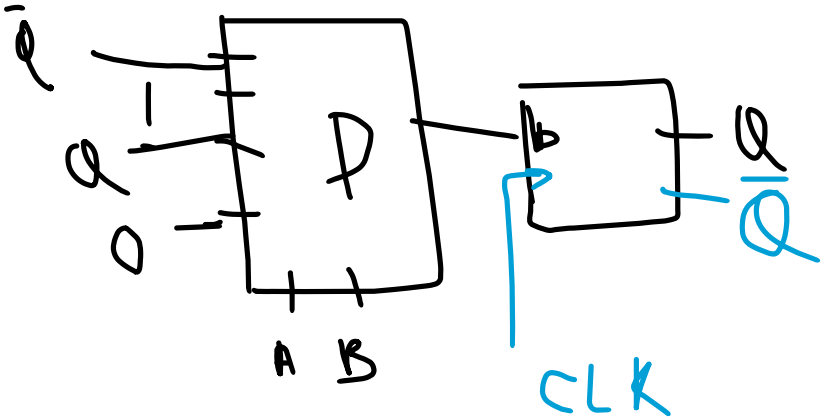
Consider a new type of Flip-flop with two inputs A and B whose characteristic table is as follows.

Write down its excitation table. Then implement the flip-flop using a D flip-flop and a 4 to 1 multiplexer

A	B	Q
0	0	$\overline{Q_n}$
0	1	1
1	0	Q_n
1	1	0

Qn	Qn+1	A	B
0	0	1	X
0	1	0	X
1	0	0 1	0 1
1	1	1 0	0 1

Multiplexer



Question 5b

2 marks

Write down the typical stages in processor running an instruction e.g. ADD A=B, C

1. first the instruction is fetched from the memory.

2. then the instruction is decoded.

3. then B and C will be read from the memory.

4. Execute instruction will compute B+C

5. Answer is written back to the memory at the address of A

Question 5c

2 marks

Explain why do we break the process into stages compared to having a single stage implementing all calculations.

To save computation cycles.

If a single stage is used, then next instruction can only run after previous instruction is completed.

When multiple stages are used, each stage can handle a different instruction, leading to a pipeline.

Pipelining refers to the use of each stage by a different instruction in the following order. Pipelining attempts to keep every part of the processor busy with some instruction by dividing incoming instructions into a series of sequential steps by different processor units with different parts of instructions processed in parallel.

d.

2 marks

What does processor access memory?

Via a Bus such as AXI. On axi bus there is a master and there is a slave. When processor wants to read something, it turns on the axi address and read control signal. The device at this address responds with the corresponding data and read valid.

Similarly axi write also occurs.