ESC201A EndSem Part 3

RAGHAV SHUKLA

TOTAL POINTS

10 / 20

QUESTION 1

Q1 10 pts

1.1 1(a) 1 / 2

+ 2 pts Completely Correct

✓ **+ 0 pts** *Completely Incorrect*

+ 0 pts Not Attempted

+ 0 pts Copied

+ 1 *Point adjustment*

1.2 1(b) 3 / 3

+ 3 pts Completely Correct

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

✓ **+ 1 pts** *Correct number of 1 to 2 decoders used*

✓ **+ 2 pts** *Final implementation correct*

1.3 1(c) 4 / 5

+ 5 pts Completely Correct

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

✓ **+ 2 pts** *Minimized PoS expression correct*

+ 3 pts Final implementation using 2-input NOR gates correct

+ 2 *Point adjustment*

QUESTION 2

Q2 10 pts

2.1 2(a) 2 / 4

+ 4 pts Completely Correct

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

✓ **+ 2 pts** *Excitation table correct*

+ 2 pts Final implementation correct

2.2 2(b) 0 / 6

+ 6 pts Completely Correct

+ 0 pts Completely Incorrect

✓ **+ 0 pts** *Not Attempted*

+ 0 pts Copied

+ 1 pts Counter states and transitions correctly identified

+ 3 pts Assignment to D inputs of the two flip flops correct

+ 2 pts Final implementation schematic correct

Name: RAGHAV SHUKLA | Roll No.: 210800 | Seat/Room No.: 260 / L19

1 (a). Prove using basic postulates of Boolean algebra that $x+\bar{x}.y = x+y$. [2]

R.H.S = $x+y = (x+y).(x+\bar{x})$ [$\because x+\bar{x}=1$ and $(x+y).1 = x+y$]

$= x.x + x.\bar{x} + y.x + y.\bar{x}$ [Distributivity over multiplication]

$= x.x + (x.x + x.\bar{x}) + (x.x + y.x) + (y.\bar{x})$

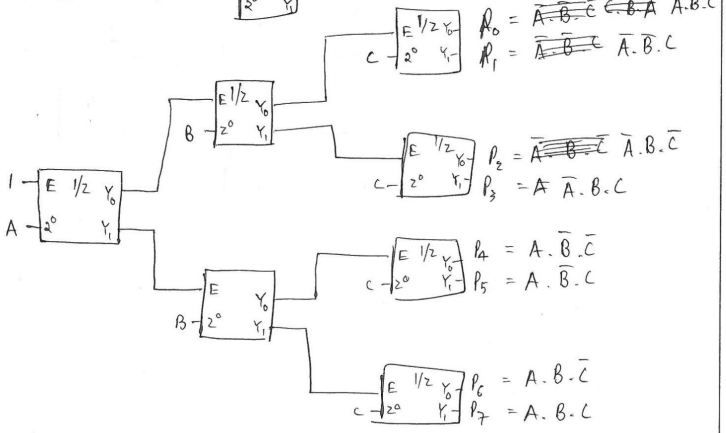
$= x.x + x(x+\bar{x}) + x(1+y) + y.\bar{x}$ [$x.x = x$, $1+y=1$]

$= x + x + x + y.\bar{x} = x + y.\bar{x} =$ L.H.S [$x+x=x$]

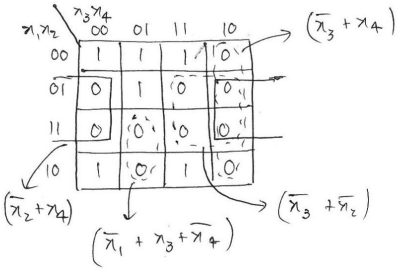
~~Also, $p+qr = (p+q)(p+r)$~~

1(b). Implement a 3 to 8 decoder using only 1 to 2 decoders. Assume that each decoder has an enable signal. Label all the input and output lines. [3]

Standard Decoder ≡ 



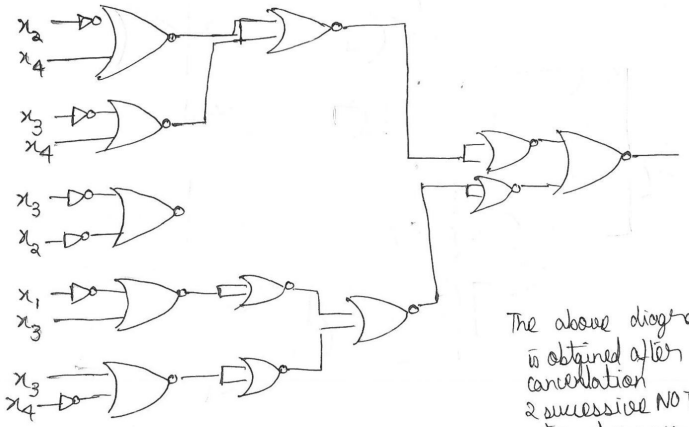
1(c). Determine the minimized product of Sum (PoS) expression for the K-map shown below and implement using only 2-input NOR gates. Assume that complements of input variables are also available and need not be generated using gates. [5]



X_1X_2 \ X_3X_4	00	01	11	10
00	1	1	1	0
01	0	1	0	0
11	0	0	0	0
10	1	0	1	0

Minimised POS expression = $(\bar{x}_2 + x_4).(\bar{x}_3 + x_4).(\bar{x}_3 + \bar{x}_2).(\bar{x}_1 + x_3 + \bar{x}_4)$

~~A POS This POS expression corresponds to a OR-AND network.~~



The above diagram is obtained after cancellation 2 successive NOT gates wherever encountered.

2(a). For the Flip-flop with two inputs A and B whose characteristic table is shown below, determine first the excitation table and then implement the flip-flop using a D flip-flop and a 4 to 1 multiplexer. [4]

A	B	Q(t+1)	State
0	0	1	Set
0	1	$\overline{Q(t)}$	Toggle
1	0	0	Reset
1	1	Q(t)	Hold

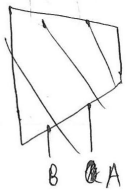
Excitation table

Q(t)	Q(t+1)	A & B	D
0	0	1 X	0
0	1	0 X	1
1	0	01 or 10	0
1	1	00 or 11	1

We want $D = f(A, B, Q)$

observe that when $Q = 0$, $D = \overline{A}$

$Q = 1$, $D = A \cdot B + \overline{A} \cdot \overline{B} = A \odot B$



2(b). Design a synchronous circuit using D flip-flops that can produce the outputs y_0 and y_1 from a clock input X as shown below. The output sequence repeats after the dotted line shown below. [6]