Experiment 8
Waveshaping

Introduction

The following is a collection of simple circuits that shape the input signal in various ways. Some use operational amplifier for this purpose, while the others are built using basic nonlinearities such as available in the diode. We assume here that you are already familiar with using the op amp in both linear and nonlinear configurations.

1. Diode Parallel Clipper

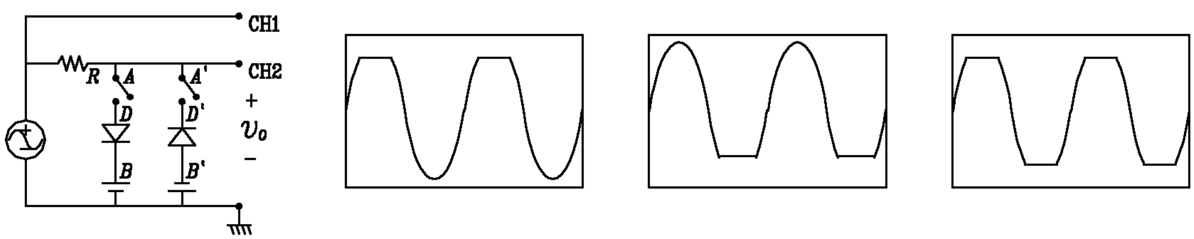


Figure 1

Specs: supply 15V p-p 1kHz sine; V_B and $V_{B'}$ (5±1)V; R = 4.7kΩ

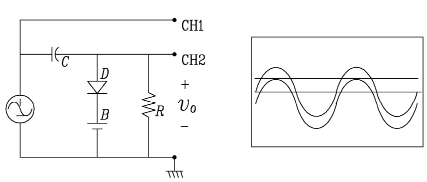
Construct the circuit in the diagram shown in Fig.1. A and A′ are supposed to be switches, but all you need is a jumper that you can disconnect or connect at will. D1 and D2 are identical diodes, B and B′ dc voltages that determine the behavior of the clipper circuit and R is chosen as 4.7kΩ. Its primary purpose is to limit the circuit current. **Take extreme care with the diode and dc voltage polarities: getting them wrong will burn many things including the diodes at once, when you switch on.** Initially, keep A closed and A′ open.

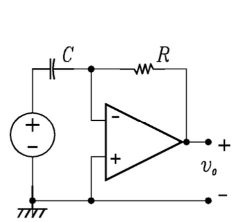
Set the FG to a sinusoid, 1kHz, 15V p-p, and set B to 5V (B can be drawn from the 5V section of the dc power supply unit on your desk). Exhibit both the input and output signals on the DSO. Vary B over the permitted range of 4.5-5.5V and see the effect on the output. Sketch input and output waveforms at B = 5V.

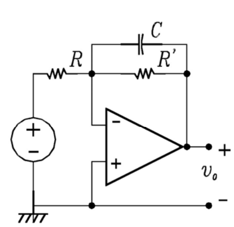
Now open A, close A′, use the same dc supply (with appropriately reversed polarity) as B′. Repeat the observations.

Finally, close both A and A′, Provide B from the 30V part of the desktop dc power supply unit, after adjusting the value to 4V. Now both parallel paths are simultaneously present. Display and sketch the input and output waveforms.

2. Diode Clamper







Clamper Differentiator Integrator

Figure 2

Specs: supply 15V p-p 1kHz sine; C = 0.1μF; V_B = -5V to +5V; R = 1kΩ

The clamper circuit is shown in the first diagram of Fig.2. Its function is to provide a constant vertical shift to the signal. If we assume for simplicity that B = 0V, to begin with, this is achieved for the input sinusoid of 1 kHz, 10V p-p as follows: initially C is uncharged, and as the input sinusoidal voltage rises from zero, C charges up almost instantaneously through the very small forward diode resistance.

If R were absent, the output remains at 0V for the first quarter cycle of the sinusoid, while C keeps charging up. When the input begins to fall after the peak, the diode turns off, and the output becomes $v_i(t) - v_C(T/4) = v_i(t) - V_m$, which is the input – its peak value. Since the capacitor never gets a chance to discharge later, the output remains at $v_i(t) - V_m$. This is effectively a shift (downward) of the input by V_m. If B were set at some voltage, say V_0, the capacitor begins charging only when the input exceeds V_0, and charges up to $V_m - V_0$. This results in a vertical shift of the output by V_0 as shown in the adjoining figure.

Finally, the role of the resistor R is to bleed the capacitor at a slow rate compared to the period of the signal so that the clamper can respond, at least gradually, to input signal level changes. Too low a value for RC would impede the clamping operation, as the capacitor voltage would begin to follow the input even within the cycle. Sketch the input and output waveforms.

3. Op-amp Based Integrator and Differentiator

Specs: (integrator): supply 4V p-p 25kHz square; R = 10kΩ; R′ = 100kΩ; C = 0.01μF

(differentiator): supply 4V p-p 1kHz triangular; R = 1kΩ; C = 0.1μF

These circuits use op-amps (see schematics adjoining the clamper in Fig.2) to improve upon the less than ideal behavior of the earlier attempted integrators and differentiators (Expt.3).

The right-hand side of the capacitor is held to a voltage of 0 volts, due to the "virtual ground" effect. Therefore, current "through" the capacitor is solely due to *change* in the input voltage. A steady input voltage won't cause a current through C, but a *changing* input voltage will.

Capacitor current moves through the feedback resistor, producing a drop across it, which is the same as the output voltage. A linear, positive rate of input voltage change will result in a steady negative voltage at the output of the op-amp. Conversely, a linear, negative rate of input voltage change will result in a steady positive voltage at the output of the op-amp. This polarity inversion from input to output is due to the fact that the input signal is being sent (essentially) to the inverting input of the op-amp, so it acts like the inverting amplifier mentioned previously. The faster the rate of voltage change at the input (either positive or negative), the greater the output voltage, which is consistent with differentiation. The formula for determining voltage output for the differentiator is: $v_o = -RC\, dv_i/dt$

In the case of the integrator, the op-amp circuit would generate an output voltage proportional to the magnitude and duration that an input voltage signal has deviated from 0 volts. Stated differently, a constant input signal would generate a certain *rate of change* in the output voltage: differentiation in reverse. To do this, all we have to do is swap the capacitor and resistor in the previous circuit:

As before, the negative feedback of the op-amp ensures that the inverting input will be held at 0 volts (the virtual ground). If the input voltage is exactly 0 volts, there will be no current through the resistor, therefore no charging of the capacitor, and therefore the output voltage will not change. We cannot guarantee what voltage will be at the output with respect to ground in this condition, but we can say that the output voltage *will be constant*. In real situations, it often happens that the source signal is never exactly zero, and this causes the output to drift steadily towards one of the (positive or negative) saturation points, never to return. To prevent this, without impeding the integrator like behavior, a rather large resistor, (say 22kΩ) across the capacitor is recommended to reduce the effects of integration drift (not shown in the figure).

If we apply a constant, positive voltage to the input, the op-amp output will fall negative at a linear rate, in an attempt to produce the changing voltage across the capacitor necessary to maintain the current established by the voltage difference across the resistor. Conversely, a constant, negative voltage at the input results in a linear, rising (positive) voltage at the output. The output voltage rate-of-change will be proportional to the value of the input voltage. The formula for determining voltage output for the integrator is as follows: $dv_o/dt = -v_i(t)/RC$, so that vo(t) = $v_o(t) = v_o(0) + \frac{-1}{RC}\int_0^t v_i(t)dt$.

4. Op-amp Based Astable Multivibrator

Specs: no supply; $C = 1\mu F$; R = 10kΩ; R_1 = 10kΩ; R_2 = 4.7kΩ; ; R'_2 = 10kΩ pot.

An astable multivibrator (Fig.3) is a circuit that repeatedly moves between two states as long as it is powered up. The given circuit works as follows. Unlike in a linear op-amp circuit, this op-amp is always saturated, either at $+V_{sat}$ or at $-V_{sat}$. If we denote $R_1/(R_1+R_2+R'_2)$ by k, then $v_+ = kv_o$. Suppose at some time, $v_o = +V_{sat}$. Since the inverting terminal cannot supply or sink any current, the capacitor charges through R, causing v_- to rise towards $+V_{sat}$. In the process, v_- is bound to cross $v_+ = kV_{sat}$ at some time. When it does so, the output switches to $-V_{sat}$, causing the capacitor to begin charging in the opposite direction, towards $-V_{sat}$. This, again, it does, until v_- crosses $v_+ = -kV_{sat}$. Hence, the capacitor voltage executes an approximation of a sawtooth, as it repeatedly charges and discharges to approach $+V_{sat}$ and $-V_{sat}$, alternately. At the output is seen the alterrnation of v_o from $+V_{sat}$ to $-V_{sat}$. Manipulating k by controlling the R'_2 potentiometer changes the switching voltages, which in turn has a slight effect upon the frequency of the oscillation. A more direct effect upon the oscillation frequency results from changing the values of R and C: this changes the time constant RC of the charging curve. Observe the changes in the capacitor voltage and output waveforms under manipulation of ***k*** through the potentiometer, and under the change of R and C. Sketch the capacitor and op-amp output waveforms.

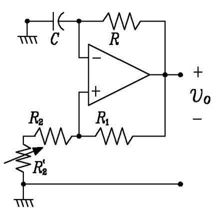


Figure 3