ESC201A EndSem Part 3

SHIV NARAYAN

TOTAL POINTS

16 / 20

QUESTION 1

Q1 10 pts

1.1 1(a) **2 / 2**

✓ **+ 2 pts** *Completely Correct*

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

1.2 1(b) **0 / 3**

+ 3 pts Completely Correct

✓ **+ 0 pts** *Completely Incorrect*

+ 0 pts Not Attempted

+ 0 pts Copied

+ 1 pts Correct number of 1 to 2 decoders used

+ 2 pts Final implementation correct

1.3 1(c) **5 / 5**

+ 5 pts Completely Correct

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

✓ **+ 2 pts** *Minimized PoS expression correct*

✓ **+ 3 pts** *Final implementation using 2-input NOR gates correct*

QUESTION 2

Q2 10 pts

2.1 2(a) **3 / 4**

+ 4 pts Completely Correct

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

✓ **+ 2 pts** *Excitation table correct*

+ 2 pts Final implementation correct

+ 1 *Point adjustment*

Final implementation is partially correct

2.2 2(b) **6 / 6**

✓ **+ 6 pts** *Completely Correct*

+ 0 pts Completely Incorrect

+ 0 pts Not Attempted

+ 0 pts Copied

+ 1 pts Counter states and transitions correctly identified

+ 3 pts Assignment to D inputs of the two flip flops correct

+ 2 pts Final implementation schematic correct

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1 (a). Prove using basic postulates of Boolean algebra that $x+\bar{x}.y = x+y$. [2]

We know $x + x.y = x$ as $x.(1+y) = x.1 = x$ $\quad 1+y = 1$ Always

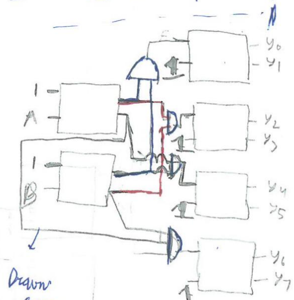
replacing x

$x + x.y + \bar{x}.y \Rightarrow x + y(x+\bar{x}) = x+y = RHS$

LHS $\quad x+\bar{x} = 1$ Always

1(b). Implement a 3 to 8 decoder using only 1 to 2 decoders. Assume that each decoder has an enable signal. Label all the input and output lines. [3]

E	A	B	C	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1							
1	0	0	1		1						
1	0	1	0			1					
1	0	1	1				1				
1	1	0	0					1			
1	1	0	1						1		
1	1	1	0							1	
1	1	1	1								1



Drawn from behind for clarity

1(c). Determine the minimized product of Sum (PoS) expression for the K-map shown below and implement using only 2-input NOR gates. Assume that complements of input variables are also available and need not be generated using gates. [5]

X_1X_2 \ X_3X_4	00	01	11	10
00	1	1	1	0
01	0	1	0	0
11	0	0	0	0
10	1	0	1	0

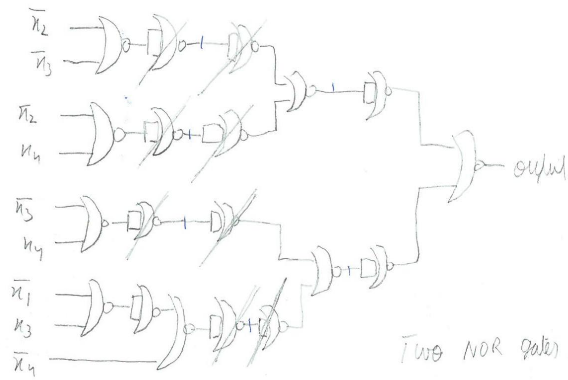
Using ① $\Rightarrow (\bar{X}_2 + \bar{X}_3)$

Using ② $\Rightarrow (X_4 + \bar{x}_2)$

Using ③ $\Rightarrow \bar{X}_3 + X_4$

Using 4 $\Rightarrow \bar{x}_1 + x_3 + \bar{x}_4$

So minimised POS = $(\bar{x}_1+x_3+\bar{x}_4).(\bar{x}_3+x_4).(x_4+\bar{x}_2)(\bar{x}_2+\bar{x}_3)$



Two NOR gates cancel as wires

2(a). For the Flip-flop with two inputs A and B whose characteristic table is shown below, determine first the excitation table and then implement the flip-flop using a D flip-flop and a 4 to 1 multiplexer. [4]

A B	Q(t+1)	State
0 0	1	Set
0 1	$\overline{Q}(t)$	Toggle
1 0	0	Reset
1 1	Q(t)	Hold

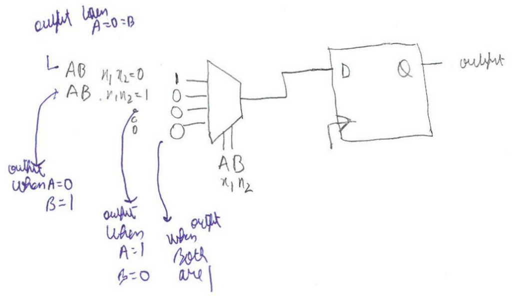
Q(t)	Q(t+1)	A B	D
0	0	1 X	0
0	1	0 X	1
1	0	0 1 / 1 0	0
1	1	0 0 / 1 1	1

$Q\overline{D} + QD$

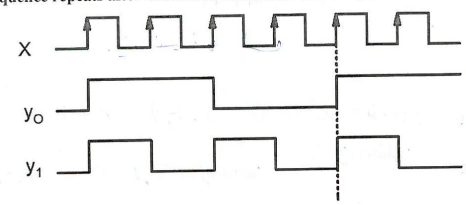
~~A = 2QB~~
~~B = 2QB~~

$D = \overline{Q}\,\overline{A}\,\overline{B} + Q\,\overline{A}\,\overline{B}$
$= \overline{A}\,\overline{B}$

A B	$\overline{A}\,\overline{B}$
0 0	1
0 1	0
1 0	0
1 1	0



2(b). Design a synchronous circuit using D flip-flops that can produce the outputs y_0 and y_1 from a clock input X as shown below. The output sequence repeats after the dotted line shown below. [6]

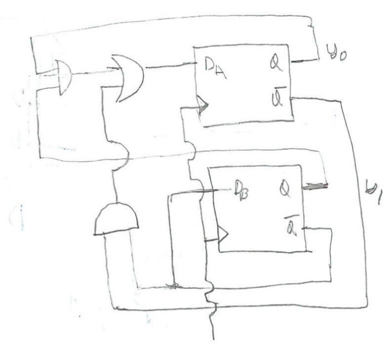


$=y_0$ A	$=y_1$ B
1	1
1	0
0	1
0	0

Present state AB	Next state AB	D_A	D_B
11	10	1	0
10	01	0	1
01	00	0	0
00	11	1	1

00 = 1
10 = 0
01 = 0
11 = 1

$D_A = A \cdot B + \overline{A}\,\overline{B}$
$D_B = A\overline{B} + \overline{A}\,\overline{B} = \overline{B}$



$A \cdot B + \overline{A}\,\overline{B} = A\overline{B} + \overline{A}B$
$B(A - \overline{A}) = \overline{B}(A - \overline{A})$
$(A - \overline{A})(B - \overline{B})$