M-3-4-B1: Design and implement the following using, (i) logisim (do not use inbuilt adder, subtractor, mux, dmux, etc. other than logic gates) (ii) Verilog (gate modelling, dataflow modelling and behavioral modelling) (**Note:** File naming should be done as, 16CO226-L4.circ (for logisim), 16CO226-VG4.v (for gate modelling), 16CO226-VD4.v (for dataflow modelling), 16CO226-VB4.v (for behavioral modelling), 16CO226-V4.v (input/data file along-with $monitor for input and output) and 16CO226-V4.vcd (for waveform))

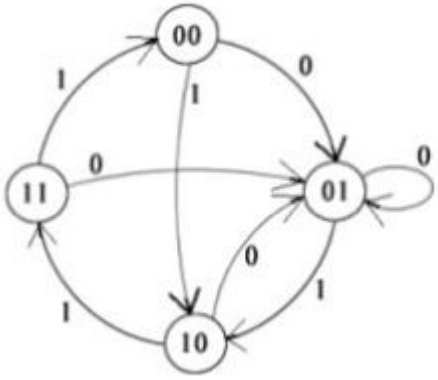
(i) 4-bit register with parallel load using D flip-flop

(ii) A sequential circuit with registers whose state table is as shown below

Present state		Input	Next state	
A_1	A_2	x	A_1	A_2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

(iii) A counter with the following binary sequence 0, 8, 5, 3, 7, 2 and repeat using T flip flop.

(iv) A counter with the following state diagram



Q. No.	Reg. No.
(i)	16CO101 - 16CO112
(ii)	16CO113 - 16CO123
(iii)	16CO124 - 16CO134
(iv)	16CO135 - 16CO145