ECE 272 Lab 3
Fall 2018

Combinational Logic (Seven-Segment Driver)

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1 Introduction

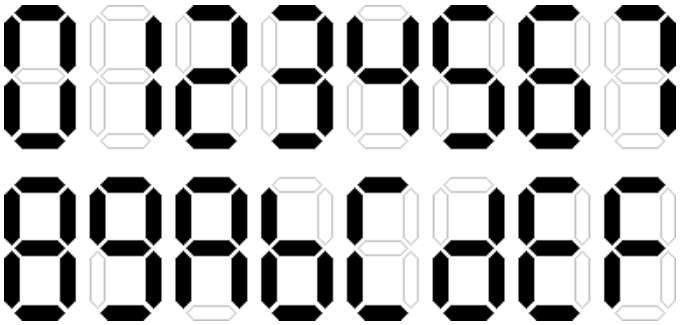

Figure 1: Seven-segment display showing hexadecimal digits [1]

2 Design

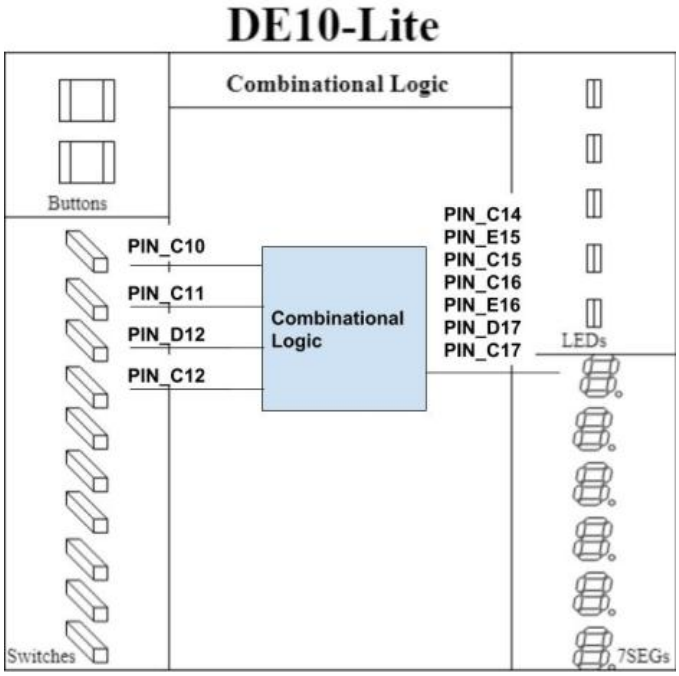

Figure 2: Block diagram

Seg_A

CD \ AB	00	01	11	10
00	0	(1)	0	0
01	(1)	0	(1)	0
11	0	0	0	(1)
10	0	0	0	0

$Seg_A = \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}\overline{D} + AB\overline{C}D + A\overline{B}CD$

Seg_B

CD \ AB	00	01	11	10
00	0	0	(1)	0
01	0	(1)	0	0
11	0	0	1	1
10	0	(1)	(1)	0

$Seg_B = BC\overline{D} + ACD + AB\overline{D} + \overline{A}B\overline{C}D$

Seg_C

CD \ AB	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	0	0	1	0
10	(1)	0	1	0

$Seg_C = ABC + AB\overline{D} + \overline{A}B\overline{C}D$

Seg_D

CD \ AB	00	01	11	10
00	0	(1)	0	0
01	(1)	0	0	0
11	0	(1)	(1)	0
10	0	0	0	(1)

$Seg_D = BCD + \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D} + A\overline{B}C\overline{D}$

Seg_E

CD \ AB	00	01	11	10
00	0	(1)	0	0
01	(1)	(1)	0	(1)
11	(1)	(1)	0	0
10	0	0	0	0

$Seg_E = \overline{A}D + \overline{A}B\overline{C} + \overline{B}C\overline{D}$

Seg_F

CD \ AB	00	01	11	10
00	0	0	0	0
01	(1)	0	(1)	0
11	(1)	(1)	0	0
10	1	0	0	0

$Seg_F = \overline{A}CD + \overline{A}B\overline{D} + \overline{A}B\overline{C} + AB\overline{C}D$

Seg_G

CD \ AB	00	01	11	10
00	(1)	0	(1)	0
01	(1)	0	0	0
11	0	(1)	0	0
10	0	0	0	0

$Seg_G = \overline{A}\overline{B}\overline{C} + \overline{A}BCD + AB\overline{C}\overline{D}$

Input (Hexadecimal)	Input (4-bit Binary)	$\mathbf{Seg_A}$	$\mathbf{Seg_B}$	$\mathbf{Seg_C}$	$\mathbf{Seg_D}$	$\mathbf{Seg_E}$	$\mathbf{Seg_F}$	$\mathbf{Seg_G}$
0	0000	0	0	0	0	0	0	1
1	0001	1	0	0	1	1	1	1
2	0010	0	0	1	0	0	1	0
3	0011	0	0	0	0	1	1	0
4	0100	1	0	0	1	1	0	0
5	0101	0	1	0	0	1	0	0
6	0110	0	1	0	0	0	0	0
7	0111	0	0	0	1	1	1	1
8	1000	0	0	0	0	0	0	0
9	1001	0	0	0	0	1	0	0
a	1010	0	0	0	1	0	0	0
b	1011	1	1	0	0	0	0	0
c	1100	0	1	1	0	0	0	1
d	1101	1	0	0	0	0	1	0
e	1110	0	1	1	0	0	0	0
f	1111	0	1	1	1	0	0	0

Table 1: Conversion table between hexadecimal, 4-bit binary, and seven-segment decoder

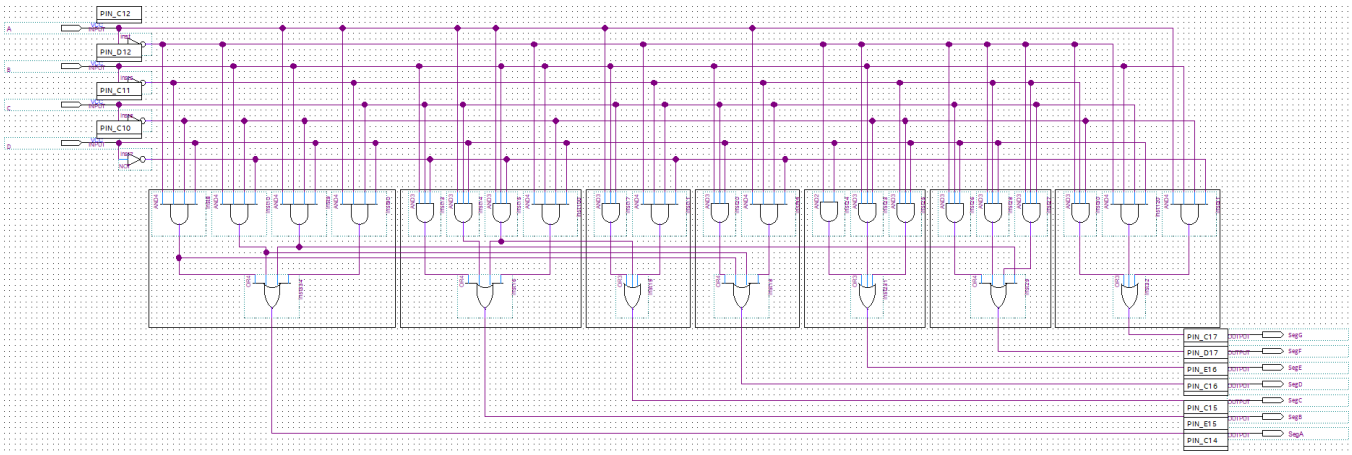

Figure 3: A schematic for the seven-segment display decoder. Due to the large difference between the size of the schematic and the available space, an image with higher resolution has been uploaded here.

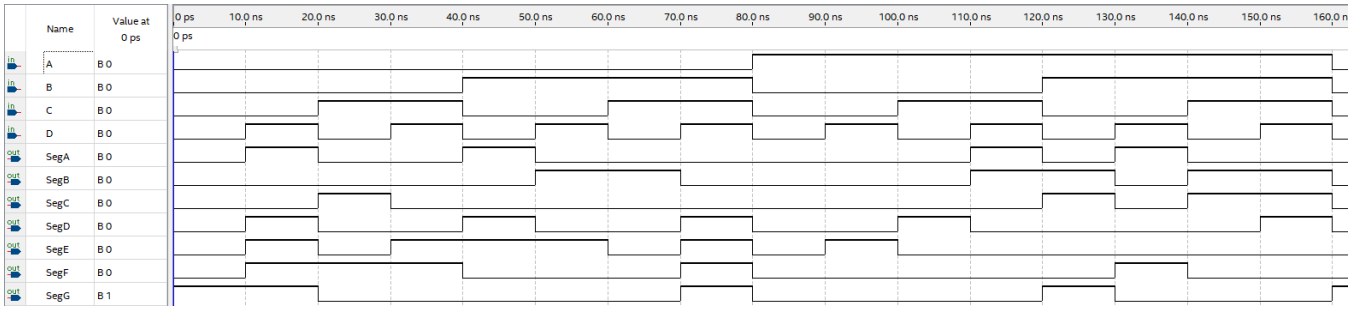

Figure 4: Simulation waveform of the program with each 10-nanosecond interval representing a hexadecimal digit

3 Results

4 Experiment Notes

Reflection

Study Questions

1. When is a simulation necessary? Was it useful for this section?

Appendix

No appendix is available in this lab.

References

[1] E. E. S. Exchange, "Hex to 7 segment decoder for a common anode 7 seg display." https://electronics.stackexchange.com/questions/373034/hex-to-7-segment-decoder-for-a-common-anode-7-seg-display, 2018.