

ECE 272 Pre-Lab 4
Fall 2018

System Verilog and Complex Projects
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Lab 4 is the first lab implemented with a hardware description language. For this class, we will be using System Verilog. Take a look at chapter 4 of the textbook and answer the following questions:

1. In your own words, what is a module?

A module is a standalone subsystem with inputs, outputs, and internal structures. It acts like a black box and can connect with other modules to make up a grand system that serves particular purposes.

2. What is a Bus? How do you designate one in System Verilog?

A Bus is a single wire running across a common signal of all—for example, modules—and connecting each of the signal into that wire. I think of the bus seats as the common signal of the modules and the bus floor as the Bus wire connecting all signals into a single Bus signal.

In Verilog, a Bus can be designated by being connected to multiple signal across the system.

3. What does the term Logic mean in System Verilog?

A *Logic* in Verilog can be used either as a *wire* or as a *register*. Logic blocks are generally busses, and the way they are used determines whether they are wires or registers.