

ECE 272 Pre-Lab 4
Fall 2018

System Verilog and Complex Projects
Phi Luu

October 24th, 2018
Grading TA: Edgar Perez

Lab 4 is the first lab implemented with a hardware description language. For this class, we will be using System Verilog. Take a look at chapter 4 of the textbook and answer the following questions:

1. In your own words, what is a module?
2. What is a Bus? How do you designate one in System Verilog?
3. What does the term Logic mean in System Verilog?