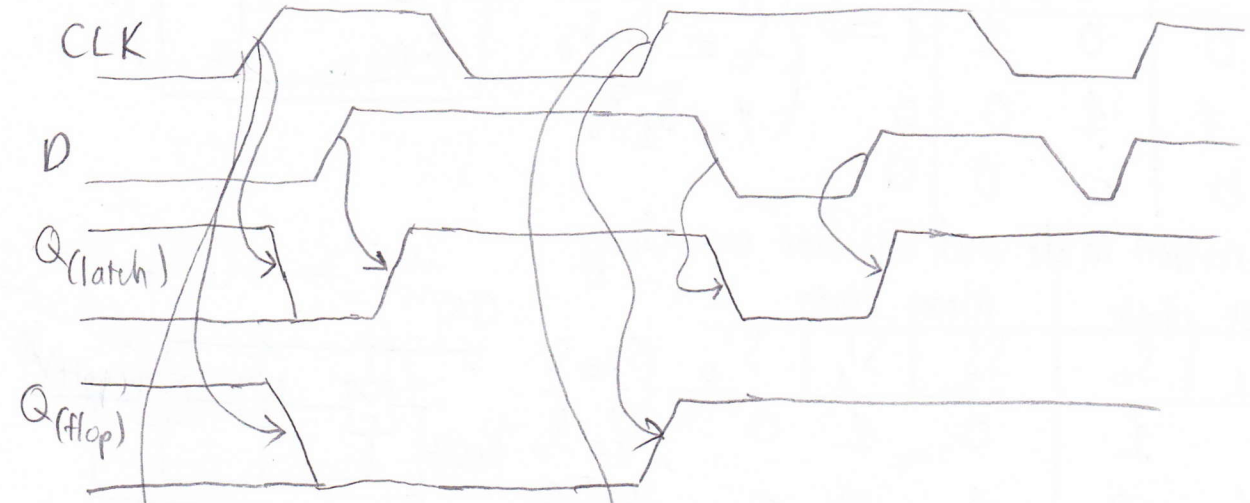
EXAMBLE PROBLEMS

Example 3.1: How many transistors are needed to build the D flip-flop described in this section?

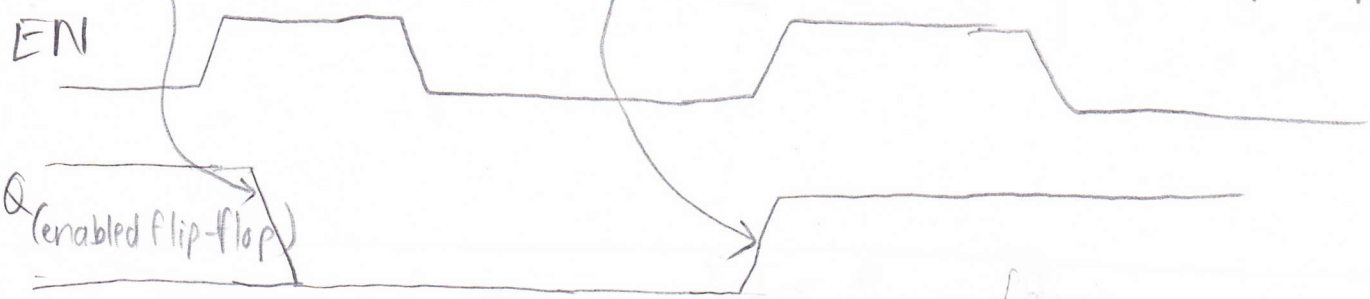
Device	Number of transistors
2-input NAND/NOR	4
NOT	2
2-input AND/OR	6 (NAND/NOR + NOT)
SR latch	8 (2×NOR)
D latch	22 (SR latch + 2× AND + NOT)
D flip-flop	46 (2× D latch + NOT)

Variation: How many transistors are needed to build an enabled flip-flop?
An enabled flip-flop uses a D flip-flop and a 2-input AND gate.
Thus, an enabled flip-flop requires 52 transistors

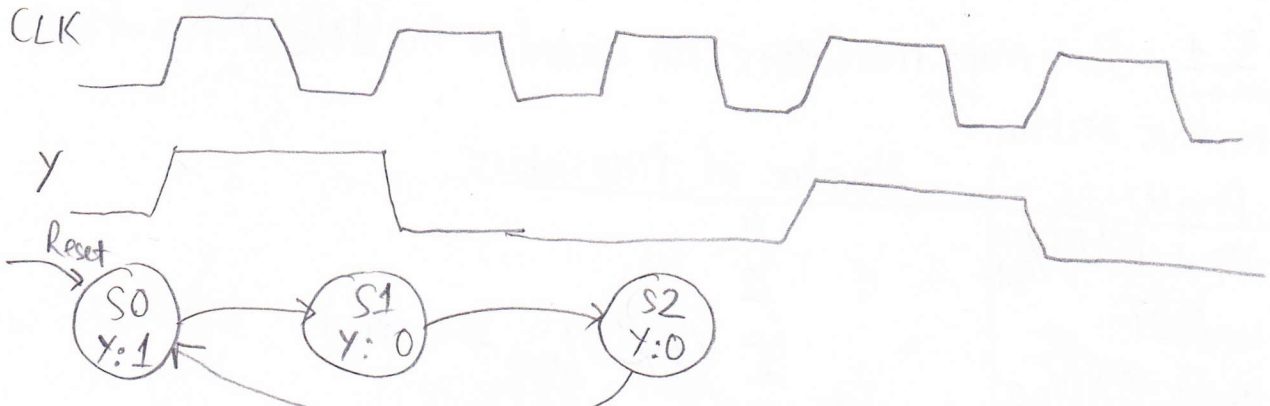
Example 3.2: Determine output Q from the waveforms of CLK and D



Variation: Same graph as above but with an enabled flip-flop



Example 3.6 : FSM state encoding



State transition table

current state	next state
S0	S1
S1	S2
S2	S0

State Encoding

State	$S_{1:0}$
S0	00
S1	01
S2	10

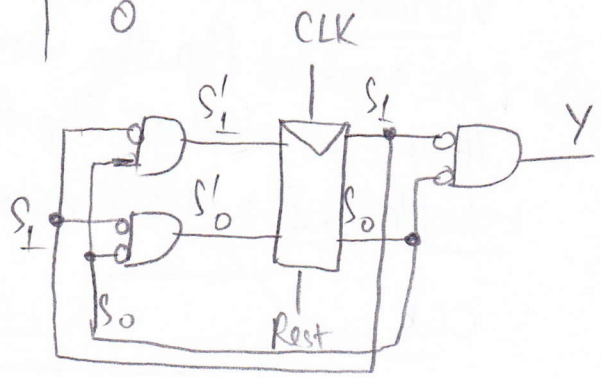
Divide-by-3 output table

current state	output
S0	1
S1	0
S2	0

State transition table with binary encoding

current state S_1	current state S_0	next state S_1'	next state S_0'	Output Y
0	0	0	1	1
0	1	1	0	0
1	0	0	0	0

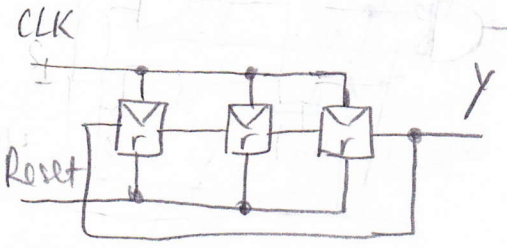
$$\Rightarrow \begin{cases} S_1' = \overline{S_1} S_0 \\ S_0' = \overline{S_1}\,\overline{S_0} \\ Y = \overline{S_1}\,\overline{S_0} \end{cases}$$



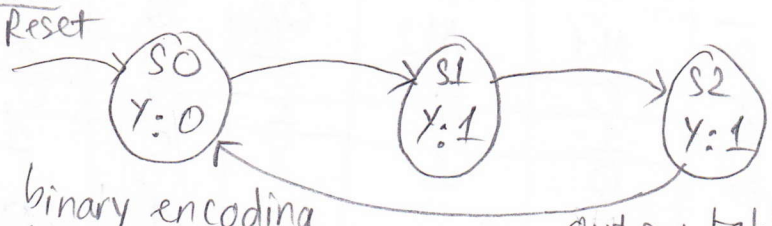
State transition table with one-hot encoding

Current state S_2	Current state S_1	Current state S_0	Next state S_2'	Next state S_1'	Next state S_0'
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	0	0	1

$$\begin{cases} S_2' = S_1 \\ S_1' = S_0 \\ S_0' = S_2 \\ Y = S_0 \end{cases}$$



Variation:



State binary encoding

State	$S_{1:0}$
S0	00
S1	01
S2	10

output table:

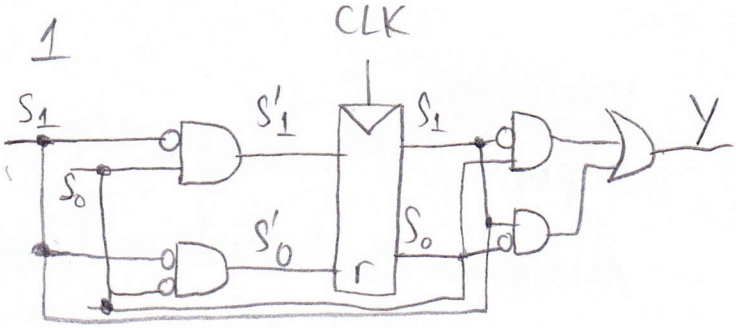
current state	output
S0	0
S1	1
S2	1

State transition table with binary encoding

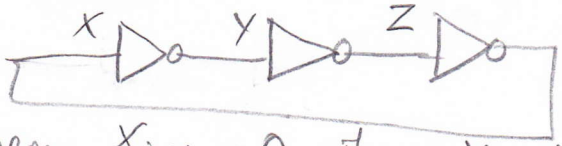
current state		next state		output
S_1	S_0	S'_1	S'_0	Y
0	0	0	1	0
0	1	1	0	1
1	0	0	0	1

$$\Rightarrow \begin{cases} S'_1 = \bar{S}_1 S_0 \\ S'_0 = \bar{S}_1 \bar{S}_0 \\ Y = \bar{S}_1 S_0 + S_1 \bar{S}_0 \end{cases}$$

Sketch:

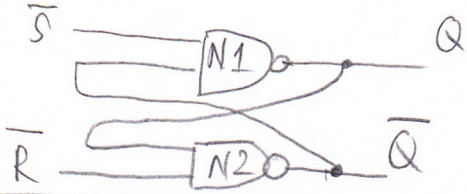


Example 3.3: Astable circuits



Suppose $X_{init} = 0$. Then, $Y = 1$ and $Z = 0$, but then $X = 1$.
Suppose $X_{init} = 1$. Then, $Y = 0$ and $Z = 1$, but then $X = 0$.
The circuits has no stable state. (astable circuit)
X, Y, and Z will oscillate between 0 and 1

Variation:



is this circuit stable or astable?

Truth table:

S	R	$\bar{S}$	$\bar{R}$	N1	N2	Q_{prev}	Q	$\bar{Q}$
0	0	1	1	0	1	0	0	1
				1	0	1	1	0
0	1	1	0	0	1	X	0	1
1	0	0	1	1	0	X	1	0
1	1	0	0	1	1	X	1	1

=> Stable sequential circuit

Example 3.10 : Timing Analysis

$t_{pcq} = 80ps$, $t_{setup} = 50ps$, $t_{pd} = 40ps$, 3 logic gates. $f_{c\,max} = ?$

Minimum clock cycle = $T_{c\,min} = t_{pcq} + 3t_{pd} + t_{setup} = 250\,ps$

Maximum clock frequency = $f_{c\,max} = \frac{1}{T_{c\,min}} = 4\,GHz$

Variation:

$t_{pcq} = 75ps$, $t_{setup} = 10ps$, $t_{pd} = 100ps$, 7 logic gates. $f_{c\,max} = ?$

Minimum clock cycle = $T_{c\,min} = t_{pcq} + 7t_{pd} + t_{setup} = 785\,ps$

Maximum clock frequency = $f_{c\,max} = \frac{1}{T_{c\,min}} = 1.274\,GHz$