

ECE 271 - Chapter 2 Reading Report

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1 Chapter Outline

This chapter covers the basics of combinational logic design and heavily focuses on the functional and timing relationships between inputs and outputs of a circuit. In this chapter, the authors use boolean and boolean algebra to establish multilevel combinational logic and help reduce the amount of hardware to build more complex circuits. Another focus of this chapter is showing how to use Karnaugh maps (or K-maps) to minimize logic in a more graphical and intuitive way. Each of the topics mentioned will be discussed further throughout the following sections.

1. **Introduction**
2. Boolean Equations
3. Boolean Algebra
4. From Logic to Gates
5. Multilevel Combinational Logic
6. X's and Z's, Oh My
7. Karnaugh Maps
8. Combinational Building Blocks
9. Timing
10. Summary

- 2 Grey Box Exploration
- 3 Figures
- 4 Example Problems
- 5 Glossary
- 6 Interview Question
- 7 Reflection
- 8 Questions for Lecture