Management and analysis of physics dataset: FPGA Counter

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```vhdl
-- (this is a VHDL comment)

-- import std_logic from the IEEE library
library IEEE;
use IEEE.std_logic_1164.all;

-- this is the entity
entity ANDGATE is
   port (
     I1 : in std_logic;
     I2 : in std_logic;
     O  : out std_logic);
end entity ANDGATE;

-- this is the architecture
architecture RTL of ANDGATE is
begin
   O <= I1 and I2;
end architecture RTL;
```

Figure 1