

Neural Spike Digital Detector on FPGA

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Introduction

- Many advanced neurobiology techniques require a communication interface to analyse neural activity and to perform neural stimulation

- It needs advanced electronics systems composed by:
 - analog stages to acquire biological signals
 - **advanced algorithms** to separate signals from **background noise**
 - electrical stimulation stages



Fig: Neuron cartoon

Neuron communication

- Neuron communication is carried out through **action potentials** (AP) → trans-membrane voltage of 100 mV_{PP} and few kHz

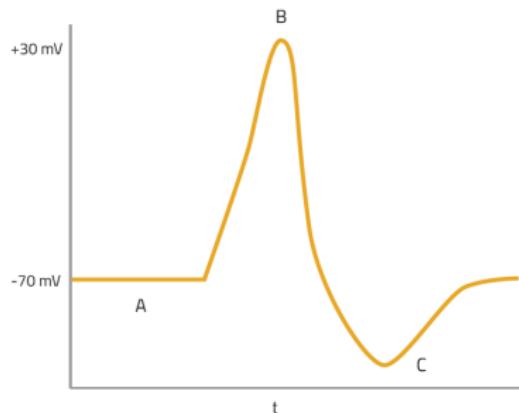


Fig: Action Potential

- Most common technique to observe neurons utilized needle-shaped probes that deeply penetrate the cells:
 - ✓ high signal-to-noise ratio
 - ✗ average cell life of few days

State-of-the-art approaches

- Minimally-invasive sensing techniques, based on **CMOS** microelectrode arrays, are state-of-the-art approaches
 - ✓ preserve cell for long time observations
 - ✗ low signal-to-noise ratio
- Recorded signals are improved by advanced post-processing **spike sorting algorithms** that separate relevant neural spikes from background noise

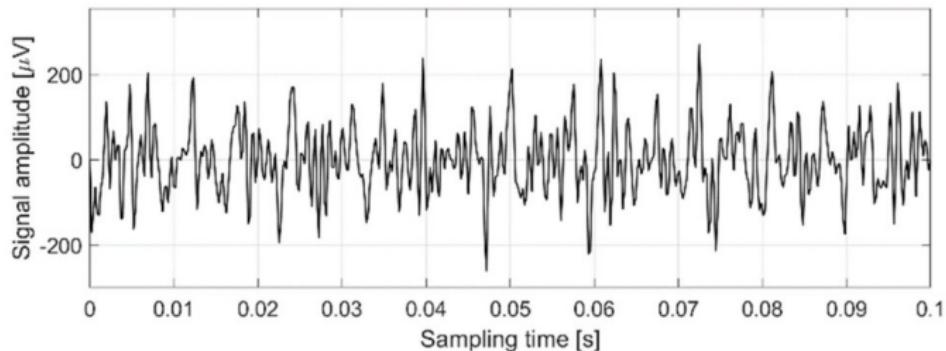


Fig: Single pixel signal time evolution

Neural Spike Digital Detector (i)



- This work analyzes the **neural spike digital detector** (NSDD) hardware design
- An action potential detector has been implemented on a FPGA
- It identifies single AP signals with amplitudes around $200 - 600 \mu V$ recorded on pixels of a CMOS MEA
- In situ neural activity recognition greatly limits the bandwidth required to transmit data and the associated power consumption

Neural Spike Digital Detector (ii)

- Neuronal cells are seeded on the CMOS MEA composed by:
 - the capacitive sensor matrix (256×384 pixels)
 - the electronics signal processing stages
- A communication interface forward the digitized signals from the output to the NSDD FPGA at **14.1 MS/s**.

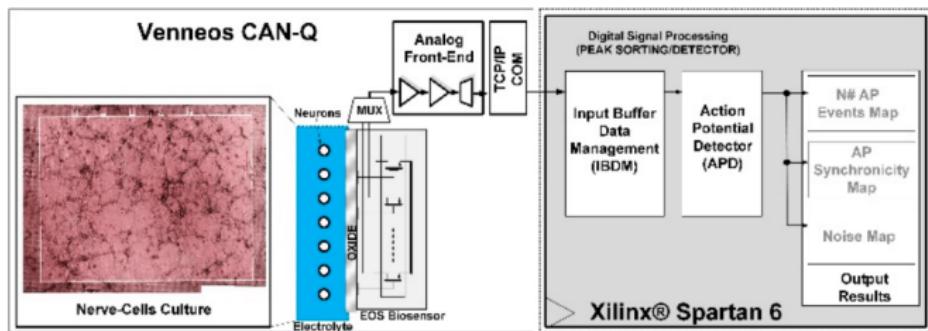


Fig: Neuronal-cell culture experimental setup

Neural Interface Noise

- Extracellular signal amplitudes are two orders of magnitude smaller than invasive techniques.
- Adhesion of cells to the surface increases the noise power
- An **accurate noise evaluation** and a proper spike detector is needed to avoid discarding most of the action potentials

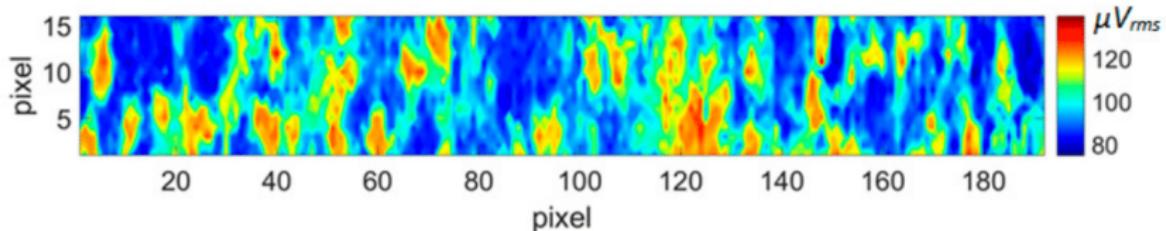


Fig: Noise power spatial map

- In areas without cell exhibit the noise is $80 \mu V_{RMS}$
- In pixel beneath cell the noise is $120 \mu V_{RMS}$

Principal Component Analysis (i)

- MEAs are characterized by high spatial and temporal resolution → a single AP event can be detected:
 - by 9 adjacent pixels
 - for 3 consecutive time samples
- PCA algorithm calculate the probability to detect signal in front of statistical thermal fluctuation
- AP is detected if:

$$\sum_{pixj=1 \rightarrow 9} \frac{\sum_{\{n, n-i, n-2\}} PIXj(n)^2}{\sigma_{NOISE,j}^2} \geq AP_Threshold \cong 84.6 \quad (1)$$

where $PIXj$ is the j -th pixels at three instants n , $n - i$ and $n - 2$

- Improve global SNR at cost of a small spatial resolution reduction

Principal Component Analysis (ii)

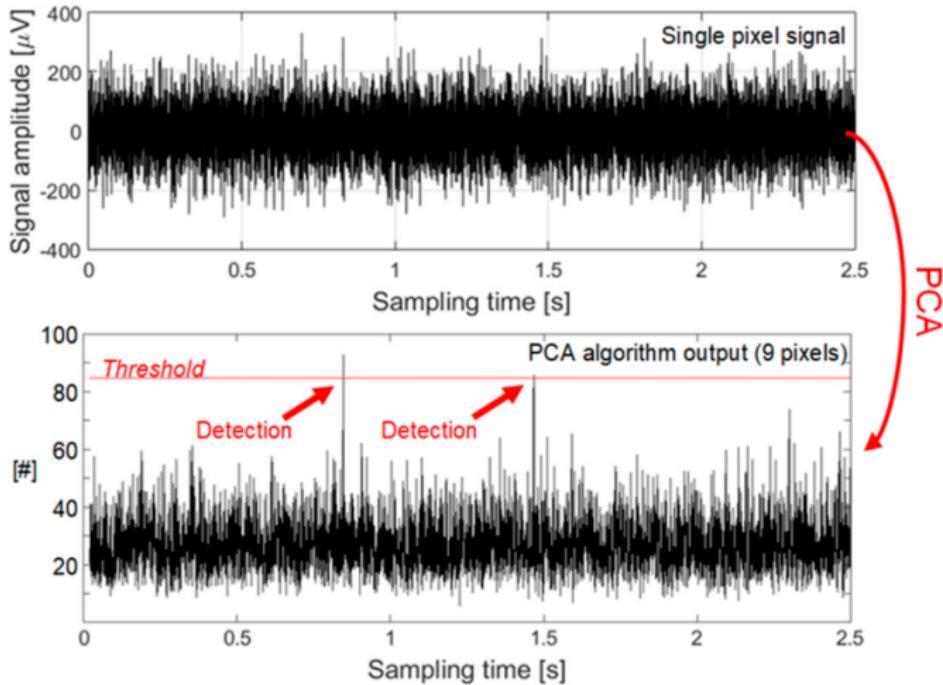


Fig: PCA output compared with threshold

Neural Spike Digital Detector on FPGA



The digital design for the PCA algorithm on FPGA consists of three main stages:

- the input-buffer-data-management (IBDM) synchronously receives the data coming from the biosensor via the TCP/IP communication interface
- the action potential detector (APD), that is the digital circuit implementing the PCA algorithm
- a specific set of MATLAB functions that provide graphical representation of the on-going neural activity.

Neural Spike Digital Detector on FPGA

To achieve the aim of real-time analysis it must be:

$$\frac{\text{NSDD data throughput}}{\text{MEA sample rate}} \geq 1 \Rightarrow f_{CLK} \geq N_{CLK} \cdot MEA_{out} \quad (2)$$

- MEA_{out} : MEA sample rate
- f_{CLK} : FPGA master clock frequency
- N_{CLK} : Clock cycles needed to process one sample

From neurons to PCA

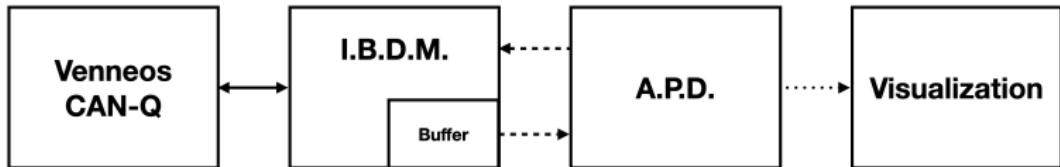
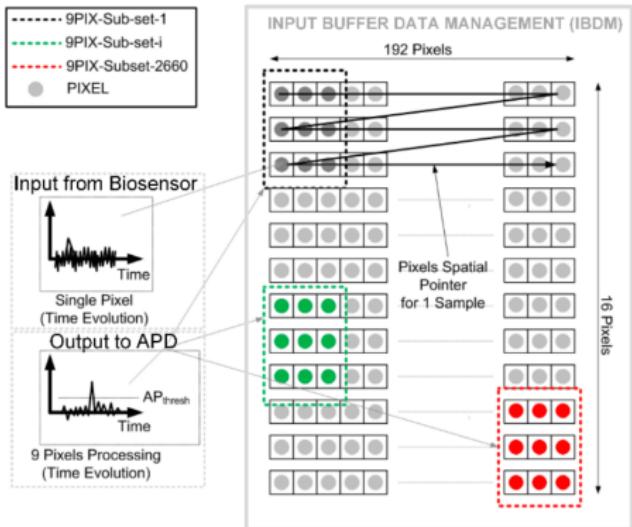


Fig: Data movement inside the system.

- NSDD receives a stream of data from the Venneos-CAN-Q machine via an Ethernet connection using TCP/IP protocol.
- data are sent from the buffer to the APD stage to perform the PCA algorithm.

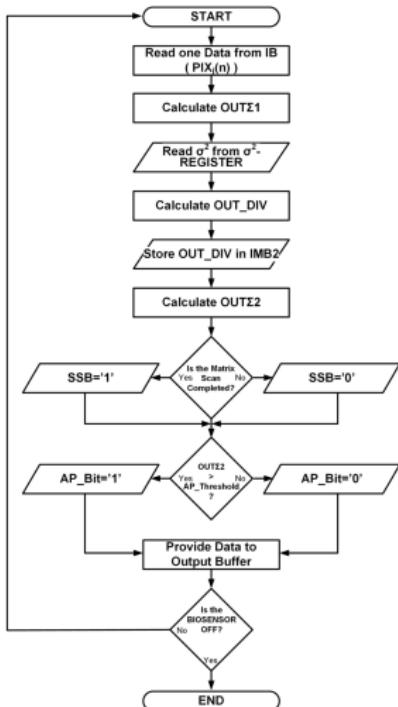
From neurons to PCA



- Total number of pixels: 3072
- Matrix acquisition frequency: $14.1Ms/s$
- Start-up time: 6531 clock cycles $\simeq 447.3 \mu s$

Fig: IBDM functional scheme

Action Potential Detector Algorithm



- Each time a new data ($PIX_j(n)$), is received from the MEA, the APD executes the operations illustrated in the flowchart.
- The APD performs all the operations that are required to verify the specific condition expressed in Equation:

$$\sum_{pixj=1 \rightarrow 9} \frac{\sum_{\{n, n-i, n-2\}} PIX_j(n)^2}{\sigma^2_{NOISE,j}} \geq AP_Threshold$$

Fig: PCA algorithm.

Output signals

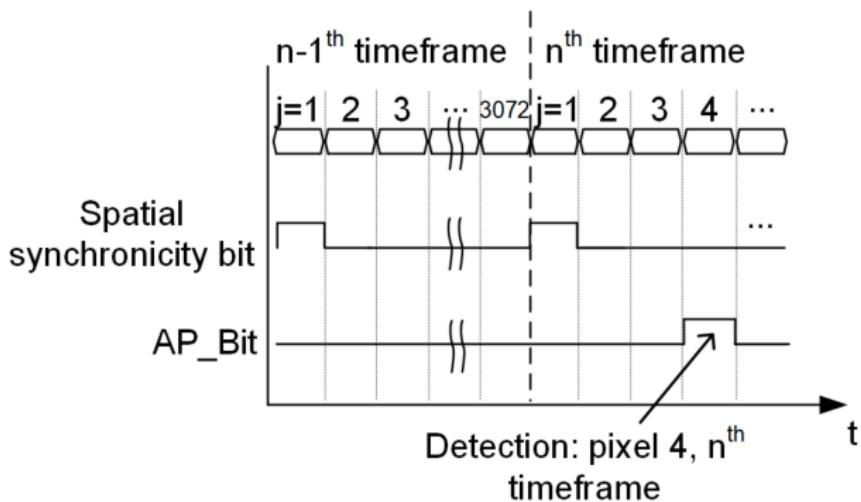


Fig: Output signal encoded spatial and temporal information

Output signals

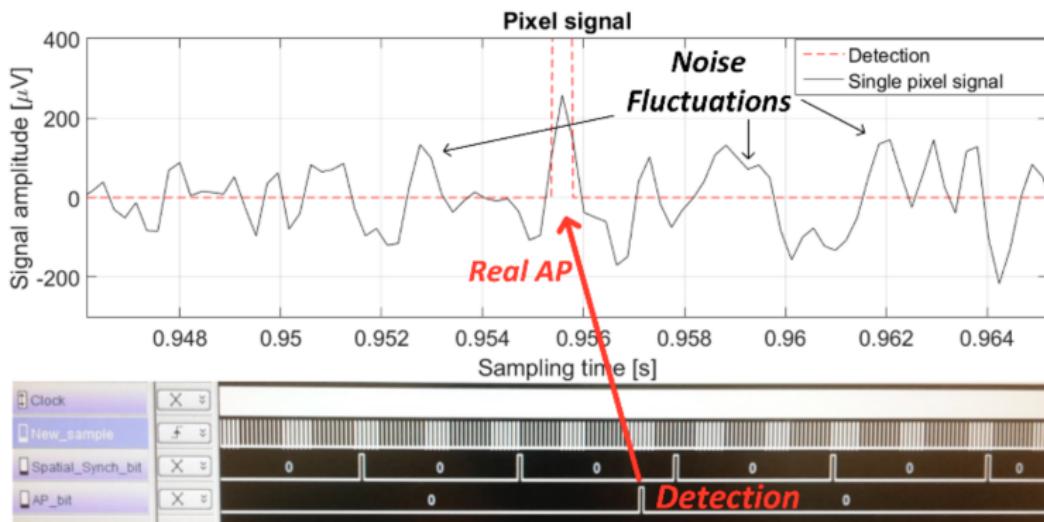


Fig: AP detection and single pixel signal with AP.

APD FPGA Hardware Implementation



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The APD algorithm is implemented by a VHDL digital circuit with:

- Control Unit (**CU**);
- Arithmetic Logic Unit (**ALU**).

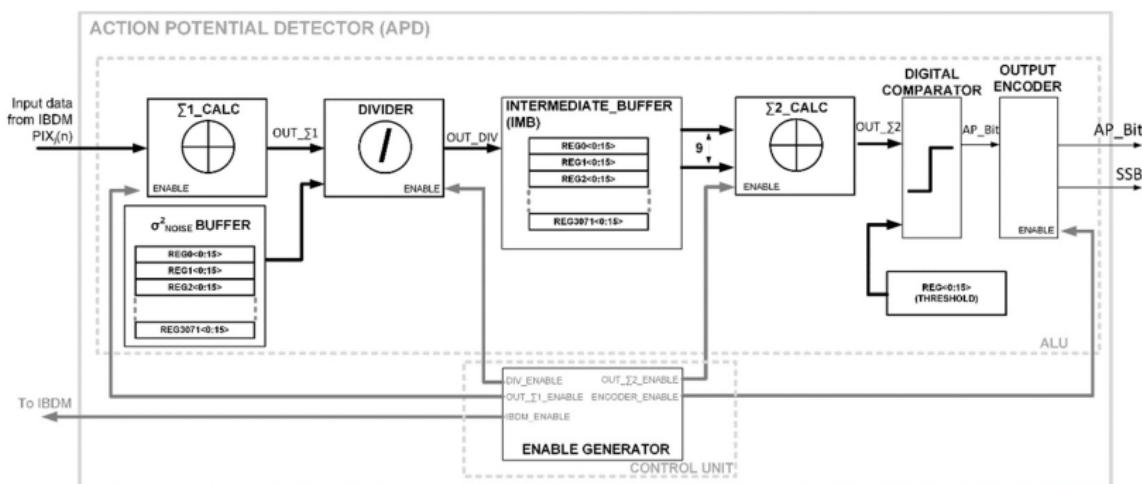


Fig: Action Potential Detector (APD) block scheme.

APD FPGA Hardware Implementation

Arithmetic Logic Unit (ALU)

ALU : arithmetic, logic and memory blocks that perform the operations presented before. Technical details:

- Input data encoded as signed **14-bit integers**.
- Then recoded to **9-bit resolution**.
- The operations are then performed with **unsigned integer arithmetic**.
- After each block of the ALU, data recoded again to the **minimum needed resolution**.
- Computational errors only in the division between integers (**Radix-2 algorithm**).
- To minimize this error, both the numerator and the threshold are multiplied by 256.

APD FPGA Hardware Implementation

Control Unit (CU)

CU : it regulates the behaviour of the ALU using specific enable signals and spatial pointers, which control the evolution of the algorithm.

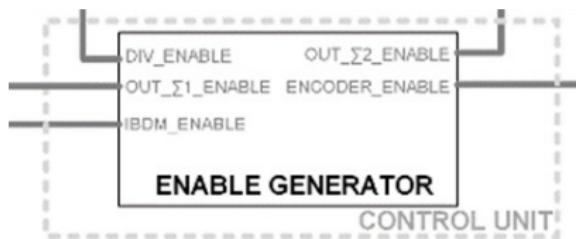


Fig: Signals of the CU block.

APD FPGA Hardware Implementation

Control Unit (CU)

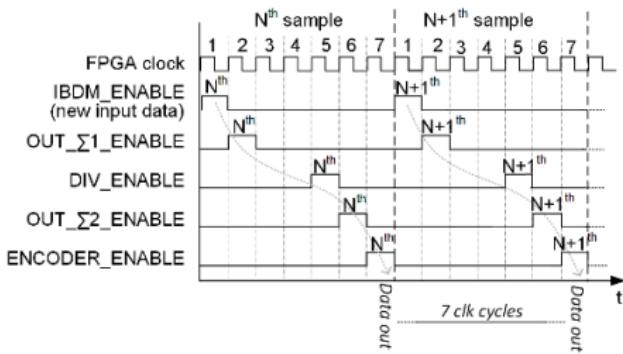


Fig: Time evolution of CU.

In sequence:

- 1 **IBDM_ENABLE**
- 2 **OUT_Σ1_ENABLE**
- 3 **DIV_ENABLE**
- 4 **OUT_Σ2_ENABLE**
- 5 **ENCODER_ENABLE**

APD FPGA Hardware Implementation

Control Unit (CU)

This configuration allows to encode the entire spatial and temporal activity of the biological neuronal net in three single bits:

- **AP_Bit**: detection information.
- **FPGA master clock**: temporal pointer.
- **SSB**: spatial pointer.

Each operation is performed during a single cycle of the FPGA master clock, except the division that lasts three clock cycles.

⇒ **7 clock cycles to process a single data.**

APD Control Unit Pipeline Approach

Input data rate:

$$\text{MEA}_{\text{OUT},\text{RATE}} = 14.1 \text{ MS/s} \xrightarrow{7 \text{ clk}/\text{data}} f_{\text{clk}} = 98.7 \text{ MHz}$$

It is possible to achieve the same data throughput with a reduced f_{clk} by using a **pipeline approach**:

- Optimization of the intrinsic parallelization properties of the FPGA.
- Technique: provide a new data input to the ALU as soon as the first stage has produced an output.

APD Control Unit Pipeline Approach

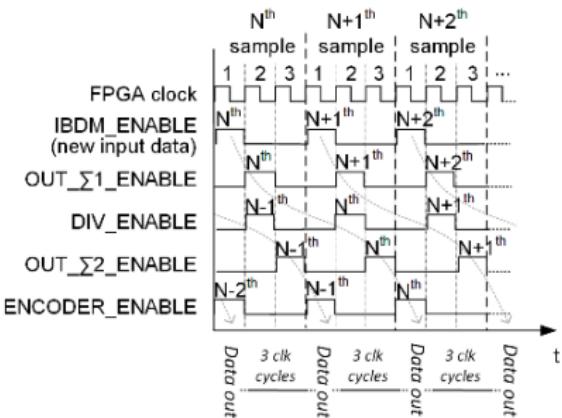


Fig: Pipelined controller unit enable signals after diagram.

In this way, the system will accept a new input data every three master clock cycles. So:

$$f_{\text{clk}} = 42.3 \text{ MHz}$$

Final clock frequency:

$$f_{\text{clk}} = 42 \text{ MHz}$$

Experimental Results

NSDD for real-time detection of the neural spikes has been validated by two different setups:

- **Behavioral validation:** test-bench → check the efficacy of the digital system vs. single pixel SNR.
- **Biological validation** → directly check the NSDD behavior under the signals coming from the CMOS MEA.

Behavioral validation

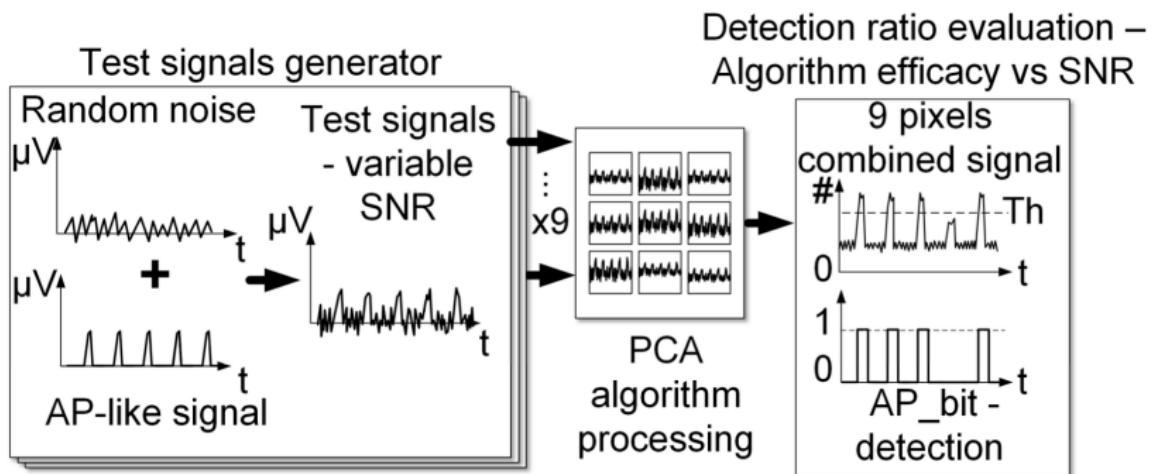
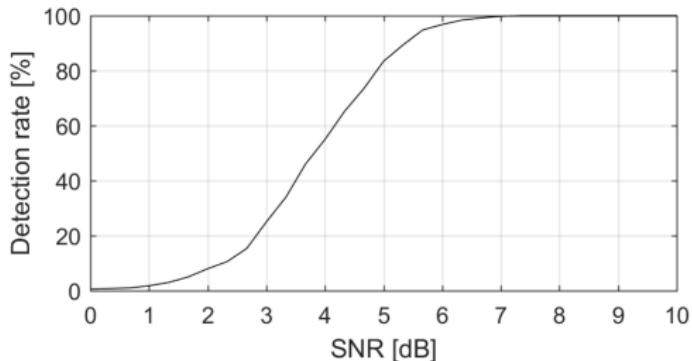


Fig: Behavioral setup functional scheme.

Behavioral validation

Since the pattern is a priori known, it is possible to **compare** the NSDD output bit with the input pattern.



⇒ APs with $250\mu V_0$ -peak amplitude are detected with 98% efficacy.

Fig: Percentage of detected AP versus SNR.

Biological validation

NSDD has been tested with the signals coming from the neurons culture.

The FPGA-APD data allows representing the neuronal cells culture electrical activity by:

- neural spike spatial map;
- noise power spatial map;
- action potential bursting map.

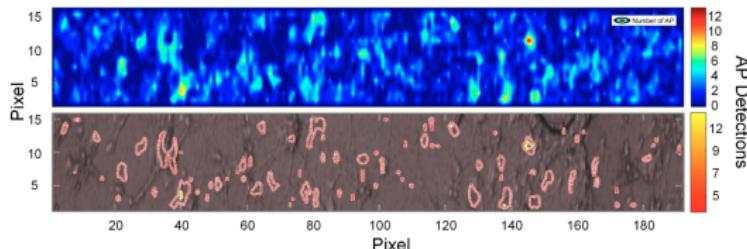


Fig: Neural spike (action potential) spatial map.

Biological validation

AP_Bit encodes the detection information (spatial and temporal):

- it can be processed to perform spatial and temporal mapping of the APs above the MEA.
- it enables event-driven communication and/or it can be used for instantaneous control of the electrical stimulation signal;

Action Potential Bursting

AP_Bit can be used to detect whether any synchronous activity of the neuron population is happening at any given moment.

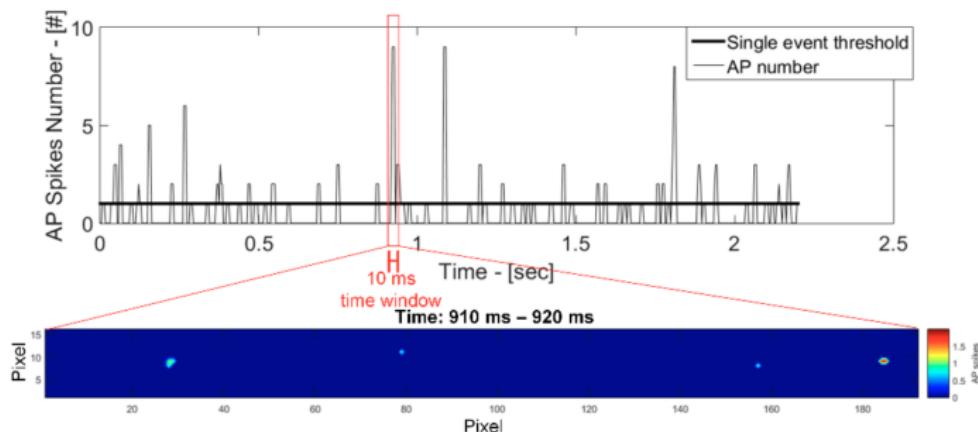


Fig: Neuronal spikes map of action potential bursting.

Conclusions

Design of a **complete FPGA-based** circuit:

- **monitors** the electrical activity of a hippocampal neuronal cells culture over a micro-electrode array;
- **detects** action potentials from background noise.

The system is composed by:

- VHDL-based FPGA design;
- set of MATLAB functions for data evalutation.

Conclusions



The system implementation allows:

- real-time detection;
- encoding temporal and spatial information.

It has been experimentally validated by producing a spatial map of the on-going electrical activity, which is consistent with spontaneous neural activity rates.

Finally, the output bit-stream has been used to detect AP bursting events.

Grazie per l'attenzione.