National Institute of Technology Mizoram

Mid – Semester Examination, Odd Semester - 2022

Digital Logic Design (ECL 1302)

3rd Semester (ECE/CSE/EEE) **Full Marks: 30 marks** **Duration: 1:30 hours**

Answer all 3 (Three) Questions. All Questions Carry Same Marks
(3 * 10 = 30 Marks)

1. Answer (a) or (b)

(a) Reduce using k-map the expression Π M(2,8,9,10,11,12,14) in both SOP and POS form. Then implement the minimal expression in universal logic. Show all the necessary steps. [4+4+2]

OR

(b) Reduce using k-map the expression ∑m(0,1,2,3,5,7,8,9,10,12,13) in both SOP and POS form. Then implement the minimal expression in universal logic. Show all the necessary steps. [4+4+2]

2. Answer (a) or (b)

(a) Explain the operation of a full adder circuit with block diagram and provide its logic expression based on possible combinations and derive to its simplest form. Also give the truth table, and the combinational logic diagram. Draw the logic circuit using only NOR logic gates providing the exact output generated after each gate used while also derive the NOR logic operation using Boolean expression. [2+2+1+2+3]

OR

(b) Explain the working of 8-line to 1-line Multiplexer with diagram and truth table. Implement the following logic function using an 8 x 1 MUX while drawing the circuit:
F(A, B, C, D) = ∑m(1, 3, 4, 11, 12, 13, 14, 15) [3+7]

3. Answer (a) or (b)

(a) What is ECL and how does it work? Explain its operation and characteristics features. Convert the following number systems as mentioned showing all the related steps:
(i) $(11011.101)_2$ to decimal (ii) $(110101.101010)_2$ to octal [2+2+3+3]

OR

(b) How does a Two-input TTL NAND Gate work and function? Convert the following number systems as mentioned showing all the related steps:
(i) $(A0F9.0EB)_{16}$ to decimal (ii) $(B9F.AE)_{16}$ to octal [4+3+3]

National Institute of Technology Mizoram
End – Semester Examination, Odd Semester - 2022
Digital Logic Design (ECL 1302)

3rd Semester (ECE/CSE/EEE) Full Marks: 50 marks Duration: 3:00 hours

Answer all 5 (Five) Questions, All Questions Carry Same Marks
(5 * 10 = 50 Marks)

1. (i) Minimize the following expression using QUINE-MCCLUSKY method
$\Sigma m(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$ [8]

(ii) Perform the addition of 37 + 28 in XS-3 code. [2]

2. Perform the subtraction using 2's complement method.
(i) 110011 - 111011 (ii) 11010 – 1101 (iii) 101 – 110000

Design and explain the working of an Even parity generator for 4-bit input with truth table, logic gates and its realization: [4+6]

3. (i) The waveforms shown in Fig 1(a) are applied to the master-slave J-K flip-flop shown in fig 1(b). Draw the output waveforms and explain its operation. (ii) Design of 4-bit binary-to-gray code converter and show how the programmable ROM (PROM) circuit can be programmed to implement the 3-bit binary-to-gray code conversion. [7+3]

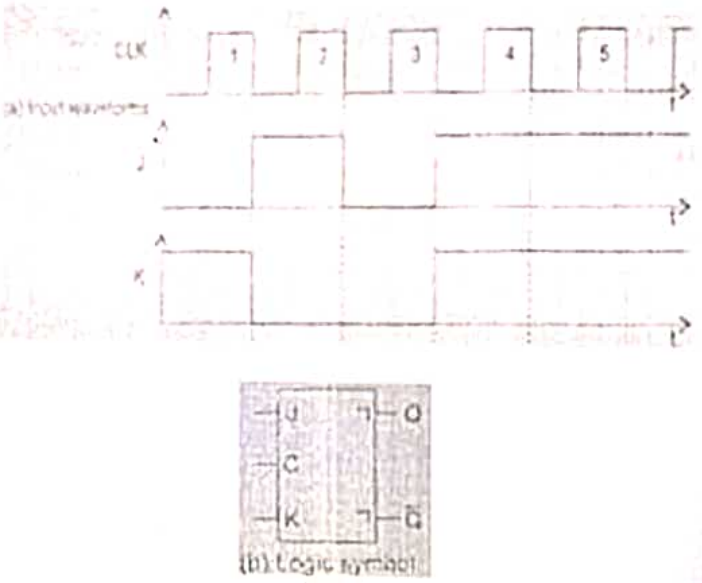

Fig 1

4. The waveforms shown in Fig 2(a) are applied to the positive edge triggered S-R flip-flop shown in Fig 2(b). Sketch the output waveforms and explain how you arrive at your conclusion. Draw and explain the operation of a CMOS based two-input NOR gate and its equivalent gate combinations. [6+4]

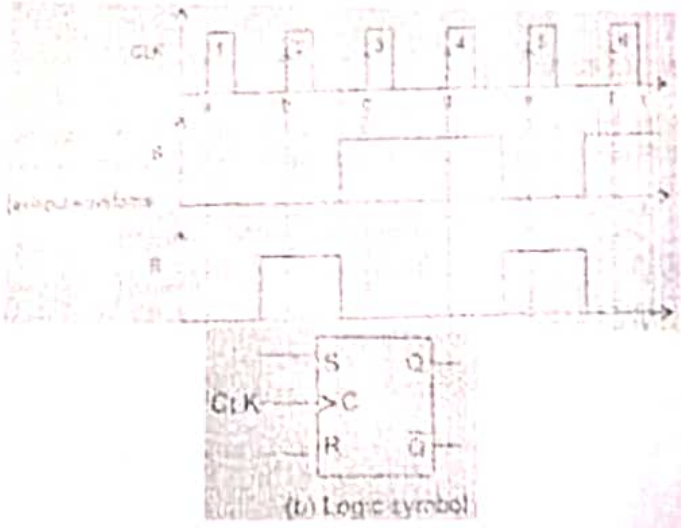

Fig 2

5. (i) Draw the block diagram of a CPLD and explain how it works. (ii) Draw and explain the operation of a 4-bit twisted Johnson counter using D flip-flops, providing related sequence table, state diagram and a proper set of timing diagram. [3+7]

National Institute of Technology, Mizoram

Mid – Semester Examination 2021

Digital Logic Design (ECL 1302)

3rd Semester (ECE, EEE, CSE) **Full Marks: 15 marks** **Duration: 1:00 hour**

Answer all questions

1. (a) Implement the expression using a 16:1 Multiplexer.
$f(A,B,C,D) = \sum m(0,2,3,6,8,9,12,14)$ (5)

(b) Implement the Boolean expression and logic diagram of Full Subtractor using only NAND gates. (5)

(d) For the logic circuit shown in the figure 1 below, the output Y is equal to
(A) $\overline{ABC}$ (B) $\overline{A} + \overline{B} + \overline{C}$ (C) $\overline{AB} + \overline{BC} + \overline{A} + \overline{C}$ (D) $\overline{AB} + \overline{BC}$ (2.5)

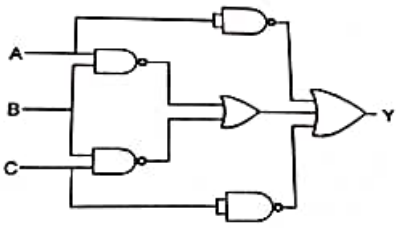

Figure 1

(e) The switching circuit given in the figure 2 can be expressed in binary logic notation as
(A) L = (A+B) (C+D) E (B) L = AB + CD + E (2.5)
(C) L = E + (A+B) (C+D) (D) L = (AB+CD) E

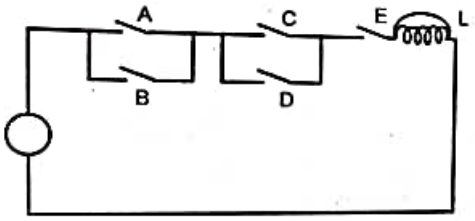

Figure 2