

SUBJECT- ADVANCED COMPUTER ARCHITECTURE SEMESTER - 7TH

QUIZ-1(13.10.2022) FULL MARKS: 20 TIME: 30 MINUTES

1. Assume an L1 cache with a hit rate of 70%, and an L2 cache with a local mis rate of 10%. If there are 1000 memory access initiated by CPU, then the number of access that will find a hit in L2 cache is (3)	of
2. A cache has a hit rate of 95% and a hit time of 10 ns. The cache block size is 3 bytes and the word length of the processor is 16 bits. During a cache miss, it take 'x' ns to fetch the first word of a block and 5 ns for fetching each subsequer word. The average memory access time is 15 ns. The value of x is (5)	s nt
3. Register renaming helps in solving which types of hazards? (2)
4. Consider an instruction pipeline of an issue width of 1 that uses <u>Tomasulo's</u> algorithm with one reservation station per functional unit. There is one Integer MU unit, one Integer DIV unit and one Integer ADD unit all connected to a single CDE The functional units are not pipelined. An instruction waiting for data on CDB carnove to its EX stage in the cycle after the CDB broadcast. The instructions are:	IL 3.
I1: ADDI R1, R1, #8 I2: DIV R3, R2, R1 I3: MUL R4, R1, R3 I4: DIV R5, R4, R1 Assume the following information about functional units. Functional unit type Cycles in EX stage Integer MUL unit 4 Integer DIV unit 8 Integer ADD unit 1	
Show the final RSI also. (5)
 5. Consider an in-order MIPS multi-cycle pipeline that supports operand forwarding and executes the following instructions: I1: LD F1, 0(R2) I2: LD F2, 8(R2) I3: FADD F3, F1, F2 I4: SD F3, 8(R2) 	

If the instruction fetch for I1 starts at clock cycle 1, in which cycle the instruction I4 access memory to store the data? (5)

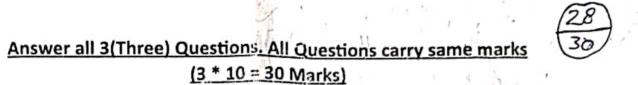
National Institute of Technology Mizoram Mid- Semester Examination, Odd Semester (2022-23)

Advanced Computer Architecture (CSL - 1703)

B.Tech Semester - 7th

Full Marks - 30

Duration - 1:30 hours



1. a) A new floating-point unit speeds up floating point operations by two times In an application one fifth of the instructions are floating-point operations.

ii) Assume that the speeding up of the floating-point unit mentioned above slowed down data cache accesses resulting in a 1.8x slowdown. Assume the load instructions constitute 20% and store instructions constitute 8% of the total instruction what is the effective overall speedup now?

Or

b) Draw Flynn's Taxonomy and provide brief example for each classification. (5)
c' Briefly mention the issues in Longer Latency Pipelines and how are they avoided?

(5)

(1+4) What are the different types of Data Hazards possible in a multi cycle pipeline?

b) Given an instruction pipeline running at 1GHz that takes 5 cycles to finish an instruction. 30% memory instructions result in a stall of 50 cycles. Assume a base CPI without stalls as 1 and there are 10% memory instructions, what is the effective CPI?

(5)

Or

c) What do you mean by 'Loop-unrolling'? What are its advantages and disadvantages? Unroll the following loop and represent the code. (2+2-1)

for (i=0; i<100; i++) g();

d) Differentiate among 'Anti-dependence' and 'Output dependence' with example.

3. a) Explain briefly how 'Strip mining' helps in Loop Unrolling.	(5)
b) What is the clock cycle latency you obtain between one 'FP ALU or	peration' and
'Store Double' operation? Explain with an example. "	(5)
Or /	
Or What are the various performance metrics for measuring the per	formance of
CPU? How SPEC benchmark suite plays its role in the above?	(2+3)
What do you mean by Control Dependence of a line of code on anot	her? Why is
it important to analyse?	(5)

National Institute of Technology Mizoram

End - Semester Examination, Odd Semester - 2022

Advanced Computer Architecture (CSL 1703)

В.	Tech 7th Semester	Full Marks: 50	Duration: 3:00	hours
	All questions	s are Compulsory. All Ques $(5 \times 10 = 50 \text{ Mag})$	tions Carry the Same Marks	
A	اهر) How structural hazard State the difference be	nta hazard even with operar ils are avoided in pipelining etween 1-bit and 2-bit brack g can be a valid instruction	?	Explain your
2 // // //	,		echniques to deal with it? Expl e disk design. Mention the adva	(2.5x2)
, To	How reservation station in What is Branch Target Bufive stage pipeline.	s helpful in Dynamic Sched iffer(BTB)? With a neat dia	uling? Give example. gram explain the steps when us	(5) sing <u>BTB fer</u> (5)
4. (Co	Compare between Scalar of de For i = 0 to 49 C[i] = (A[i] + B[i])		ns of no of cycles required for t	the following (6)
<i>y</i> ,	Mention the different tech	niques to optimise the perfo	ormance of cache?	(4)
31	multimedia instructions multimedia instructions,	given to the processor by what is the overall speedup	processor speeds up the co y 4 times. Assuming a progra p gained while running the proce an when it is run on the proce	am has 46% 1.4 gram when it
X	With neat diagram diffe multiprocessor.	rentiate among Centralised	d shared memory and distribu	ited memory (5)
			÷	4