National Institute of Technology Mizoram
Mid Semester Examination
Microprocessors and Microcontrollers (ECL 1502)

Duration: 1 H

Department- ECE, EEE & CSE 5th Semester **Full Marks: 15 marks**

Note: All Questions are Compulsory

1. Draw the block diagram/architecture of 8085 microprocessors. And briefly describe each block. [5]

2. Draw the timing diagram of OUT 01 H. [5]

3. Identify the mode 0 control word to configure port A and port C_U as output ports and port B and port C_L as input ports. [2]

4. Write down the different addressing mode of 8085 microprocessors with example? [3]

NATIONAL INSTITUTE OF TECHNOLOGY MIZORAM

Mid – Semester Examination, ODD Semester (2022 – 23)
Microprocessors and Microcontrollers (ECL 1502)

5th Semester (ECE/EEE/CSE) **Full Marks: 30 Marks** **Duration: 1:30 Hrs**

NOTE the following carefully:

- Answer all 3 (Three) Questions. All Questions Carry Same Marks (3 × 10 = 30 Marks).
- Each question has part (a) and part (b), attempt/solve only one of them. In case you attempt both part (a) and part (b), then evaluation of part (a) for that question will be considered only.
- Draw diagram(s) wherever necessary with proper labelling.
- In case, any parameter is missing, consider the standard value of the same.

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1. a) i. Explain the difference between *microprocessor* and *microcomputer.* [2.0]

ii. What is an *assembler*? [2.0]

iii. Define *word*, and *instruction.* [2.0]

iv. State the functional relationship between the operating system and the hardware of a computer. [4.0]

OR

b) i. Explain the translation of high-level language program into machine code. [3.0]

ii. Identify the difference of ASCII and the extended ASCII codes. [2.0]

iii. Describe the procedure of *hand assembly* with an example. [5.0]

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2. a) i. Explain the *externally initiated signals* in an 8085 microprocessor. [6.0]

ii. Fill the details of *status signal* and *control signal* for the given machine cycle of an 8085 microprocessor. [4.0]

Machine Cycle	Status Signal			Control Signal
	IO/$\overline{M}$	S1	S0	
Opcode Fetch				
Interrupt Acknowledge				
Hold				

OR

b) i. Explain the *Flags* of an 8085 microprocessor. [5.0]

ii. State an example of 3-Byte instructions. [3.0]

iii. What are the *machine control* instructions? [2.0]

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3. a) i. Explain the significance of *Chip Select* in a microprocessor. [4.0]

ii. Describe the working of *Read Only Memory* (ROM). [6.0]

OR

b)	i.	Why are the program counter and stack pointer 16-bit registers?	[2.0]
	ii.	If the memory chip size is 256 × 1 bits, how many chips are required to make up 1K (1024) bytes of memory?	[3.0]
	iii.	The memory address of 8K byte memory chip is FFFFH. What is the starting address?	[2.0]
	iv.	Explain Tri-State devices.	[3.0]

NATIONAL INSTITUTE OF TECHNOLOGY MIZORAM

End Semester Examination, AUTUMN / ODD 2022

ECL 1502: μProcessors & μControllers

Duration: 3 Hrs — 5th Semester ECE / EEE / CSE — **Full Mark:** 50

Instructions to be followed:

- Answer all 5 (Five) Questions. All Questions Carry Same Marks ($5 \times 10 = 50$ Marks).
- Draw diagram(s) wherever necessary with proper labelling.
- In case, any parameter is missing, consider the standard value of the same.

Q1. (i) State the data format(s) used in 8085 μprocessor. [6.0]

(ii) Explain the procedure to generate control signals, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, and $\overline{IOW}$ in 8085 μprocessor. [4.0]

Q2. (i) The given below instructions are intended to clear ten memory locations starting from the memory address 0009H. However, it is observed that a large memory block is cleared / erased. Explain this peculiar observation. [2.0]

```
        LXI H, 0009H
LOOP:   MVI M, 00H
        DCX H
        JNZ LOOP
        HLT
```

(ii) Identify the register contents and flags as the following instructions are being executed. [3.0]

	A	S	Z	CY
MVI A, 80H				
ORA A				
RAR				

(iii) Specify the number of times the loop is executed. [2.0]

```
LOOP:   MVI B, 64H
        NOP
        DCR B
        JNZ LOOP
```

(iv) Comment on the "Time Delay using a Register Pair". [3.0]

Q3. (i) Write a program to clear all the flags. [3.0]

(ii) Write a program to load FFH in the accumulator, and demonstrate that the Zero flag is not affected by the data transfer instruction. [3.0]

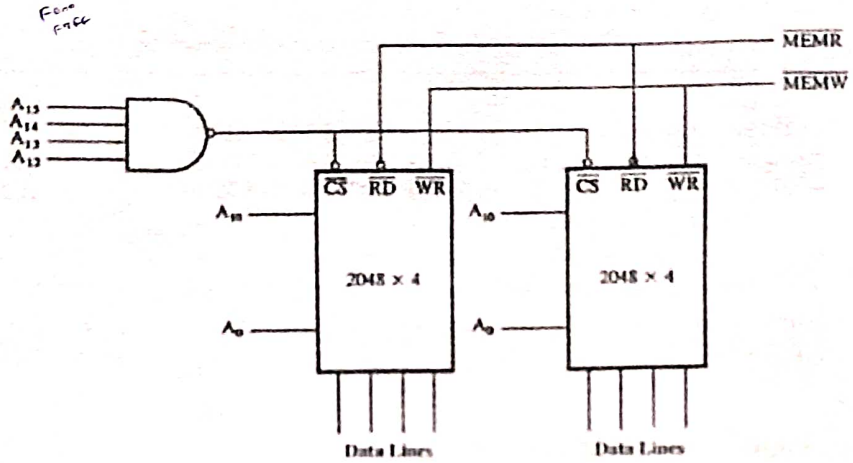
(iii) Explain the timing for execution of below mentioned instruction. [4.0]

Memory Address	Machine Code	Mnemonics
2050	32	STA 8000H
2051	00	
2052	80	

Q4. (i) Discuss the addressing modes with examples. [6.0]

(ii) Write a program to perform subtraction of two unsigned numbers, and to display the answer at PORT1. [2.0]

(iii) Identify the memory addresses, assuming don't care address line A_{11} at logic 0. [2.0]



Q5. (i) The memory map of a 4K (4096) byte memory chip begins at the location 2000H. Specify the address of the last location on the chip and the number of pages in the chip. [2.0]

(ii) How many address lines are used to identify an I/O port in the peripheral I/O and in the memory-mapped I/O methods? [2.0]

(iii) For the loop given below, calculate the delay assuming system clock period is 0.5 μs. [6.0]

Label	Mnemonics	8085 T-States
	LXI B, 12FFH	10
DELAY:	DCX B	10
	XTHL	16
	XTHL	16
	NOP	4
	NOP	4
	MOV A, C	4
	ORA B	4
	JNZ DELAY	10/7