National Institute of Technology Mizoram

Mid – Semester Examination, Even Semester - 2022

Computer Organization and Architecture (CSL 1401)

B.Tech 4th Semester (CSE+ECE) **Full Marks: 15** **Duration: 1:00 hours**

ANSWER ALL QUESTIONS

1. Prove with proper explanation that CLA produces less Gate Delay than RCA. [5]

2. a) Perform the following Binary operations using 2's complement representation.

i) (-7) - (-5) ii) (-8) + (-3) iii) (12) - (-3) [3]

b) Perform the arithmetic right shift by 2 positions of the following signed binary numbers

i) 010001 ii) 10101 [2]

3. Draw the General Purpose Register Organization (with a register stack of 7 registers) and write the 'Control Word' for the following instruction assuming the opcode for operation is 10011.

R3 <——R4+R1 [5]

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ANSWER ALL QUESTIONS

1. Explain with example how the same logic circuit can be used for binary numbers addition and subtraction with the help of a control input. [5]

2. Given an opportunity to compare and take the best computer system out of two available systems which one you will choose as efficient and how? Explain your answer. What would be your choice if you are supposed to choose between two servers instead of the two computer systems. [5]

3. Differentiate between any two categories of computer organisations you know of. Which one according to you is more likely to be existing in the current age computer systems. [5]

National Institute of Technology Mizoram
End-Semester Examination, Even Semester (2022-23)
Computer Organization and Architecture (CSL – 1401)
B.Tech (CSE+ECE) Semester - 4th Full Marks - 50 Duration - 2:30 hours

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Answer all Questions. All Questions carry same marks
(5 * 10 = 50 Marks)

1. What is the basic principle behind 'Cache Memory' ? Explain briefly. Which among the Cache mapping technique is the best? Give reasons for your answer. For the given data calculate the no of bits required for each fragment of the address.

Consider a 4-way set associative cache memory of 256 blocks where each block has 16 words in it. The main memory is addressible by 16 bit address. (3+3+4)

2. What is the importance of Pipelining in a computer system? What are the possible Hazards in pipelining? Explain briefly. How do you avoid each of them? (1+3+6)

3. What do you mean by Interrupts in a Computer system? What is the importance of Vectored Interrupt? How interrupt requests from multiple devices are handled? Explain with proper diagram. (1+3+6)

4. a) Write the Microroutine for the following. (5)

MOV X(Rsrc), Rdst

The source and destination operands are specified in indexed and register addressing modes respectively.

b) How Translation Look Aside Buffer (TLB) improves the performance of Virtual Memory address translation process? Explain with figure. (5)

5. Give Example of the following concepts. (4+3+3)

a) Little Endian & Big Endian Addressing

b) Memory Interleaving

c) Distributed Arbitration