SUBJECT- ADVANCED COMPUTER ARCHITECTURE

SEMESTER - 7TH

QUIZ-1(13.10.2022) FULL MARKS: 20 TIME: 30 MINUTES

1. Assume an L1 cache with a hit rate of 70%, and an L2 cache with a local miss rate of 10%. If there are 1000 memory access initiated by CPU, then the number of access that will find a hit in L2 cache is _____. (3)

2. A cache has a hit rate of 95% and a hit time of 10 ns. The cache block size is 32 bytes and the word length of the processor is 16 bits. During a cache miss, it takes 'x' ns to fetch the first word of a block and 5 ns for fetching each subsequent word. The average memory access time is 15 ns. The value of x is _____. (5)

3. Register renaming helps in solving which types of hazards? (2)

4. Consider an instruction pipeline of an issue width of 1 that uses Tomasulo's algorithm with one reservation station per functional unit. There is one Integer MUL unit, one Integer DIV unit and one Integer ADD unit all connected to a single CDB. The functional units are not pipelined. An instruction waiting for data on CDB can move to its EX stage in the cycle after the CDB broadcast. The instructions are:

I1: ADDI R1, R1, #8
I2: DIV R3, R2, R1
I3: MUL R4, R1, R3
I4: DIV R5, R4, R1
Assume the following information about functional units.

Functional unit type	Cycles in EX stage
Integer MUL unit	4
Integer DIV unit	8
Integer ADD unit	1

Show the final RSI also. (5)

5. Consider an in-order MIPS multi-cycle pipeline that supports operand forwarding and executes the following instructions:
I1: LD F1, 0(R2)
I2: LD F2, 8(R2)
I3: FADD F3, F1, F2
I4: SD F3, 8(R2)

If the instruction fetch for I1 starts at clock cycle 1, in which cycle the instruction I4 access memory to store the data? (5)

National Institute of Technology Mizoram
Mid- Semester Examination, Odd Semester (2022-23)
Advanced Computer Architecture (CSL – 1703)
B.Tech Semester - 7th Full Marks - 30 Duration - 1:30 hours

28/30

Answer all 3(Three) Questions. All Questions carry same marks
(3 * 10 = 30 Marks)

1. a) A new floating-point unit speeds up floating point operations by two times. In an application one fifth of the instructions are floating-point operations.
   i) What is the overall speedup? (Ignore the penalty to other instructions).
   ii) Assume that the speeding up of the floating-point unit mentioned above slowed down data cache accesses resulting in a 1.8x slowdown. Assume the load instructions constitute 20% and store instructions constitute 8% of the total instruction what is the effective overall speedup now? (5x2)

Or

b) Draw Flynn's Taxonomy and provide brief example for each classification. (5)

c) Briefly mention the issues in Longer Latency Pipelines and how are they avoided? (5)

2. a) What are the different types of Data Hazards possible in a multi cycle pipeline? Give example of each. (1+4)

b) Given an instruction pipeline running at 1GHz that takes 5 cycles to finish an instruction. 30% memory instructions result in a stall of 50 cycles. Assume a base CPI without stalls as 1 and there are 10% memory instructions, what is the effective CPI? (5)

Or

c) What do you mean by 'Loop unrolling'? What are its advantages and disadvantages? Unroll the following loop and represent the code. (2+2+1)

```
for (i=0 ; i<100 ; i++)
  g();
```

d) Differentiate among 'Anti-dependence' and 'Output dependence' with example. (5)

3. a) Explain briefly how 'Strip mining' helps in Loop Unrolling. (5)

b) What is the clock cycle latency you obtain between one 'FP ALU operation' and 'Store Double' operation? Explain with an example. (5)

Or

a) What are the various performance metrics for measuring the performance of CPU? How SPEC benchmark suite plays its role in the above? (2+3)

b) What do you mean by Control Dependence of a line of code on another? Why is it important to analyse? (5)

BT19CS012

National Institute of Technology Mizoram

End – Semester Examination, Odd Semester - 2022

Advanced Computer Architecture (CSL 1703)

B.Tech 7th Semester **Full Marks: 50** **Duration: 3:00 hours**

All questions are Compulsory. All Questions Carry the Same Marks
(5 × 10 = 50 Marks)

1. a) What is Vector Chaining?
b) Give an example of data hazard even with operand forwarding.
c) How structural hazards are avoided in pipelining?
d) State the difference between 1-bit and 2-bit brach predictor.
e) Which of the following can be a valid instruction for an Accumulator machine? Explain your answer.
(A) Load B. (B) Push B (C) Load R, B (D) Add R, B

2
a) What is Cache Coherence? What are the different techniques to deal with it? Explain briefly. (2.5x2)
b) Describe any two different RAID levels of magnetic disk design. Mention the advantages and disadvantages of each. (2.5x2)

3.
a) How reservation station is helpful in Dynamic Scheduling? Give example. (5)
b) What is Branch Target Buffer(BTB)? With a neat diagram explain the steps when using BTB for a five stage pipeline. (5)

4.
a) Compare between Scalar code and Vector code in terms of no of cycles required for the following code (6)

```
For i = 0 :to 49
  C[i] = (A[i] + B[i]) / 2
```

b) Mention the different techniques to optimise the performance of cache? (4)

5.
a) A new multimedia unit (MU) that is added in a processor speeds up the completion of multimedia instructions given to the processor by 4 times. Assuming a program has 40% multimedia instructions, what is the overall speedup gained while running the program when it is executed on the processor with the new MU than when it is run on the processor without this MU? (5)

b) With neat diagram differentiate among Centralised shared memory and distributed memory multiprocessor. (5)