

Introduction to K2E Devices

KeyStone Training

Multicore Applications

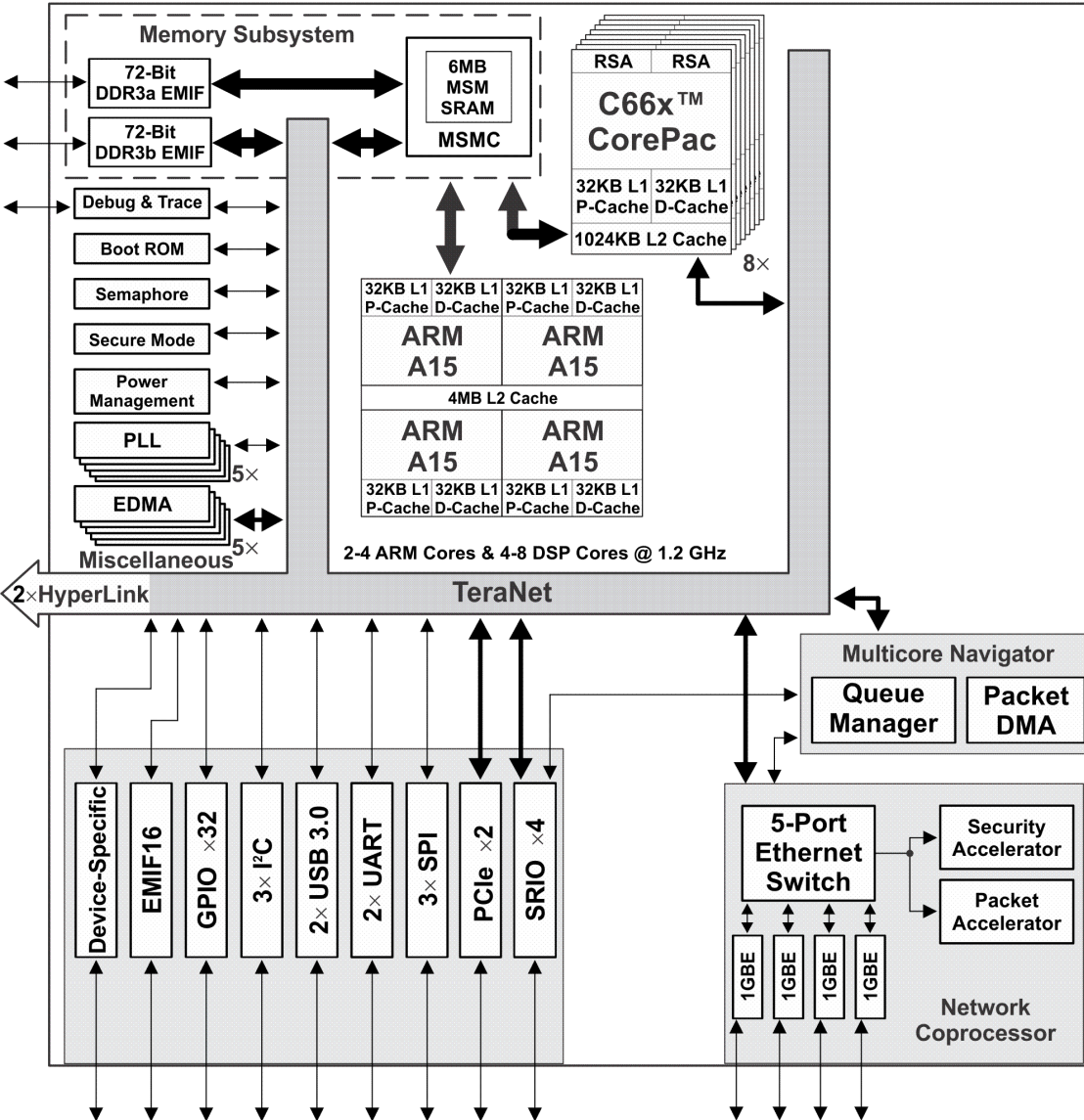
Ran Katzur, Senior Applications Engineer, Training Lead

Agenda

- KeyStone Device Overview
- Introducing K2E (Edison)
- K2E Software
- For More Information

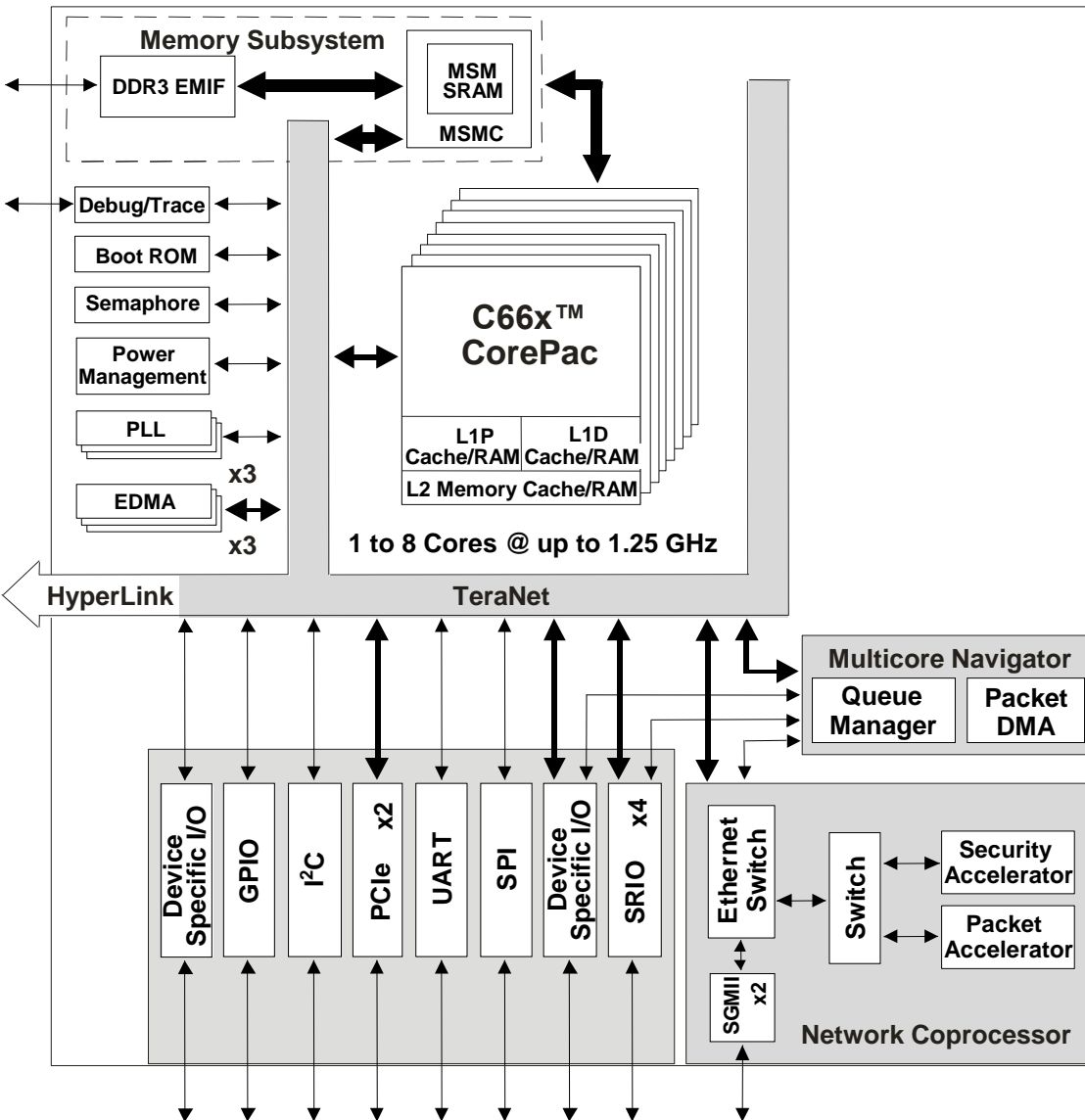
KeyStone Device Overview

Keystone II: K2H/K2K Devices



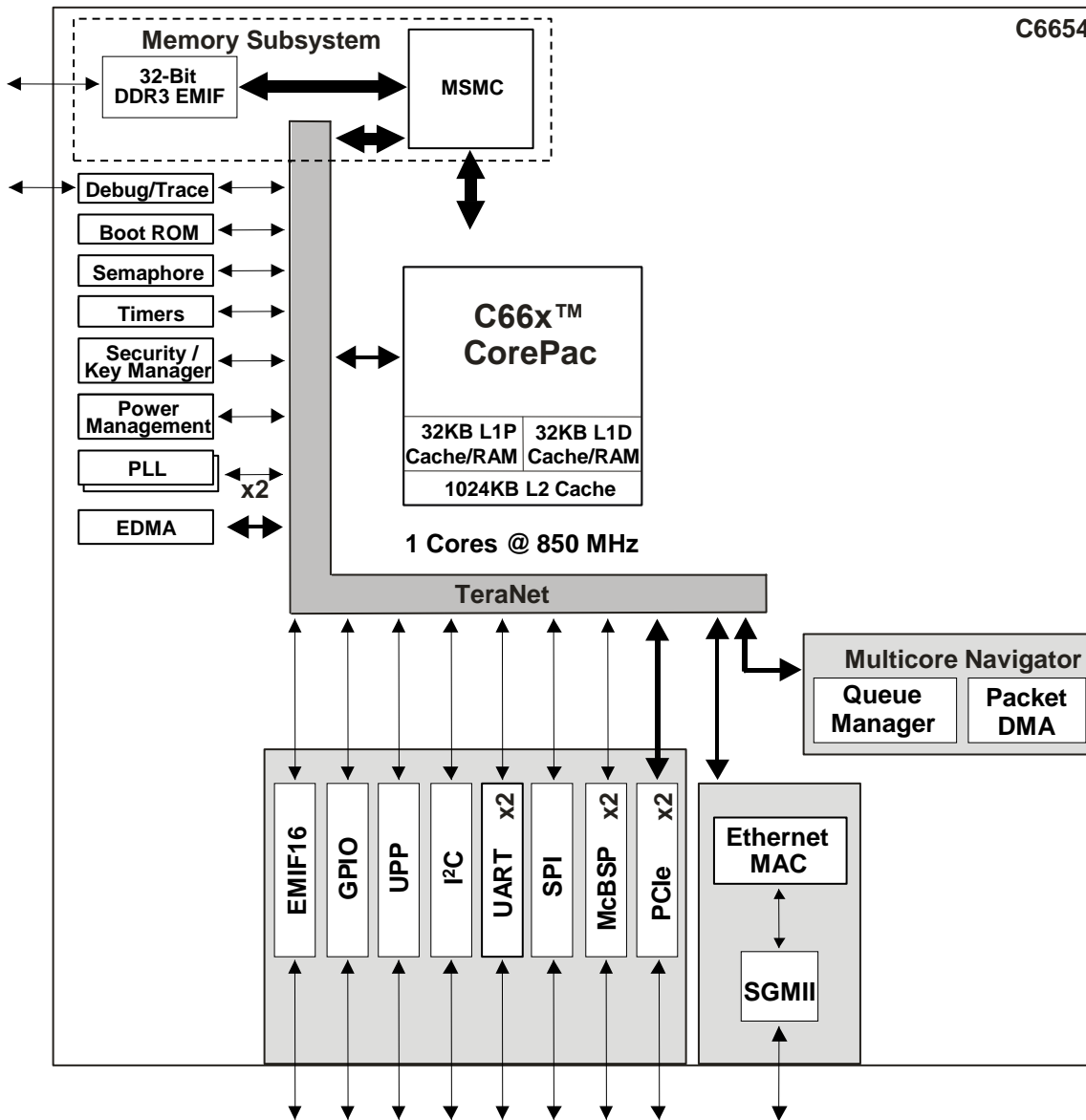
- High-performance ARM + DSP
- Memory Subsystem:
 - Multi-bank shared memory
 - 32- to 36- (40) bit translation
 - Smart access arbitration
 - Error detect/protect/correct
- Multicore Navigator: HW routing
- NETCP: HW acceleration
- Lots of connectivity:
 - High bit-rate peripherals: SRIO, PCIe, Ethernet
 - Device-specific: TSIP
 - HyperLink: Seamless interface
- TeraNet:
 - Non-blocking
 - Smart arbitration
 - Fast and wide

Keystone I: C667x Devices



- High end of the market for signal processing:
 - Amazing performance
 - Great SOC features
- Challenges for broad market:
 - Power consumption 10-15W
 - Prices reflect performance

Keystone I: C665x Devices (Gauss)

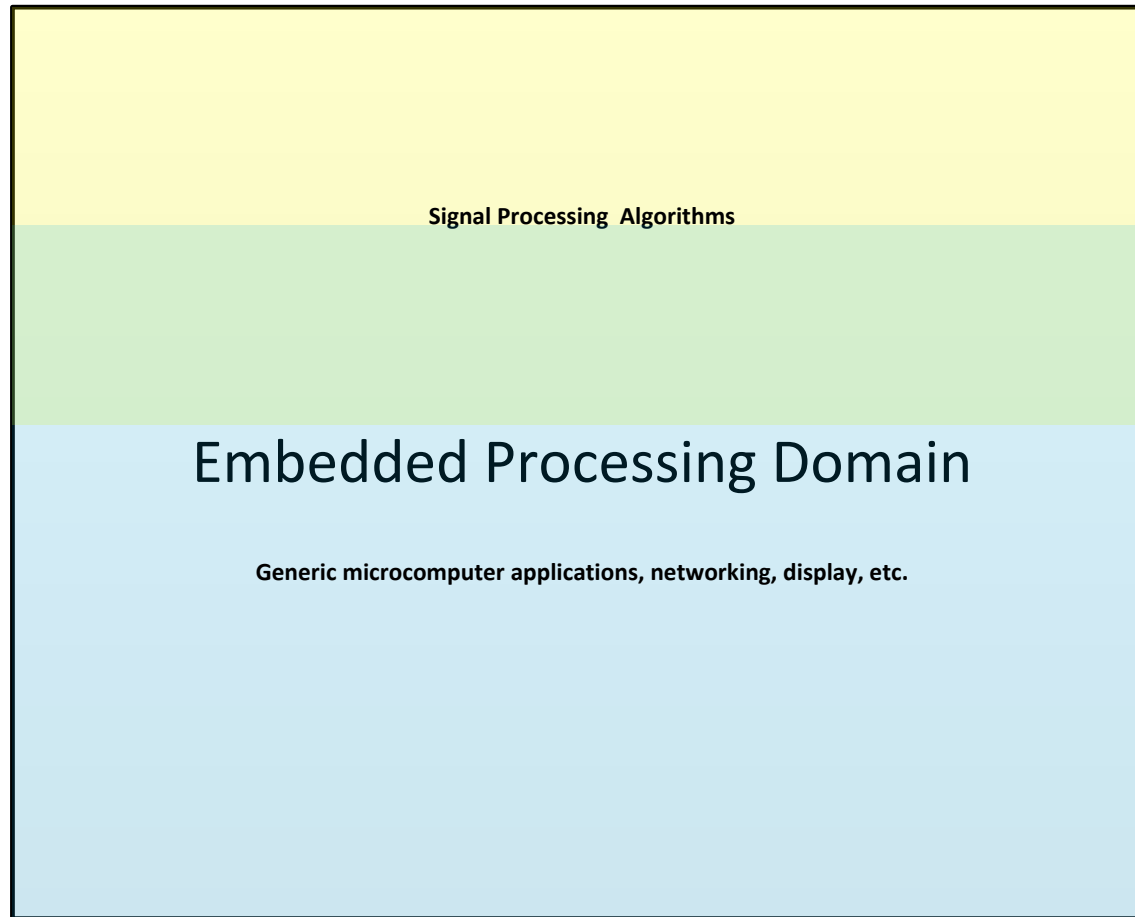


- Signal Processing Engine
- **Maintains most advantages of KeyStone, except:**
 - Few, more generic, accelerators
 - No NETCP
 - No TSIP, but McBSP
 - Smaller, slower DDR, less pins

Typical applications:

- Power limitations (sealed box)
- Performance requirements that can be achieved with 1-2 DSP cores
- No requirement for accelerators or TSIP
- Smaller DDR requirements

Embedded Processing Domain

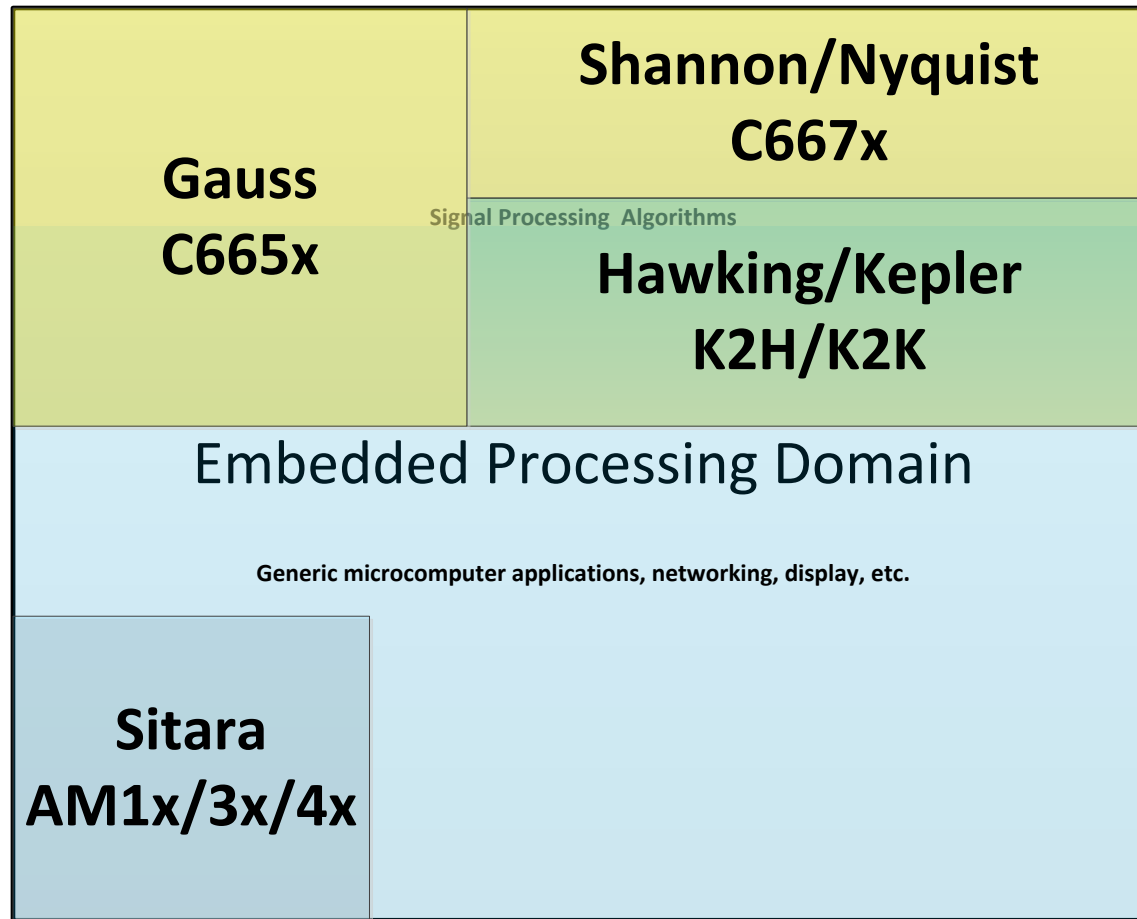


Low-End
Power/Cost/Performance

High-End
Power/Cost/Performance

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TI Embedded Processing Devices



Low-End
Power/Cost/Performance

High-End
Power/Cost/Performance

Introducing K2E (Edison)

K2E Features Summary

- Powerful Quad-ARM A15 CorePac with 0-1 DSP CorePac support, as needed
- Robust Ethernet options:
 - Up to 2 ports 10G and 8 ports 1G
 - Multiple MDIOs support multiple physical Ethernet interfaces
- Optimized external data movement:
 - Standard high-bit rate interfaces: Ethernet and PCIe (No SRIO)
 - EDMA and Multicore Navigator
- Optimized internal traffic, priorities, arbitrations
 - TeraNet bus
 - MSMC
- Fast (1600 MHz), wide (72 bits), and large (8G) external memory; DDRA only

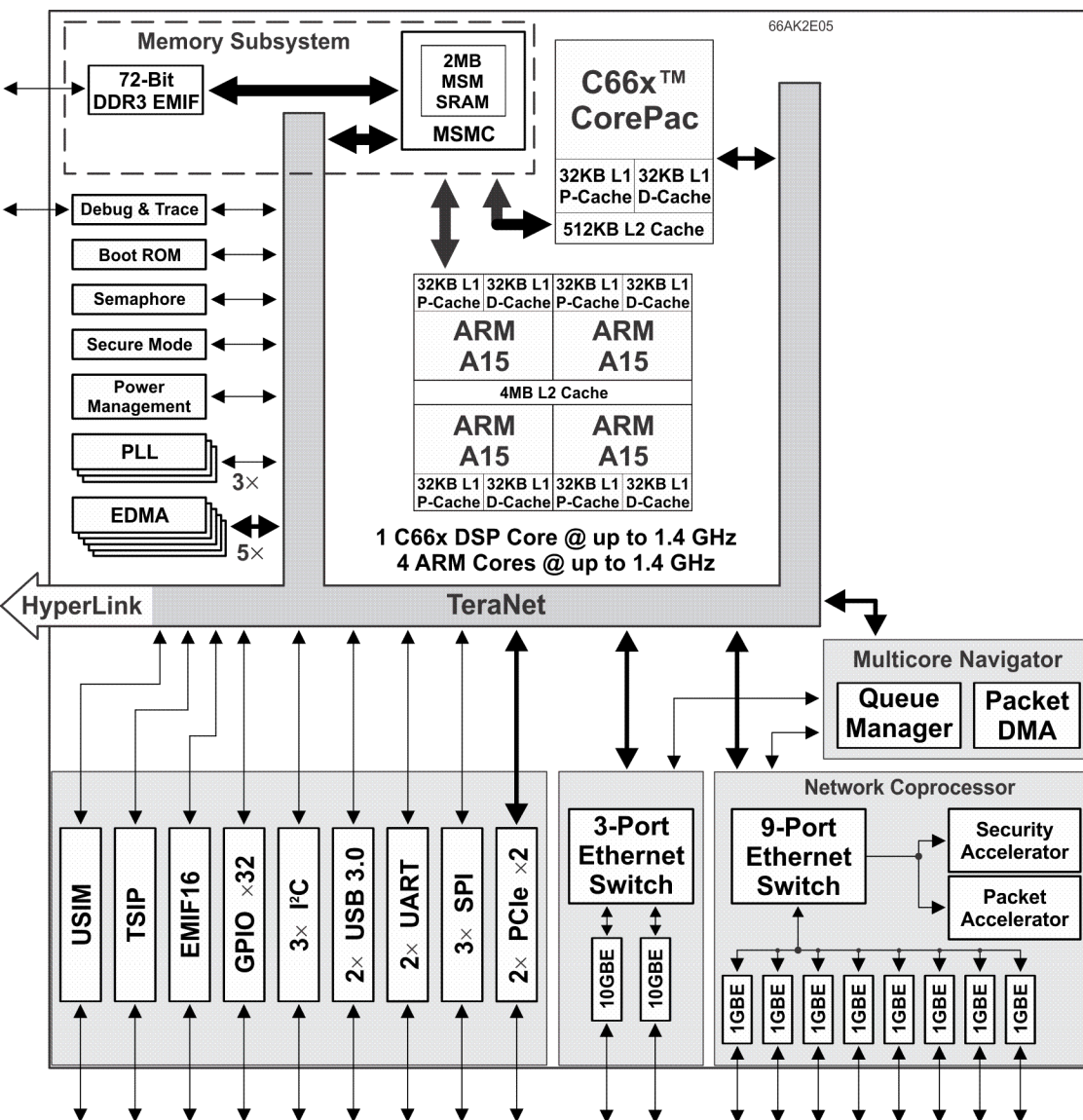
Comparing K2H and K2E Architecture

	K2H	K2E
ARM CorePacs	2 or 4	1, 2, or 4
DSP CorePacs	4 or 8	0 or 1
DSP Maximum Clock	1.2 GHz	1.4 GHz
External Memory	DDRA and DDRB	DDRA only
MSMC Memory (Shared L2)	6 MB	2 MB
PLL	5x	3x
SRIO	4x (20 Gbaud)	NA
Multicore Navigator	2 QMSS (16K queues)	Single QMSS (8K queues)
Hyperlink	2x	1x
5-Port 1GB Switch	1x	1-2x
3-Port 10GB Switch	NA	1x
USIM (Universal Subscriber Identity Module)	NA	1x
TSIP	NA	1x
USB 3.0	1x	2x
Secure Mode	No	Yes
MDIO	1x	3x

Typical K2E Application Requirements

- Small, medium, or large I/O bandwidth
- Efficient signal-processing calculations; Fixed-point or floating-point or both
- Efficient power and performance:
 - ARM A15 has high processing-to-power ratio
 - NETCP offloads network processing
- Communication and networking interfaces
 - 2x 10G and 8x 1G
 - 2x PCIe and 3x USB

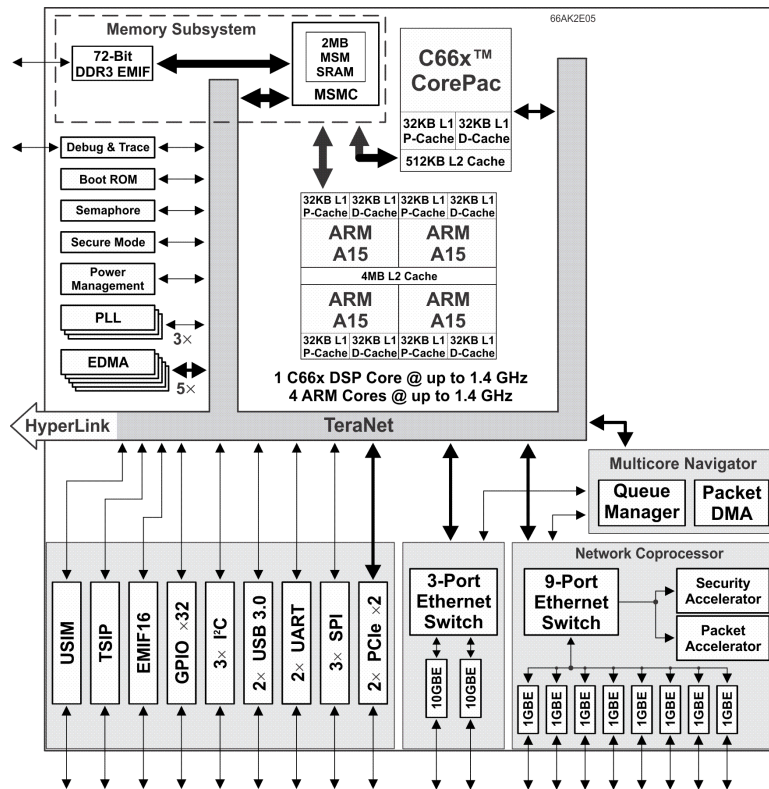
66AK2E05 Key Features



- Powerful microcomputer with DSP coprocessor
- Quad-ARM A15 CorePac
- 1x Queue Manager supports up to 8K queues
- 1x Network Coprocessor (NETCP)
- 1x 3-port 10GBE Switch Subsystem
- 10 Ethernet ports:
 - 2x 10G
 - 8x 1G
- Telecommunications Serial Port (TSIP)
- 2x PCIe and 2x USB 3.0 to support solid-state drive

66AK2E05 Applications

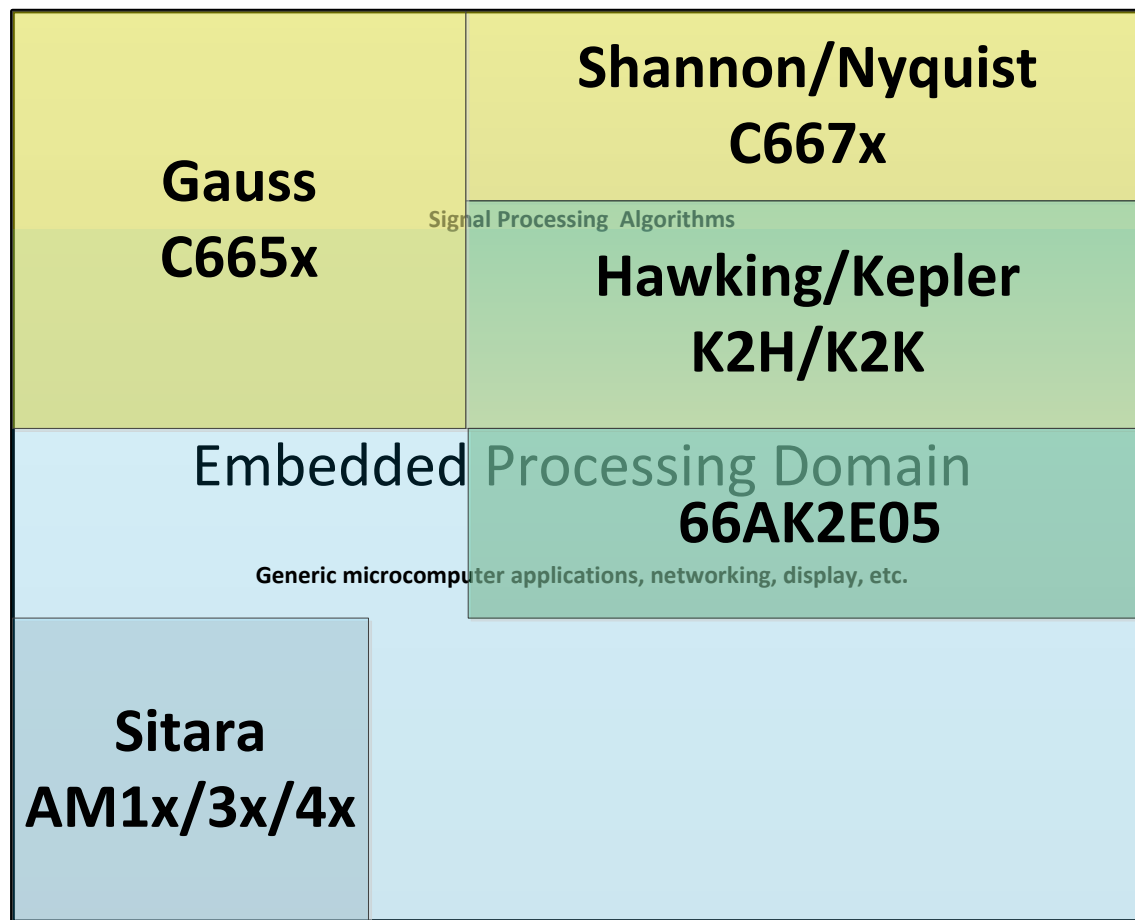
- Communication and networking
- Fast hard-disk storage (PCIe, USB)
- Imaging, including analytics
- Example: Defense communication systems



Advantages

- Integrated SOC solution
- High-speed communication and disk bandwidth for data storage
- DSP enables on-the-fly data processing
- Ability to scale up using HyperLink, or scale down using 66AK2E02
- Low power (compared to other solutions)

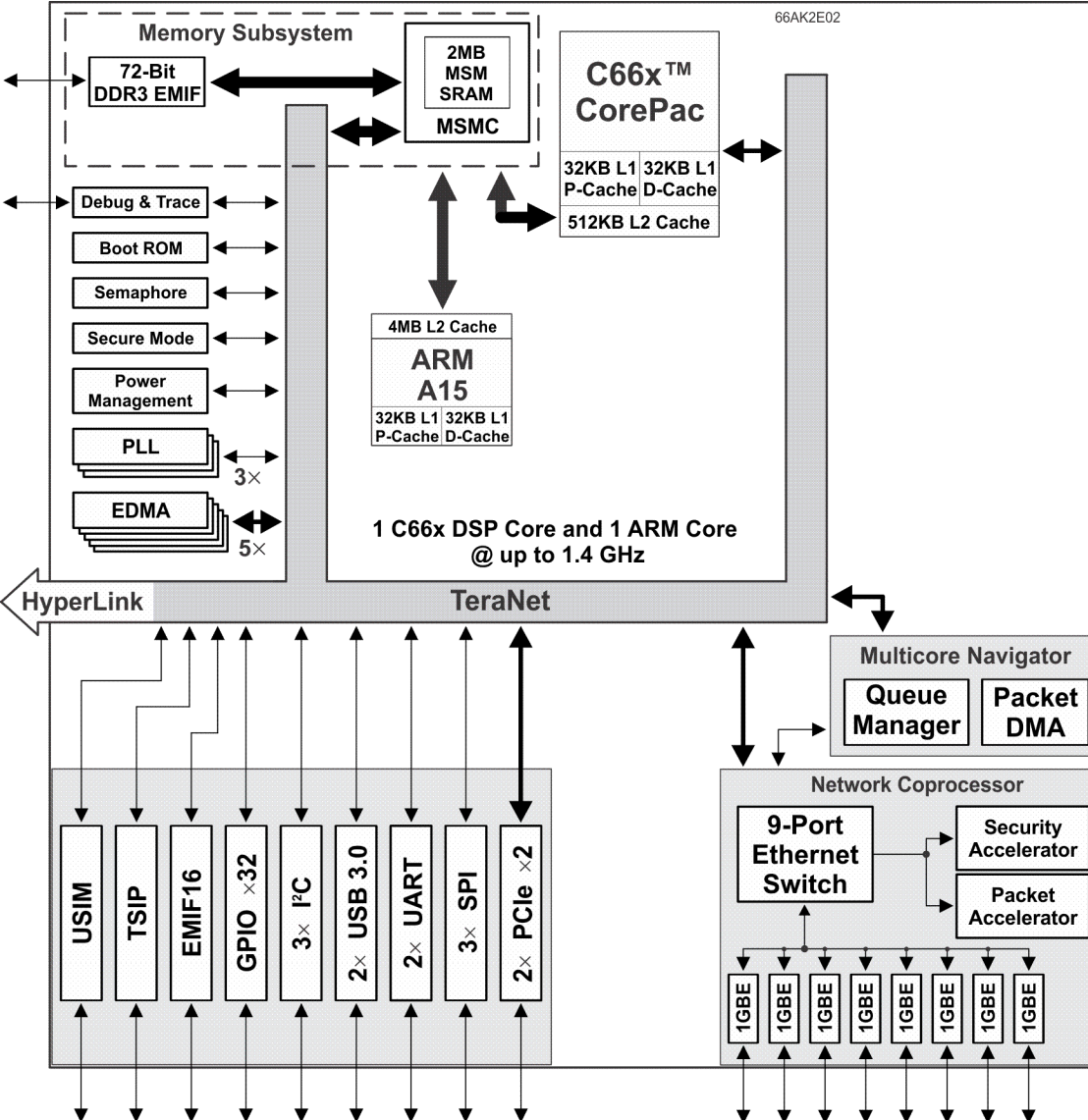
TI Embedded Processing Devices



Low-End
Power/Cost/Performance

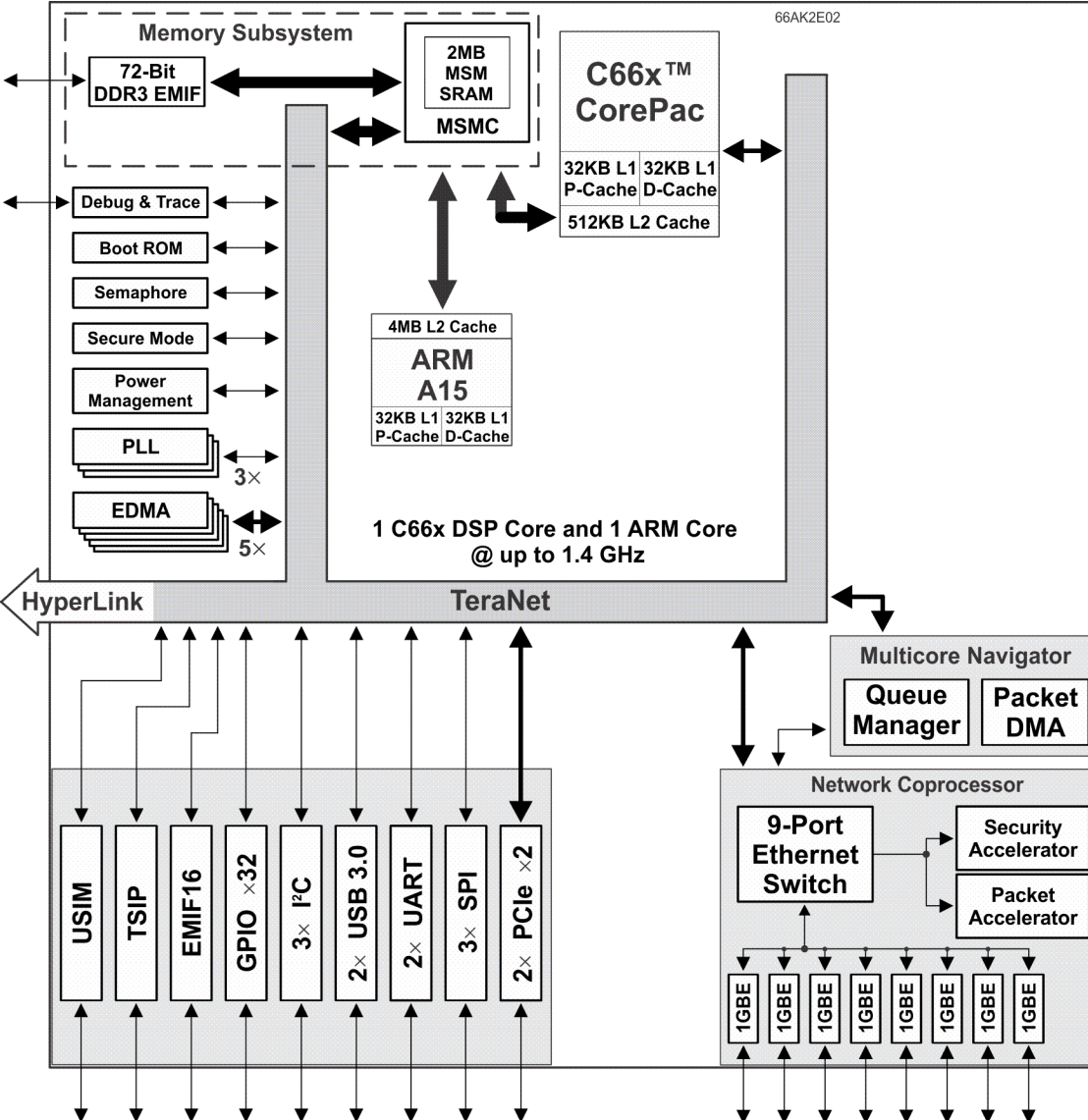
High-End
Power/Cost/Performance

66AK2E02 Key Features



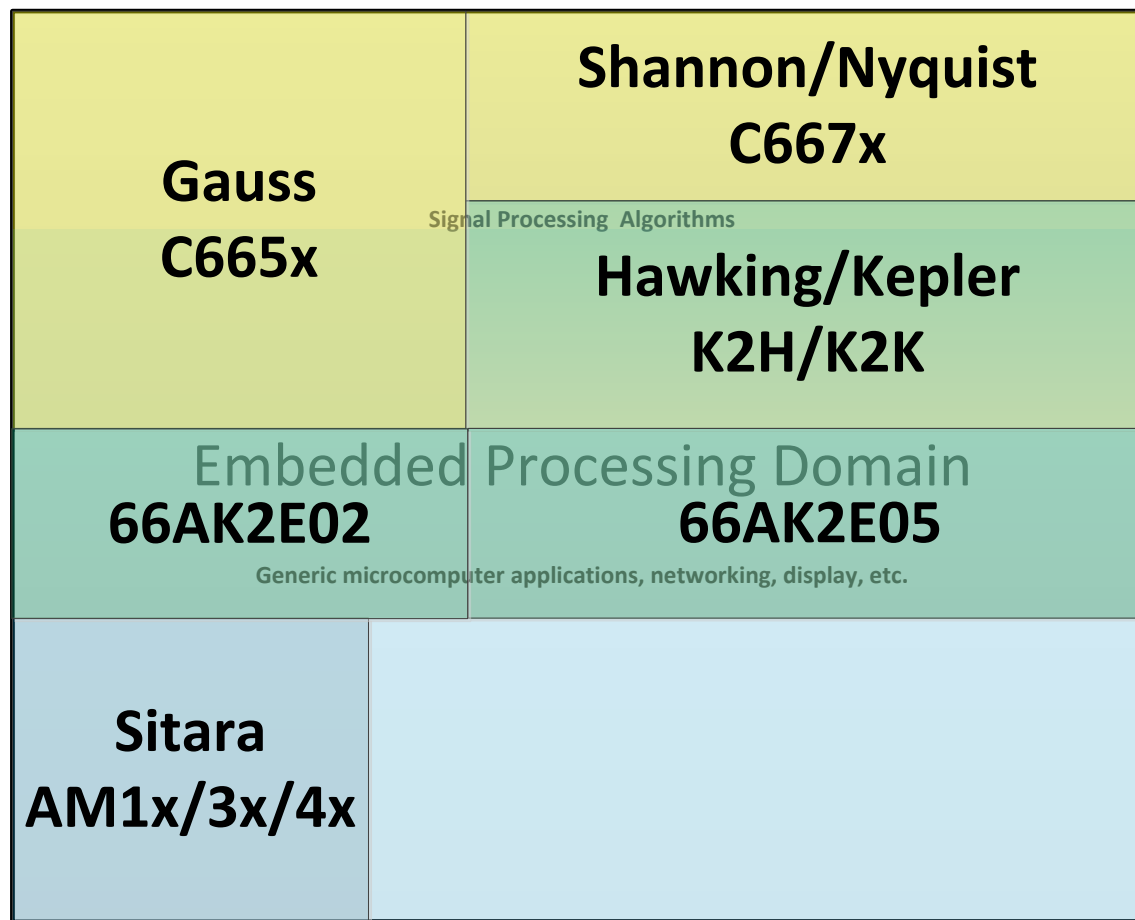
- Scaled-down version of 66AK2E05
- High connectivity, but does not have 10GBE
- 2x PCIe and 2x USB 3.0 enables fast disk storage
- Communication, storage with some analytics

66AK2E02 Applications



- Smart Grid and Smart Metering
- Factory automation
- Building control
- Aerospace and defense
- Industrial networking and Fieldbus protocols (IEC 61158)
- Medical imaging

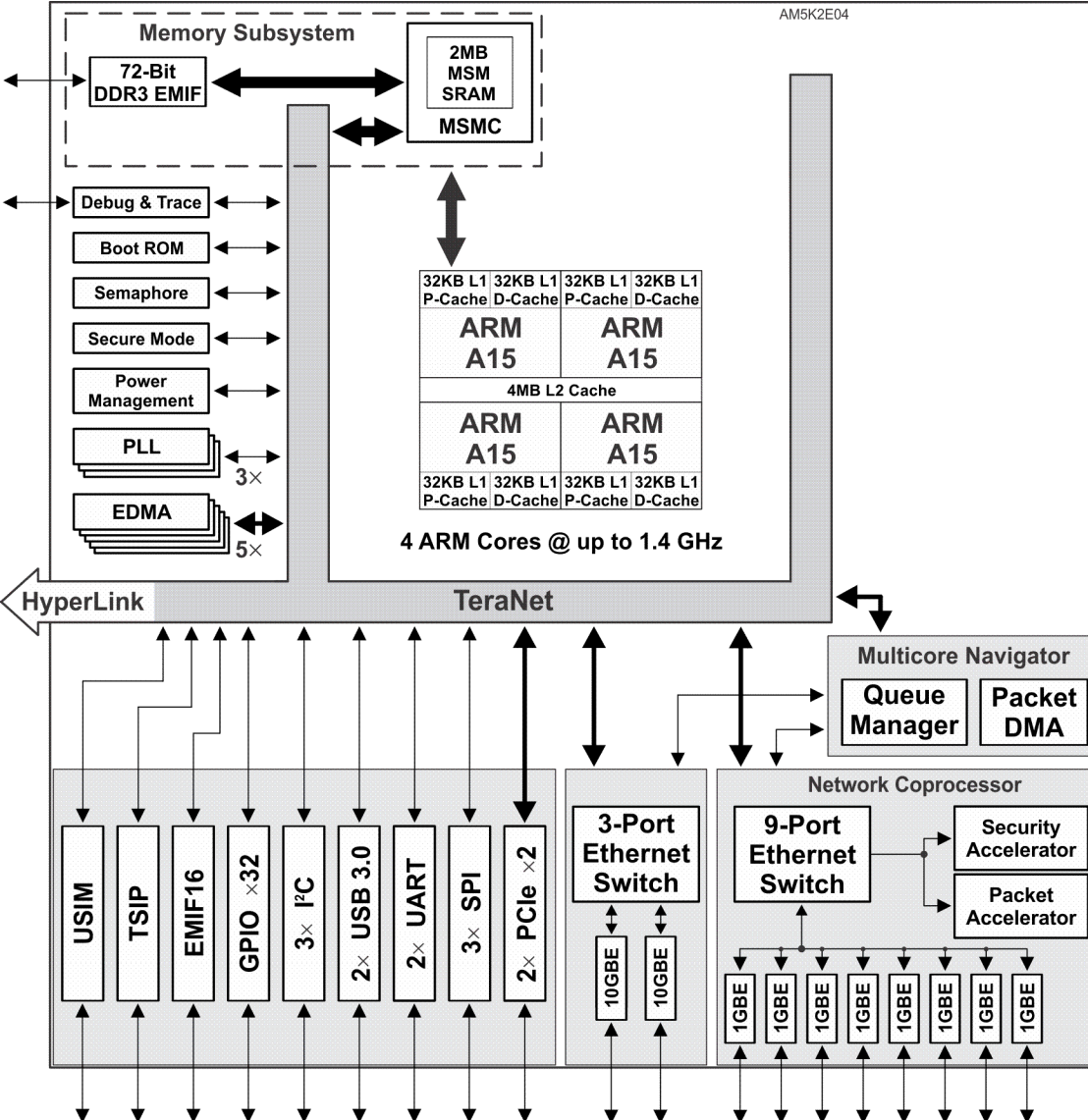
TI Embedded Processing Devices



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Power/Cost/Performance

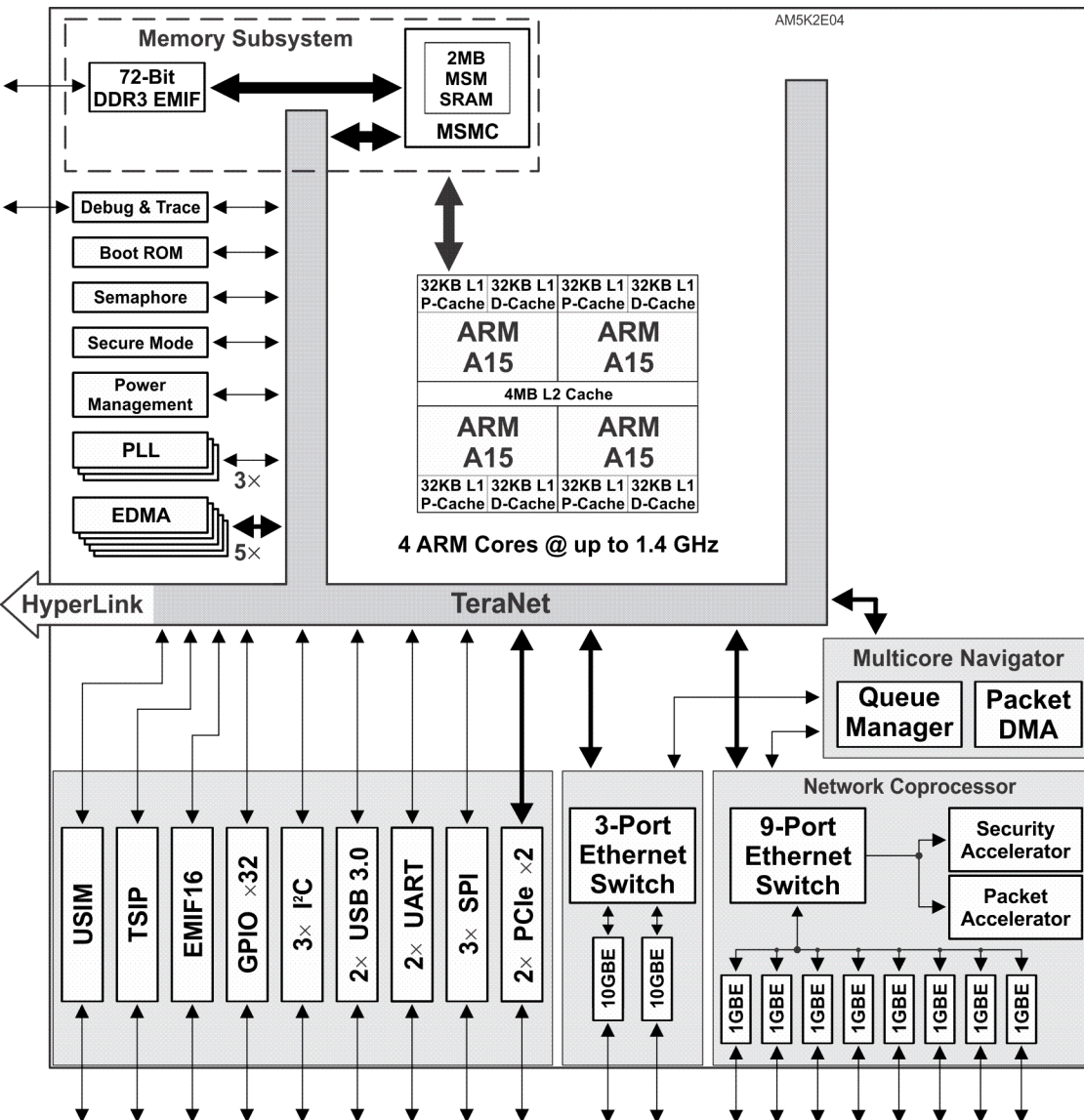
High-End
Power/Cost/Performance

AM5K2E04 Key Features



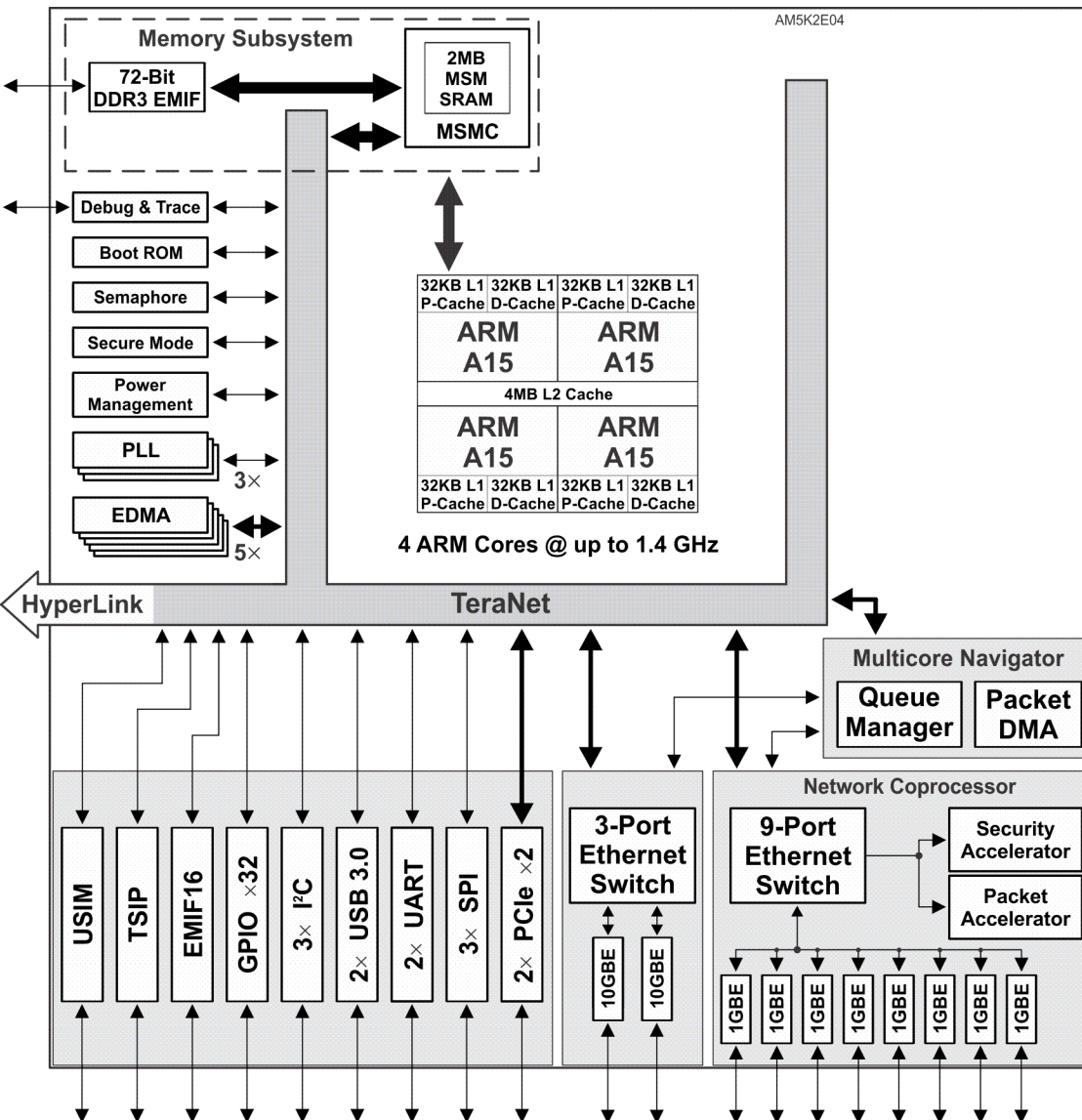
- ARM-only TI multicore device (First in the KeyStone architecture)
- Quad-ARM A15 CorePac
- 1x Queue Manager supports up to 8K queues
- 1x Network Coprocessor (NETCP)
- 1x 3-port 10GBE Switch Subsystem
- Telecommunications Serial Port (TSIP)
- 2x PCIe and 2x USB 3.0 to support solid-state drive

AM5K2E04 Applications



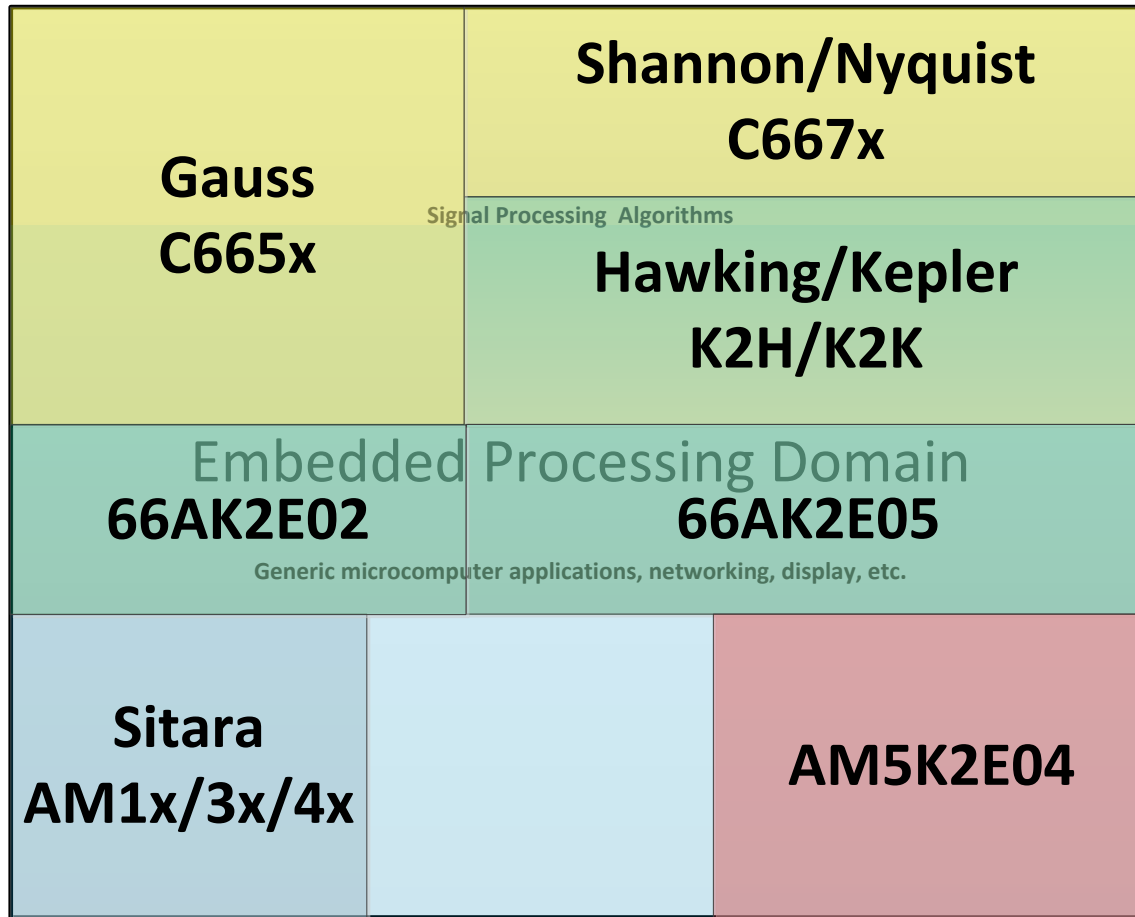
- Networking:
 - Enterprise
 - Service Provider
 - Data Center/Cloud
 - Industrial network and Fieldbus protocols (IEC 61158)
- Other industrial applications that do not require DSP

AM5K2E04 Wins



- Defense Munitions
 - Power efficiency
 - High-performance processing
 - Large amount of internal memory
 - Efficient ARM instructions
- Flight Control Panel
 - High-performance, Linux-based processor
 - Open-source applications available
 - Efficient memory and internal bus utilization (MSMC, TeraNet)
 - Support for big Endian

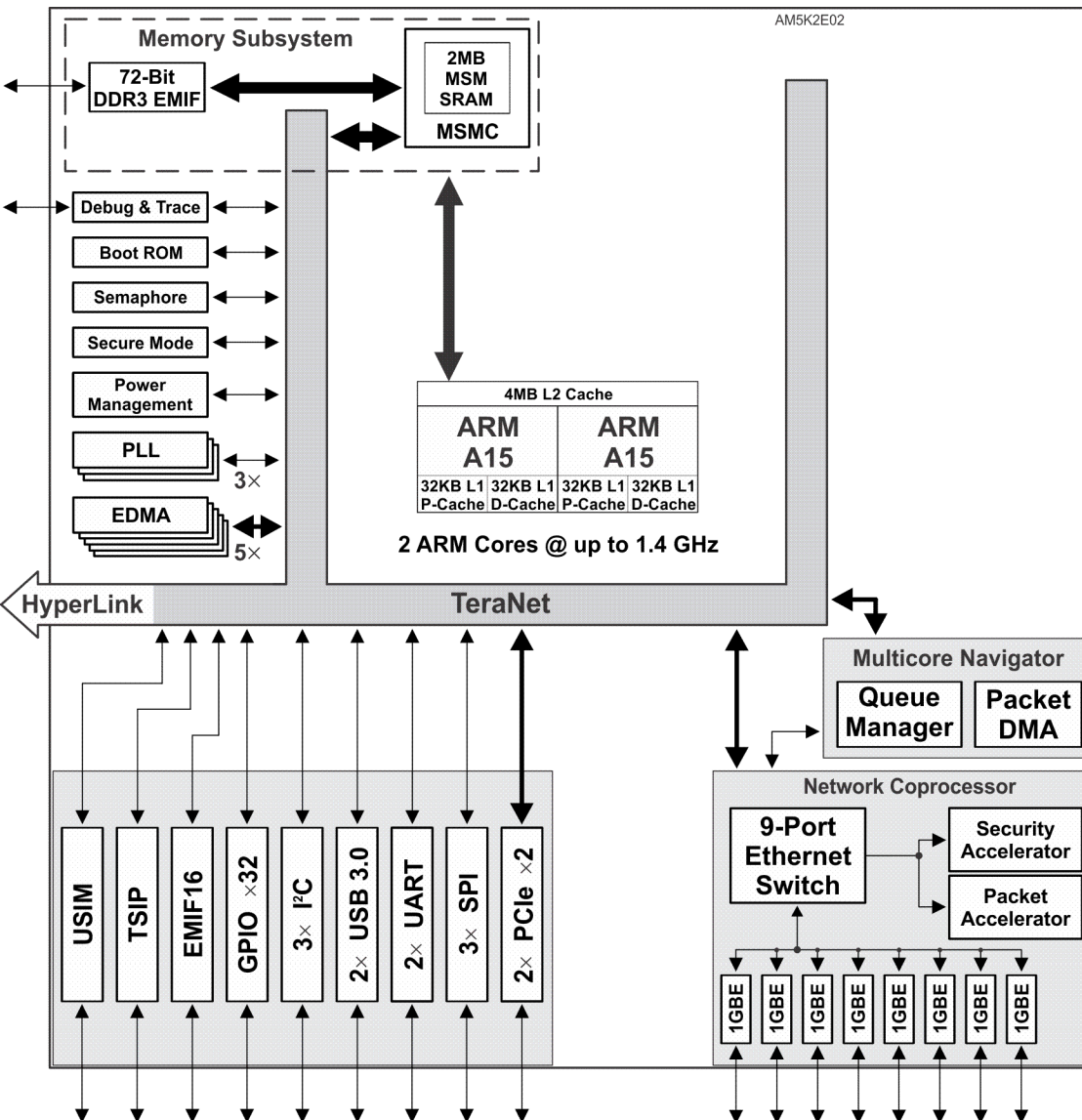
TI Embedded Processing Devices



Low-End
Power/Cost/Performance

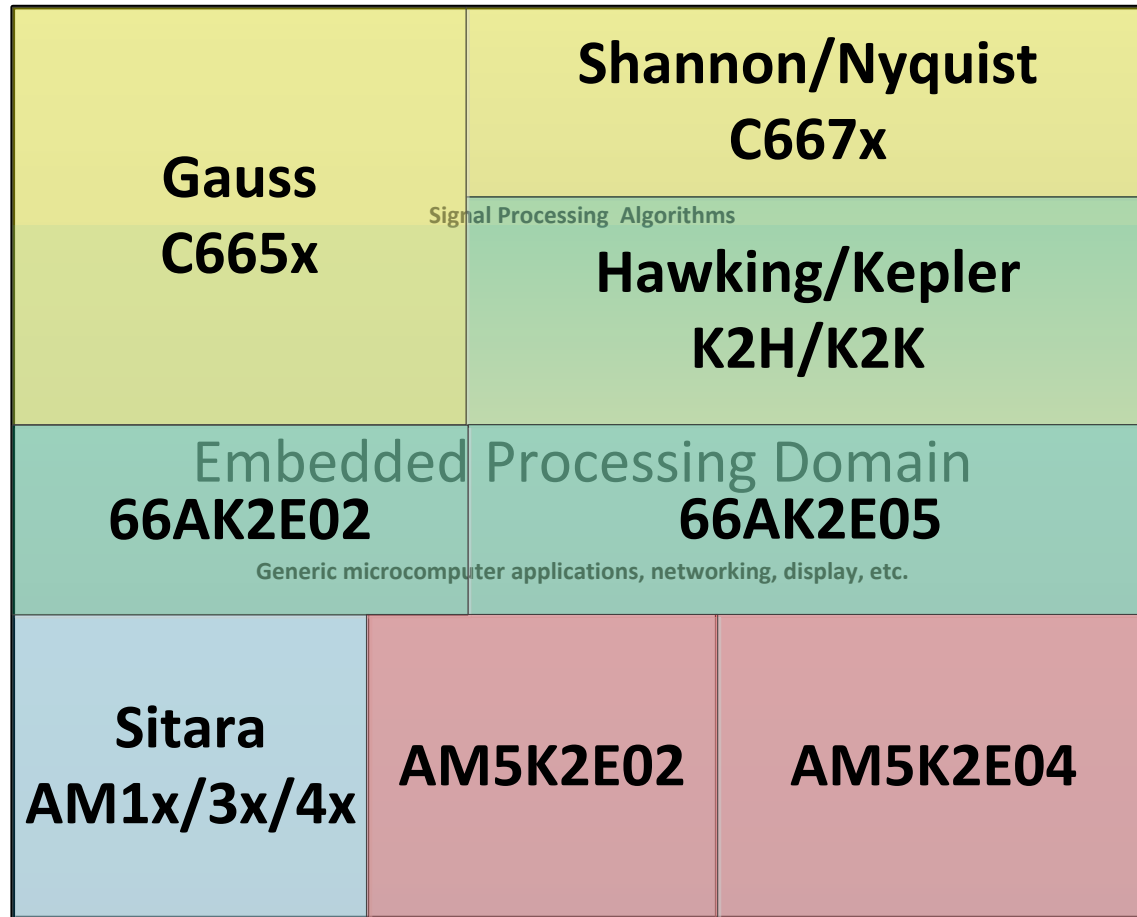
High-End
Power/Cost/Performance

AM5K2E02 Key Features/Applications



- Scaled-down version of AM5K2E04
- Dual-ARM A15 CorePac
- 1x NETCP
- 10GBE not included
- Supports low-end applications of AM5K2E04

TI Embedded Processing Devices



Low-End
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Power/Cost/Performance

K2E Software

K2E Software Support

MCSDK _03_01_XX supports K2E and K2L (also, K2K and K2H):

- Contiguous memory (cmem) allocation for ARM User Space enables internal and external DMA-based communication.
- User Space IO (UIO) driver support for mmap interface, interrupt handling, and chip power control
- TSIP LLD:
`MCSDK_3_1_0_2\pdk_keystone2_3_01_00_02\packages\ti\drv\tsip`
- mmap LLD:
`MCSDK_3_1_0_2\pdk_keystone2_3_01_00_02\packages\ti\runtime\mmap`
- Automatic setting of EVM frequency based on the chip EFUSE value instead of environment variable in Uboot

For More Information

- Datasheets:
 - 66AK2E05/02: <http://www.ti.com/lit/SPRS865>
 - AM5K2E04/02: <http://www.ti.com/lit/SPRS864>
- Product Folders:
 - 66AK2E05: <http://www.ti.com/product/66ak2e05>
 - 66AK2E02: <http://www.ti.com/product/66ak2e02>
 - AM5K2E04: <http://www.ti.com/product/am5k2e04>
 - AM5K2E02: <http://www.ti.com/product/am5k2e02>
- For questions regarding topics covered in this training, visit the support forums at the [TI E2E Community](#) website.