KeyStone Training

Network Coprocessor (NETCP) Overview

Agenda

- What is NETCP?
- Purpose of the NETCP
- NETCP Block Diagram
- Internet Protocol Classification Levels
- Communication with the NETCP

NETCP Subsystem Overview

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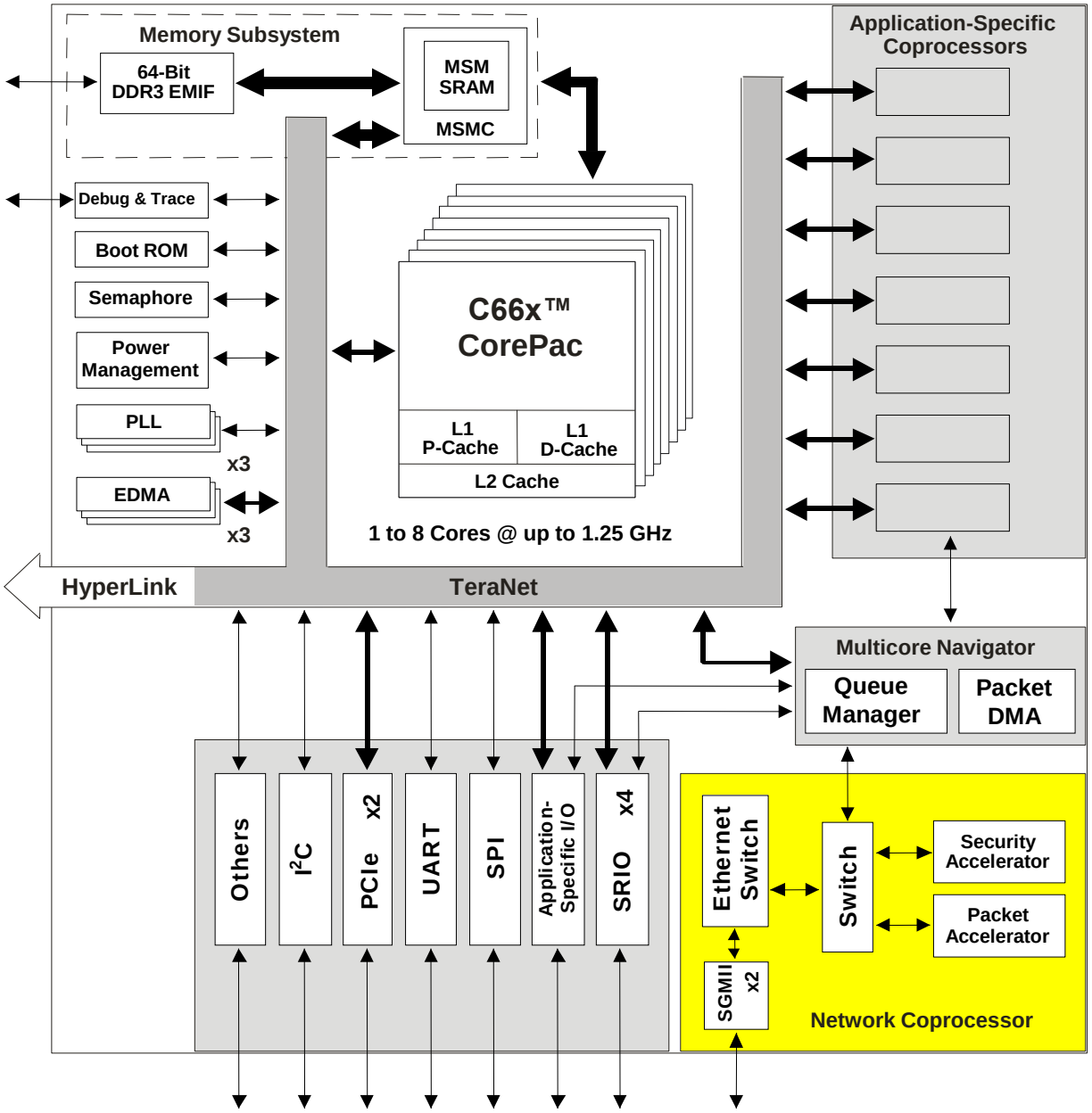
What is the Network Coprocessor (NETCP)?



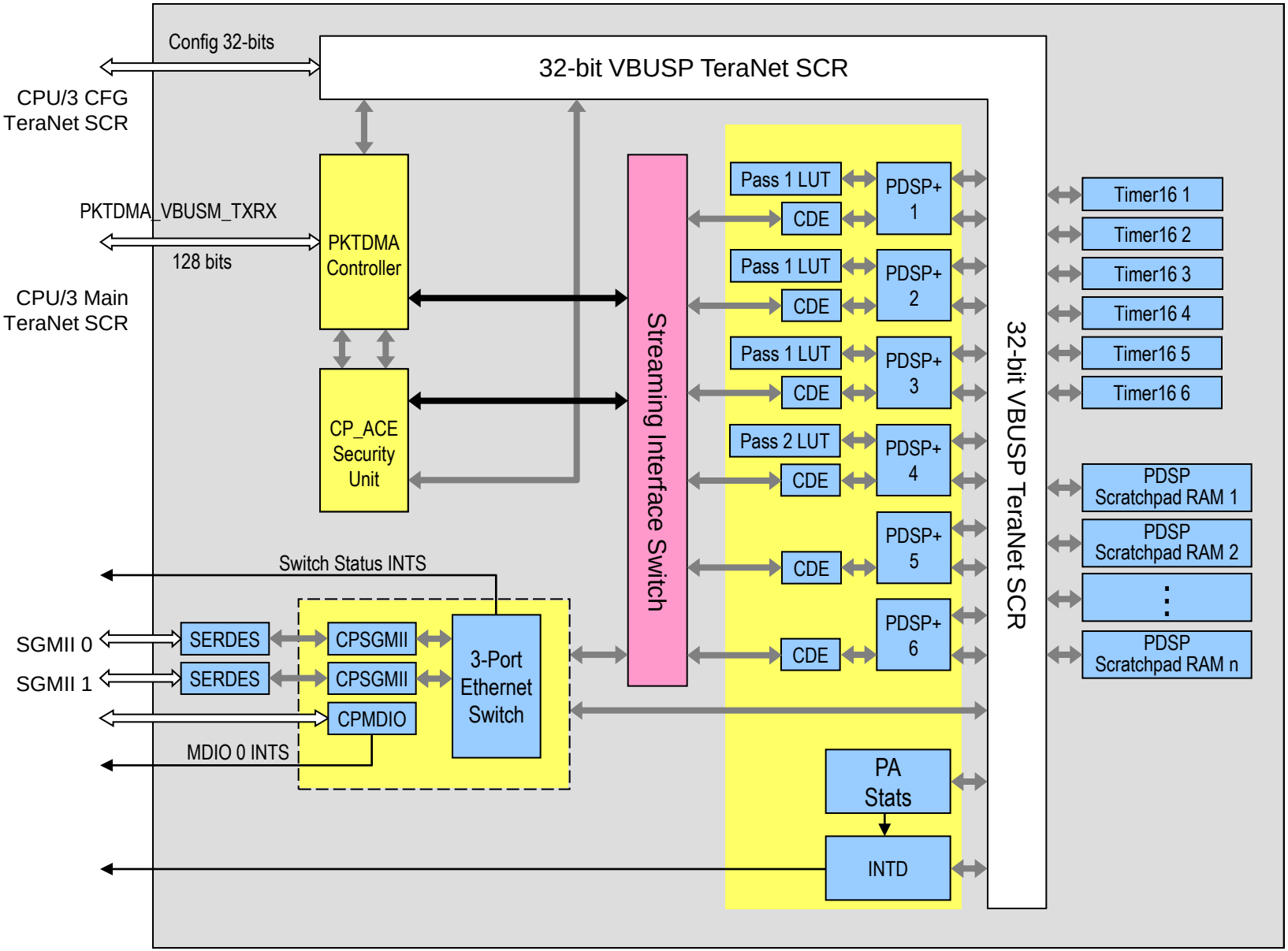
Network Coprocessor consists of the following modules:

- Packet Accelerator (PA)
- Security Accelerator (SA)
- Ethernet Subsystem
- Packet DMA (PKTDMA) Controller

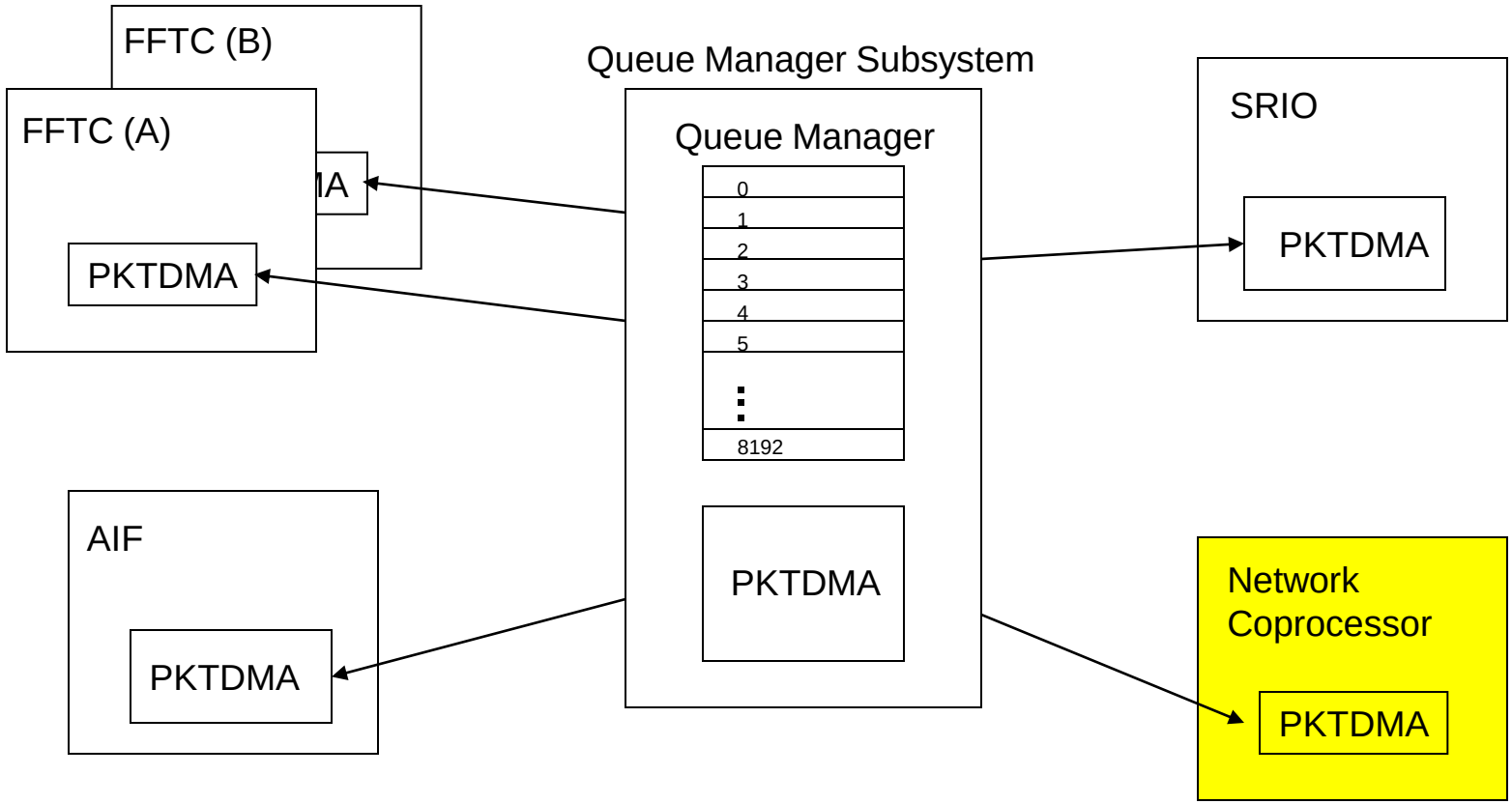
Purpose of the Network Coprocessor

- Motivation behind NETCP:
  - Use hardware accelerators to do L2, L3, and L4 processing and encryption that was previously required to be done in software
- Goals for both Packet Accelerator and Security Accelerator:
  - Offload DSP processing power
  - Improve system integration
  - Allow cost savings at the system level
  - Expand DSP usability within current products
  - Allow DSP usage in new product areas
- Security Key applications:
  - IPSec tunnel endpoint (e.g. LTE eNB, ...)
  - Secure RTP (SRTP) between gateways
  - Air interface (3GPP, Wimax) security processing

NETCP Block Diagram



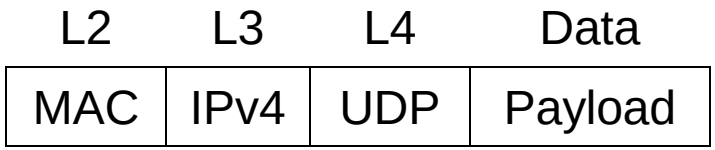
Packet DMA in NETCP



Internet Protocol Classification Layers

- Layer 2 (L2): Media Access Control (MAC) Layer
  - IEEE 802.3 standard
- Layer 3 (L3): Internet Layer
  - Internet Protocol Version 4 (IPv4)
  - Internet Protocol Version 6 (IPv6)
  - Custom L3 Classification
- Layer 4 (L4): Transport Layer
  - User Datagram Protocol (UDP)
  - Transmission Control Protocol (TCP)
  - Custom L4 Classification

Example Packet



Communication with the NETCP

NETCP relies on QMSS and PKTDMA to communicate with the CorePac.

- TX Queue Mapping
  - Q640: PDSP1
  - Q641: PDSP2
  - Q642: PDSP3
  - Q643: PDSP4
  - Q644: PDSP5
  - Q645: PDSP6
  - Q646: SASS0
  - Q647: SASS1
  - Q648: Switch
- RX Queues
  - Can use any general purpose queues (Q864-Q8191)
  - Can also use other special purpose queues (e.g. 704-735)

Table 5-1 Queue Map

Queue Range	Number of Queues	Purpose
0 to 511	512	Low priority accumulation. These 512 queues are divided into 16 groups, each group with 32 continuous queues. Each group is monitored with one interrupt.
512 to 639	128	AIF Tx queues. Each queue has a dedicated queue pending signal which drives a CDMA Tx channel.
640 to 671	32	PA Tx queues. Each queue has a dedicated queue pending signal which drives a CDMA Tx channel.
672 to 687	16	SRIO Tx queues. Each queue has a dedicated queue pending signal which drives a CDMA Tx channel.
688 to 691	4	FFTC Tx queues. Each queue has a dedicated queue pending signal which drives a CDMA Tx channel.
692 to 703	12	General purpose.
704 to 735	32	High priority accumulation. Each high priority queue can be monitored based on watermark, and each queue has an interrupt signals.
736 to 799	64	Queues with starvation counters readable by the host. Starvation counters increment each time a pop is performed on an empty queue, and reset when the queue is not empty (or when the starvation count is read).
800 to 831	32	QMSS Tx queues. Used for Infrastructure (core to core) DMA copies and notification.
832 to 863	32	Generic queues reserved for traffic shaping, if it is configured in firmware to support this feature.
864 to 8191	7328	General purpose. It is not safe to use queue 8191 however, because some CDMA override functions use 0xFFF in the low 12 bits to specify non-override conditions.

End of Table 5-1

PKTDMA TX channels mapped to QMSS PA TX queues

Table 5-2 CDMA Channel Map

CDMA Parameters	QMSS	SRIO	PA	FFTC	AIF
Rx Channels	32	16	24	4	128
Tx Channels	32	16	10	4	128
Rx Flows	64	20	32	8	128

End of Table 5-2

For More Information

- For more information, refer to the Network Coprocessor (NETCP) User Guide.
  http://www.ti.com/lit/SPRUGZ6
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website.