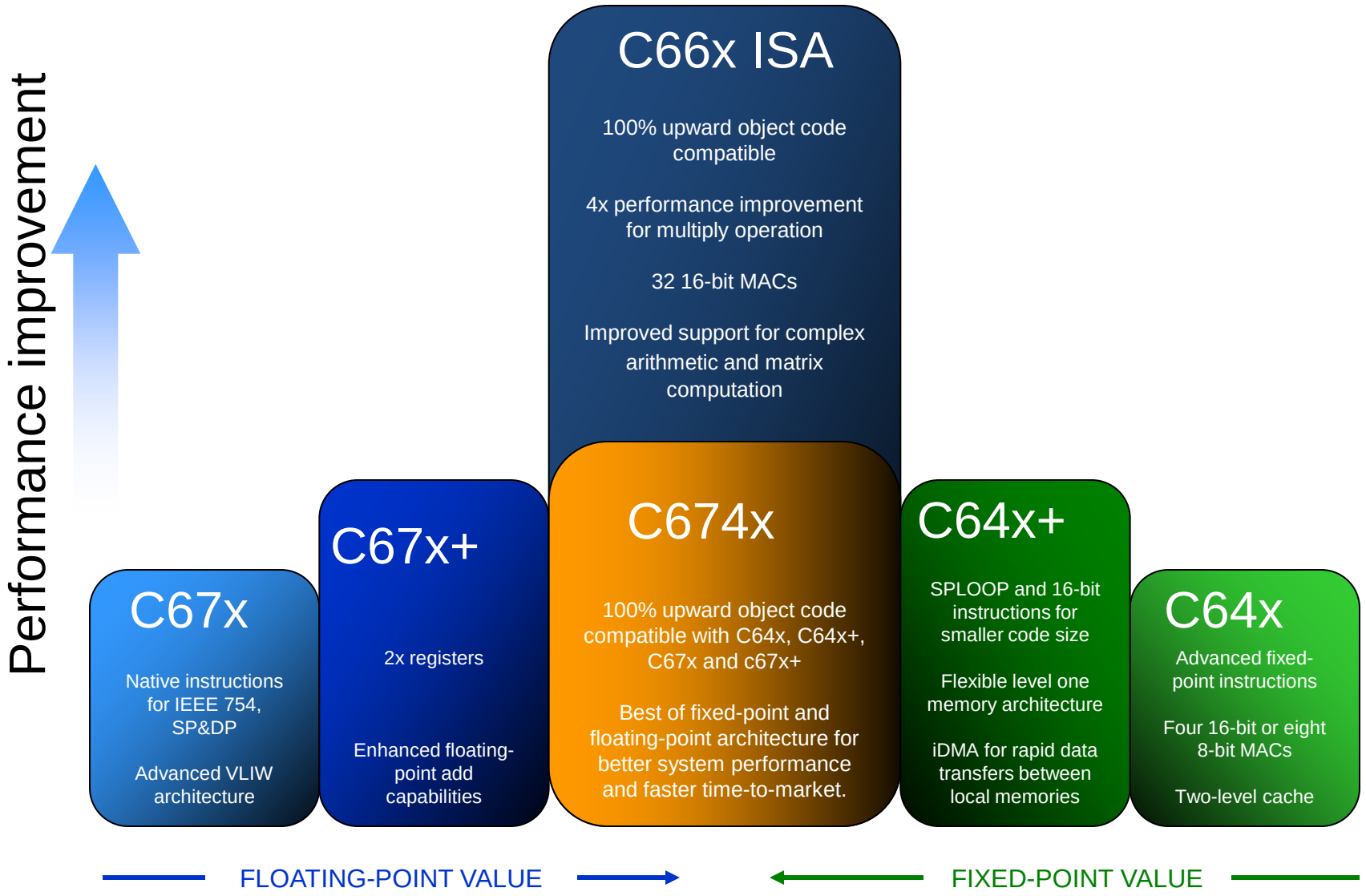
KeyStone C66x Multicore SoC Overview

Multicore Applications Team

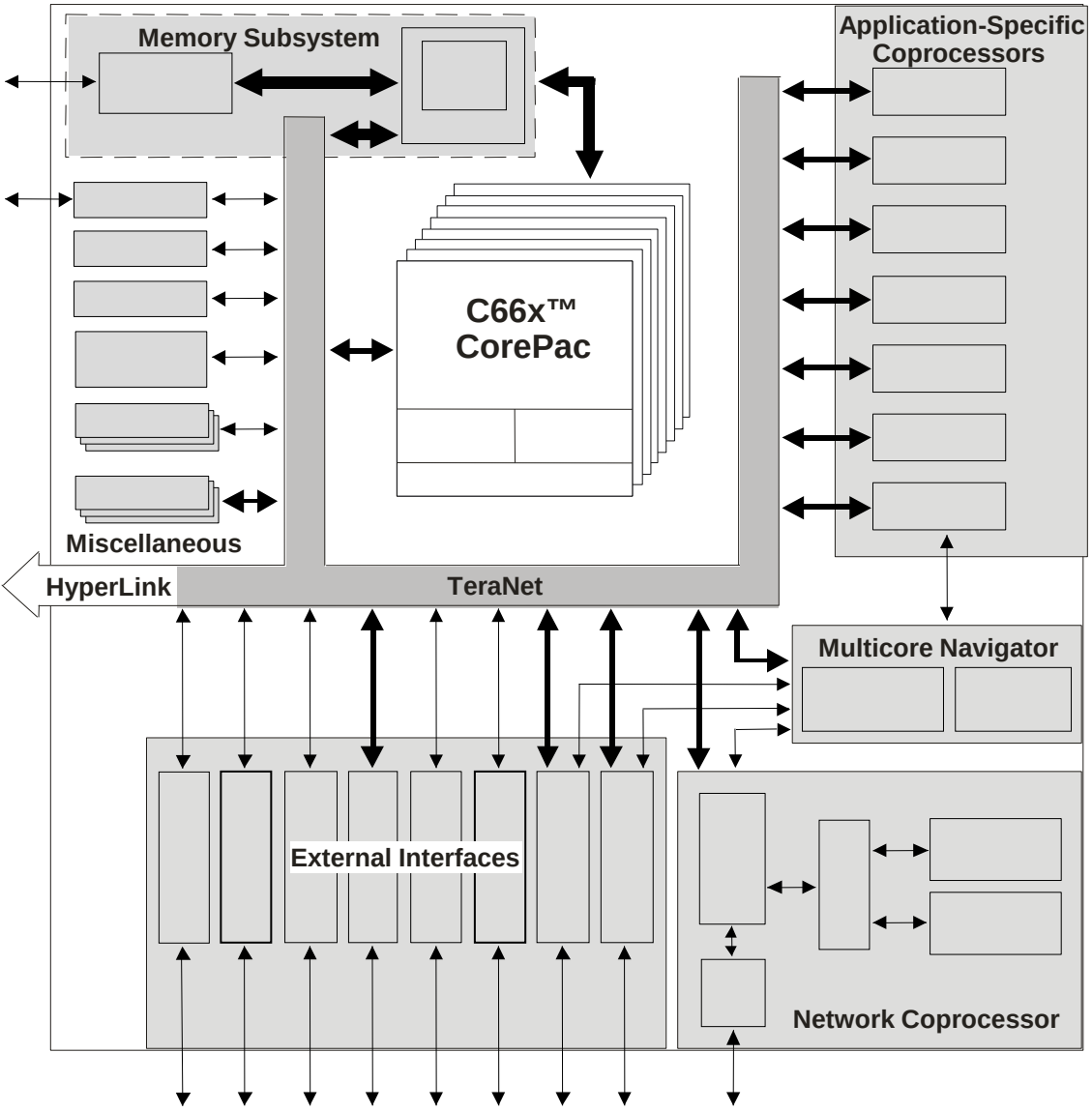
KeyStone Overview

- **KeyStone Architecture**
  - CorePac & Memory Subsystem
  - Internal Communications and Transport
  - External Interfaces
  - Coprocessors and Accelerators
  - Debug
  - Miscellaneous
  - Application- and Device-specific

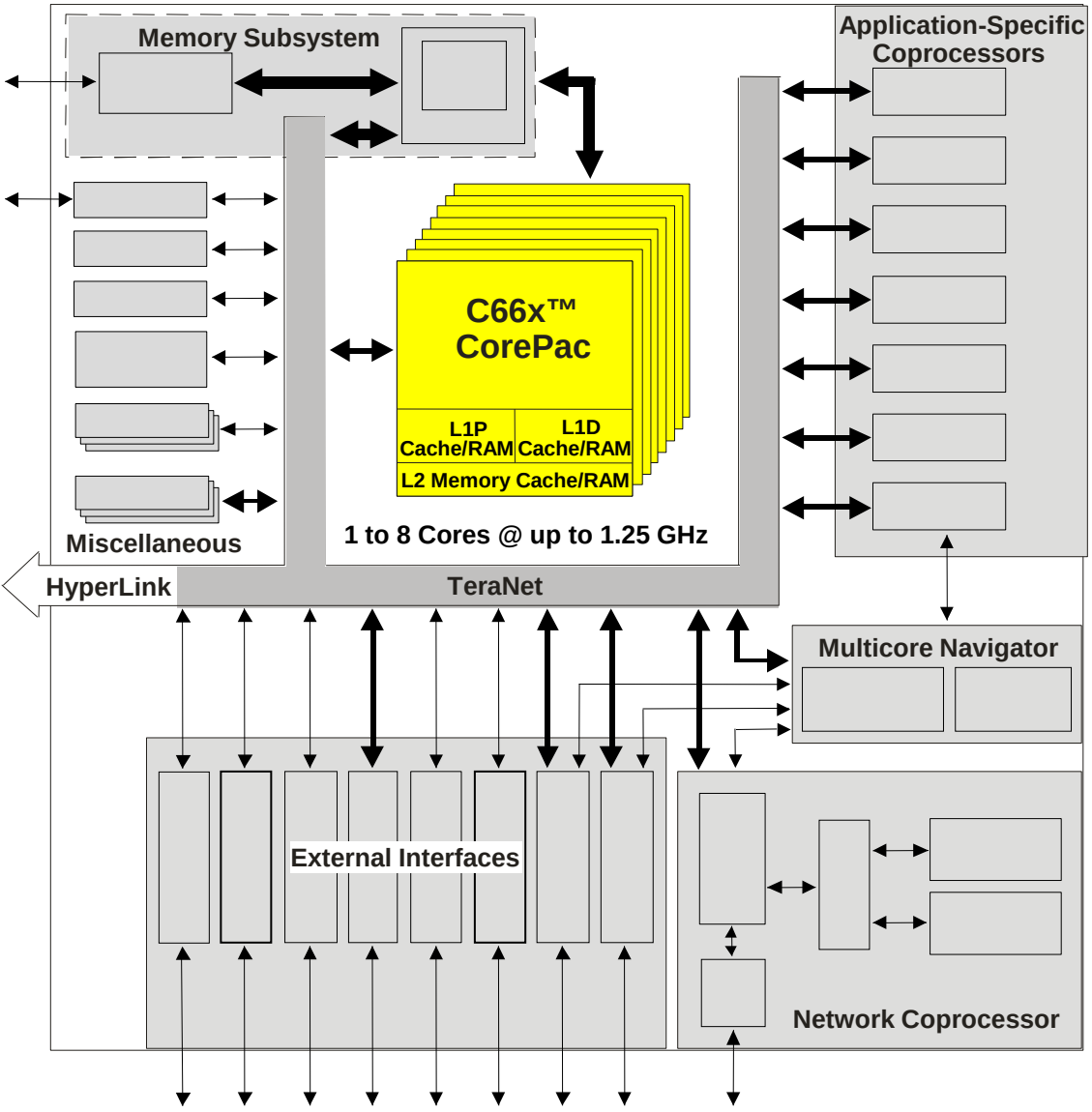
Enhanced DSP Core



KeyStone Device Architecture

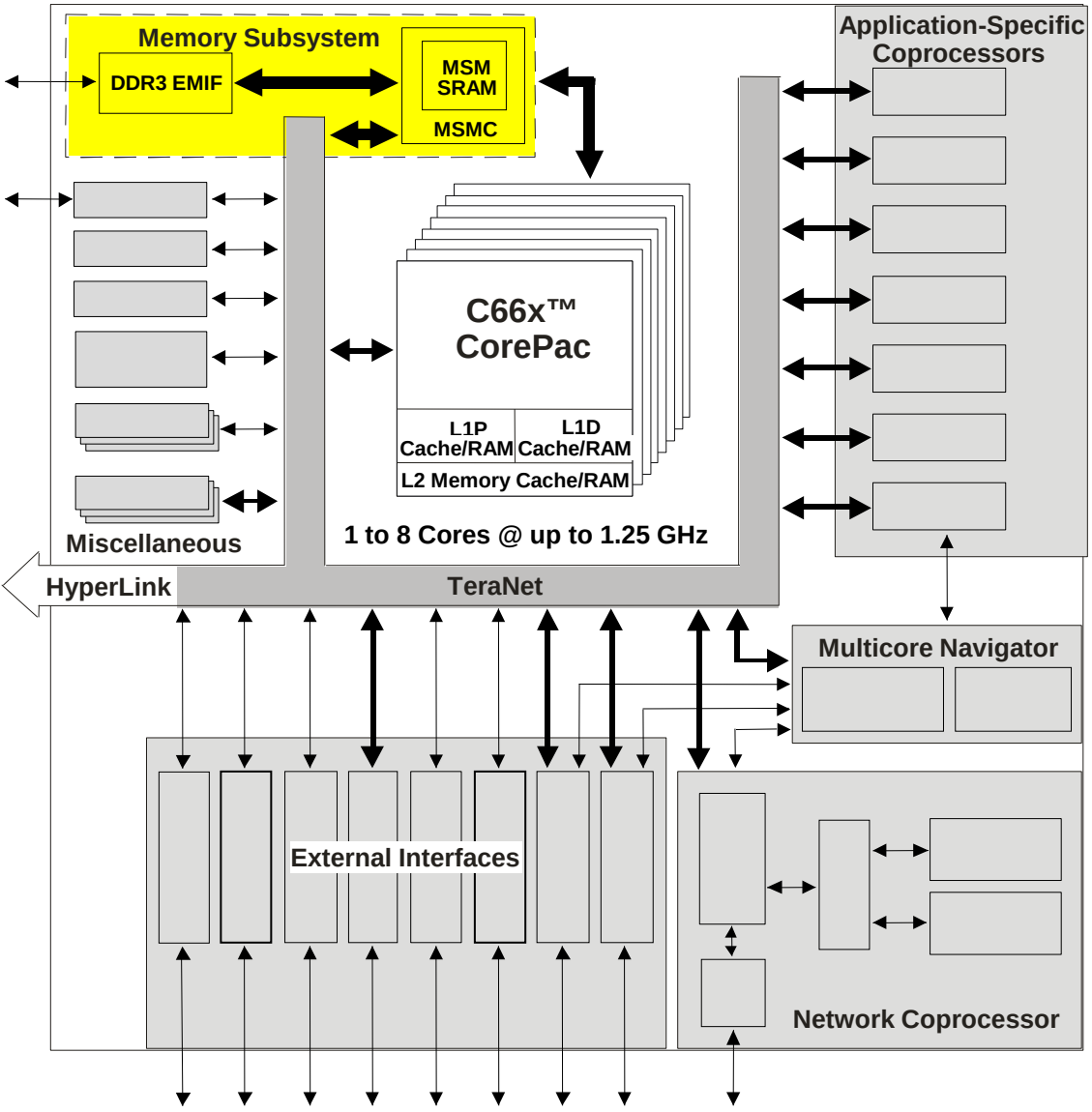


CorePac



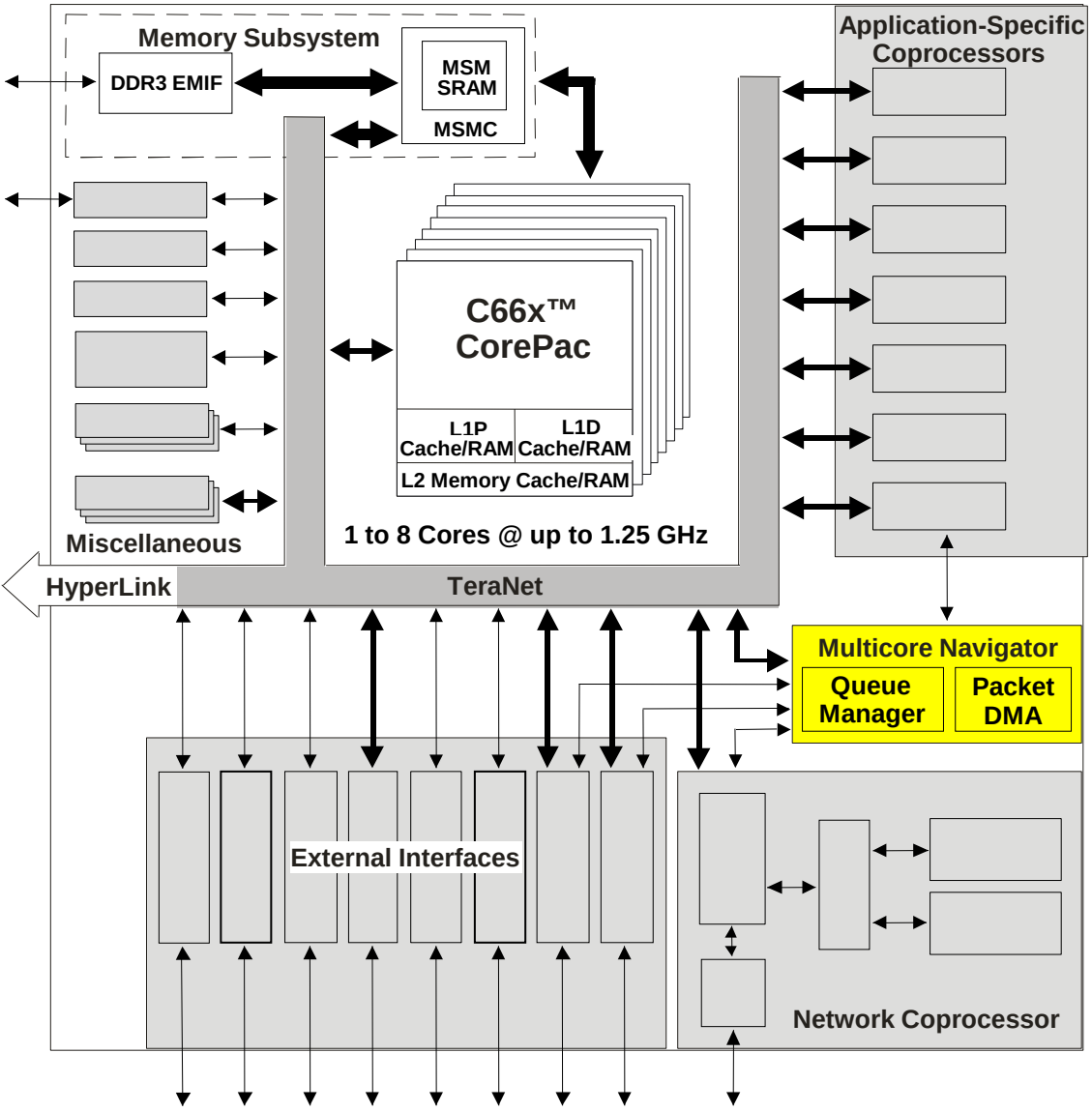
- 1 to 8 C66x CorePac DSP Cores operating at up to 1.25 GHz
  - Fixed- and floating-point operations
  - Code compatible with other C64x+ and C67x+ devices
- L1 Memory
  - Can be partitioned as cache and/or RAM
  - 32KB L1P per core
  - 32KB L1D per core
  - Error detection for L1P
  - Memory protection
- Dedicated L2 Memory
  - Can be partitioned as cache and/or RAM
  - 512 KB to 1 MB Local L2 per core
  - Error detection and correction for all L2 memory
- Direct connection to memory subsystem

Memory Subsystem



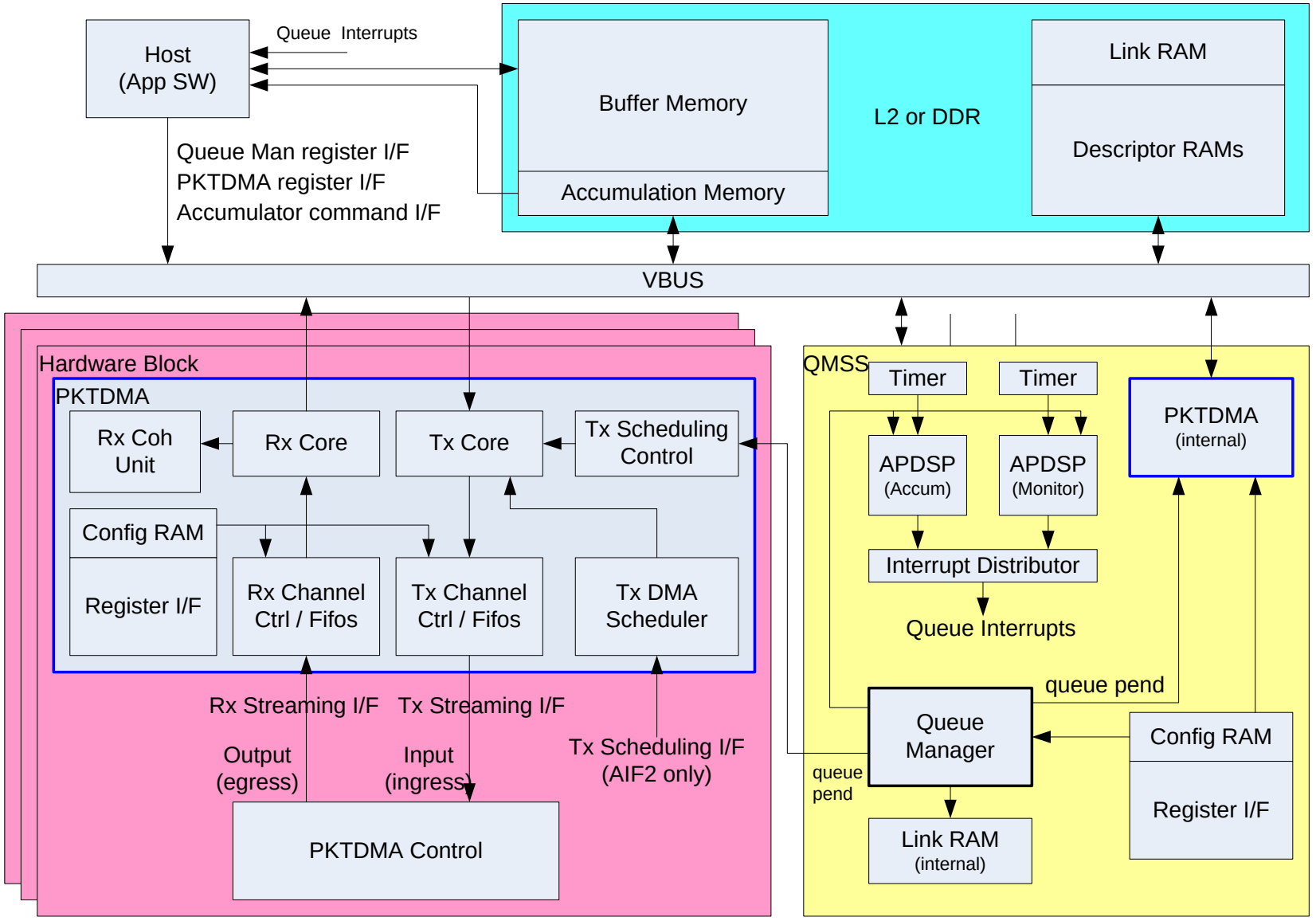
- Multicore Shared Memory (MSM SRAM)
  - 1 to 4 MB
  - Available to all cores
  - Can contain program and data
  - All devices except C6654
- Multicore Shared Memory Controller (MSMC)
  - Arbitrates access of CorePac and SoC masters to shared memory
  - Provides a connection to the DDR3 EMIF
  - Provides CorePac access to coprocessors and IO peripherals
  - Provides error detection and correction for all shared memory
  - Memory protection and address extension to 64 GB (36 bits)
  - Provides multi-stream pre-fetching capability
- DDR3 External Memory Interface (EMIF)
  - Support for 16-bit, 32-bit, and (for C667x devices) 64-bit modes
  - Specified at up to 1600 MT/s
  - Supports power down of unused pins when using 16-bit or 32-bit width
  - Support for 8 GB memory address
  - Error detection and correction

Multicore Navigator

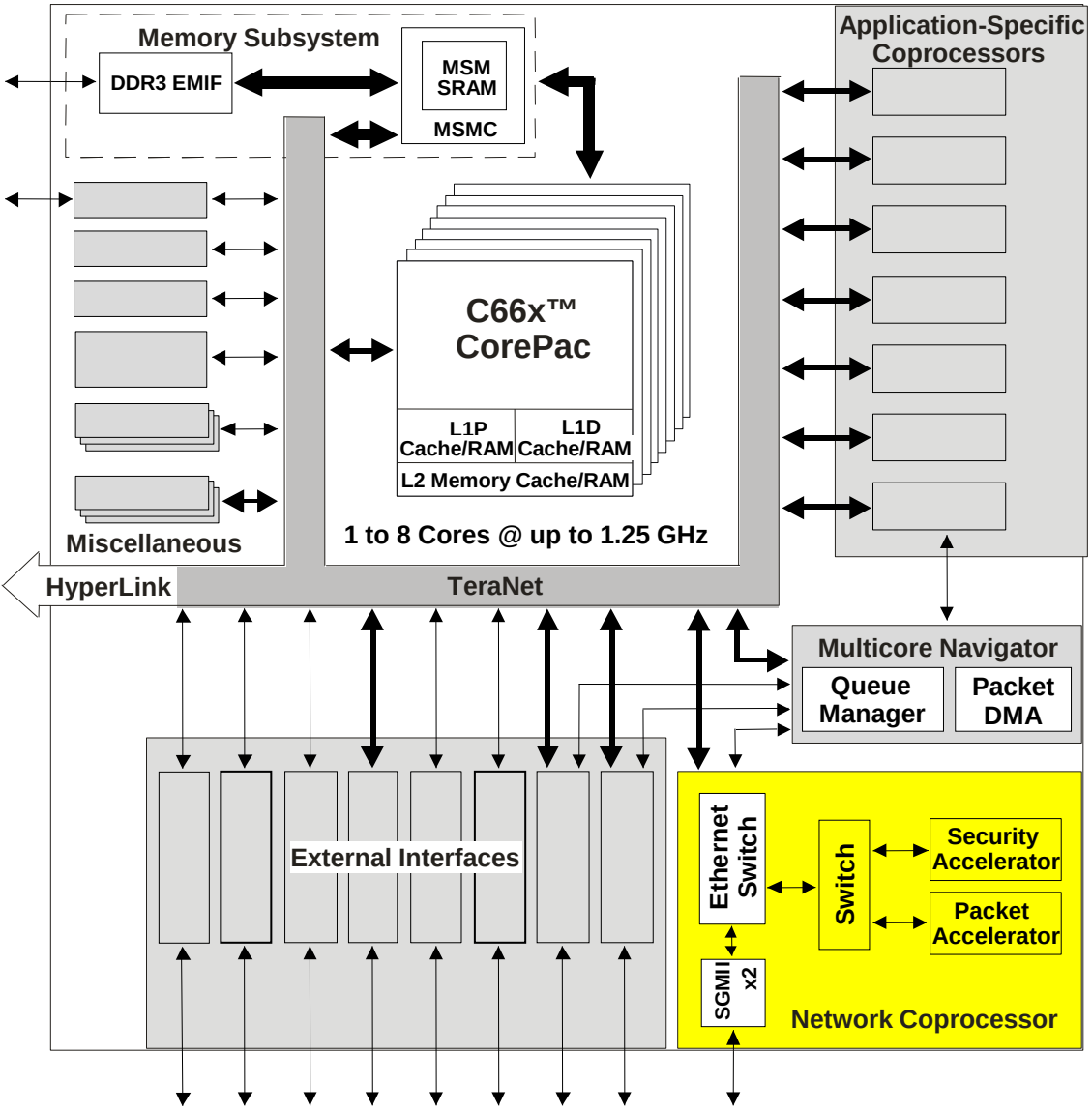


- Provides seamless inter-core communications (messages and data exchanges) between cores, IP, and peripherals. "Fire and forget"
- Low-overhead processing and routing of packet traffic to and from peripherals and cores
- Supports dynamic load optimization
- Data transfer architecture designed to minimize host interaction while maximizing memory and bus efficiency
- Consists of a Queue Manager Subsystem (QMSS) and multiple, dedicated Packet DMA engines

Multicore Navigator Architecture

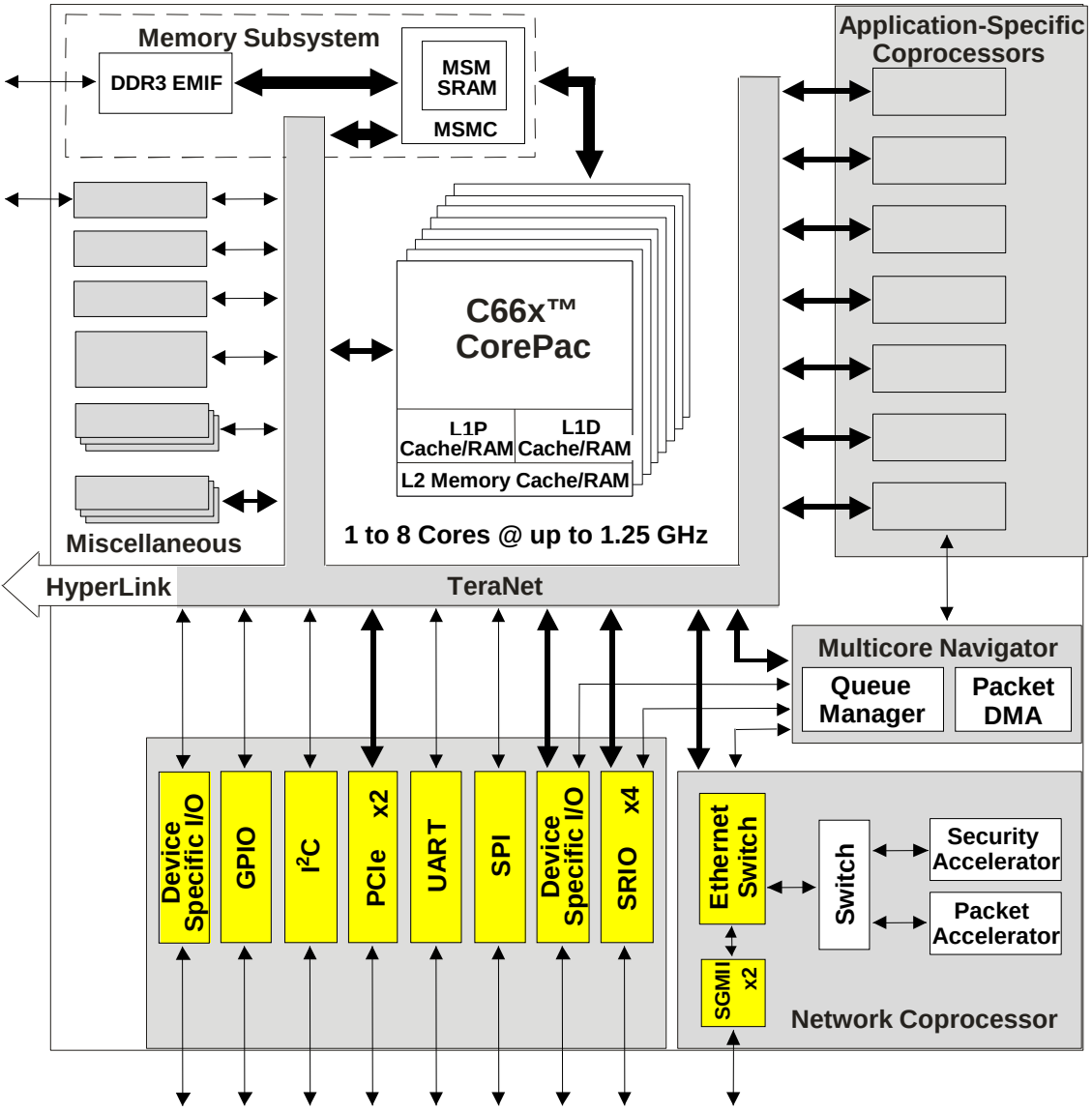


Network Coprocessor (C667x)



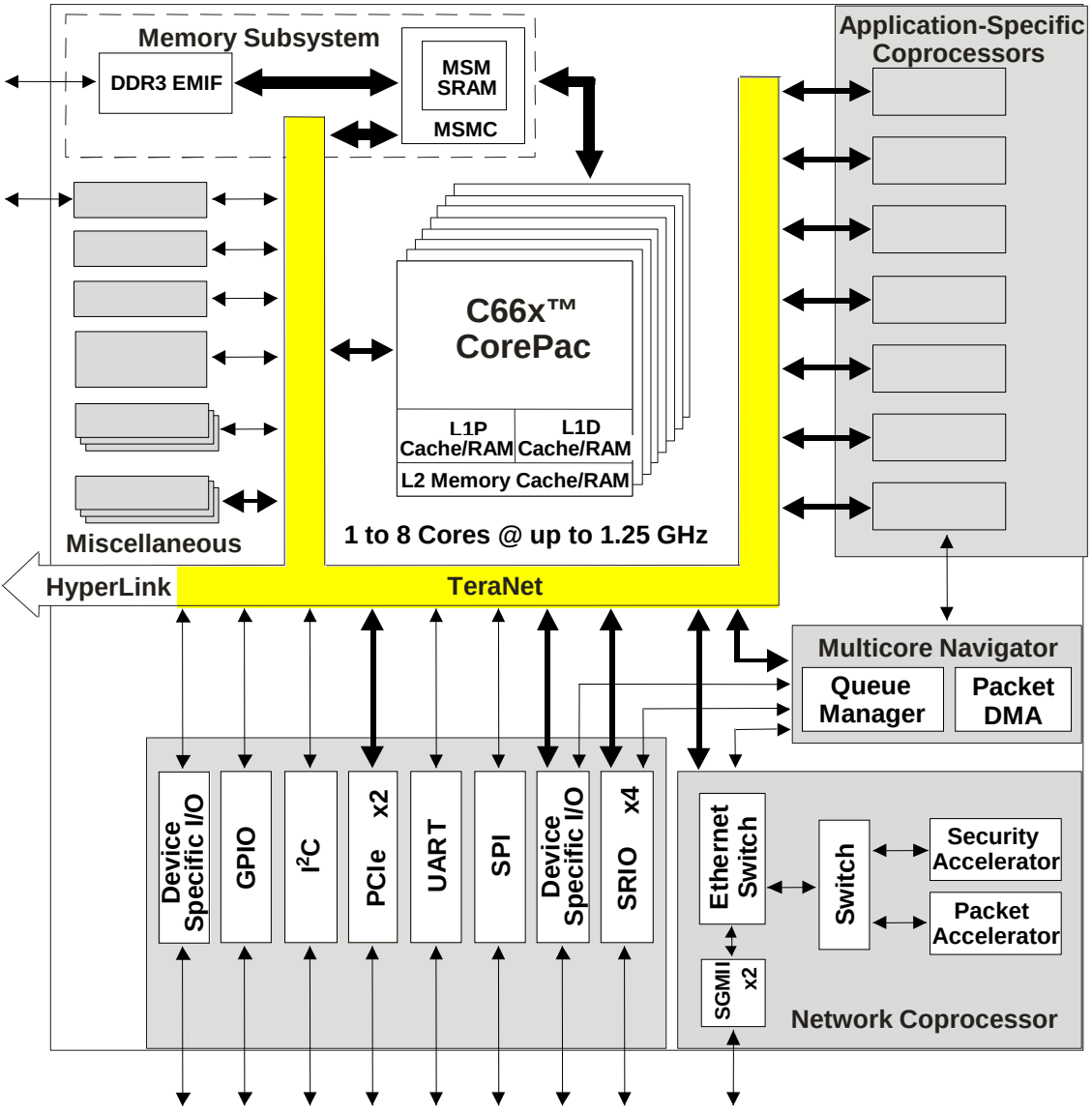
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - 8K multiple-in, multiple-out HW queues
  - Single IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple queues
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols

External Interfaces



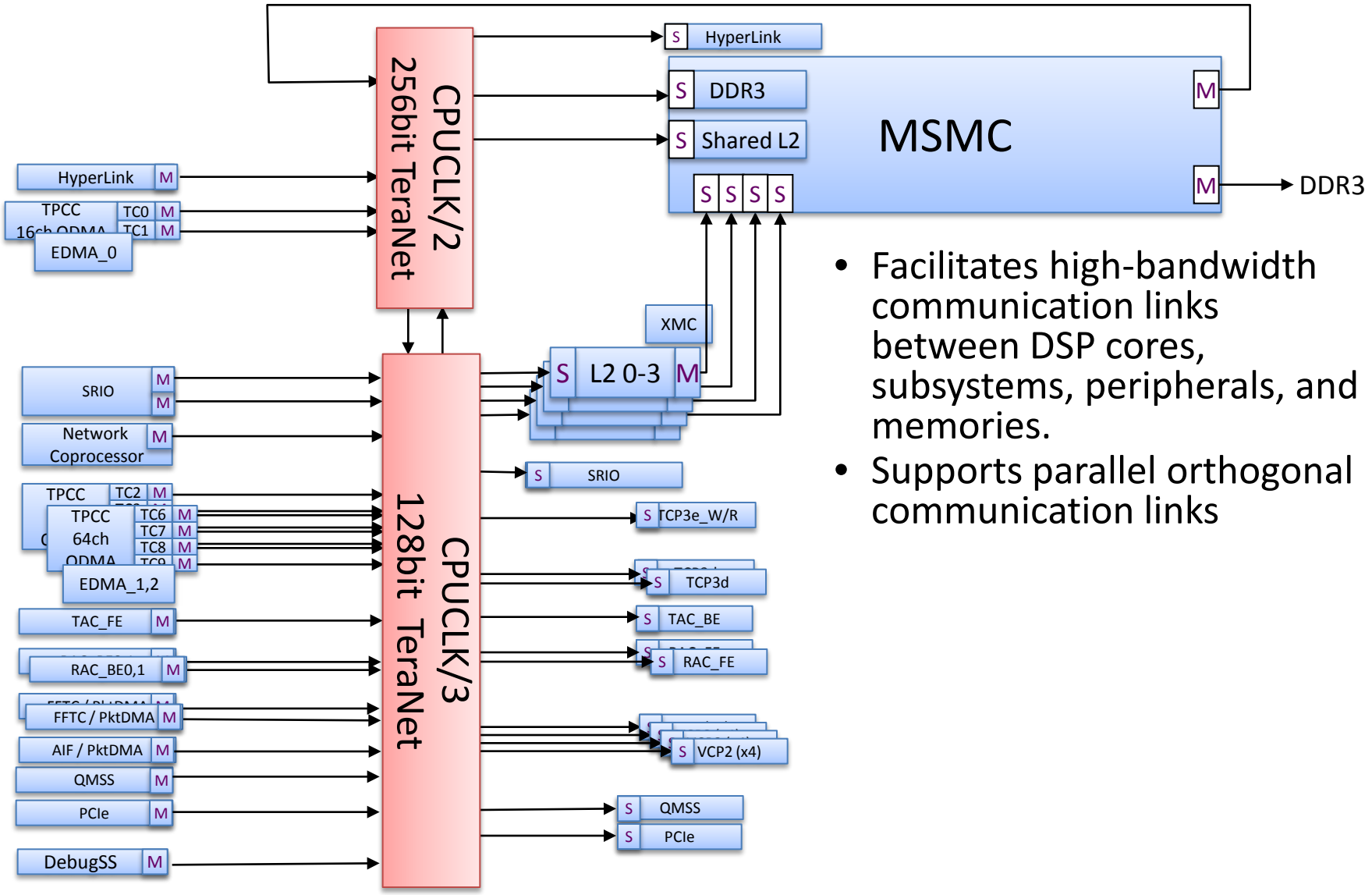
- 2x SGMII ports support 10/100/1000 Ethernet
- 4x high-bandwidth Serial RapidIO (SRIO) lanes for inter-DSP applications
- SPI for boot operations
- UART for development/testing
- 2x PCIe at 5 Gbps
- I2C for EPROM at 400 Kbps
- GPIO
- Device-specific Interfaces
  - Wireless Applications
  - General Purpose Applications

TeraNet Switch Fabric



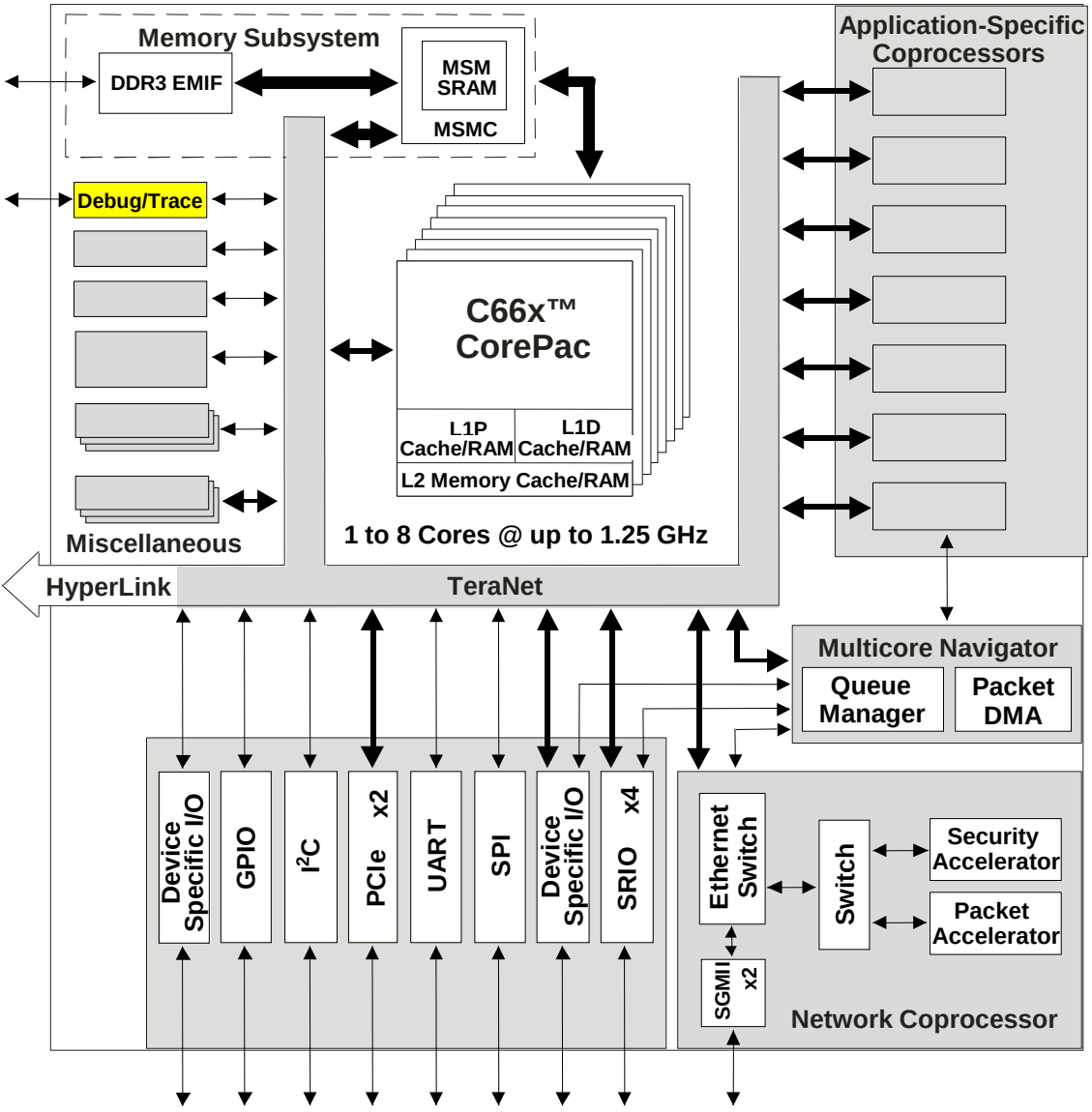
- A non-blocking switch fabric that enables fast and contention-free internal data movement
- Provides a configured way – within hardware – to manage traffic queues and ensure priority jobs are getting accomplished while minimizing the involvement of the CorePac cores
- Facilitates high-bandwidth communications between CorePac cores, subsystems, peripherals, and memory

TeraNet Data Connections



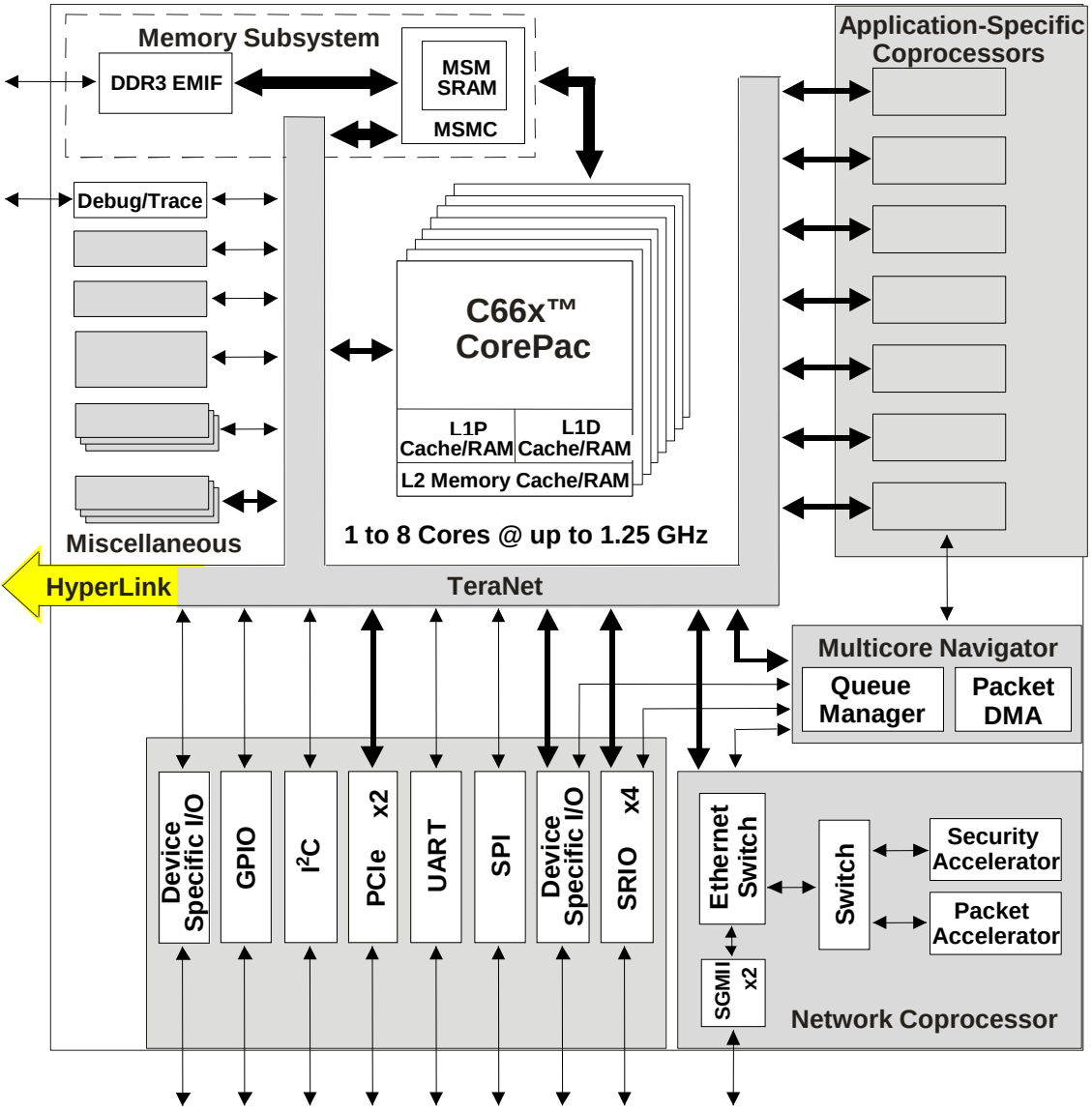
- Facilitates high-bandwidth communication links between DSP cores, subsystems, peripherals, and memories.
- Supports parallel orthogonal communication links

Diagnostic Enhancements



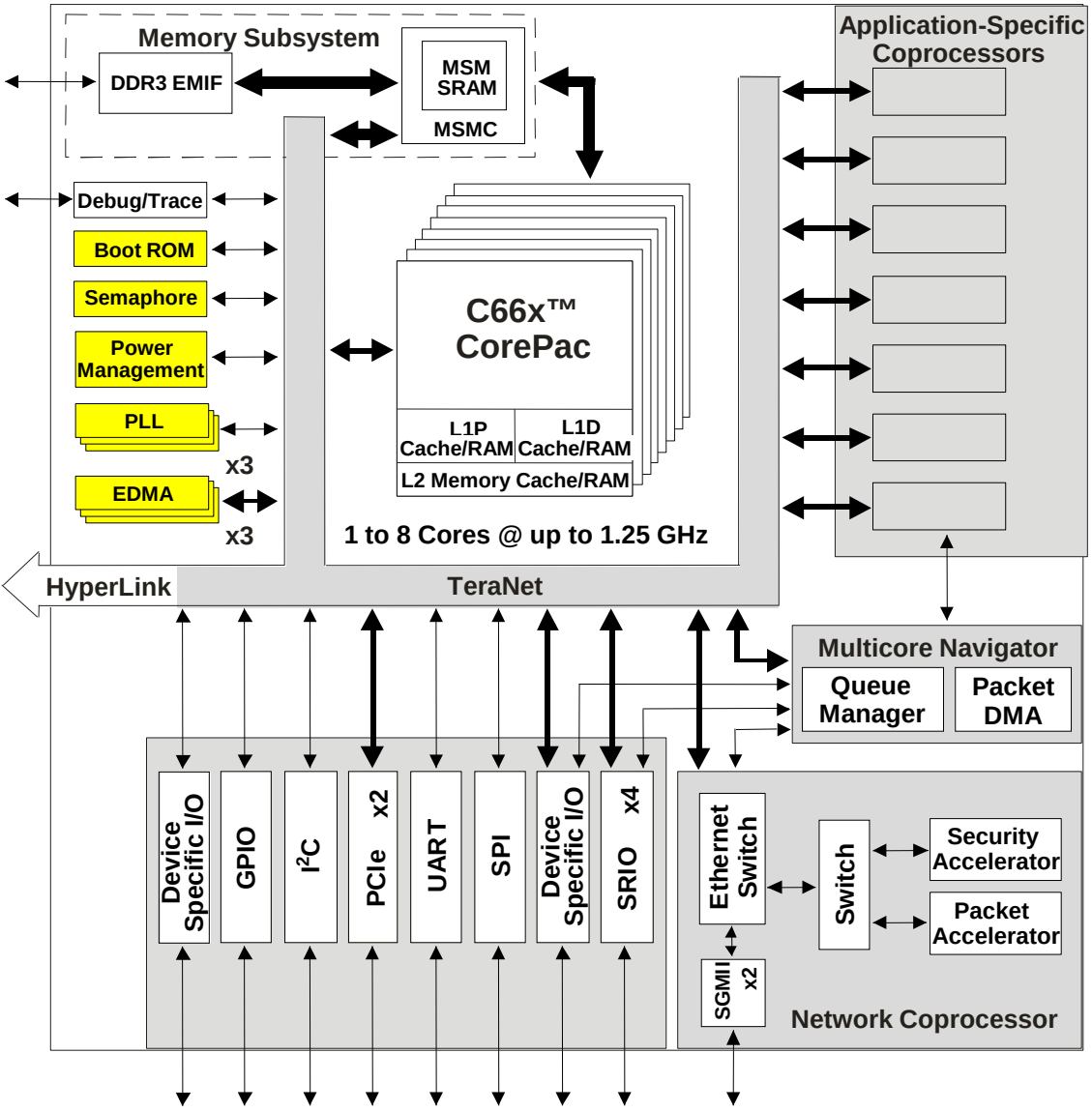
- Embedded Trace Buffers (ETB) enhance the diagnostic capabilities of the CorePac.
- CP Monitor enables diagnostic capabilities on data traffic through the TeraNet switch fabric.
- Automatic statistics collection and exporting (non-intrusive)
- Monitor individual events for better debugging
- Monitor transactions to both memory end point and Memory-Mapped Registers (MMR)
- Configurable monitor filtering capability based on address and transaction type

HyperLink Bus



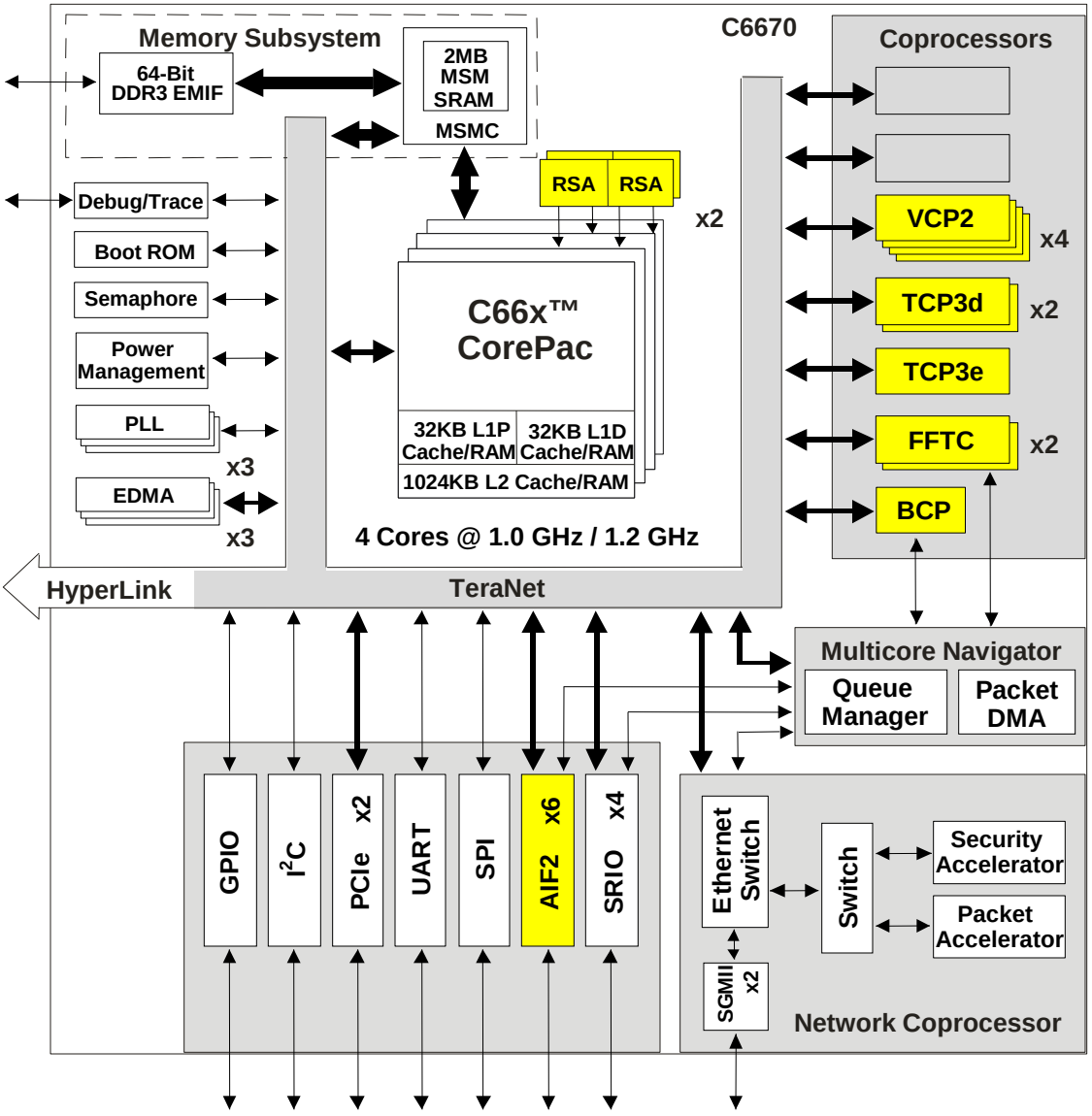
- Provides the capability to expand the device to include hardware acceleration or other auxiliary processors
- Supports four lanes with up to 12.5 Gbaud per lane

Miscellaneous Elements



- Boot ROM
- Semaphore module provides atomic access to shared chip-level resources.
- Power Management
- Three on-chip PLLs:
  - PLL1 for CorePacs, except
  - PLL2 for DDR3
  - PLL3 for Packet Acceleration
- Three EDMA controllers
- Eight 64-bit timers
- Inter-Processor Communication (IPC) Registers

Device-Specific: C6670 for Wireless Apps



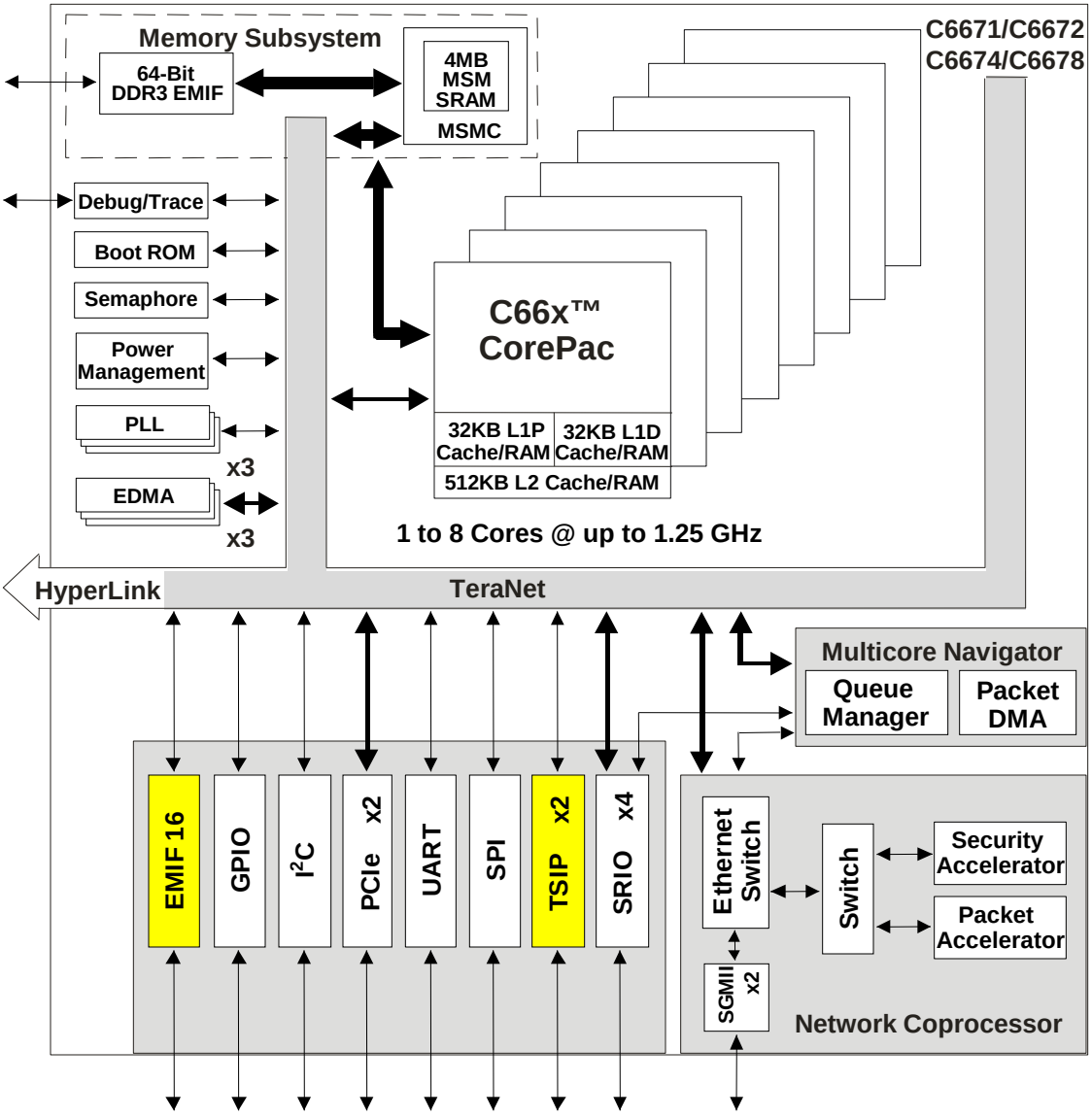
Device-specific Coprocessors:

- 2x FFT Coprocessor (FFTC)
- Turbo Decoder/Encoder Coprocessor (TCP3d/3e)
- 4x Viterbi Coprocessor (VCP2)
- Bit-rate Coprocessor (BCP)
- 2x Rake Search Accelerator (RSA)

Device-specific Interfaces:

- 6x Antenna Interface 2 (AIF2)

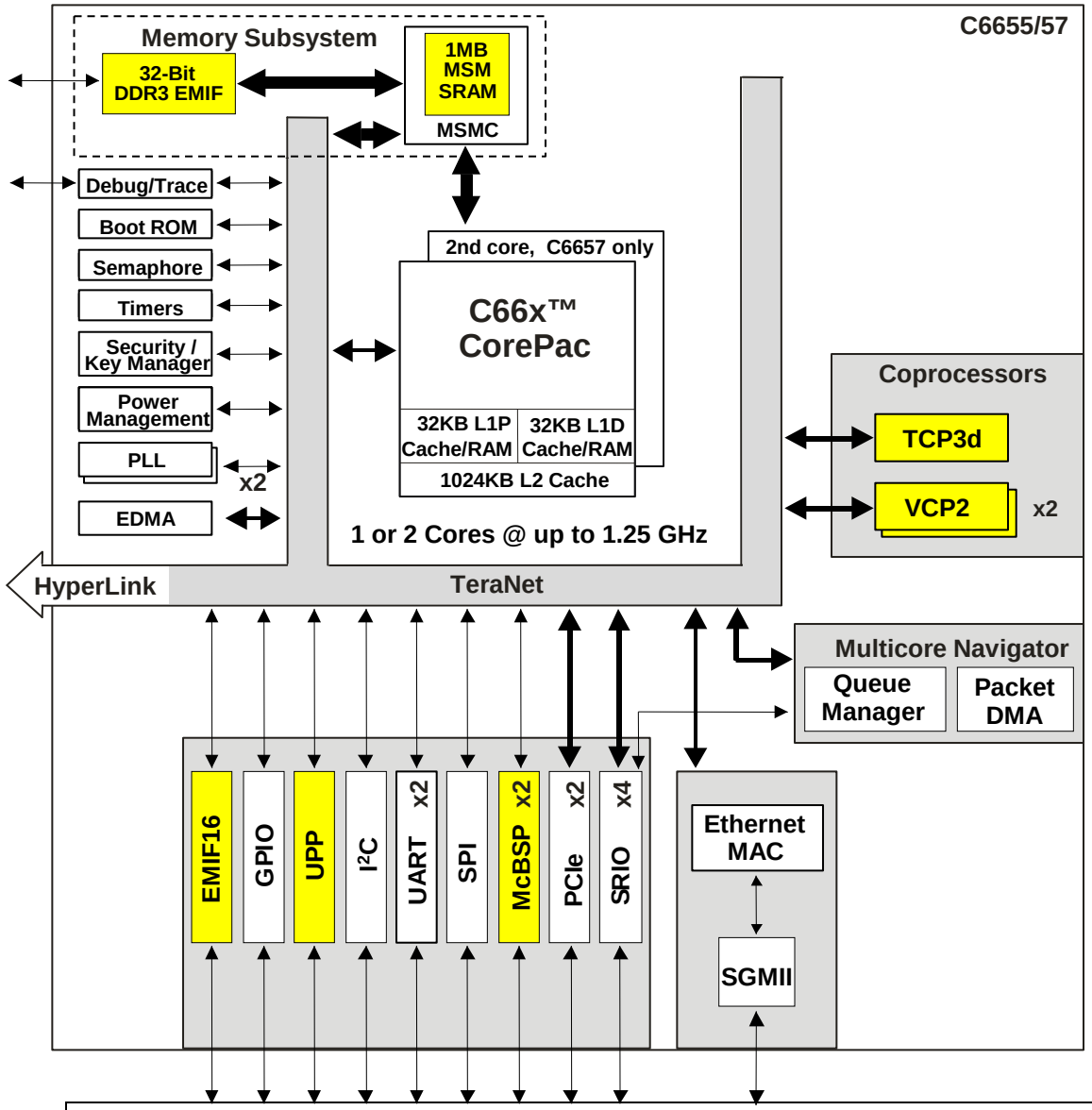
Device-Specific: C667x General Purpose



Device-specific Interfaces:

- 2x Telecommunications Serial Port (TSIP)
- Asynchronous Memory Interface (EMIF16):
  - Connects memory up to 256 MB
  - Three modes:
    - Synchronized SRAM
    - NAND flash
    - NOR flash

Device-Specific: C665x General Purpose



Device-specific Coprocessors:

- Turbo Decoder Coprocessor (TCP3d)
- 2x Viterbi Coprocessor (VCP2)

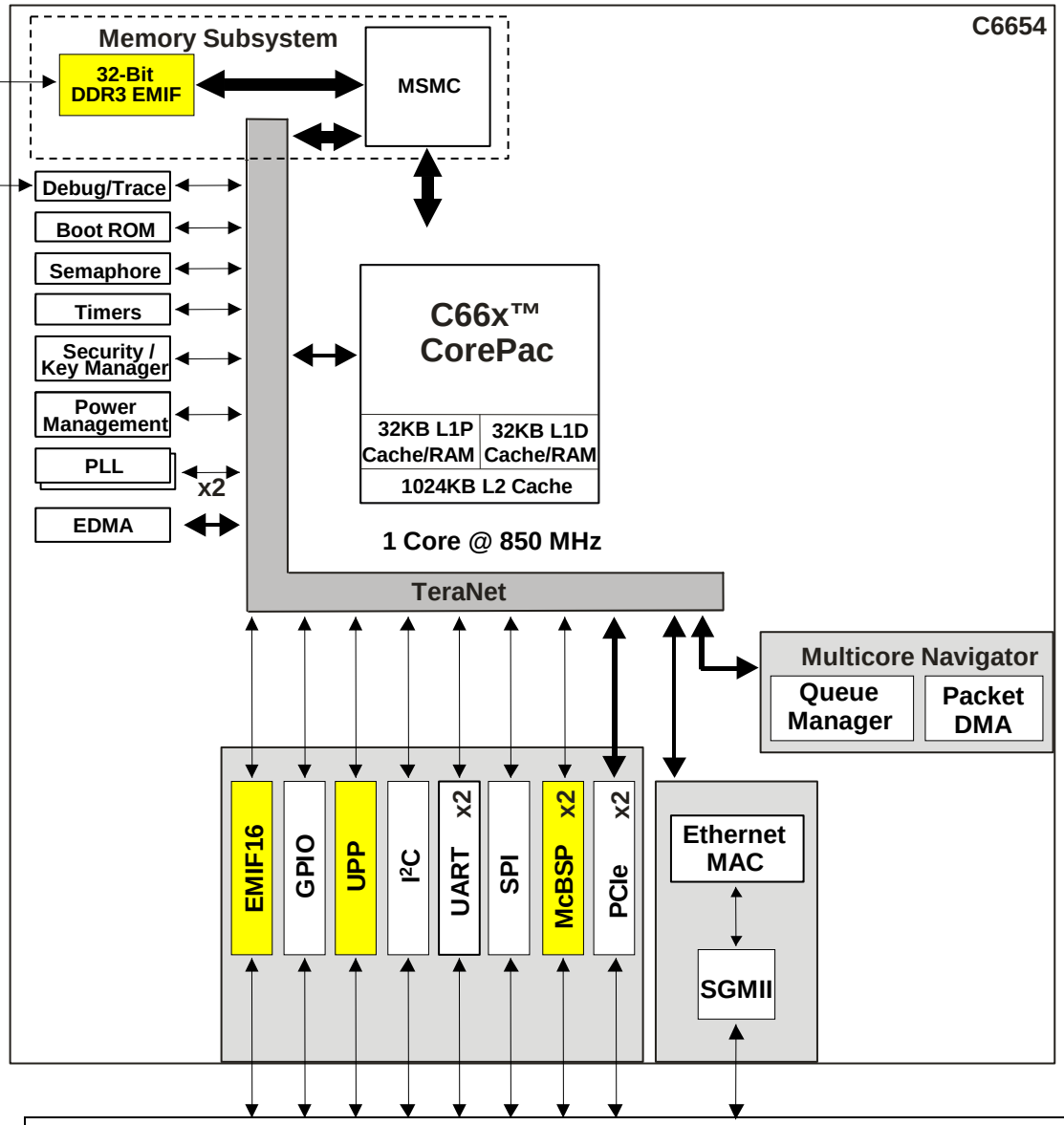
Device-specific Interfaces:

- Asynchronous Memory Interface (EMIF16)
- Universal Parallel Port (UPP)
- 2x Multichannel Buffered Serial Ports (McBSP)

Device-specific Memory:

- 1 MB Multicore Shared Memory (MSM SRAM)
- 32-bit DDR3 Interface

Device-Specific: C665x Power Optimized



Device-specific Interfaces:

- Asynchronous Memory Interface (EMIF16)
- Universal Parallel Port (UPP)
- 2x Multichannel Buffered Serial Ports (McBSP)

Device-specific Memory:

- 32-bit DDR3 Interface

KeyStone C665x: Key HW Variations

HW Feature	C6654	C6655	C6657
CorePac Frequency (GHz)	0.85	1 @ 1.0, 1.25	2 @ 0.85, 1.0, 1.25
Multicore Shared Memory (MSM)	No	1024KB SRAM	
DDR3 Maximum Data Rate	1066	1333	
Serial Rapid I/O Lanes	No	4x	
HyperLink	No	Yes	
Viterbi Coprocessor (VCP)	No	2x	
Turbo Coprocessor Decoder (TCP3d)	No	Yes	
Network Coprocessor (NETCP)	No	No	

For More Information

- For more information, refer to the C66x Getting Started page to locate the data manual for your KeyStone device.
- View the complete C66x Multicore SOC Online Training for KeyStone Devices, including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website.