KeyStone Multicore Workshop

North West (Week of 2/25)

**Day One**

START: 8:30 AM

* Agenda/Introductions (15 minutes) – **Business Developer** or trainer
* KeyStone (I and II) Device Overview (60 minutes) introduces the C66x SoC functional architecture including the CorePac, Memory Subsystem, internal transport mechanisms, external interfaces, accelerators and coprocessors, and other miscellaneous features. -
* C66 CorePac (45 minutes provides a more detailed description of the C66 CorePacs including the functional units, internal and external interfaces, interrupt controller etc. -
* Elective – if the customers need ARM –
  + ARM CorePac Overview (60 minutes) provides a more detailed description of the four ARM Cortex A15 CorePacs including the functional units, Neon and VFP, cache coherency, etc. -
* Elective – If the customers do not need ARM
  + Introduction to code Composer Studio (CCS) Overview (60 minutes) examines the Eclipse-based CCS IDE from TI, with an emphasis on the new elements incorporated into CCS Version 5.x -

11:30 AM BREAK (15 minutes)

* KeyStone (I and II) Software Overview (75 minutes) introduces the suite of tools provided by TI and third-party partners to enable application development on C66x SoC devices, including Code Composer Studio (CCS), the Multicore Software Development Kit (MCSDK), third-party plug-ins, and the C66x Lite Evaluation Module (EVM). In addition, ARM Software Overview presents the software structures (Linux, SysLink, LLD) that can be called from a Linux-run ARM -

12:45 PM LUNCH (60 minutes)

* C66 Out-of-the-box LAB (30 minutes) including basic tasks associated with working in the CCSv5 development environment
* Introduction to SYS/BIOS (60 minutes) -

3:15 PM BREAK (15 minutes)

* Multicore Design Considerations (75 minutes) introduces the concepts of parallel programming and processing and illustrates their implementation through video-encoding use case scenario- including vlfft Demo or Lab. –
* LAB: MCSDK Example Code (SRIO Direct IO) (45 minutes)
  + Import Example Project
  + Create Target Configuration
  + Connect/Load/Build/Run

END: 5:30 PM

**Day Two**

START: 8:30 AM

* Introduction to CCS and basic debug functionality (2.5 hours) includes the following demos AND labs: -
  + - How to create a new project, build, and run (single core)
    - How to import a project from the release, build, and run (single core)
    - One or more of the above projects extended across on multiple cores
    - Debug one or more of the prior projects with bugs. The first debug can be presented as a demo, followed by a hands-on lab

11:00 AM BREAK (15 minutes)

* Introduction to Interprocessor Communication (60 minutes) provides an overview of basic IPC concepts, compares and contrasts different services  
  provided within the IPC framework, analyzes support utilities, describes configuration, and provides a few IPC usage examples. -

12:15 PM LUNCH (60 minutes)

* LAB: IPC Shared Memory (60 minutes)
* LAB: IPC Multicore Navigator Transport (30 minutes)

2:45 PM BREAK (15 minutes)

* Multicore Navigator Usage (90 minutes) provides an overview of the hardware mechanism that facilitates data movement and multicore cooperation in KeyStone SoC devices. Topics include the Navigator subsystem architecture, use cases and example code, configuration, and low level drivers. -
* LAB: MCSDK Sample Application: Image Processing (60 minutes)

END: 5:30 PM

**Day Three**

START: 8:30 AM

* C66 Single-core optimization, include pipeline considerations, software pipeline and how to achieve it, useful optimization techniques (75 minutes) -
* LAB: Optimization (90 minutes)

11:15 AM BREAK (15 minutes)

* Multicore EDMA Usage (60 minutes) takes a look at different DMA methods used on the C66x including EDMA3, QDMA, and IDMA. It provides information on programming, linking, and chaining EDMA3, examples of the transfer and sorting functions, and an introduction to TeraNet bridging. –

12:30 PM LUNCH (60 minutes)

* Bootloader (45 minutes) provides an introduction to the C66x bootloader including configuration, device startup, and runtime modes. -
* Advance debug /trace presentation (90 minutes) includes the following demos AND labs - :
  + Usage of STM library for real-time printf (based on prior SRIO demonstration)
  + Demonstrate usage of debug module instrumentation.

3:45 PM BREAK (15 minutes)

* HyperLink Overview (45 minutes) –
* HyperLink Lab – (45 minutes)

END: 5:15 PM