KeyStone Multicore Train-the-trainer for Europe FAEs

Freising, DE May 14-16, 2012

**Monday, May 14**

START @ TBD AM

* Agenda/Introductions (15 minutes)
* General DSP Roadmap Overview (30 minutes)
* CorePac: Achieving High Performance (60 minutes, Ran Katzur)
  + CorePac Architecture
  + Single Instruction Multiple Data (SIMD)
  + Memory Access
  + Pipeline Concept

BREAK (15 minutes)

* KeyStone Architecture (60 minutes, Ran)
  + SoC Architecture
  + CorePac & Memory Subsystem
  + Interfaces and Peripherals
  + Coprocessors and Accelerators
  + Debug
* KeyStone II Architecture (30 minutes, Dan)
  + SoC Architecture
  + Key Differences

LUNCH (60 minutes)

* KeyStone SW Development Ecosystem (30 minutes, Dan Rinkes)
  + CCSv5
  + MCSDK
  + C66x EVM
  + Third Party Tools
* LAB 1: MCSDK Example Code: SRIO DIO (60 minutes, Dan/Ran)
  + Import Example Project
  + Create Target Configuration
  + Connect/Load/Build/Run

BREAK (15 minutes)

* Introduction to Multicore: Design Considerations (60 minutes, Ran)
  + Parallel Processing
  + Video Encoding Example
* LAB 2: MCSDK Sample Application: Image Processing (45 minutes)
* Peripherals: PCIe Usage (45 minutes, Eric Ding via WebEx)
  + PCIe Overview
  + Address Translation
  + Configuration
  + PCIe Boot Demo

END @ TBD PM

**Tuesday, May 15**

START @ TBD AM

* TeraNet/EDMA Usage (30 minutes, Dan)
  + EDMA3 Overview
  + TeraNet Bridging
  + Programming EDMA3
  + Linking vs. Chaining
  + QDMA
  + IDMA
* DEMO: Multicore Partitioning: VLFFT (60 minutes, Ran/Dan)
  + Basic Algorithm for Parallelizing DFT
  + Multi-core Implementation of DFT
  + Review Benchmark Performance

BREAK (15 minutes)

* Peripherals: HyperLink (60 minutes, Ran)
  + HyperLink Overview
  + Address Translation
  + Configuration
  + Example
* LAB2: HyperLink Project (45 minutes, Dan/Ran)
  + Import Example Project
  + Create Target Configuration
  + Modify Parameters
  + Connect/Load/Build/Run

LUNCH (60 minutes)

* Multicore Navigator (60 minutes, Ran)
  + Queue Manager Subsystem (QMSS)
  + Packet DMA (PKTDMA)
  + Working Together
  + Configuration
  + LLD API
  + Examples
* OpenEM Operation & Demonstration (60 minutes, Filip)

BREAK (15 minutes)

* Peripherals: SRIO Overview (45 minutes, Ran)
  + Usage Model
  + Master/Slave Protocol
  + Configuration
  + Application Algorithm
  + Build and Run
* LAB4: SRIO Projects (60 minutes, Dan/Ran)
  + Single Board Unfair
  + Single Board Debug
  + Board-to-board (optional)

END @ TBD PM

**Thursday, May 16**

START @ TBD AM

* Network Coprocessor: Packet Accelerator (30 minutes, Ran)
  + Applications
  + Hardware Modules
  + Firmware
  + PA Low Level Driver (LLD)
  + Programming Example
* Bootloader Usage (45 minutes, Dan)
  + Boot Modes
  + Device Startup
  + Boot Configuration
  + Secondary Bootload

BREAK (15 minutes)

* Tools & Debugging (60 minutes, Dan)
  + Debug Architecture Overview
  + Advanced Event Triggering
  + DSP Core Trace
  + System Trace
  + Application Embedded Debug Support
  + Multicore System Analyzer (MCSA)
* LAB5: Memory Optimization (60 minutes, Dan/Ran)

LUNCH (60 minutes)

* Video Infrastructure Demo on MCSDK (30 minutes, Dan)
* OpenMP Presentation (60 minutes, Uday Gurnani, remote via WebEx)

BREAK (15 minutes)

* Server Blades: Practical Challenges when DIN-ing multicore (Philippe Malleth)
* Explain Small Cell strategy into broader market (Josef Alt)
* C vs. TCI partnumbering
* Discussion on: Linux on DSP vs. ARM, Generic MC programming (OpenMP, AMP, SMP) PolyCore, Critical Blue, 3L, RunTime Navigator.... (Field owner)