Lab 2

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Index No:- 210206B

About Lab2

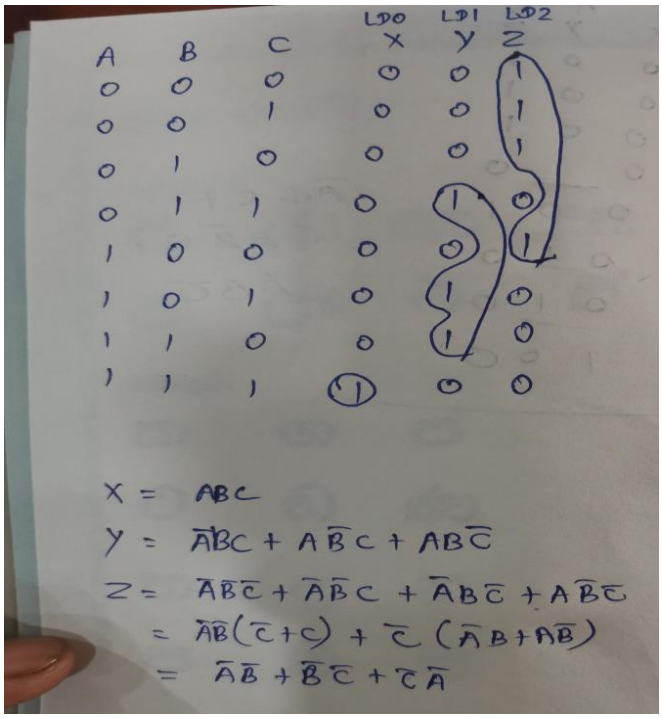
Lab is about build the circuit that state the function status about power generator system of the city.

Green light should be on when all three generators of functioning correctly. Whereas Amber light should be on only when 2 generators are functioning correctly. Red light should come up if less than 2 generators are functioning correctly.

1st we have to build circuit using Boolean expressions

Then simulating the circuit after creating simulation with modified test file

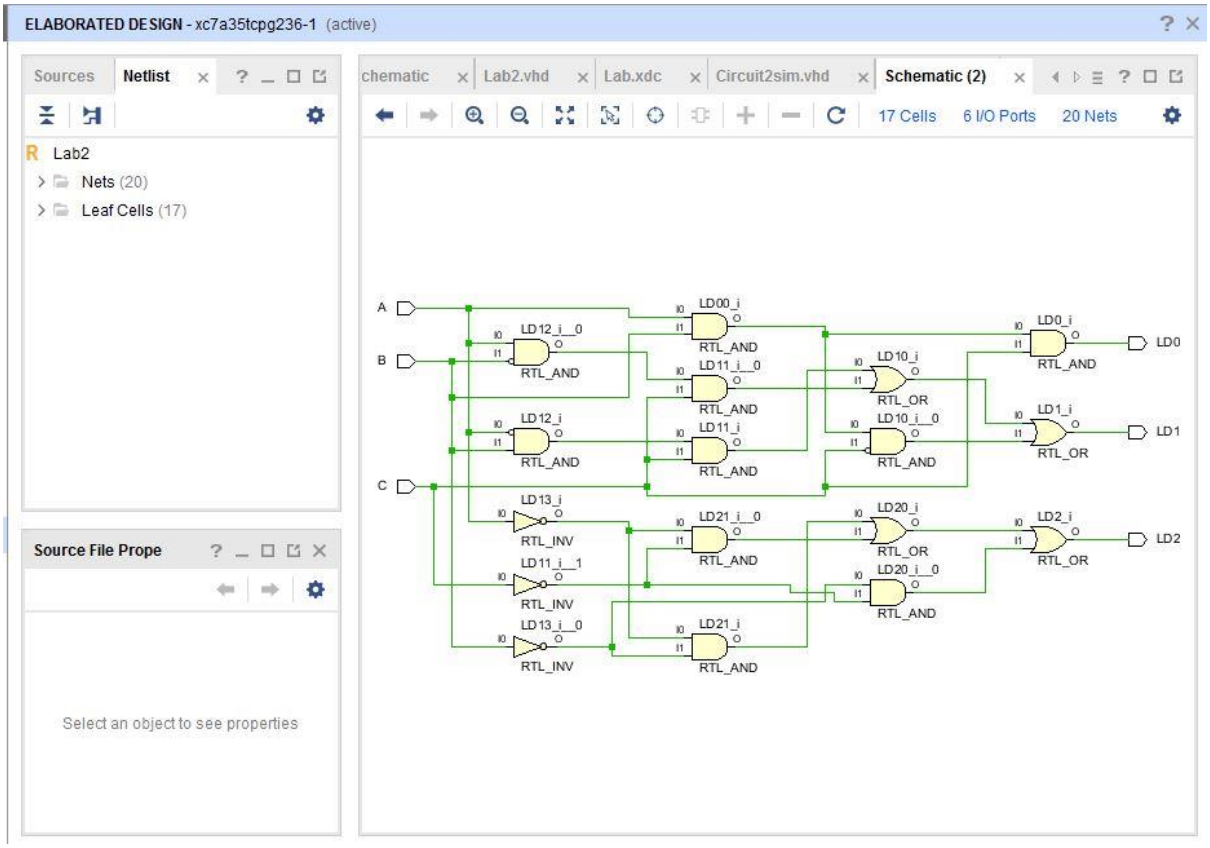
Steps for Boolean



VHDL Design Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity Lab2 is
   Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          C : in STD_LOGIC;
          LD0 : out STD_LOGIC;
          LD1 : out STD_LOGIC;
          LD2 : out STD_LOGIC);
end Lab2;
architecture Behavioral of Lab2 is
begin
   LD0 <= A AND B AND C;
   LD1 <= ((NOT A) AND B AND C) OR ( A AND (NOT B) AND C) OR (A AND B AND (NOT C));
   LD2 <= ((NOT A) AND (NOT B)) OR ((NOT A) AND (NOT C)) OR ((NOT B) AND (NOT C));

end Behavioral;
```

Schematic circuit



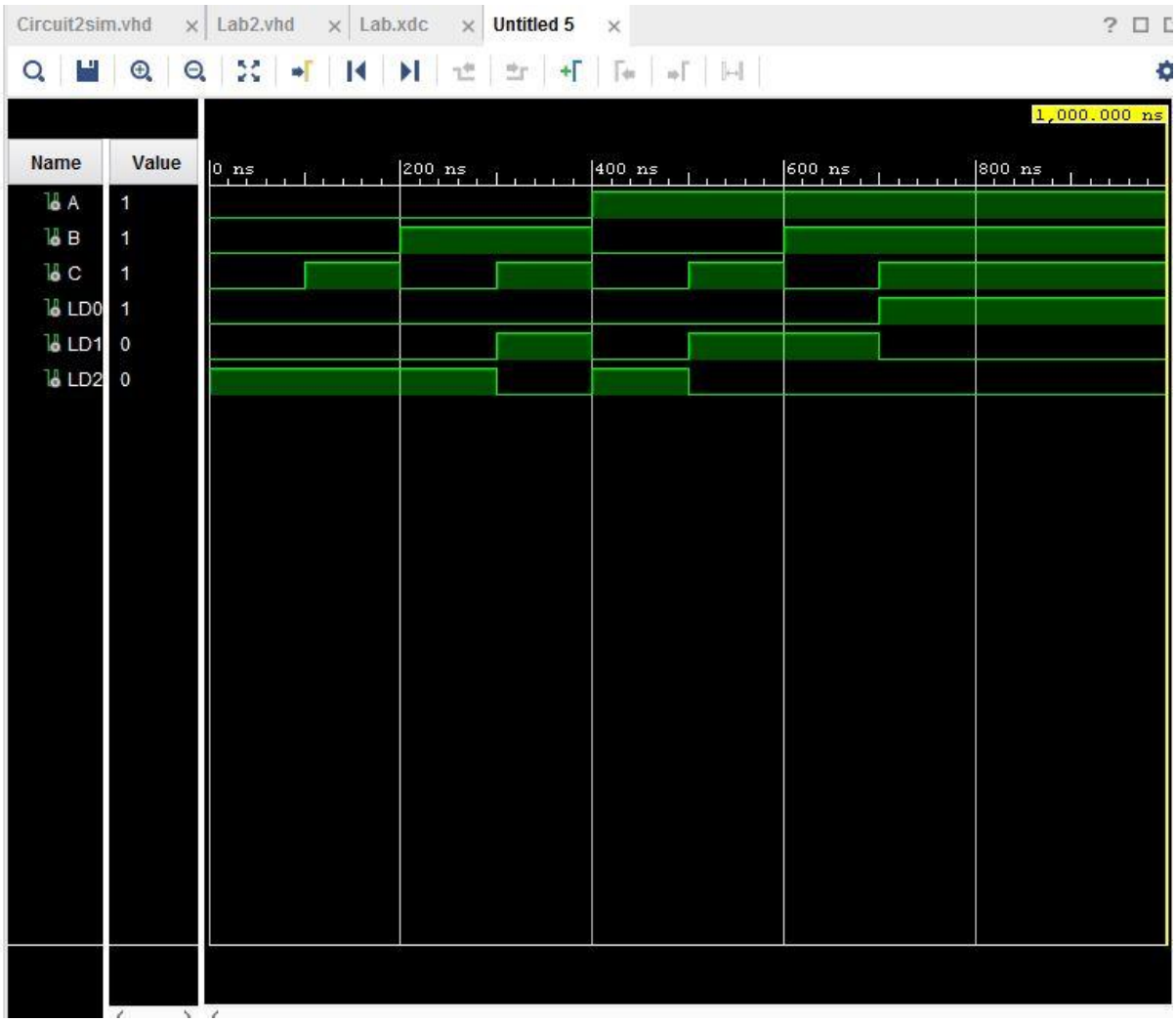
Test Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity Circuit2sim is
--  Port ( );
```

```
end Circuit2sim;



architecture Behavioral of Circuit2sim is
COMPONENT Lab2
   PORT( A, B, C : IN STD_LOGIC;
         LD0, LD1, LD2 : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A, B, C : std_logic;
SIGNAL LD0, LD1, LD2 : std_logic;

begin
UUT: Lab2 PORT MAP(
A => A,
B => B,
C => C,
LD0 => LD0,
LD1 => LD1,
LD2 => LD2);
process
  begin
  A <= '0'; -- set initial values
  B <= '0';
  C <= '0';
  WAIT FOR 100 ns; -- after 100 ns change inputs
  C <= '1';
  WAIT FOR 100 ns; --change again
  B <= '1';
  C <= '0';
  WAIT FOR 100 ns; --change again
  C <= '1';
  WAIT FOR 100 ns; --change again
  A <= '1';
  B <= '0';
  C <= '0';
  WAIT FOR 100 ns; --change again
  C <= '1';
  WAIT FOR 100 ns; --change again
  B <= '1';
  C <= '0';
  WAIT FOR 100 ns; --change again
  C <= '1';
  WAIT; -- will wait forever
end process;
```

end Behavioral;

Timing diagram from XSim



Conclusion

In this lab, i built a logic circuit that can indicate whether all generators of a power station are correctly functioning.

By this lab I learned design and develop a simple logic circuit using schematics and verify its functionality via simulation