Name:- N.Harikishna

Index No:- 210206B

Section 01

1)RCA_4

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 07:46:15 PM
-- Design Name:
-- Module Name: RCA_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
--Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity RCA_4 is
    Port ( A0 : in STD_LOGIC;
           A1 : in STD_LOGIC;
           A2 : in STD_LOGIC;
           A3 : in STD_LOGIC;
           B0 : in STD_LOGIC;
           B1 : in STD_LOGIC;
           B2 : in STD_LOGIC;
           B3 : in STD_LOGIC;
           C_in : in STD_LOGIC;
```

```
        S0 : out STD_LOGIC;
        S1 : out STD_LOGIC;
        S2 : out STD_LOGIC;
        S3 : out STD_LOGIC;
        C_out : out STD_LOGIC);
end RCA_4;

architecture Behavioral of RCA_4 is
 component FA
   port (
    A: in std_logic;
    B: in std_logic;
    C_in: in std_logic;
    S: out std_logic;
    C_out: out std_logic);
 end component;

SIGNAL FA0_S, FA0_C, FA1_S, FA1_C, FA2_S, FA2_C, FA3_S, FA3_C  : std_logic;
begin
 FA_0 : FA
  port map (
  A => A0,
  B => B0,
  C_in => '0', -- Set to ground
  S => S0,
  C_Out => FA0_C);

 FA_1 : FA
  port map (
  A => A1,
  B => B1,
  C_in => FA0_C,
  S => S1,
  C_Out => FA1_C);

 FA_2 : FA
  port map (
  A => A2,
  B => B2,
  C_in => FA1_C,
  S => S2,
  C_Out => FA2_C);

 FA_3 : FA
  port map (
  A => A3,
  B => B3,
  C_in => FA2_C,
  S => S3,
  C_Out => C_out);


end Behavioral;
```

2)Slow_Clk

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 01:37:40 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
-- Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
 Port ( Clk_in : in STD_LOGIC;
        Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is
signal count: integer := 1;
signal clk_status: std_logic := '0';
begin
process (Clk_in) begin
 if (rising_edge (Clk_in)) then
     count <= count+1;
     if(count =4)then
         clk_status <= not (clk_status);
         Clk_out <= clk_status;
         count <= 1;
     end if;
```

```
 end if ;
end process;
end Behavioral;
```

3)Reg

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/28/2023 01:51:02 PM
-- Design Name:
-- Module Name: Reg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
-- Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg is
    Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
           En : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end Reg;

architecture Behavioral of Reg is

begin
process (Clk) begin
   if (rising_edge(Clk)) then -- respond when clock rises
     if En = '1' then -- Enable should be set
```

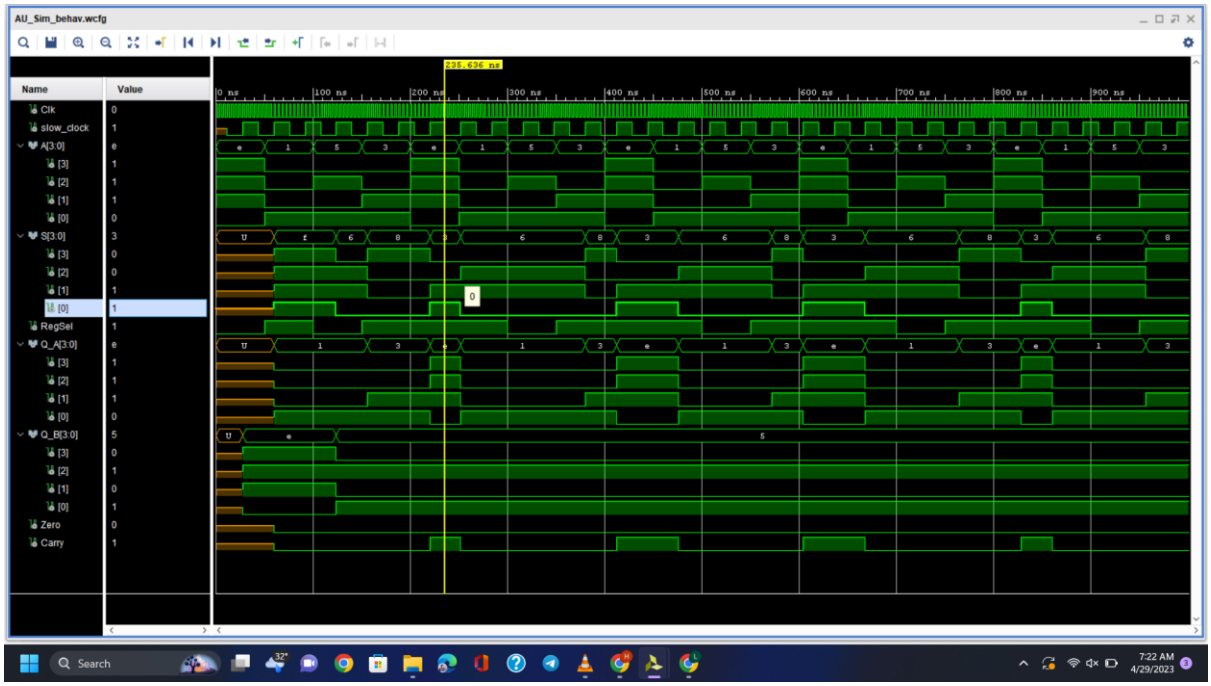
```
      Q <= D;
    end if;
  end if;
end process;

end Behavioral;
```

4)AU_Sim

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/28/2023 03:30:59 PM
-- Design Name:
-- Module Name: AU_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU_Sim is
--  Port ( );
end AU_Sim;

architecture Behavioral of AU_Sim is
component AU
```

```
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           RegSel : in STD_LOGIC;
           Clk : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR (3 downto 0);
           Zero : out STD_LOGIC;
           Carry : out STD_LOGIC);
end component;
signal A, S : STD_LOGIC_VECTOR (3 downto 0) := "0000";
signal RegSel , Clk, Zero, Carry : STD_LOGIC :='0';
begin
UUT :AU
    PORT MAP (
     A => A,
     RegSel => RegSel,
     Clk => Clk,
     S => S,
     Zero => Zero,
     Carry => Carry
     );

process
begin
    Clk <= NOT(Clk);
    wait for 2ns;
end process;

 process
begin
     --My index No:- 210206B
     A <= "1110" ;

     wait for 50ns;
     RegSel <= '1';
     A <= "0001" ;

     wait for 50ns;
     RegSel <= '0';
     A <= "0101" ;

     wait for 50ns;
     RegSel <= '1';
     A <= "0011" ;
     wait for 50ns;

end process;


end Behavioral;
```

Section 02


AU_Sim_behav.wcfg
Name
Value
Clk
slow_clock
A[3:0]
S[3:0]
RegSel
Q_A[3:0]
Q_B[3:0]
Zero
Carry
Search
7:22 AM
4/29/2023