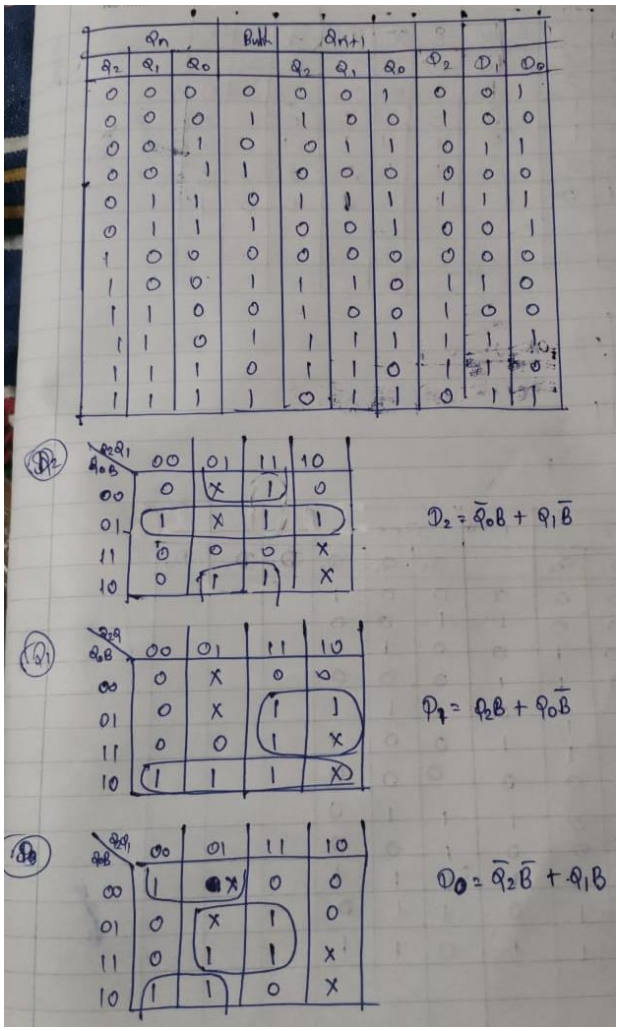
Name: N.Harikishna

Index No: 210206B

Section 01

This lab is focused on designing a 3-bit counter that can count in both clockwise and anticlockwise directions based on an external input. The lab requires knowledge of digital logic design, specifically flip-flops, combinational logic, and decoders.
The lab outcomes include the ability to design and develop a 3-bit counter, count in both directions based on an external input, and verify its functionality through simulation and on a development board.

Section 02



Section 03

1)D_FF

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 11:49:45 AM
-- Design Name:
-- Module Name: D_FF - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: N.Harikishna
-- Index No: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           QbaR : out STD_LOGIC);
end D_FF;

architecture Behavioral of D_FF is

begin
 process(Clk) begin
    if (rising_edge(Clk)) then
      if Res = '1' then
         Q <= '0';
         Qbar <= '1';
```

```
      else
         Q <= D;
         Qbar <= not D;
      end if;
    end if;
 end process;

end Behavioral;
```

2) D_FF_Sim

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 11:55:27 AM
-- Design Name:
-- Module Name: D_FF_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: N.Harikishna
-- Index No: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF_Sim is
--  Port ( );
end D_FF_Sim;

architecture Behavioral of D_FF_Sim is
component D_FF
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           QbaR : out STD_LOGIC);
```

```
end component;
signal D,Res : std_logic;
signal Clk : std_logic := '0';
signal Q,Qbar: std_logic;
begin
UUT: D_FF PORT MAP(
D => D,
Res => Res,
Clk => Clk,
Q => Q,
Qbar => Qbar
);

process
begin
    wait for 30 ns;
    Clk <= not Clk;
end process;

process
begin
 D <= '0';
 Res <= '1';

 wait for 20 ns;
 Res <= '0';

 while now < 1000 ns loop
  D <= not D ;
  wait for 25 ns;
 end loop;
 end process;
end Behavioral;
```

3)Slow_Clk

```
----------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 01:37:40 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name : N.Harikishna
```

```
-- Index No: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
 Port ( Clk_in : in STD_LOGIC;
        Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is
signal count: integer := 1;
signal clk_status: std_logic := '0';
begin
process (Clk_in) begin
 if (rising_edge (Clk_in)) then
      count <= count+1;
     if(count = 12) then
         clk_status <= not (clk_status);
         Clk_out <= clk_status;
         count <= 1;
      end if;
 end if ;
end process;
end Behavioral;
```

4)Slow_Clk_Sim

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 02:10:03 PM
-- Design Name:
-- Module Name: Slow_Clk_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
```

```
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk_Sim is
--  Port ( );
end Slow_Clk_Sim;

architecture Behavioral of Slow_Clk_Sim is
component Slow_Clk
Port ( Clk_in : in STD_LOGIC;
       Clk_out : out STD_LOGIC);
end component;
signal Clk_in : STD_LOGIC := '0';
signal Clk_out : STD_LOGIC;
begin
uut : Slow_Clk port map (
    Clk_in => Clk_in,
    Clk_out => Clk_out
    );
process
begin
       wait for 20 ns;
       Clk_in <= not Clk_in;
end process;
end Behavioral;
```

5) Counter

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 02:26:40 PM
-- Design Name:
-- Module Name: Counter - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
```

```
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end Counter;


architecture Behavioral of Counter is
 component D_FF
 port (
 D : in STD_LOGIC;
 Res: in STD_LOGIC;
 Clk : in STD_LOGIC;
 Q : out STD_LOGIC;
 Qbar : out STD_LOGIC);
 end component;

 component Slow_Clk
 port (
 Clk_in : in STD_LOGIC;
 Clk_out: out STD_LOGIC);
 end component;

 signal D0, D1, D2 : std_logic; -- Internal signals
 signal Q0, Q1, Q2 : std_logic; -- Internal signals
 signal Clk_slow : std_logic; -- Internal clock


begin
 Slow_Clk0 : Slow_Clk
 port map (
 Clk_in => Clk,
 Clk_out => Clk_slow);

 D0 <= ((not Q2) and (not Dir)) or (Q1 and Dir);
```

```
 D1 <= (Q2 and Dir) or (Q0 and (not Dir));
 D2 <= ((not Q0) and Dir) or (Q1 and (not Dir));

 D_FF0 : D_FF
 port map (
 D => D0,
 Res => Res,
 Clk => Clk_slow,
 Q => Q0);

 D_FF1 : D_FF
 port map (
 D => D1,
 Res => Res,
 Clk => Clk_slow,
 Q => Q1);

 D_FF2 : D_FF
 port map (
 D => D2,
 Res => Res,
 Clk => Clk_slow,
 Q => Q2);

 Q(0) <= Q0;
 Q(1) <= Q1;
 Q(2) <= Q2;
end Behavioral;
```

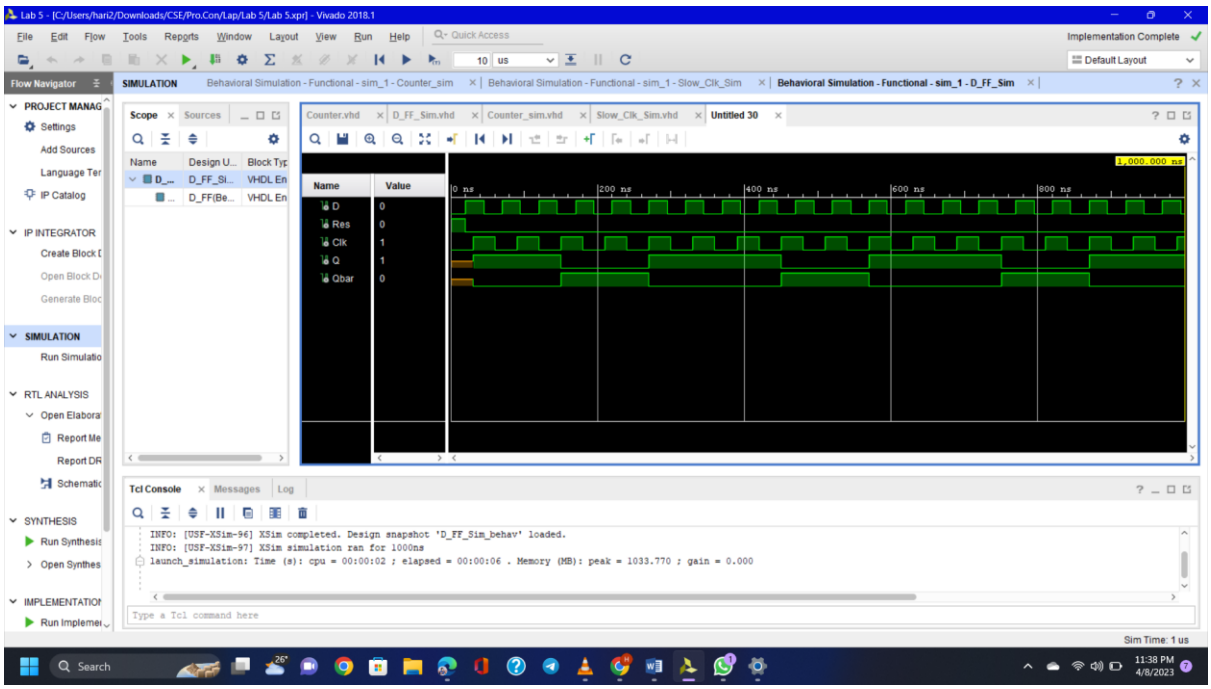
6)Counter_sim

```
----------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 11:09:53 PM
-- Design Name:
-- Module Name: Counter_sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

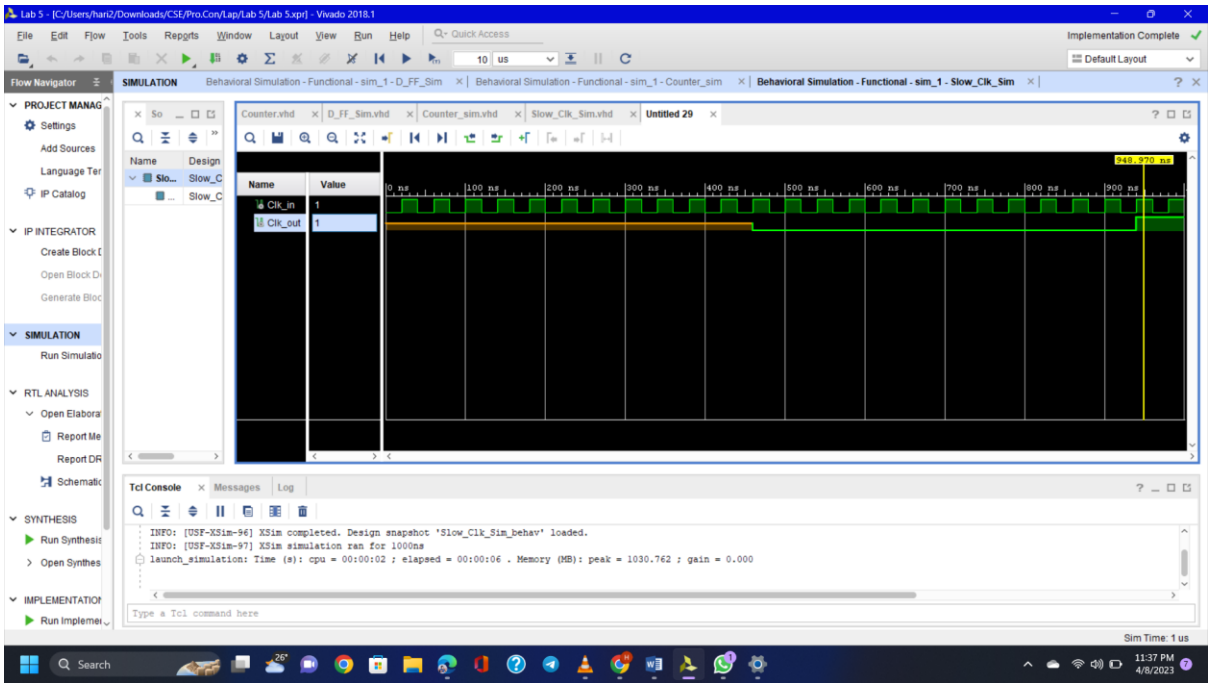
```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter_sim is
--  Port ( );
end Counter_sim;

architecture Behavioral of Counter_sim is
component Counter
    Port ( Dir : in STD_LOGIC;
       Res : in STD_LOGIC;
       Clk : in STD_LOGIC;
       Q : out STD_LOGIC_VECTOR (2 downto 0));
end component;
signal Dir,Clk : std_logic :='0';
signal Res : std_logic :='1';
signal Q : std_logic_vector (2 downto 0);
begin
UUT: Counter port map(
Dir => Dir,
Res => Res,
Clk => Clk,
Q => Q );

process
begin
wait for 1 ns;
Clk <= not Clk;
end process;

process
begin
wait for 50 ns;
Res <= '1';
wait for 20 ns;
Res <= '0';

Dir <= '0';
wait for 250 ns;
Dir <= '1';
wait;

end process;
end Behavioral;
```

Section 04

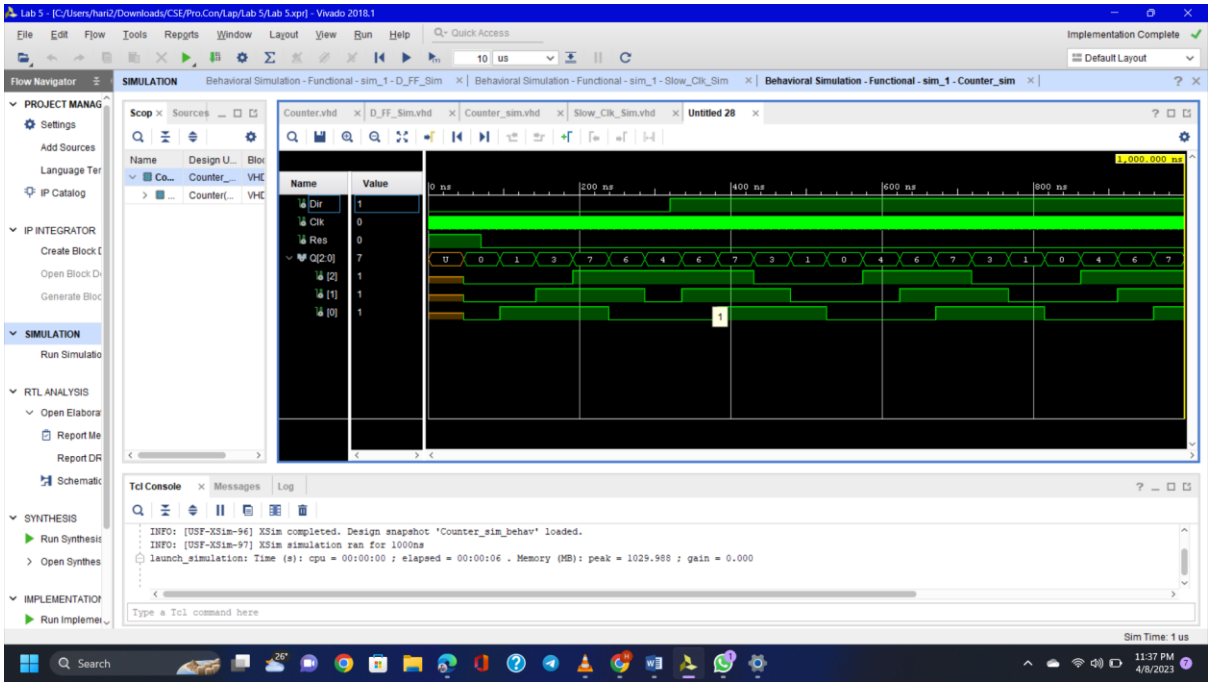
1)D_FF_Sim



2)Slow_Clk



3) Counter



Section 05

In this lab, I will designed a 3-bit counter with an external input.

After completing the lab, I am able to

: design and develop a 3-bit counter

: count in clockwise and anticlockwise directions based on an external input

:verify its functionality via simulation and on the development board