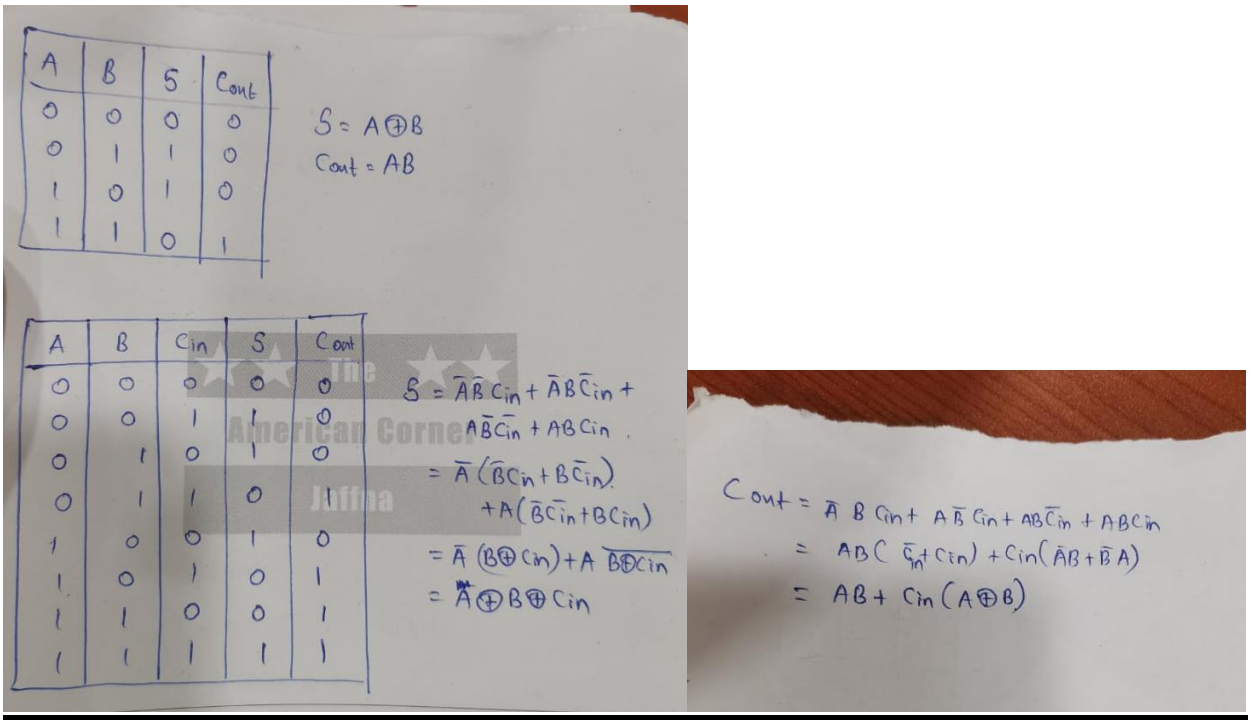
Name :- N. Harikishna

Index No :- 210206B

About Lab

The lab task requires designing a 4-bit Ripple Carry Adder (RCA) using Half Adders (HAs) and Full Adders (FAs). This involves building more complex components using basic components and following hierarchical design principles. The functionality of the RCA will be verified through simulation and testing on a development board. The RCA will be used for addition, and later in the course, it will be extended to support subtraction.

Truth table And Boolean Expressions



A	B	S	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = A \oplus B$

$Cout = AB$

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$= \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}) + A(\bar{B}\bar{C}_{in} + BC_{in})$

$= \bar{A}(B \oplus C_{in}) + A\overline{B \oplus C_{in}}$

$= A \oplus B \oplus C_{in}$

$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

$= ABC(\bar{C}_{in} + C_{in}) + C_{in}(\bar{A}B + \bar{B}A)$

$= AB + C_{in}(A \oplus B)$

VHDL Files

1)HA

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/17/2023 03:31:57 PM
-- Design Name:
-- Module Name: HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
--Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity HA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           S : out STD_LOGIC;
           C : out STD_LOGIC);
```

```
end HA;

architecture Behavioral of HA is

begin
    S <= A XOR B;
    C <= A AND B;

end Behavioral;
```

2)FA

```
----------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/17/2023 04:11:03 PM
-- Design Name:
-- Module Name: FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
--Index: 210206B
----------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
```

```
--use UNISIM.VComponents.all;

entity FA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
end FA;

architecture Behavioral of FA is
component HA
 port (
 A: in std_logic;
 B: in std_logic;
 S: out std_logic;
 C: out std_logic);
end component;
SIGNAL HA0_S, HA0_C, HA1_S, HA1_C : std_logic;

begin
HA_0 : HA
  port map (
  A => A,
  B => B,
  S => HA0_S,
  C => HA0_C);

HA_1 : HA
  port map (
  A => HA0_S,
  B => C_in,
  S => HA1_S,
  C => HA1_C);


  C_out <= HA0_C OR HA1_C;
  S <= HA1_S;


end Behavioral;
```

3)TB_HA

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/17/2023 03:43:21 PM
-- Design Name:
-- Module Name: TB_HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
--Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_HA is
--  Port ( );
end TB_HA;

architecture Behavioral of TB_HA is
COMPONENT HA
    PORT(A ,B: IN STD_LOGIC;
```

```
    S, C : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A ,B : std_logic;
SIGNAL S, C : std_logic;

begin
UUT: HA PORT MAP(
A => A,
B => B,
S => S,
C => C
);

process
begin
A <= '0';
B <= '0';


WAIT FOR 250 ns;
B <= '1';

WAIT FOR 250 ns;
A <= '1';
B <= '0';

WAIT FOR 250 ns;
B <= '1';

WAIT;

end process;
end Behavioral;
```

4)TB_FA

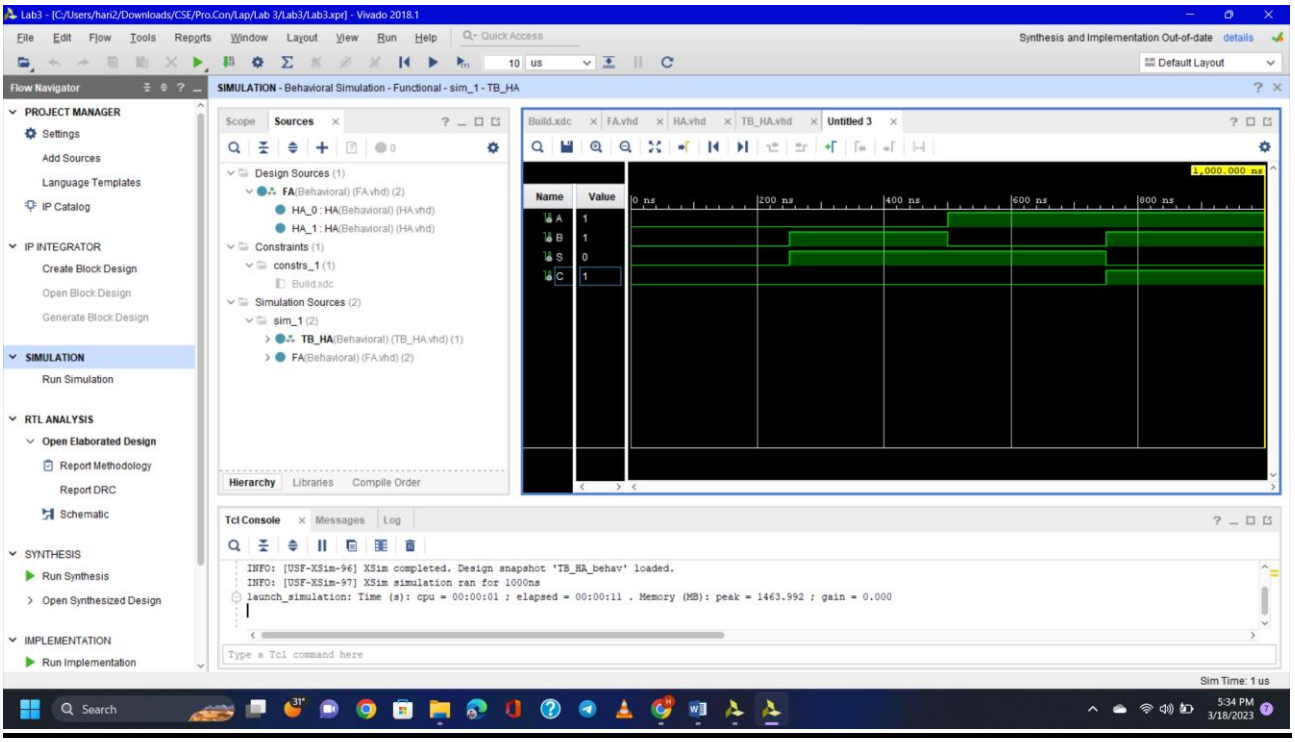
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 05:41:19 PM
-- Design Name:
-- Module Name: TB_FA - Behavioral
-- Project Name:
```

```
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
--Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_FA is
--  Port ( );
end TB_FA;

architecture Behavioral of TB_FA is
COMPONENT FA
    PORT(A ,B ,C_in: IN STD_LOGIC;
    S, C_out : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A ,B ,C_in : std_logic;
SIGNAL S, C_out : std_logic;

begin
UUT: FA PORT MAP(
A => A,
B => B,
C_in => C_in,
```

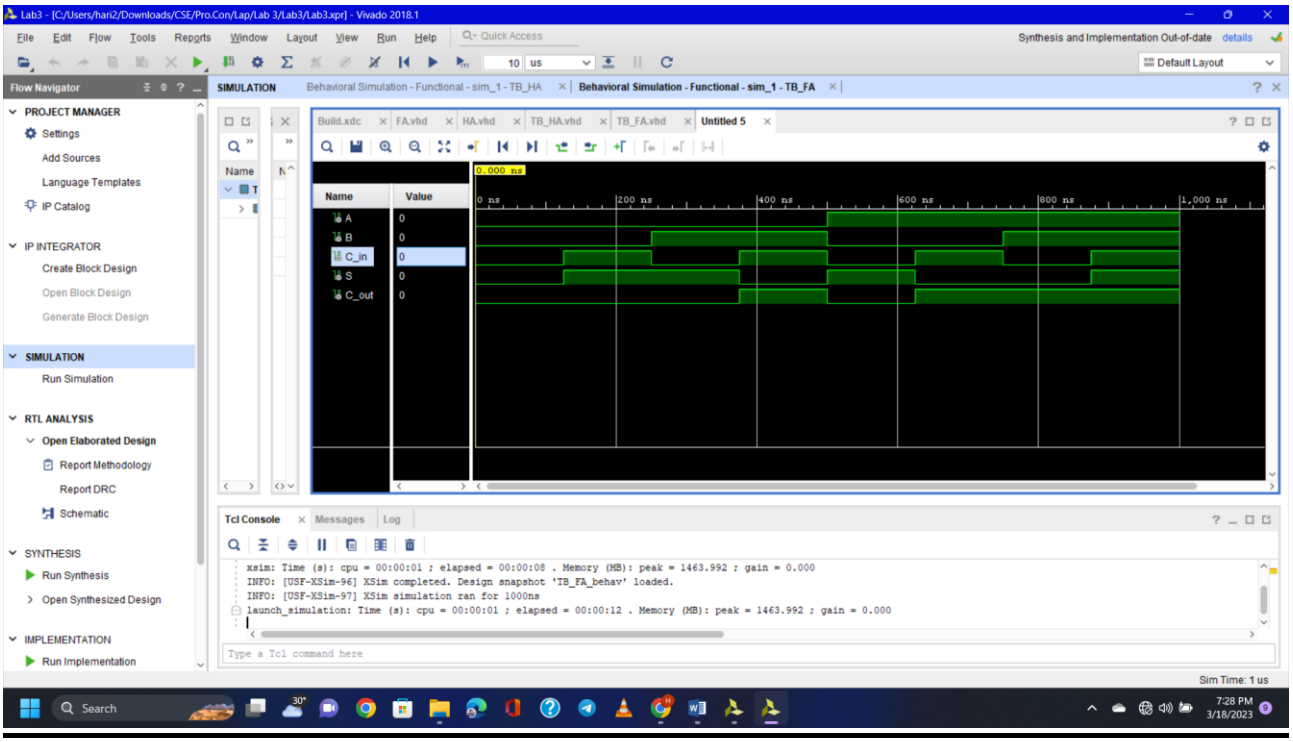
```
S => S,
C_out => C_out
);

process
begin
A <= '0';
B <= '0';
C_in <= '0';

WAIT FOR 125 ns;
C_in <= '1';

WAIT FOR 125 ns;
B <= '1';
C_in <= '0';

WAIT FOR 125 ns;
C_in <= '1';

WAIT FOR 125 ns;
A <= '1';
B <= '0';
C_in <= '0';

WAIT FOR 125 ns;
C_in <= '1';

WAIT FOR 125 ns;
B <= '1';
C_in <= '0';

WAIT FOR 125 ns;
C_in <= '1';

WAIT;

end process;
end Behavioral;
```

Timing Diagrams

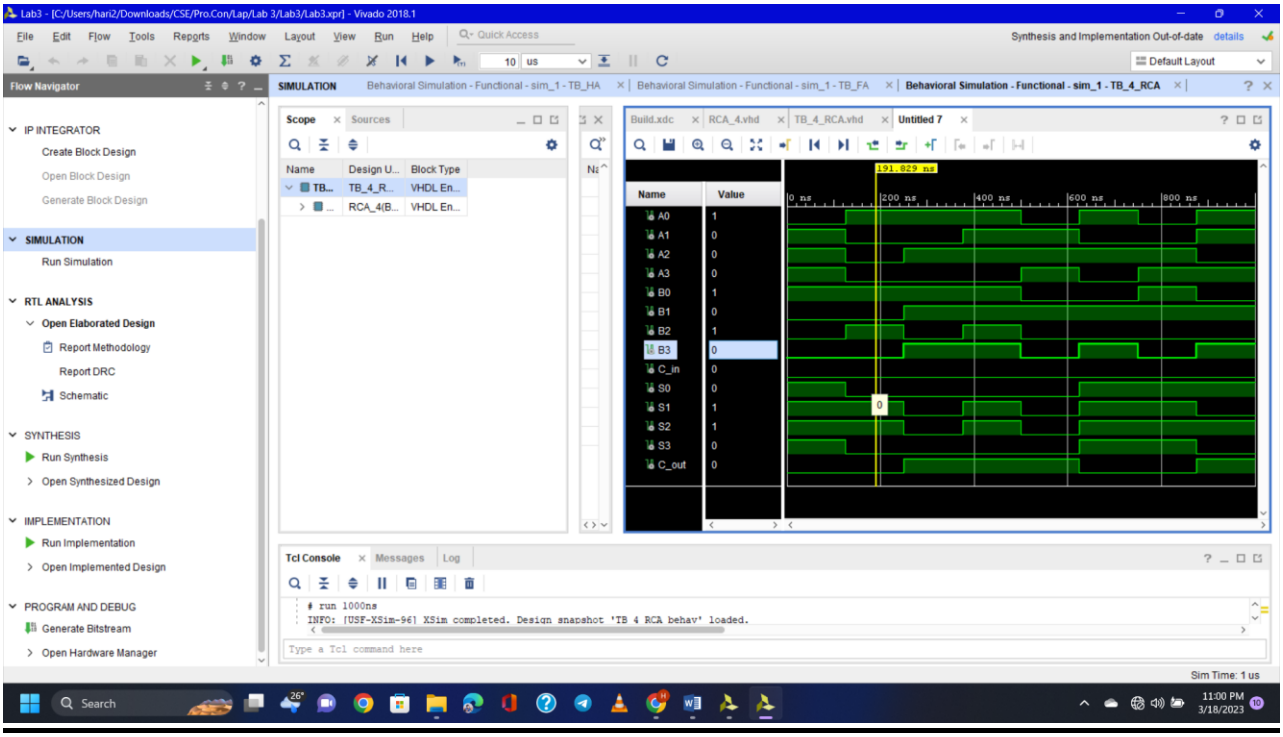
1)HA



2)FA



3)RCA_4



Discussion about LED representation

Since the inputs to the LED LD0-LD3 are represented in binary, they can only display a limited range of numbers. For example, if LD0-LD3 can display a maximum of 15 (1111 in binary), then any input combination that results in a sum greater than 15 cannot be displayed on the LED. In such cases, LD15 acts as an overflow indicator and lights up to signal that the output exceeds the range of the LED display.

Conclusions

Overall, this lab is a great way to gain practical knowledge about digital circuit design and verification. By building a 4-bit Ripple Carry Adder, I will gain hands-on experience with digital circuit design and learn about using simulation and development boards to test and verify the functionality of the circuit. This lab provides a solid foundation in digital circuit design and is a great starting point for learning about more advanced topics in digital systems and microprocessor design.