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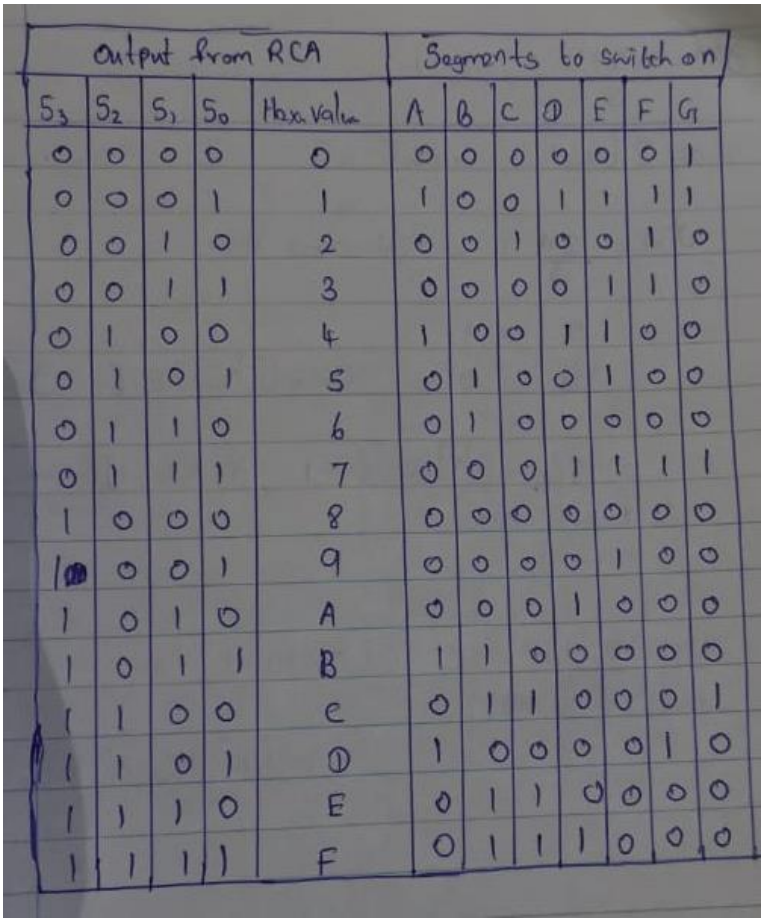
Index No:- 210206B

Section 01

The assigned lab task is to display the output of a 4-bit arithmetic unit as a hexadecimal number using a 7-segment display in BASYS 3. This involves mapping the 4-bit sum produced by the RCA to the appropriate segments on the display using a lookup table built using a ROM. The specific segments to be lit up depend on the hexadecimal value of the sum, and this can be achieved by implementing logic equations or using a lookup table.

Section 02



Output from RCA					Segments to switch on						
S_3	S_2	S_1	S_0	Hex value	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	0	0	1	1	1	1
0	0	1	0	2	0	0	1	0	0	1	0
0	0	1	1	3	0	0	0	0	1	1	0
0	1	0	0	4	1	0	0	1	1	0	0
0	1	0	1	5	0	1	0	0	1	0	0
0	1	1	0	6	0	1	0	0	0	0	0
0	1	1	1	7	0	0	0	1	1	1	1
1	0	0	0	8	0	0	0	0	0	0	0
1	0	0	1	9	0	0	0	0	1	0	0
1	0	1	0	A	0	0	0	1	0	0	0
1	0	1	1	B	1	1	0	0	0	0	0
1	1	0	0	C	0	1	1	0	0	0	1
1	1	0	1	D	1	0	0	0	0	1	0
1	1	1	0	E	0	1	1	0	0	0	0
1	1	1	1	F	0	1	1	1	0	0	0

Section 03

Annex 1 (Reg)

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/28/2023 01:51:02 PM
-- Design Name:
-- Module Name: Reg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
-- Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg is
    Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
           En : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end Reg;
```

```
architecture Behavioral of Reg is

begin
process (Clk) begin
  if (rising_edge(Clk)) then -- respond when clock rises
    if En = '1' then -- Enable should be set
      Q <= D;
    end if;
  end if;
end process;

end Behavioral;
```

Annex 2 (Slow_Clk)

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 01:37:40 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- Name: Harikishna
-- Index: 210206B
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
```

```
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
 Port ( Clk_in : in STD_LOGIC;
        Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is
signal count: integer := 1;
signal clk_status: std_logic := '0';
begin
process (Clk_in) begin
 if (rising_edge (Clk_in)) then
      count <= count+1;
      if(count =4)then
         clk_status <= not (clk_status);
         Clk_out <= clk_status;
         count <= 1;
      end if;
 end if ;
end process;
end Behavioral;
```

Annex 2 (LUT_16_7)

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 05/03/2023 07:25:44 PM
-- Design Name:
-- Module Name: LUT_16_7 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
```

```
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LUT_16_7 is
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end LUT_16_7;

architecture Behavioral of LUT_16_7 is

type rom_type is array (0 to 15) of std_logic_vector(6 downto 0);

 signal sevenSegment_ROM : rom_type := (
 "1000000", -- 0
 "1111001", -- 1
 "0100100", -- 2
 "0110000", -- 3
 "0011001", -- 4
 "0010010", -- 5
 "0000010", -- 6
 "1111000", -- 7
 "0000000", -- 8
 "0010000", -- 9
 "0001000", -- a
 "0000011", -- b
 "1000110", -- c
```

```
 "0100001", -- d
 "0000110", -- e
 "0001110"  -- f
 );

begin
data <= sevenSegment_ROM(to_integer(unsigned(address)));
end Behavioral;
```

Annex 4 (AU)

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/28/2023 02:00:30 PM
-- Design Name:
-- Module Name: AU - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity AU is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           RegSel : in STD_LOGIC;
           Clk : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR (3 downto 0);
           Zero : out STD_LOGIC;
           Carry : out STD_LOGIC);
end AU;

architecture Behavioral of AU is
component Slow_clk
     Port ( Clk_in : in STD_LOGIC;
            Clk_out : out STD_LOGIC);
end component;
component RCA_4
   Port ( A0 : in STD_LOGIC;
          A1 : in STD_LOGIC;
          A2 : in STD_LOGIC;
          A3 : in STD_LOGIC;
          B0 : in STD_LOGIC;
          B1 : in STD_LOGIC;
          B2 : in STD_LOGIC;
          B3 : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S0 : out STD_LOGIC;
          S1 : out STD_LOGIC;
          S2 : out STD_LOGIC;
          S3 : out STD_LOGIC;
          C_out : out STD_LOGIC);
end component;
component Reg
     Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
           En : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end component;
signal slow_clock : STD_LOGIC;
signal En_A,En_B,C_out : STD_LOGIC;
signal Q_A, Q_B, S_RCA : STD_LOGIC_VECTOR (3 downto 0);
begin

Slow_Clk_0 : Slow_Clk
```

```
    PORT MAP(
          Clk_in => Clk,
          Clk_out => slow_clock
           );

Reg_A : Reg
    PORT MAP(
          D => A,
          En => En_A,
          Clk => slow_clock,
          Q => Q_A
    );

Reg_B : Reg
    PORT MAP(
          D => A,
          En => En_B,
          Clk => slow_clock,
          Q => Q_B
    );

RCA_4_0 : RCA_4
    PORT  MAP(
          A0 => Q_A(0),
          A1 => Q_A(1),
          A2 => Q_A(2),
          A3 => Q_A(3),
          B0 => Q_B(0),
          B1 => Q_B(1),
          B2 => Q_B(2),
          B3 => Q_B(3),
          C_in =>'0',
          S0 => S_RCA(0),
          S1 => S_RCA(1),
          S2 => S_RCA(2),
          S3 => S_RCA(3),
          C_out => C_out
     );

    En_A <= RegSel;
    En_B <= NOT(RegSel);
    Carry <= C_out;
    S <= S_RCA;
```

```
    Zero <= NOT(S_RCA(0)) AND NOT(S_RCA(1)) AND NOT(S_RCA(2)) AND
NOT(S_RCA(3)) ;
end Behavioral;
```

Annex 5 (AU_7seg)

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 05/03/2023 08:38:41 PM
-- Design Name:
-- Module Name: AU_7_seg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU_7_seg is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           RegSel : in STD_LOGIC;
```

```
        S_LED : out STD_LOGIC_VECTOR (3 downto 0);
        S_7Seg : out STD_LOGIC_VECTOR (6 downto 0);
        Carry : out STD_LOGIC;
        Zero : out STD_LOGIC;
        Anode : out STD_LOGIC_VECTOR (3 downto 0)
        );
end AU_7_seg;

architecture Behavioral of AU_7_seg is
component AU
  Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
       RegSel : in STD_LOGIC;
       Clk : in STD_LOGIC;
       S : out STD_LOGIC_VECTOR (3 downto 0);
       Zero : out STD_LOGIC;
       Carry : out STD_LOGIC);

end component;

component LUT_16_7
   Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
       data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

component Slow_Clk
   Generic(count_max:integer);
   Port ( Clk_in : in STD_LOGIC;
       Clk_out : out STD_LOGIC);
end component;

signal S: STD_LOGIC_VECTOR (3 downto 0);
signal S_7s : STD_LOGIC_VECTOR (6 downto 0):= "0000000";
signal C, Clk_7seg: STD_LOGIC;
signal selected_7seg : integer := 0;

begin
AU_0: AU
     Port map (
       A => A,
       RegSel => RegSel,
       Clk => Clk_7seg,
       S => S,
       Zero => Zero,
```

```
        Carry => C);

LUT_16_7_0: LUT_16_7
    Port map (
        address => S,
        data => S_7s );

Slow_Clk_7seg: Slow_Clk

    Generic map(count_max => 100000)
    Port map (
        Clk_in => Clk,
        Clk_out => Clk_7seg);


S_LED <= S;
Carry <= C;
Anode <="1110";
end Behavioral;
```

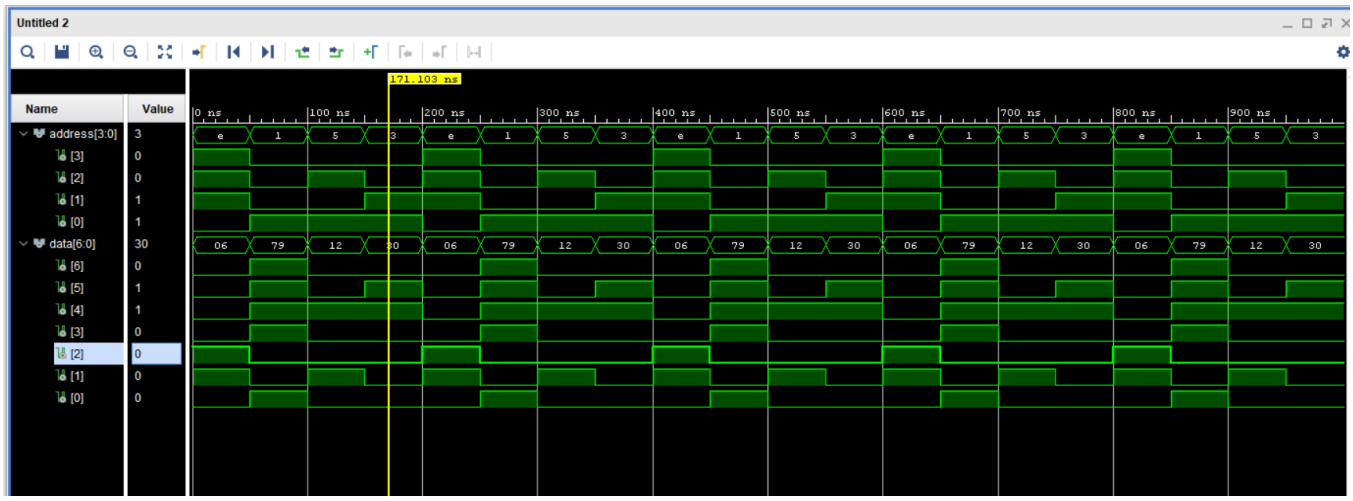
Annex 6 (LU_sim)

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 05/04/2023 07:30:37 PM
-- Design Name:
-- Module Name: LUT_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LUT_Sim is
--  Port ( );
end LUT_Sim;

architecture Behavioral of LUT_Sim is
component LUT_16_7
   Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
          data : out STD_LOGIC_VECTOR (6 downto 0));
end component;
signal address : STD_LOGIC_VECTOR (3 downto 0);
signal data : STD_LOGIC_VECTOR (6 downto 0);

begin
UUT: LUT_16_7
 port map(
     address => address,
     data => data
     );

process begin
--11 0011 0101 0001 1110
    address <="1110";
    wait for 50 ns;

    address <="0001";
    wait for 50 ns;

    address <="0101";
    wait for 50 ns;

    address <="0011";
```

```
    wait for 50 ns;

end process;
end Behavioral;
```

Section 04



Section 05

we explored the possibility of displaying the hexadecimal value of a 4-bit sum using only a single 7-segment display by splitting the sum into two groups of two bits each and displaying them on separate digits of the same display.

Section 06

1. Design and develop a lookup table using Read Only Memory (ROM) to map the output of a 4-bit arithmetic unit to a 7-segment display.
2. Design and develop a 7-segment display using the output from the lookup table to display a hexadecimal number.
3. Verify and demonstrate the functionality of the lookup table and 7-segment display through simulation and on a development board.