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-- Company:
-- Engineer:
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-- Create Date: 08.02.2023 09:47:43
-- Design Name:
-- Module Name: ALU_TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity ALU_TB is
```

```
--  Port ( );
end ALU_TB;

architecture Behavioral of ALU_TB is
SIGNAL A, B, C, D : std_logic_vector(7 downto 0);
SIGNAL C1,C3: std_logic_vector(2 downto 0);
SIGNAL C2: std_logic_vector(1 downto 0);
signal G: std_logic_vector(7 downto 0);
begin

UUT: entity work.top(behavioral)
port map( A => A, B => B, C => C, D => D, C1 => c1, C2 => c2, C3 =>
c3,G => G);

STIM: process
begin
A <= "00010000"; B <= "00000001"; C <= "00000010"; D <=
"00000001";C1 <= "000"; C2 <= "10"; C3 <= "011";
WAIT FOR 300ns;
A <= "00011001"; B <= "00000011"; C <= "00000010"; D <=
"00000111";C1 <= "010"; C2 <= "00"; C3 <= "111";
WAIT FOR 300ns;
A <= "00000111"; B <= "00000011"; C <= "00001010"; D <=
"00010011";C1 <= "111"; C2 <= "01"; C3 <= "000";
WAIT FOR 300ns;
A <= "01001001"; B <= "00010001"; C <= "01000000"; D <=
"00110011";C1 <= "100"; C2 <= "00"; C3 <= "101";
WAIT FOR 300ns;
A <= "00000111"; B <= "00000011"; C <= "00001010"; D <=
"00010011";C1 <= "111"; C2 <= "01"; C3 <= "110";
finish;
end process;
end Behavioral;
```