```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04.02.2023 14:48:04
-- Design Name:
-- Module Name: block1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

use IEEE.numeric_std.all;
```

```
entity block1 is
  Port ( y1 : out std_logic_vector(7 downto 0);
         A : in std_logic_vector(7 downto 0);
         B : in std_logic_vector(7 downto 0);
         c1 : in std_logic_vector(2 downto 0) );
end block1;

architecture Behavioral of block1 is
begin
  process (A, B, c1)
  begin
    case c1 is
      when "000" => y1 <= A and B;
      when "001" => y1 <= A or B;
      when "010" => y1 <= not (A and B);
      when "011" => y1 <= not (A or B);
      when "100" => y1 <= A xor B;
      when "101" => y1 <= not (A xor B);
      when others => y1 <= (others => 'Z');
    end case;
  end process;
end Behavioral;
```