```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.numeric_bit.all;


entity top is
port (
G: out std_logic_vector(7 downto 0);
A, B, C, D: in std_logic_vector(7 downto 0);
c1: in std_logic_vector(2 downto 0);
c2: in std_logic_vector(1 downto 0);
c3: in std_logic_vector(2 downto 0)
);
end entity;

architecture behavioral of top is
signal y1, y2, a_sig, b_sig: std_logic_vector(7 downto 0);
component block1 is
port (
y1: out std_logic_vector(7 downto 0);
A, B: in std_logic_vector(7 downto 0);
c1: in std_logic_vector(2 downto 0)
);
end component;

component block2 is
port (
y2: out std_logic_vector(7 downto 0);
C, D: in std_logic_vector(7 downto 0);
c2: in std_logic_vector(1 downto 0)
);
end component;


begin
```

```
dut1: block1 port map (y1 => y1, A => A, B => B , c1 => c1);
dut2: block2 port map (y2 => y2, C => C, D => D, c2 => c2);

process (c3, y1, y2) is
begin
case c3 is
when "000" =>
    IF (y1>y2) THEN
    G<= "11111111";
    ELSE
    G <= "00000000";
    END IF;

when "001" =>
    IF (y1<y2) THEN
    G <= "11111111";
    ELSE
    G <= "00000000";
    END IF;

when "010" =>
    IF (y1=y2) THEN
    G<= "11111111";
    ELSE
    G <= "00000000";
    END IF;

when "011" =>
    IF (y1 >= y2) THEN
    G <= "11111111";
    ELSE
    G <= "00000000";
    END IF;

when "100" =>
IF (y1 <= y2) THEN
    G <= "11111111";
```

```
    ELSE
    G <= "00000000";
    END IF;

when "101" =>
    IF (y1/= y2) THEN
    G <= "11111111";
    ELSE
    G <= "00000000";
    END IF;
 when "110" =>
    G <= "ZZZZZZZZ";
  when "111" =>
    G <= "ZZZZZZZZ";
  WHEN OTHERS =>
    G <= "00000000";
end case;
end process;

end architecture;
```