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-- Company:
-- Engineer:
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-- Create Date: 04.02.2023 14:48:49
-- Design Name:
-- Module Name: block2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity block2 is
```

```
  Port ( y2 : out std_logic_vector(7 downto 0);
         C : in std_logic_vector(7 downto 0);
         D : in std_logic_vector(7 downto 0);
         c2 : in std_logic_vector(1 downto 0);
         x: inout std_logic_vector(15 downto 0) );

end block2;

architecture Behavioral of block2 is
signal c_sig, d_sig: signed(7 downto 0);
begin
c_sig <= signed(C);
d_sig <= signed(D);
process(C,D, c2)
begin
Case c2 is
    when "00" => y2 <= std_logic_vector( c_sig + d_sig);
    when "01" => y2 <= std_logic_vector( c_sig - d_sig);
    when "10" => x <= std_logic_vector( c_sig * d_sig);
    y2 <= x(7 downto 0);
    when others => y2 <= ( others => '0');
    end case;
  end process;
end Behavioral;
```