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#-----------------------------------------------------------
# Vivado v2022.2 (64-bit)
# SW Build 3671981 on Fri Oct 14 05:00:03 MDT 2022
# IP Build 3669848 on Fri Oct 14 08:30:02 MDT 2022
# Start of session at: Thu Feb  9 10:41:05 2023
# Process ID: 6924
# Current directory: E:/img/Comp_4_Bit/Comp_4_Bit.runs/synth_1
# Command line: vivado.exe -log Comp_4_Bit.vds -product Vivado
-mode batch -messageDb vivado.pb -notrace -source Comp_4_Bit.tcl
# Log file:
E:/img/Comp_4_Bit/Comp_4_Bit.runs/synth_1/Comp_4_Bit.vds
# Journal file:
E:/img/Comp_4_Bit/Comp_4_Bit.runs/synth_1\vivado.jou
# Running On: LAPTOP-AOQK0D16, OS: Windows, CPU Frequency: 2496
MHz, CPU Physical cores: 4, Host memory: 6827 MB
#-----------------------------------------------------------
source Comp_4_Bit.tcl -notrace
create_project: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 .
Memory (MB): peak = 1000.309 ; gain = 116.934
Command: read_checkpoint -auto_incremental -incremental
E:/img/Comp_4_Bit/Comp_4_Bit.srcs/utils_1/imports/synth_1/Comp_4_Bi
t.dcp
INFO: [Vivado 12-5825] Read reference checkpoint from
E:/img/Comp_4_Bit/Comp_4_Bit.srcs/utils_1/imports/synth_1/Comp_4_Bi
t.dcp for incremental synthesis
INFO: [Vivado 12-7989] Please ensure there are no constraint
changes
Command: synth_design -top Comp_4_Bit -part xc7vx485tffg1157-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device
'xc7vx485t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or
device 'xc7vx485t'
INFO: [Common 17-86] Your Synthesis license expires in 21 day(s)
INFO: [Designutils 20-5440] No compile time benefit to using
incremental synthesis; A full resynthesis will be run
INFO: [Designutils 20-4379] Flow is switching to default flow due
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to incremental criteria not met. If you would like to alter this
behaviour and have the flow terminate instead, please set the
following parameter config_implementation
{autoIncr.Synth.RejectBehavior Terminate}
INFO: [Synth 8-7079] Multithreading enabled for synth_design using
a maximum of 2 processes.
INFO: [Synth 8-7078] Launching helper process for spawning children
vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 15012
INFO: [Synth 8-11241] undeclared symbol 'REGCCE', assumed default
net type 'wire'
[E:/Vivado/2022.2/data/verilog/src/unimacro/BRAM_SINGLE_MACRO.v:217
0]
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Starting Synthesize : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07
. Memory (MB): peak = 1440.398 ; gain = 408.051
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INFO: [Synth 8-638] synthesizing module 'Comp_4_Bit'
[E:/img/Comp_4_Bit/Comp_4_Bit.srcs/sources_1/new/Comp_4_Bit.vhd:43]
INFO: [Synth 8-226] default block is never used
[E:/img/Comp_4_Bit/Comp_4_Bit.srcs/sources_1/new/Comp_4_Bit.vhd:47]
INFO: [Synth 8-256] done synthesizing module 'Comp_4_Bit' (0#1)
[E:/img/Comp_4_Bit/Comp_4_Bit.srcs/sources_1/new/Comp_4_Bit.vhd:43]
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Finished Synthesize : Time (s): cpu = 00:00:09 ; elapsed = 00:00:10
. Memory (MB): peak = 1529.867 ; gain = 497.520
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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed
= 00:00:11 . Memory (MB): peak = 1529.867 ; gain = 497.520
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Start Loading Part and Timing Information
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Loading part: xc7vx485tffg1157-1
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Finished Loading Part and Timing Information : Time (s): cpu =
00:00:10 ; elapsed = 00:00:11 . Memory (MB): peak = 1529.867 ; gain
= 497.520
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INFO: [Device 21-403] Loading part xc7vx485tffg1157-1
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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ;
elapsed = 00:00:11 . Memory (MB): peak = 1529.867 ; gain = 497.520
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No constraint files found.
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Start RTL Component Statistics
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Detailed RTL Component Info :
+---Muxes :
       4 Input    4 Bit        Muxes := 1
-----------------------------------------------------------------------
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Finished RTL Component Statistics
-----------------------------------------------------------------------
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Start Part Resource Summary
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Part Resources:
DSPs: 2800 (col length:140)
BRAMs: 2060 (col length: RAMB18 140 RAMB36 70)
---------------------------------------------------------------------
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Finished Part Resource Summary
---------------------------------------------------------------------
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No constraint files found.
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Start Cross Boundary and Area Optimization
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WARNING: [Synth 8-7080] Parallel synthesis criteria is not met
---------------------------------------------------------------------
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Finished Cross Boundary and Area Optimization : Time (s): cpu =
00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1875.828 ; gain
= 843.480
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No constraint files found.
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Start Timing Optimization
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Finished Timing Optimization : Time (s): cpu = 00:00:22 ; elapsed =
00:00:23 . Memory (MB): peak = 1881.445 ; gain = 849.098
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Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1881.625 ; gain = 849.277

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup


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Finished IO Insertion : Time (s): cpu = 00:00:28 ; elapsed =
00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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Start Renaming Generated Instances
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-----------------------------------------------------------------------
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Finished Renaming Generated Instances : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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Start Rebuilding User Hierarchy
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-----------------------------------------------------------------------
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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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Start Renaming Generated Ports
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-----------------------------------------------------------------------
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Finished Renaming Generated Ports : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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Start Handling Custom Attributes
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Finished Handling Custom Attributes : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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-------------
Start Renaming Generated Nets
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-------------------------------------------------------------------------
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Finished Renaming Generated Nets : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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Start Writing Synthesis Report
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Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
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+------+-----+------+
|1     |LUT4 |     2|
|2     |LUT5 |     2|
|3     |IBUF |     6|
|4     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    14|
+------+---------+-------+------+
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Finished Writing Synthesis Report : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
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Synthesis finished with 0 errors, 0 critical warnings and 1
warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:28 ; elapsed
= 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
Synthesis Optimization Complete : Time (s): cpu = 00:00:28 ;
elapsed = 00:00:29 . Memory (MB): peak = 1882.426 ; gain = 850.078
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed =
00:00:00 . Memory (MB): peak = 1894.461 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed =
00:00:00 . Memory (MB): peak = 2010.176 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete, checksum: ade12a09
INFO: [Common 17-83] Releasing license: Synthesis
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19 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:32 ; elapsed = 00:00:36 .
Memory (MB): peak = 2010.176 ; gain = 986.000
INFO: [Common 17-1381] The checkpoint
'E:/img/Comp_4_Bit/Comp_4_Bit.runs/synth_1/Comp_4_Bit.dcp' has been
generated.
INFO: [runtcl-4] Executing : report_utilization -file
Comp_4_Bit_utilization_synth.rpt -pb
Comp_4_Bit_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Thu Feb  9 10:41:57 2023...
```