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# Vivado v2022.2 (64-bit)  
# SW Build 3671981 on Fri Oct 14 05:00:03 MDT 2022  
# IP Build 3669848 on Fri Oct 14 08:30:02 MDT 2022  
# Start of session at: Thu Feb 9 10:33:07 2023  
# Process ID: 8928  
# Current directory:  
E:/img/Multi32To1/Multi32To1.runs/synth_1_copy_2  
# Command line: vivado.exe -log Mux32_1.vds -product Vivado -mode  
batch -messageDb vivado.pb -notrace -source Mux32_1.tcl  
# Log file:  
E:/img/Multi32To1/Multi32To1.runs/synth_1_copy_2/Mux32_1.vds  
# Journal file:  
E:/img/Multi32To1/Multi32To1.runs/synth_1_copy_2\vivado.jou  
# Running On: LAPTOP-AOQK0D16, OS: Windows, CPU Frequency: 2496  
MHz, CPU Physical cores: 4, Host memory: 6827 MB  
#-----  
source Mux32_1.tcl -notrace  
create_project: Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 .  
Memory (MB): peak = 1001.316 ; gain = 117.465  
Command: read_checkpoint -auto_incremental -incremental  
E:/img/Multi32To1/Multi32To1.srcs/utils_1/imports/synth_1/synth_1_c  
opy_1/Mux32_1.dcp  
INFO: [Vivado 12-5825] Read reference checkpoint from  
E:/img/Multi32To1/Multi32To1.srcs/utils_1/imports/synth_1/synth_1_c  
opy_1/Mux32_1.dcp for incremental synthesis  
INFO: [Vivado 12-7989] Please ensure there are no constraint  
changes  
Command: synth_design -top Mux32_1 -part xczu19eg-ffve1924-1-i  
Starting synth_design  
Attempting to get a license for feature 'Synthesis' and/or device  
'xczu19eg'  
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or  
device 'xczu19eg'  
INFO: [Common 17-86] Your Synthesis license expires in 21 day(s)  
INFO: [Designutils 20-5440] No compile time benefit to using  
incremental synthesis; A full resynthesis will be run
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INFO: [Designutils 20-4379] Flow is switching to default flow due
to incremental criteria not met. If you would like to alter this
behaviour and have the flow terminate instead, please set the
following parameter config_implementation
{autoIncr.Synth.RejectBehavior Terminate}
INFO: [Synth 8-7079] Multithreading enabled for synth_design using
a maximum of 2 processes.
INFO: [Synth 8-7078] Launching helper process for spawning children
vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 10720
INFO: [Synth 8-11241] undeclared symbol 'REGCCE', assumed default
net type 'wire'
[E:/Vivado/2022.2/data/verilog/src/unimacro/BRAM_SINGLE_MACRO.v:217
0]
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Starting Synthesize : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08
. Memory (MB): peak = 1443.438 ; gain = 407.660
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INFO: [Synth 8-638] synthesizing module 'Mux32_1'
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux32_1.vhd:42]
INFO: [Synth 8-638] synthesizing module 'Mux8_1'
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux8_1.vhd:42]
INFO: [Synth 8-226] default block is never used
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux8_1.vhd:47]
INFO: [Synth 8-256] done synthesizing module 'Mux8_1' (0#1)
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux8_1.vhd:42]
INFO: [Synth 8-638] synthesizing module 'Mux4_1'
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux4_1.vhd:46]
INFO: [Synth 8-226] default block is never used
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux4_1.vhd:51]
INFO: [Synth 8-256] done synthesizing module 'Mux4_1' (0#1)
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux4_1.vhd:46]
INFO: [Synth 8-256] done synthesizing module 'Mux32_1' (0#1)
[E:/img/Multi32To1/Multi32To1.srcs/sources_1/new/Mux32_1.vhd:42]
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Finished Synthesize : Time (s): cpu = 00:00:09 ; elapsed = 00:00:11  
. Memory (MB): peak = 1532.762 ; gain = 496.984  
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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed  
= 00:00:11 . Memory (MB): peak = 1532.762 ; gain = 496.984  
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Start Loading Part and Timing Information  
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Loading part: xczu19eg-ffve1924-1-i  
INFO: [Synth 8-6742] Reading net delay rules and data  
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Finished Loading Part and Timing Information : Time (s): cpu =  
00:00:10 ; elapsed = 00:00:11 . Memory (MB): peak = 1532.762 ; gain  
= 496.984  
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INFO: [Device 21-403] Loading part xczu19eg-ffve1924-1-i  
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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ;  
elapsed = 00:00:12 . Memory (MB): peak = 1532.762 ; gain = 496.984  
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No constraint files found.  
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Start RTL Component Statistics  
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Detailed RTL Component Info :

+---Muxes :

4 Input      5 Bit              Muxes := 1

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Finished RTL Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 1968 (col length:264)

BRAMs: 1968 (col length: RAMB18 264 RAMB36 132)

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Finished Part Resource Summary

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No constraint files found.

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Start Cross Boundary and Area Optimization

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WARNING: [Synth 8-7080] Parallel synthesis criteria is not met

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Finished Cross Boundary and Area Optimization : Time (s): cpu =  
00:00:25 ; elapsed = 00:00:29 . Memory (MB): peak = 2556.785 ; gain  
= 1521.008

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No constraint files found.

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Start Timing Optimization  
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Finished Timing Optimization : Time (s): cpu = 00:00:25 ; elapsed =  
00:00:29 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Technology Mapping  
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Finished Technology Mapping : Time (s): cpu = 00:00:25 ; elapsed =  
00:00:29 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start IO Insertion  
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Start Flattening Before IO Insertion  
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Finished Flattening Before IO Insertion  
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Start Final Netlist Cleanup  
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Finished Final Netlist Cleanup  
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Finished IO Insertion : Time (s): cpu = 00:00:31 ; elapsed =  
00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Renaming Generated Instances  
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Finished Renaming Generated Instances : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Rebuilding User Hierarchy  
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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Renaming Generated Ports  
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Finished Renaming Generated Ports : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Handling Custom Attributes  
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Finished Handling Custom Attributes : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Renaming Generated Nets  
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Finished Renaming Generated Nets : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008  
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Start Writing Synthesis Report

Report BlackBoxes:

BlackBox name		Instances

Report Cell Usage:

	Cell	Count
1	LUT6	45
2	MUXF7	20
3	IBUF	165
4	OBUF	5

Report Instance Areas:

	Instance	Module	Cells
1	top		235

Finished Writing Synthesis Report : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008

Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:31 ; elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008

Synthesis Optimization Complete : Time (s): cpu = 00:00:31 ;  
elapsed = 00:00:36 . Memory (MB): peak = 2556.785 ; gain = 1521.008



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INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed =
00:00:00.007 . Memory (MB): peak = 2556.785 ; gain = 0.000
INFO: [Netlist 29-17] Analyzing 185 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 1 CPU
seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed =
00:00:00 . Memory (MB): peak = 2638.207 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 165 instances were transformed.
  IBUF => IBUF (IBUFCTRL, INBUF): 165 instances

Synth Design complete, checksum: 6a0dbc94
INFO: [Common 17-83] Releasing license: Synthesis
27 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:35 ; elapsed = 00:00:40 .
Memory (MB): peak = 2638.207 ; gain = 1612.008
INFO: [Common 17-1381] The checkpoint
'E:/img/Multi32To1/Multi32To1.runs/synth_1_copy_2/Mux32_1.dcp' has
been generated.
INFO: [runtcl-4] Executing : report_utilization -file
Mux32_1_utilization_synth.rpt -pb Mux32_1_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Thu Feb  9 10:34:02 2023...
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