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-- Company:
-- Engineer:
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-- Create Date: 03/27/2024 11:33:48 AM
-- Design Name:
-- Module Name: CU_With_Resistor - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity CU_With_Resistor is
--  Port ( );
```

```
generic(do:integer:=4);
Port (A, B, C, D, e, f, g, h: IN std_logic_vector(do-1 downto 0);
op: in std_logic_vector(do downto 0);
MXsel1, mxSel2: in std_logic_vector(1 downto 0);
clk:in std_logic;
R_en1,R_en2,R_en3,R_en4: in std_logic;
o: out std_logic_vector(do-1 downto 0)
 );
end CU_With_Resistor;

architecture Behavioral of CU_With_Resistor is
signal mxo1, mxo2, ro1, ro2: std_logic_vector(do-1 downto 0);
signal  ro3: std_logic_vector(do downto 0);
signal c1: std_logic_vector( do-1 downto 0);
begin
mx1: entity work.mux4_1(Behavioral)
port map(a=> a,b =>b, c=>c, d=> d ,sel => mxsel1, y => mxo1);

mx2: entity work.mux4_1(Behavioral)
port map(a=> e,b =>f, c=>g, d=> h,sel => mxsel2,y => mxo2 );

res1: entity work.registor(Behavioral)
generic map(dw=> 4)
port map(clk => clk, R_en=> R_en1,a =>mxo1, z =>ro1 );

res2: entity work.registor(Behavioral)
generic map(dw=> 4)
port map(clk => clk, R_en=> R_en2,a =>mxo2, z =>ro2 );

res3: entity work.registor(Behavioral)
generic map(dw=> 5)
port map(clk => clk, R_en=>R_en3 ,a =>op, z =>ro3 );

CU: entity work.compunit(Behavioral)
port map(A=> ro1,B => ro2,s =>ro3 ,o => c1 );

res4: entity work.registor(Behavioral)
```

```
generic map(dw=> 4)
port map(clk => clk, R_en=>R_en4 ,a =>c1, z =>o );

end Behavioral;
```