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-- Company:
-- Engineer:
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-- Create Date: 03/27/2024 04:50:45 PM
-- Design Name:
-- Module Name: Top_Box - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top_Box is
--  Port ( );
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generic(do:integer:=4);
Port (A0, A1, A2,A3, B0, B1, B2, B3: IN std_logic_vector (do-1
downto 0) ;

op0, op1, op2,op3,op4, op5, op6, op7: in std_logic_vector (do
downto 0) ;

clk: in std_logic;
MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30,
mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61,
MXsel70,mxSel71: in std_logic_vector (1 downto 0);
R_en1, R_en2, R_en3, R_en4: in std_logic;

o00,o01,o02,o03, o10, o11, o12, o13: out std_logic_vector (do-1
downto 0));
end Top_Box;

architecture Behavioral of Top_Box is
signal Y00,Y01,Y02,Y03,Y10,Y11,Y12,Y13: std_logic_vector(do-1
downto 0);
begin
cu_100: entity work.CU_With_Resistor (Behavioral)
port map( A => a0, B => y01, C => "0000", D => "0000",e => b0, f
=>y01 ,g => "0000",h => "0000" ,
 MXsel1 => mxSel00, op => op0,mxSel2 => mxSel01, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y00);

cu_101: entity work.CU_With_Resistor (Behavioral)
port map( A => a1, B => y00, C => y02, D => "0000",e => b1, f =>y00
,g => y02,h => "0000" ,
 MXsel1 => mxSel10, op => op1,mxSel2 => mxSel11, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y01);

cu_102: entity work.CU_With_Resistor (Behavioral)
port map( A => a2, B => y01, C => y03, D => "0000",e => b2, f =>y01
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,g => y03,h => "0000" ,
 MXsel1 => mxSel20, op => op2,mxSel2 => mxSel21, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y02);

cu_103: entity work.CU_With_Resistor (Behavioral)
port map( A => a3, B => y02, C => "0000", D => "0000",e => b3, f
=>y02 ,g => "0000",h => "0000" ,
 MXsel1 => mxSel30, op => op3,mxSel2 => mxSel31, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y03);

cu_110: entity work.CU_With_Resistor (Behavioral)
port map( A => y00, B => y11, C => "0000", D => "0000",e => y00, f
=>y11 ,g => "0000",h => "0000" ,
 MXsel1 => mxSel40, op => op4,mxSel2 => mxSel41, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y10);

cu_111: entity work.CU_With_Resistor (Behavioral)
port map( A => y01, B => y10, C => y12, D => "0000",e => y01, f
=>y10 ,g => y12,h => "0000" ,
 MXsel1 => mxSel50, op => op5,mxSel2 => mxSel51, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y11);

cu_112: entity work.CU_With_Resistor (Behavioral)
port map( A => y02, B => y11, C => y13, D => "0000",e => y02, f
=>y11 ,g => y13,h => "0000" ,
 MXsel1 => mxSel60, op => op6,mxSel2 => mxSel61, clk => clk,R_en1
=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y12);

cu_113: entity work.CU_With_Resistor (Behavioral)
port map( A => y03, B => y12, C => "0000", D => "0000",e => y03, f
=>y12 ,g => "0000",h => "0000" ,
 MXsel1 => mxSel70, op => op7,mxSel2 => mxSel71, clk => clk,R_en1
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=> R_en1, R_en2 => R_en2, R_en3 => R_en3, R_en4 => R_en4,
o => y13);

o00 <= y00;
o01 <= y01;
o02 <= y02;
o03 <= y03;
o10 <= y10;
o11 <= y11;
o12 <= y12;
o13 <= y13;
end Behavioral;
```