EENG HW 5Report Template

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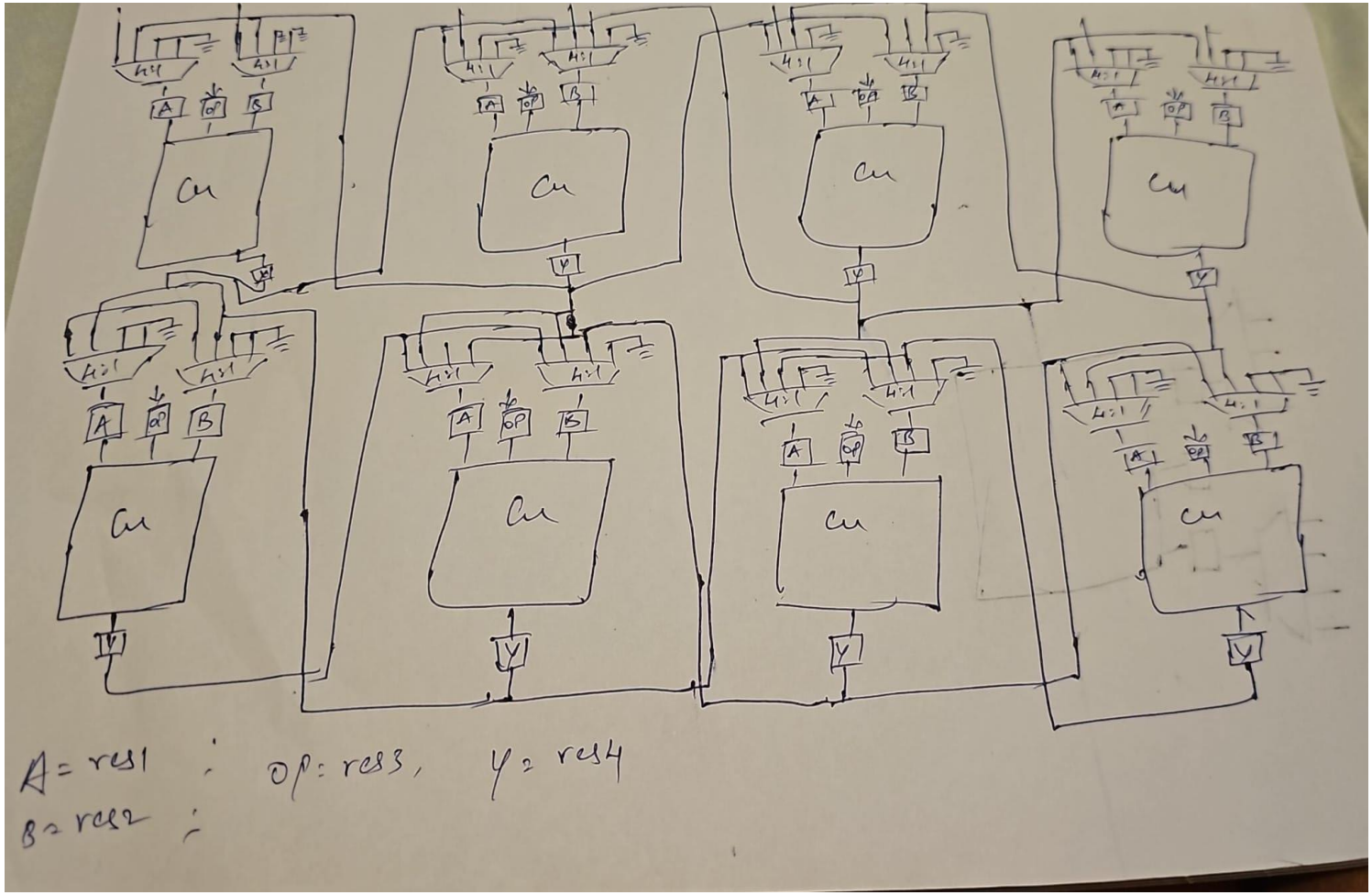
Design

Block diagrams

Overall design


4:1
A
OP
B
ALU
Y
A = reg1 ; OP: reg3, Y = reg4
B = reg2 ;

Overall component: top box

Parameters: d_w – data width (for inputs and outputs)

Input ports:

Port name	Bit width	Purpose
A0, A1, A2,A3, B0, B1, B2, B3	d_w = 4	Data inputs
op0, op1, op2,op3,op4, op5, op6, op7		Selection line for cu
MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30, mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61, MXsel70,mxSel71	2	Mux selection lines
R_en1, R_en2, R_en3, R_en4	1	enable

Output ports:

Port name	Bit width	Purpose
o00,o01,o02,o03, o10, o11, o12, o13	d_w = 4	Data output

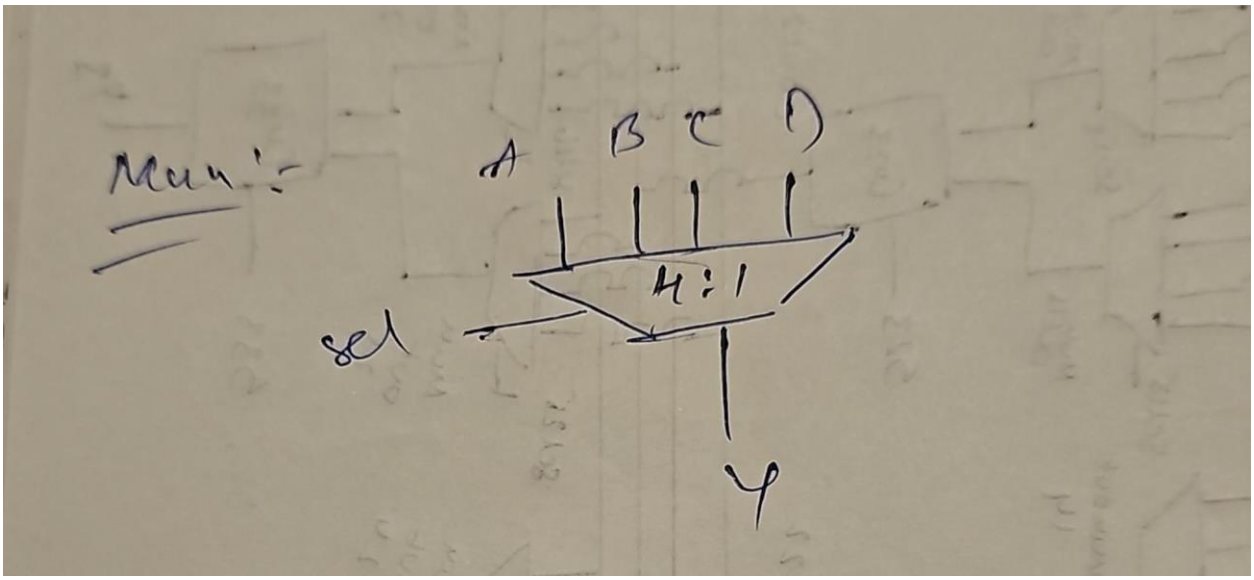
Necessary intermediate signals:

If there are no intermediate signals, you can remove this section name and table

Port name	Bit width	Purpose
Y00,Y01,Y02,Y03,Y10,Y11,Y12,Y13	d_w = 4	Intermediate signals

Subcomponents

Mux :



Input ports:

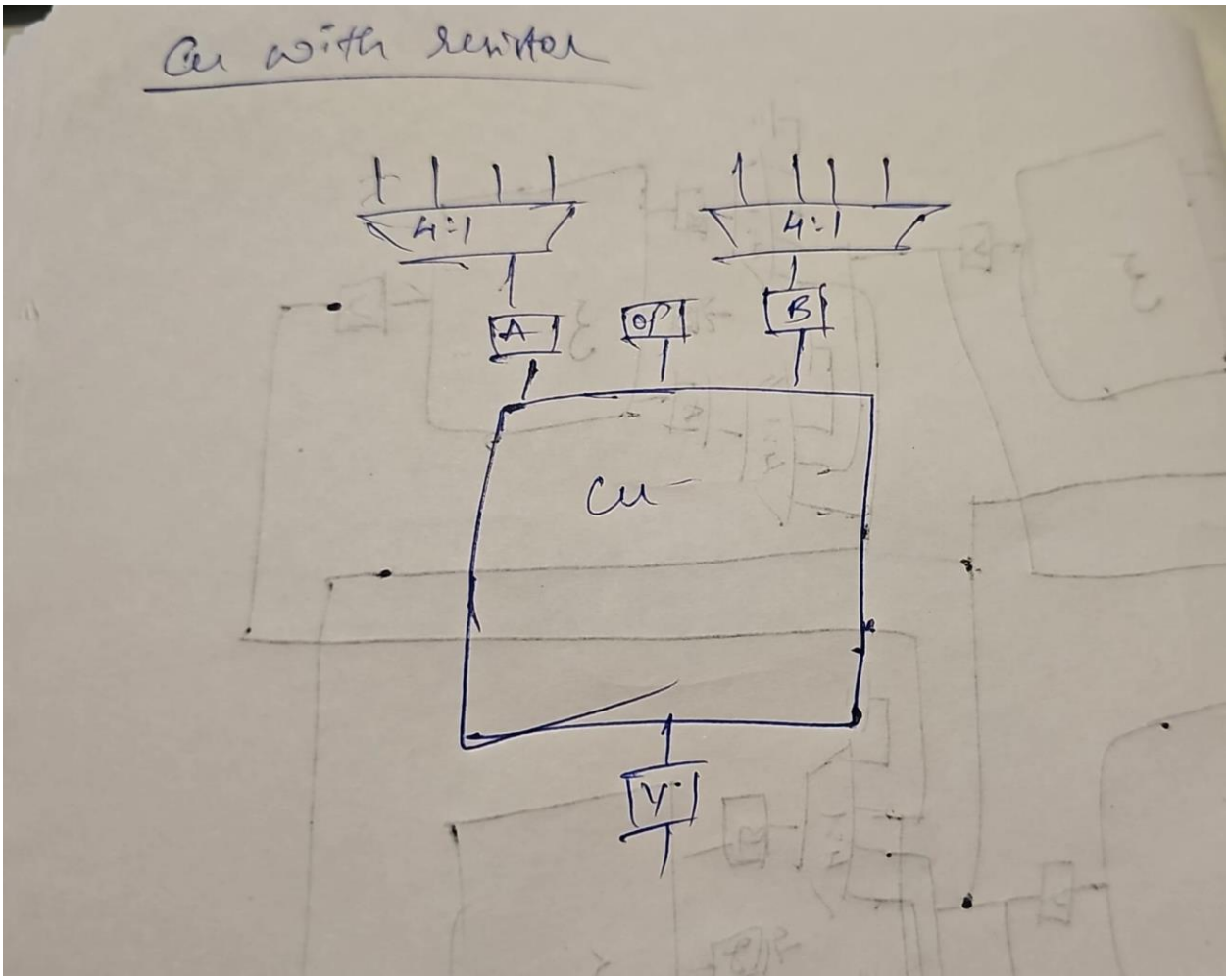
Port name	Bit width	Purpose
A,b,c,d	d_w = 4	Data inputs
Sel	1	Select line, selects which of the 2 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
Y	d_w = 4	Data output

*Necessary intermediate signals: *

Cu with resistor:



Input ports:

Port name	Bit width	Purpose
I0, I1, I2, I3	d_w = 4	Data inputs
Sel	2	Select line, selects which of the 4 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
y	d_w = 4	Data output

Design explanation

It is a 2 by 4 architecture pre configurable

Both inputs and outputs are stored units.

The data flow according to design .

A0, A1, A2,A3, B0, B1, B2, B3 are data inputs.

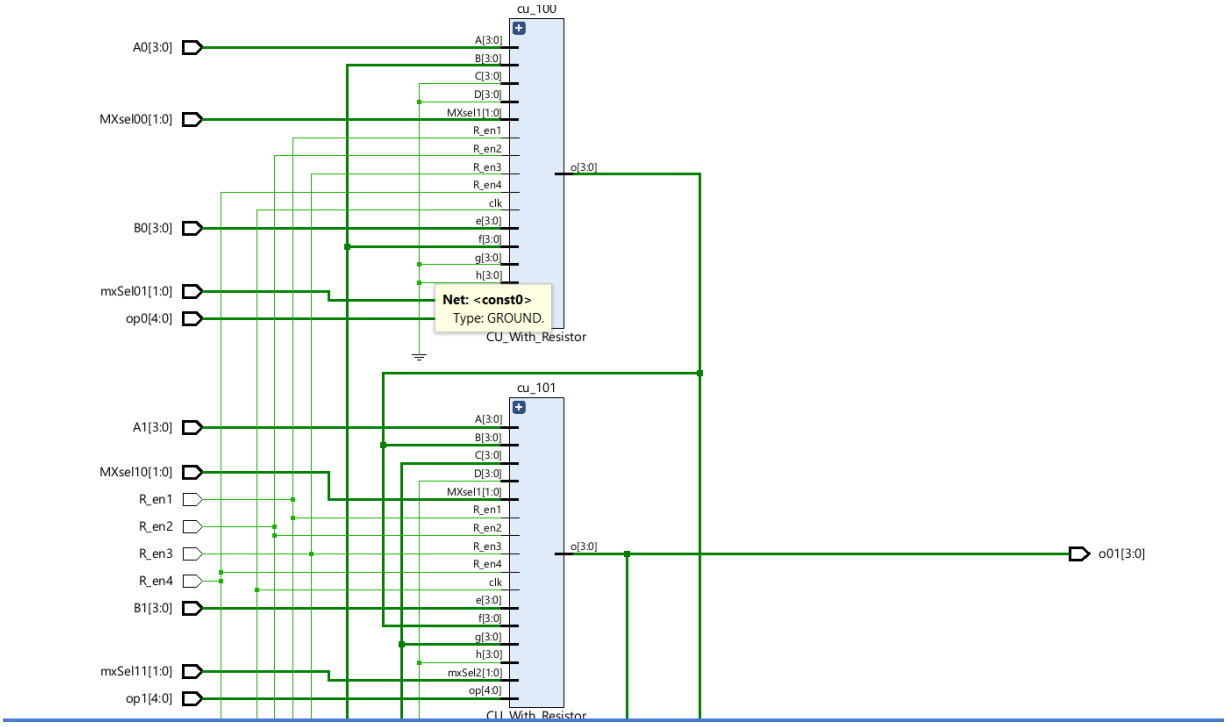
op0, op1, op2,op3,op4, op5, op6, op7 selections lines for cu.

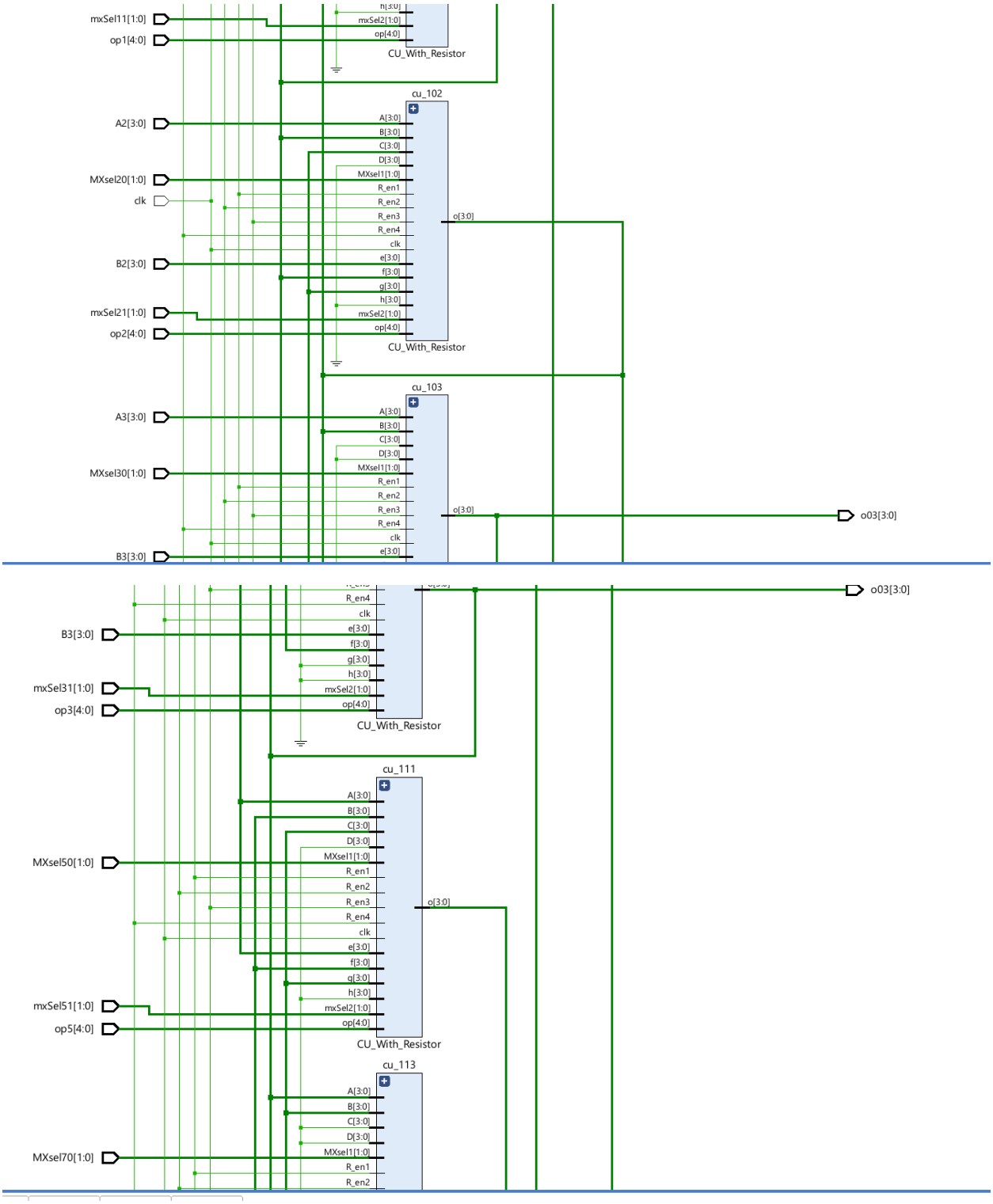
MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30, mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61, MXsel70,mxSel71 are mux selection lines.

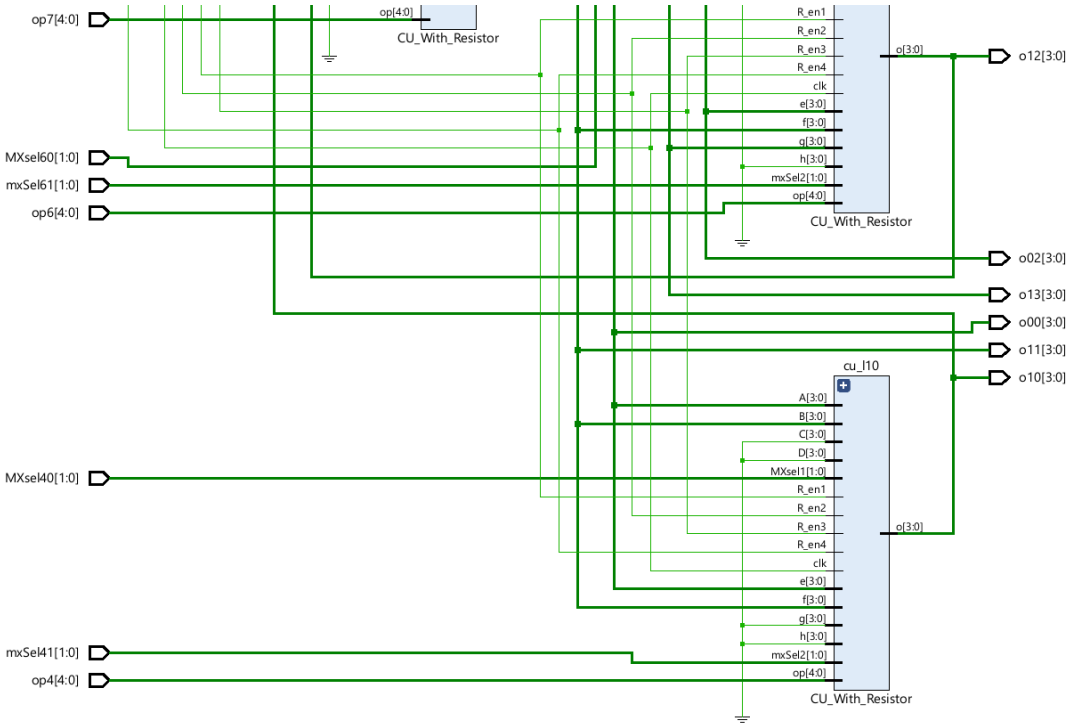
o00,o01,o02,o03, o10, o11, o12, o13 are out puts

Results

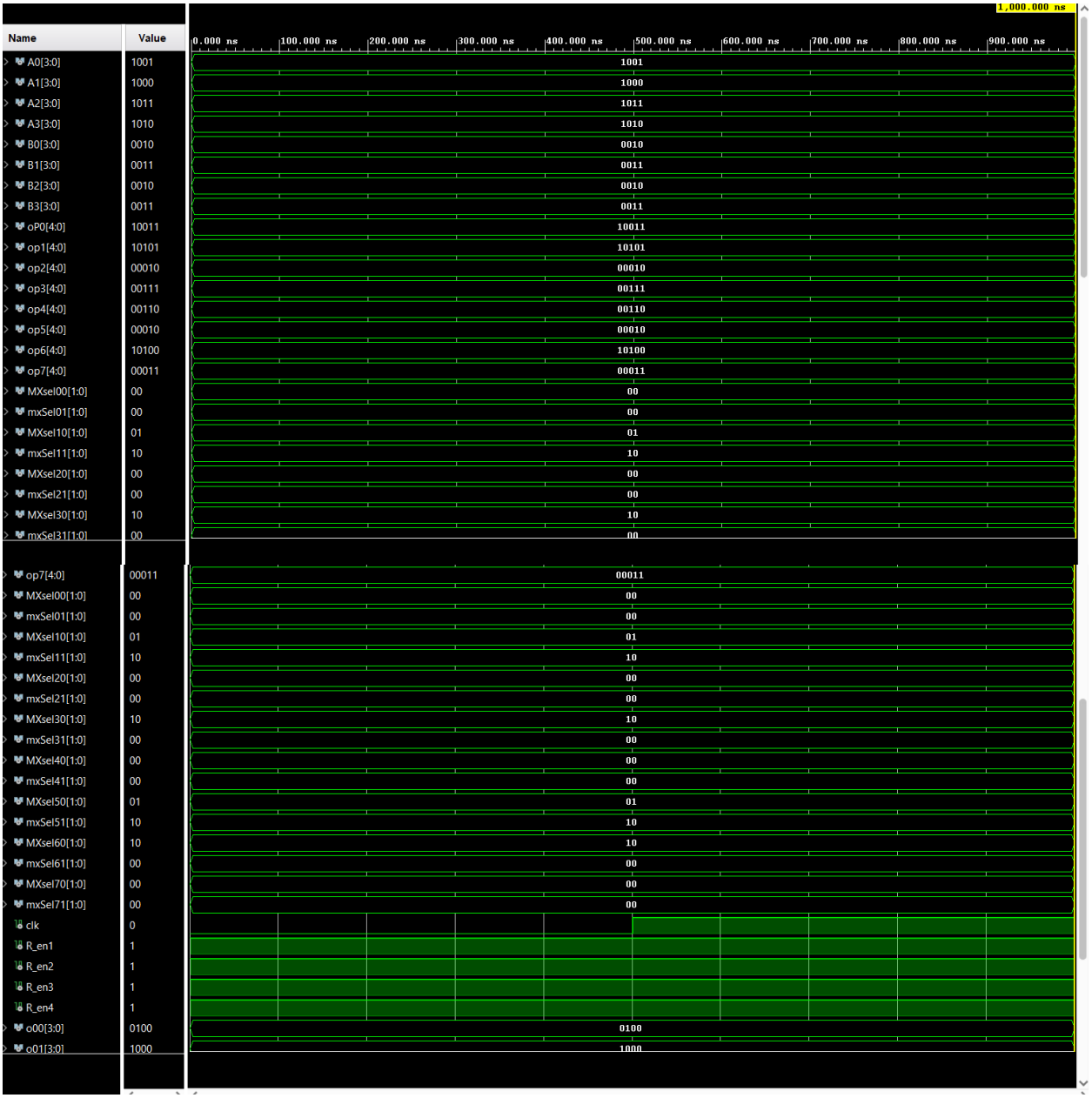
Generated Schematics

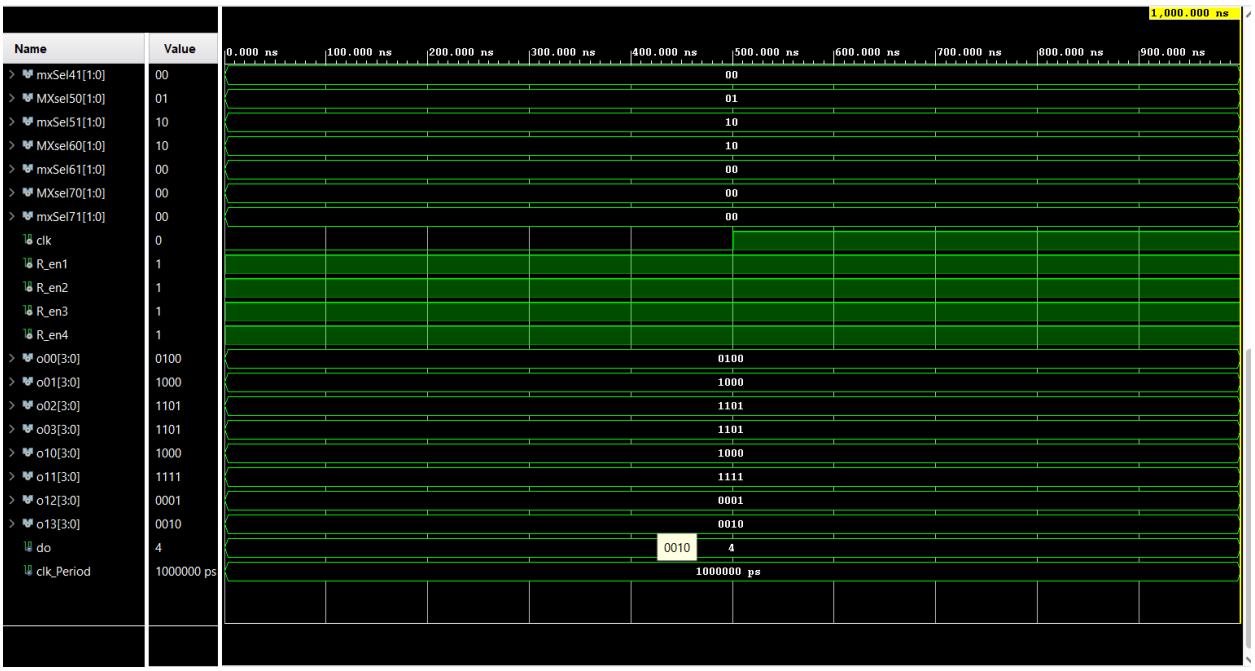



mxSel11[1:0]
op1[4:0]
CU_With_Resistor
cu_102
A2[3:0]
MXsel20[1:0]
clk
B2[3:0]
mxSel21[1:0]
op2[4:0]
CU_With_Resistor
cu_103
A3[3:0]
MXsel30[1:0]
B3[3:0]
o03[3:0]
mxSel31[1:0]
op3[4:0]
CU_With_Resistor
cu_111
MXsel50[1:0]
mxSel51[1:0]
op5[4:0]
CU_With_Resistor
cu_113
MXsel70[1:0]

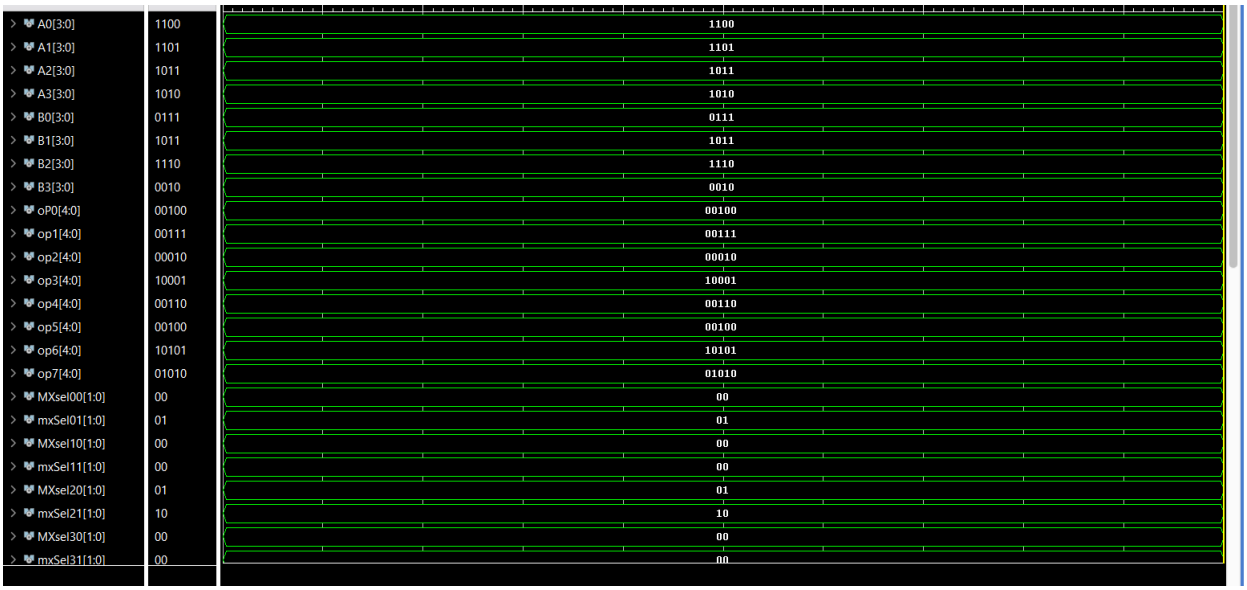

op7[4:0]
op[4:0]
CU_With_Resistor
MXsel60[1:0]
mxSel61[1:0]
op6[4:0]
R_en1
R_en2
R_en3
R_en4
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
o12[3:0]
CU_With_Resistor
o02[3:0]
o13[3:0]
o00[3:0]
o11[3:0]
o10[3:0]
cu_l10
A[3:0]
B[3:0]
C[3:0]
D[3:0]
MXsel1[1:0]
MXsel40[1:0]
R_en1
R_en2
R_en3
R_en4
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
mxSel41[1:0]
op4[4:0]
CU_With_Resistor

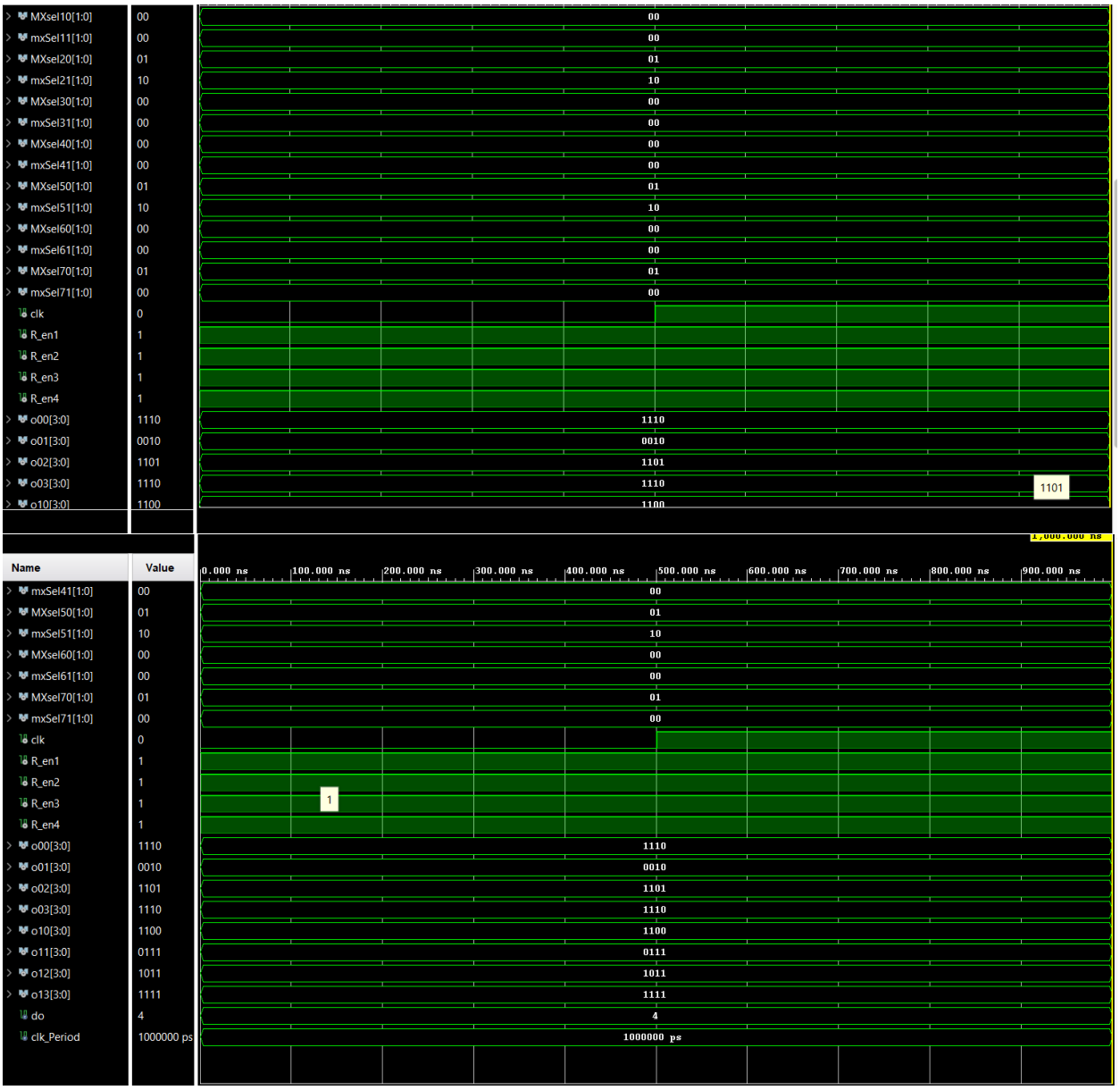
Waveforms


Name
Value
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000.000 ns
A0[3:0] 1001
A1[3:0] 1000
A2[3:0] 1011
A3[3:0] 1010
B0[3:0] 0010
B1[3:0] 0011
B2[3:0] 0010
B3[3:0] 0011
oP0[4:0] 10011
op1[4:0] 10101
op2[4:0] 00010
op3[4:0] 00111
op4[4:0] 00110
op5[4:0] 00010
op6[4:0] 10100
op7[4:0] 00011
MXsel00[1:0] 00
mxSel01[1:0] 00
MXsel10[1:0] 01
mxSel11[1:0] 10
MXsel20[1:0] 00
mxSel21[1:0] 00
MXsel30[1:0] 10
mxSel31[1:0] 00
op7[4:0] 00011
MXsel00[1:0] 00
mxSel01[1:0] 00
MXsel10[1:0] 01
mxSel11[1:0] 10
MXsel20[1:0] 00
mxSel21[1:0] 00
MXsel30[1:0] 10
mxSel31[1:0] 00
MXsel40[1:0] 00
mxSel41[1:0] 00
MXsel50[1:0] 01
mxSel51[1:0] 10
MXsel60[1:0] 10
mxSel61[1:0] 00
MXsel70[1:0] 00
mxSel71[1:0] 00
clk 0
R_en1 1
R_en2 1
R_en3 1
R_en4 1
o00[3:0] 0100
o01[3:0] 1000


Name
Value
mxSel41[1:0]
00
MXsel50[1:0]
01
mxSel51[1:0]
10
MXsel60[1:0]
10
mxSel61[1:0]
00
MXsel70[1:0]
00
mxSel71[1:0]
00
clk
0
R_en1
1
R_en2
1
R_en3
1
R_en4
1
o00[3:0]
0100
o01[3:0]
1000
o02[3:0]
1101
o03[3:0]
1101
o10[3:0]
1000
o11[3:0]
1111
o12[3:0]
0001
o13[3:0]
0010
do
4
clk_Period
1000000 ps
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000.000 ns
0010
4
1000000 ps

- Test case 2


A0[3:0]
1100
A1[3:0]
1101
A2[3:0]
1011
A3[3:0]
1010
B0[3:0]
0111
B1[3:0]
1011
B2[3:0]
1110
B3[3:0]
0010
oP0[4:0]
00100
op1[4:0]
00111
op2[4:0]
00010
op3[4:0]
10001
op4[4:0]
00110
op5[4:0]
00100
op6[4:0]
10101
op7[4:0]
01010
MXsel00[1:0]
00
mxSel01[1:0]
01
MXsel10[1:0]
00
mxSel11[1:0]
00
MXsel20[1:0]
01
mxSel21[1:0]
10
MXsel30[1:0]
00
mxSel31[1:0]
00



Table/Calculations

Overall Design

My output for test case 1 is taken from cu11 that is

Test Case # (*0ns to 5ns*):

CU#	SourceA	SourceB	A	B	Oper	Calculated Op	Simulated Op	Match
CU1	A	B	0011	0010	MULT	0110	0110	Yes
CU2	C	D	0101	0100	ADD	1001	1001	Yes
CU3	CU1	CU2	0110	1001	LT	1111	1111	Yes

…								

Test Case # (*5ns to 10ns*):

CU#	SourceA	SourceB	A	B	Oper	Calculated Op	Simulated Op	Match
CU1	A	B	0011	0010	MULT	0110	0110	Yes
CU2	C	D	0101	0100	ADD	1001	1001	Yes
CU3	CU1	CU2	0110	1001	LT	1111	1111	Yes
…								

Subcomponent test cases

Test Case # (*0ns to 5ns*):

A	B	Oper	Calculated Op	Simulated Op	Match
0011	0010	MULT (000)	0110	0110	Yes
0101	0100	ADD (001)	1001	1001	Yes
0110	1001	LT (010)	1111	1111	Yes
…					

Test Case # (*5ns to 10ns*):

A	B	Oper	Calculated Op	Simulated Op	Match
0011	0010	MULT (000)	0110	0110	Yes
0101	0100	ADD (001)	1001	1001	Yes
0110	1001	LT (010)	1111	1111	Yes
…					