```
----------------------------------------------------------------------
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-- Company:
-- Engineer:
--
-- Create Date: 03/27/2024 10:55:30 AM
-- Design Name:
-- Module Name: Mux2_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux2_1 is
--  Port ( );
```

```
generic( dw: integer:=4);
Port (a,b: in std_logic_vector(dw-1 downto 0);
sel: in std_logic_vector(dw-4 downto 0);
y: out std_logic_vector(dw-1 downto 0) );

end Mux2_1;

architecture Behavioral of Mux2_1 is

begin
process(a,b,sel)
begin
case sel is
when "0" => y <= a;
when "1" => y <= b;
when others => y <= (others => '0');
end case;
end process;
end Behavioral;
```