

# EENG HW 5Report Template

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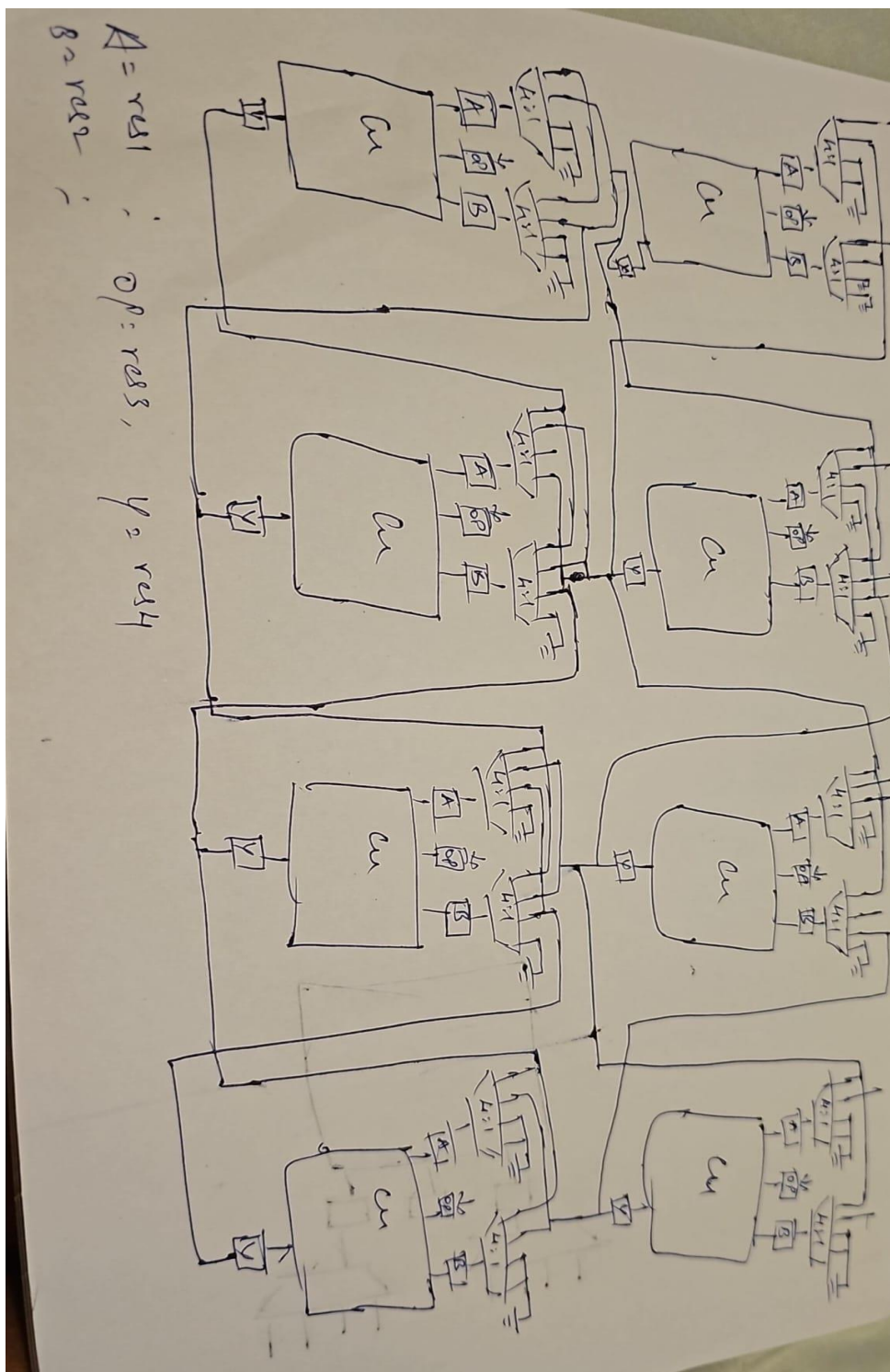
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## **Design**

**Block diagrams**

**Overall design**



Overall component: top box

Parameters: d\_w – data width (for inputs and outputs)

Input ports:

Port name	Bit width	Purpose
<b>A0, A1, A2,A3, B0, B1, B2, B3</b>	d_w = 4	Data inputs
<b>op0, op1, op2,op3,op4, op5, op6, op7</b>		Selection line for cu
<b>MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30, mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61, MXsel70,mxSel71</b>	2	Mux selection lines
<b>R_en1, R_en2, R_en3, R_en4</b>	1	enable

Output ports:

Port name	Bit width	Purpose
<b>o00,o01,o02,o03, o10, o11, o12, o13</b>	d_w = 4	Data output

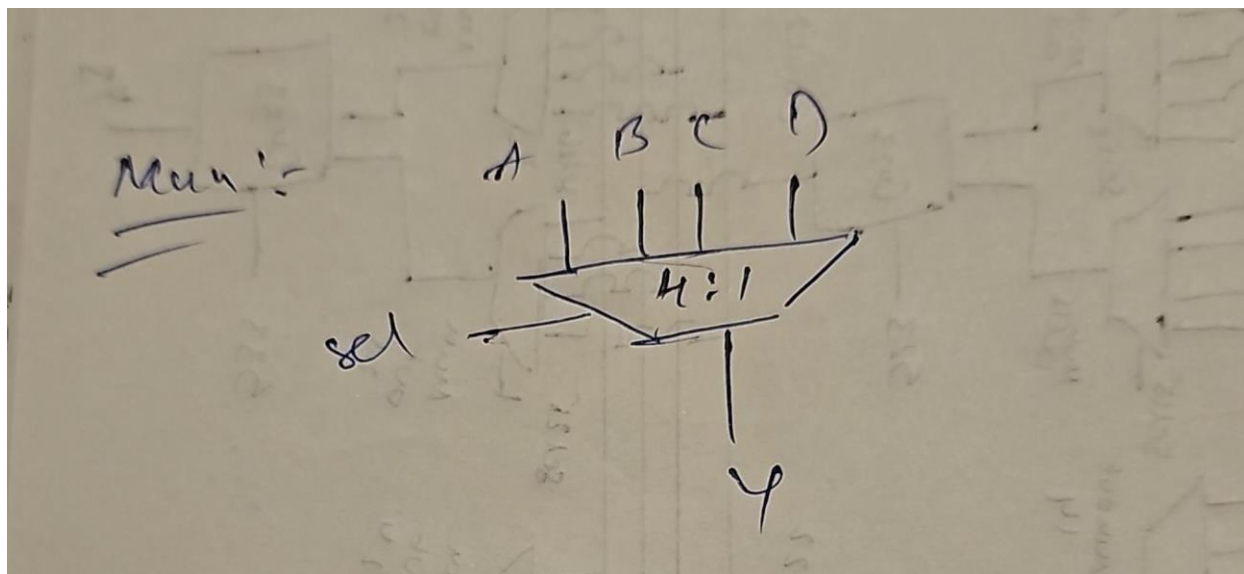
Necessary intermediate signals:

\*If there are no intermediate signals, you can remove this section name and table\*

Port name	Bit width	Purpose
<b>Y00,Y01,Y02,Y03,Y10,Y11,Y12,Y13</b>	d_w = 4	Intermediate signals

## Subcomponents

Mux :



Input ports:

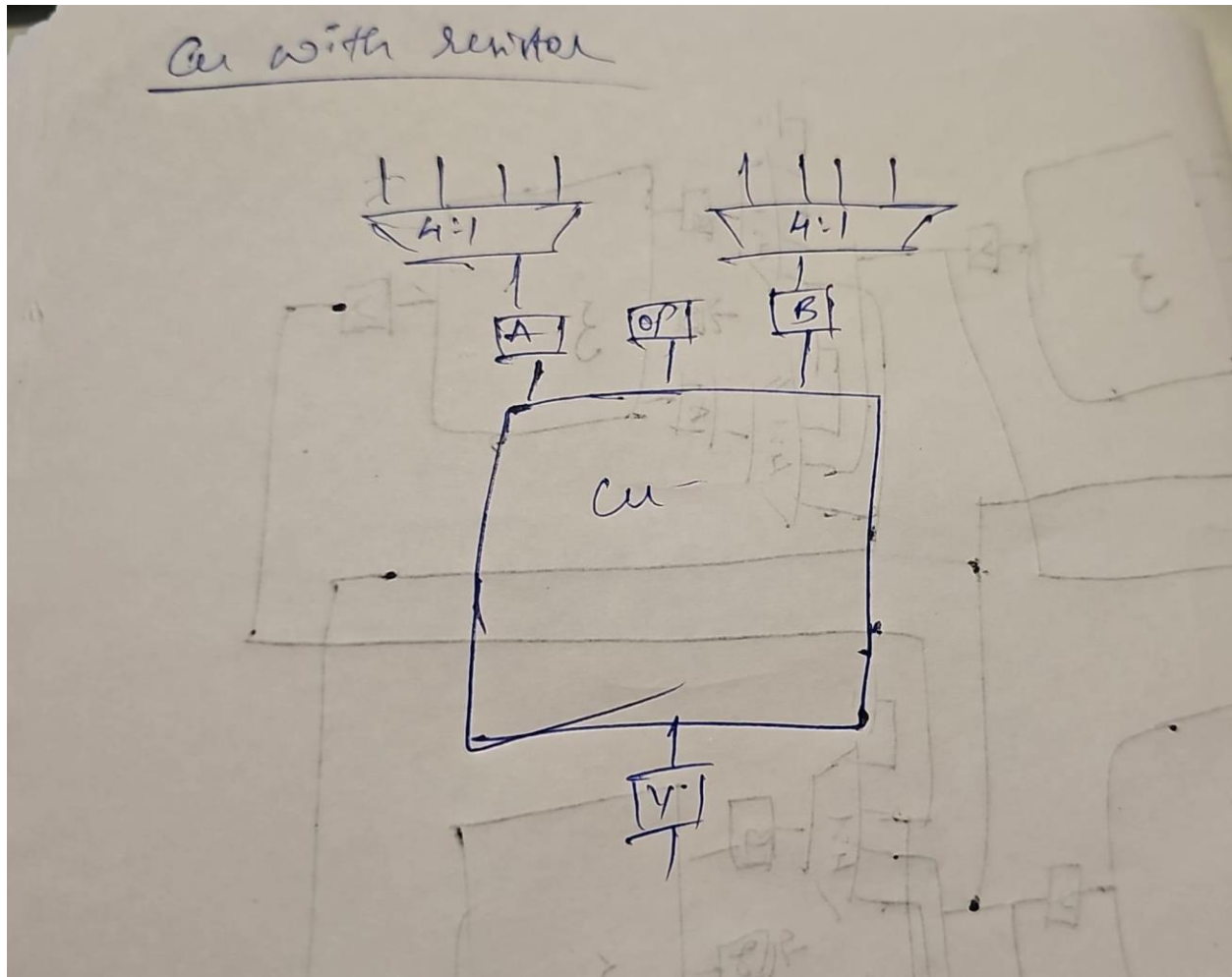
Port name	Bit width	Purpose
<b>A,b,c,d</b>	d_w = 4	Data inputs
<b>Sel</b>	1	Select line, selects which of the 2 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
<b>Y</b>	d_w = 4	Data output

\*Necessary intermediate signals: \*

Cu with resistor:



Input ports:

Port name	Bit width	Purpose
<b>I0, I1, I2, I3</b>	d_w = 4	Data inputs
<b>Sel</b>	2	Select line, selects which of the 4 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
<b>y</b>	d_w = 4	Data output

## Design explanation

It is a 2 by 4 architecture pre configurable

Both inputs and outputs are stored units.

The data flow according to design .

A0, A1, A2,A3, B0, B1, B2, B3 are data inputs.

op0, op1, op2,op3,op4, op5, op6, op7 selections lines for cu.

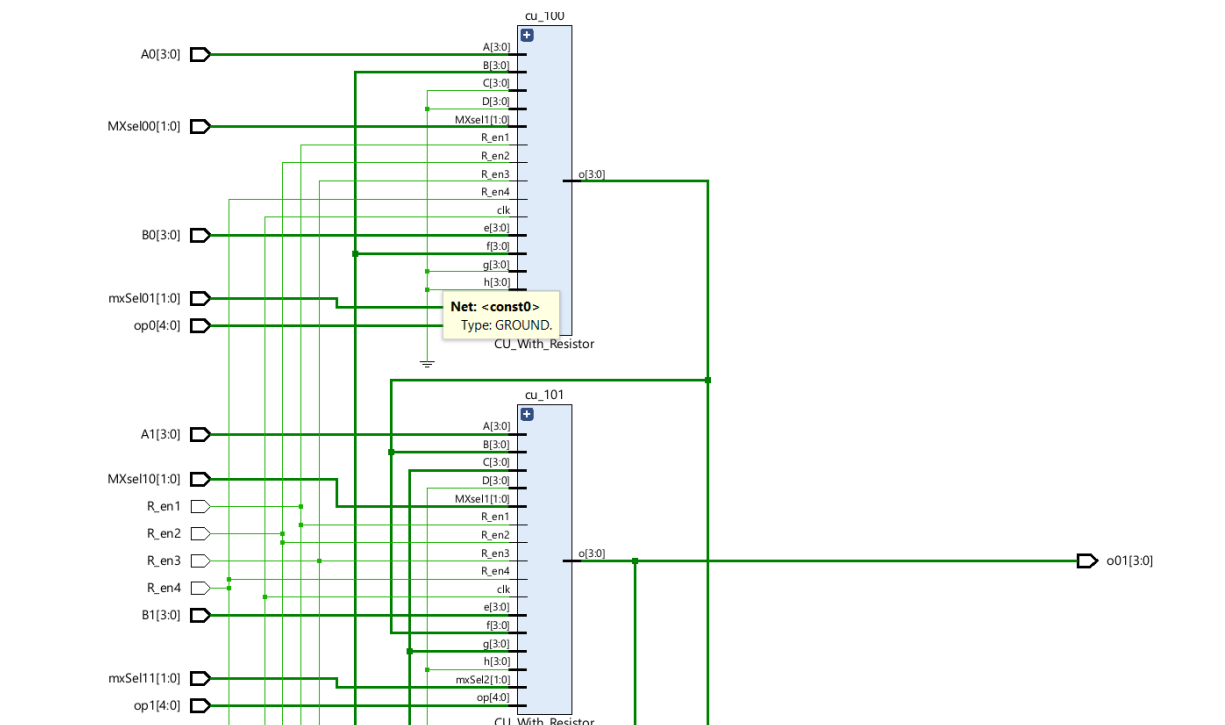
MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30, mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61, MXsel70,mxSel71 are mux selection lines.

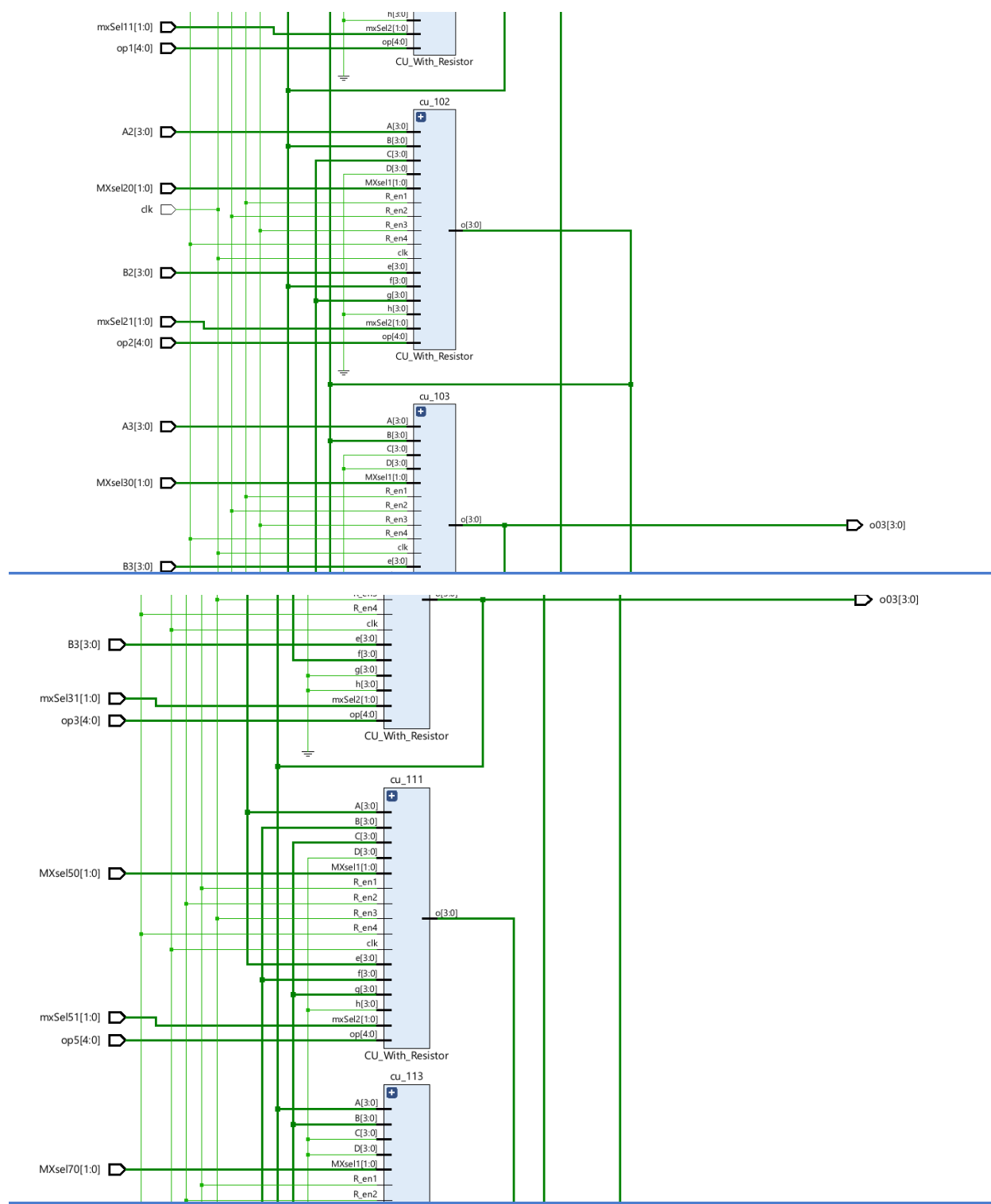
o00,o01,o02,o03, o10, o11, o12, o13 are out puts

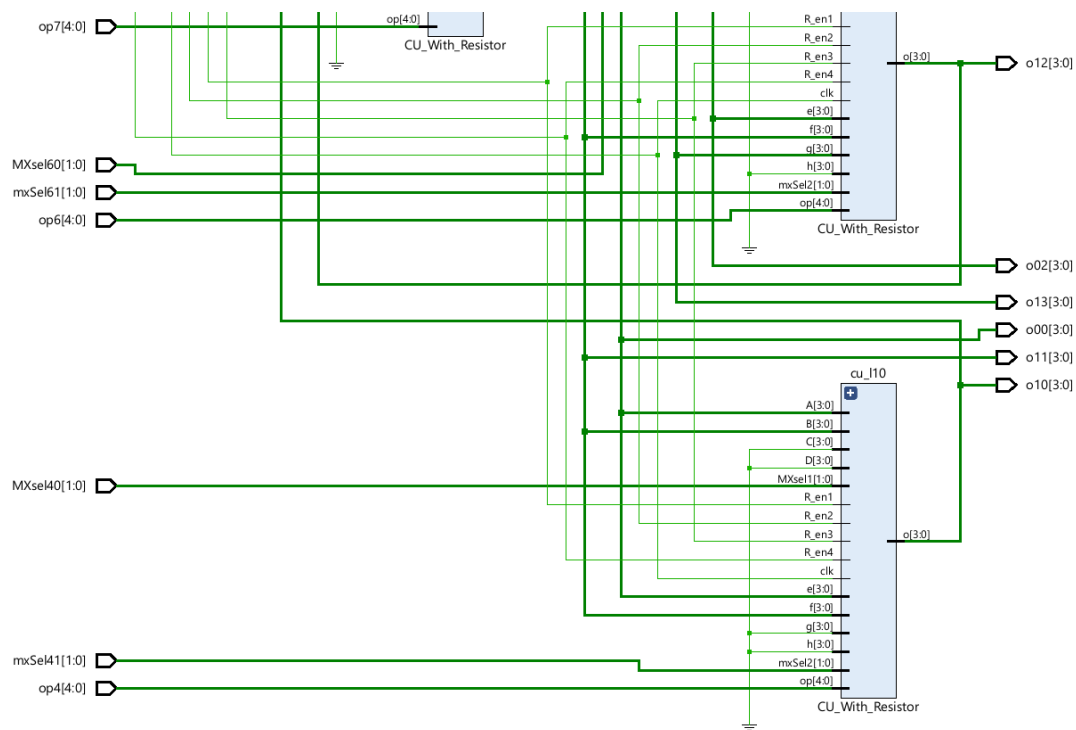


# Results

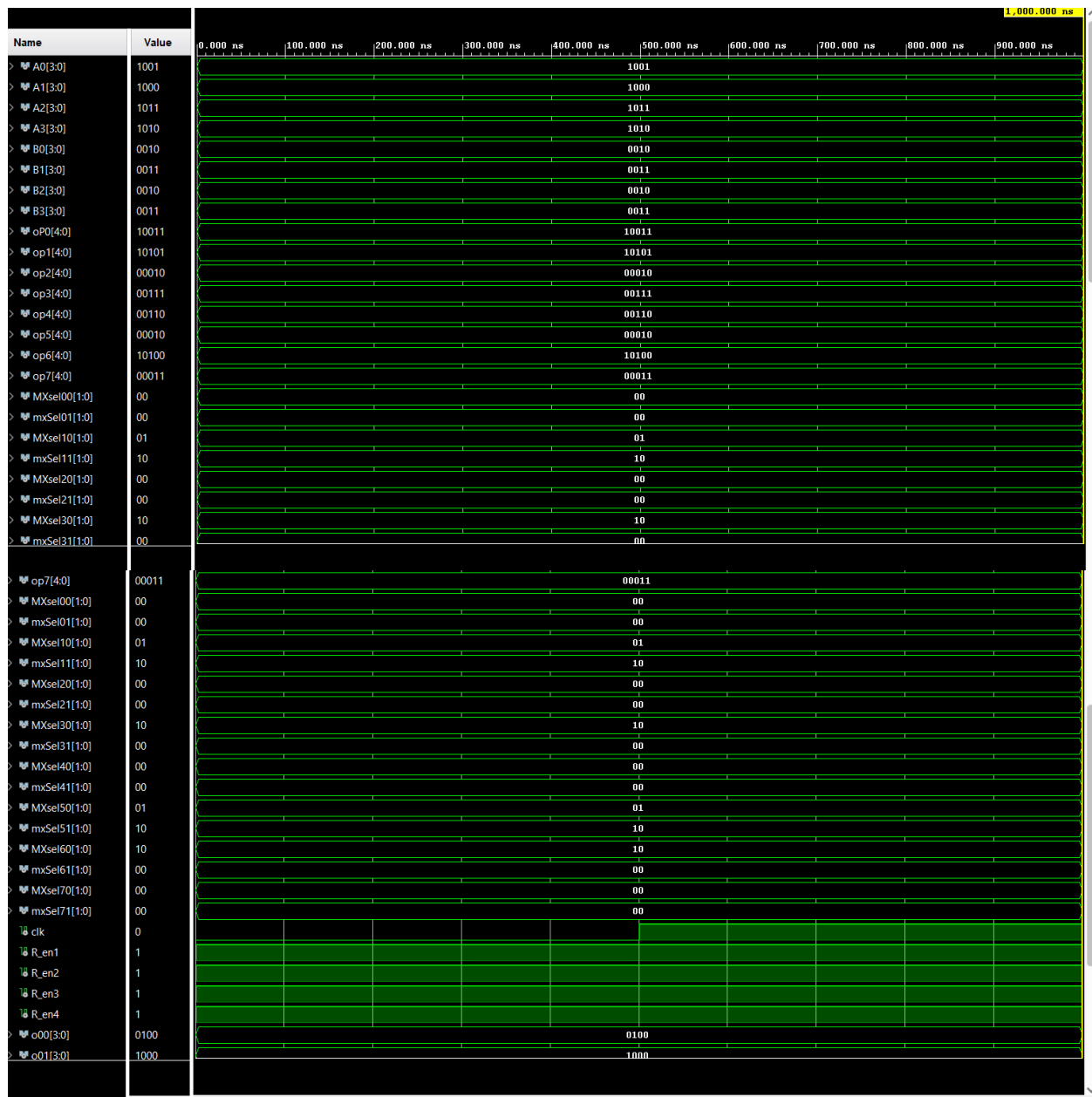
## Generated Schematics

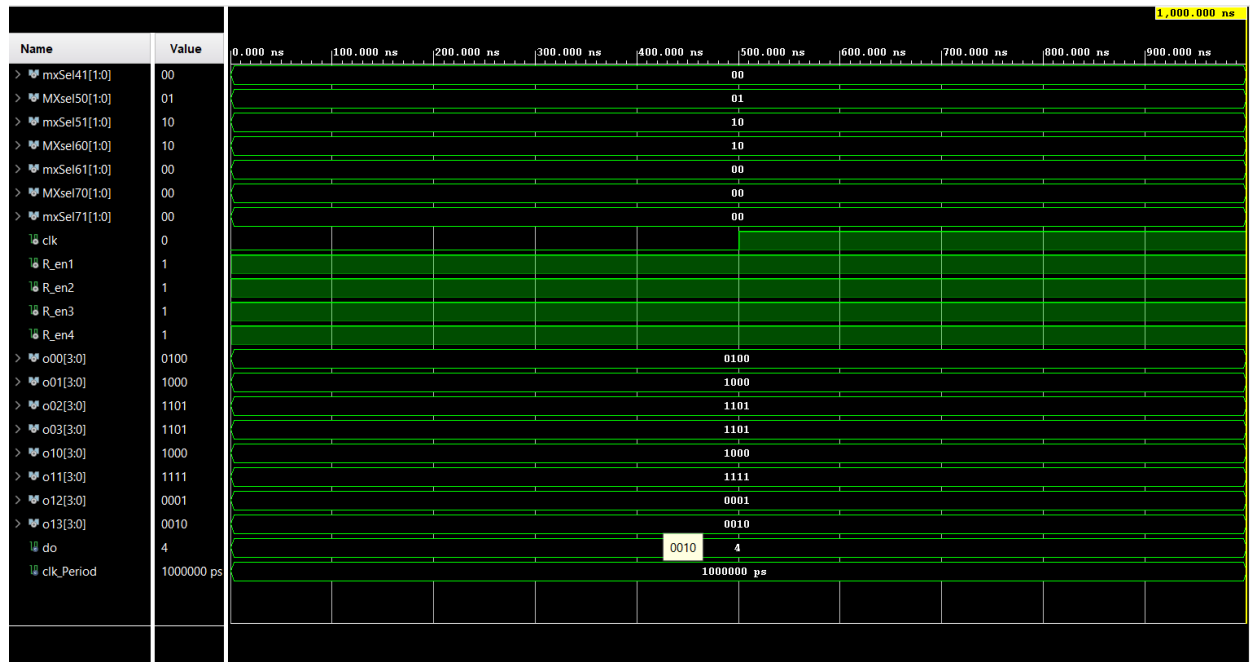




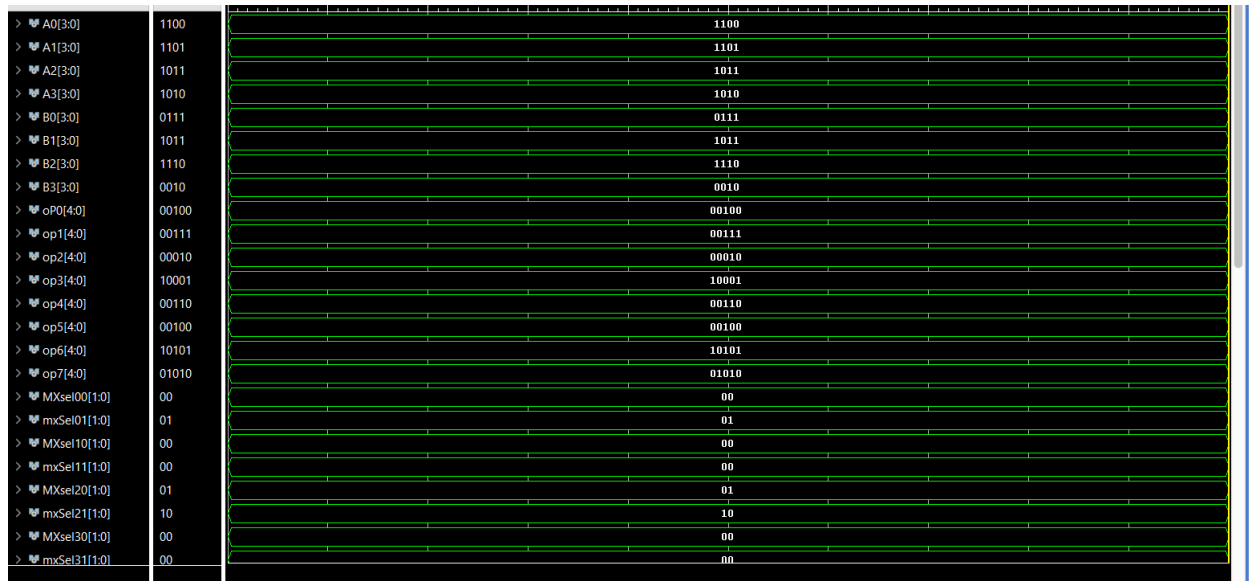


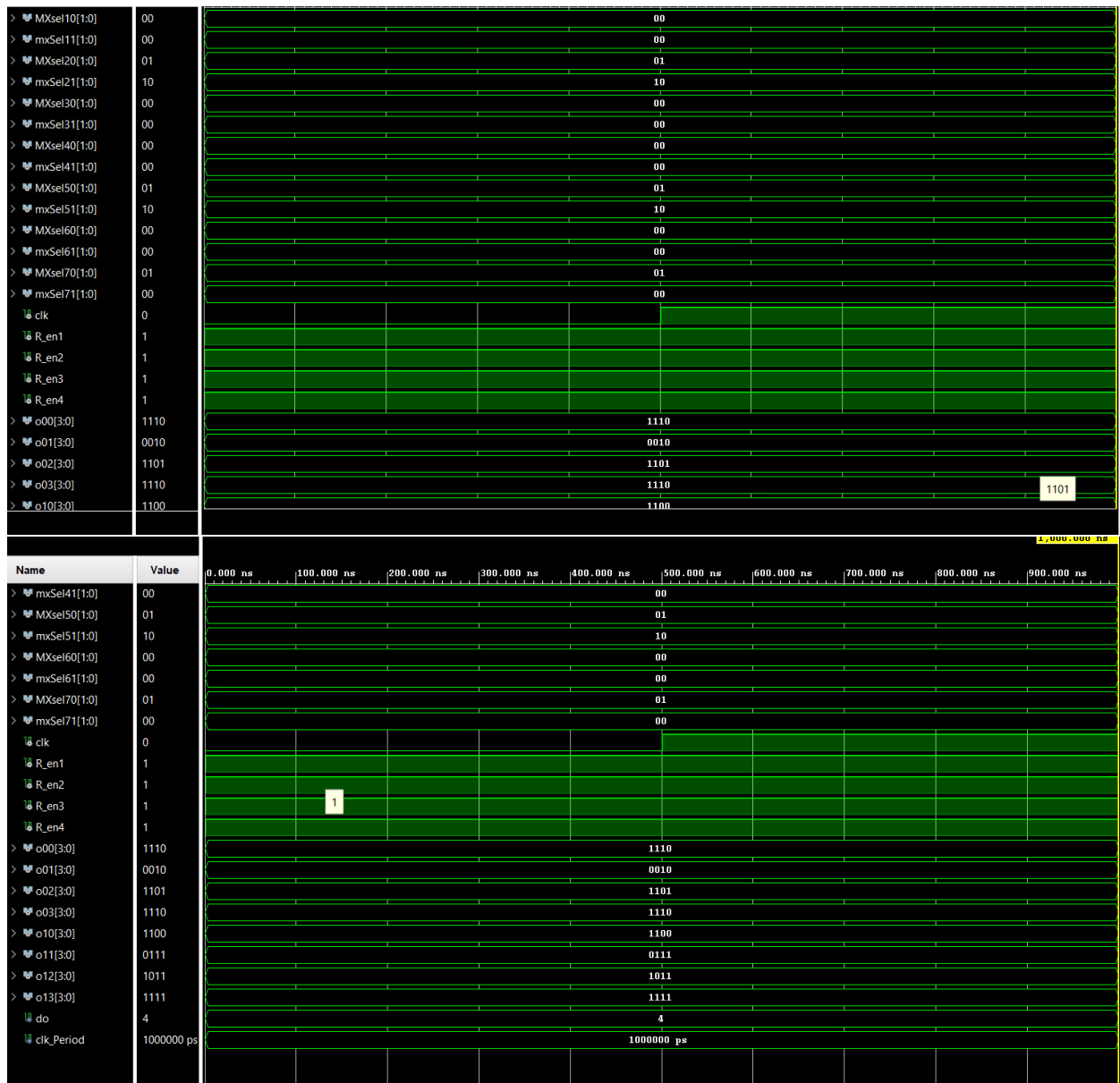
## Waveforms





- Test case 2





## Table/Calculations

### Overall Design;

Due to insufficient time I am unable to do table calculation so I am putting hand calculations. please consider atleast for partial mark for this.

Test case ①

$$cu(0,0) = 0100$$

$$cu(0,1) = 1000$$

$$cu(0,2) = 1101$$

$$cu(0,3) = 1010$$

$$cu(1,0) = 1110$$

$$cu(1,1) = 0111$$

$$cu(1,2) = 1010$$

$$cu(1,3) = 0101$$

$$y_1 = 1110$$

$$y_2 = 0111$$

$$y_3 = 1010$$

$$y_4 = 0101$$

Test Case ②

$$cu(0,0) = 0001$$

$$cu(0,1) = 0010$$

$$cu(0,2) = 1101$$

$$cu(0,3) = 1110$$

$$cu(1,0) = ~~1000~~ 1000$$

$$cu(1,1) = ~~1100~~ 1100$$

$$cu(1,2) = 1011$$

$$cu(1,3) = 0001$$

$$y_1 = 1000$$

$$y_2 = ~~1100~~ 1100$$

$$y_3 = 1010$$

$$y_4 = 0101$$

Test Case # (\*0ns to 5ns\*):

CU#	SourceA	SourceB	A	B	Oper	Calculated Op	Simulated Op	Match
CU1	A	B	0011	0010	MULT	0110	0110	Yes
CU2	C	D	0101	0100	ADD	1001	1001	Yes
CU3	CU1	CU2	0110	1001	LT	1111	1111	Yes
...								

Test Case # (\*5ns to 10ns\*):

CU#	SourceA	SourceB	A	B	Oper	Calculated Op	Simulated Op	Match
CU1	A	B	0011	0010	MULT	0110	0110	Yes
CU2	C	D	0101	0100	ADD	1001	1001	Yes
CU3	CU1	CU2	0110	1001	LT	1111	1111	Yes
...								

### Subcomponent test cases

Test Case # (\*0ns to 5ns\*):

A	B	Oper	Calculated Op	Simulated Op	Match
0011	0010	MULT (000)	0110	0110	Yes
0101	0100	ADD (001)	1001	1001	Yes
0110	1001	LT (010)	1111	1111	Yes
...					

Test Case # (\*5ns to 10ns\*):

A	B	Oper	Calculated Op	Simulated Op	Match
0011	0010	MULT (000)	0110	0110	Yes
0101	0100	ADD (001)	1001	1001	Yes
0110	1001	LT (010)	1111	1111	Yes
...					