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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/28/2024 06:10:49 PM
-- Design Name:
-- Module Name: Top_box_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top_box_tb is
```

```
--  Port ( );
 generic(do:integer:=4);
end Top_box_tb;

architecture Behavioral of Top_box_tb is


signal A0,A1, A2, A3,B0, B1, B2, B3:  std_logic_vector(do-1 downto
0);
signal oP0, op1, op2, op3, op4, op5, op6, op7:  std_logic_vector(do
downto 0);
signal MXsel00, mxSel01,MXsel10, mxSel11,MXsel20, mxSel21,MXsel30,
mxSel31,
MXsel40, mxSel41,MXsel50, mxSel51,MXsel60, mxSel61,MXsel70,
mxSel71: std_logic_vector(1 downto 0);
signal clk: std_logic;
signal R_en1,R_en2,R_en3,R_en4:  std_logic;
signal o00,o01, o02, o03, o10, o11, o12, o13: std_logic_vector(do-1
downto 0);
constant clk_Period: time:=1000ns;
begin
test: entity work.Top_box(Behavioral)
port map(A0 =>a0,A1 =>a1, A2 =>a2, A3 =>a3,b0=>b0, B1 =>b1, B2
=>b2, B3 =>b3, op0 =>op0, op1 =>op1, op2 =>op2, op3 =>op3, op4
=>op4, op5 =>op5, op6 =>op6, op7 =>op7,
MXsel00 => MXsel00, mxSel01 => MXsel01,MXsel10=> MXsel10, mxSel11=>
MXsel11,MXsel20=> MXsel20, mxSel21 => MXsel21,MXsel30 => MXsel30,
mxSel31 => MXsel31,
MXsel40 => MXsel40, mxSel41 => MXsel41,MXsel50 => MXsel50, mxSel51
=> MXsel51,MXsel60 => MXsel60, mxSel61 => MXsel61,MXsel70 =>
MXsel70, mxSel71 => MXsel71,clk => clk,
 R_en1 => R_en1,R_en2 => R_en2,R_en3 => R_en3,R_en4  => R_en4, o00
=> o00,o01=> o01, o02 => o02, o03 => o03, o10 => o10, o11=> o11,
o12 => o12, o13 => o13);

 Clock: process
begin
```

```
CLK<='0';
wait for clk_Period/2;
CLK<='1';
wait for clk_Period/2;
end process;


ts : process
begin
R_en1 <='1';
 R_en2 <='1';
 R_en3 <='1';
 R_en4  <='1';

A0 <="1001" ;A1 <="1000"; A2 <="1011"; A3 <="1010" ;
B0<="0010" ; B1 <="0011"; B2 <="0010"; B3 <="0011";
op0 <="10011";
op1 <="10101";
op2 <="00010";
op3 <="00111";
op4 <="00110";
op5 <="00010";
op6 <="10100";
op7 <="00011";
MXsel00 <="00";
mxSel01 <="00";
MXsel10<="01";
mxSel11<="10";
MXsel20<="00";
mxSel21 <="00";
MXsel30 <="10";
mxSel31 <="00";
MXsel40 <="00";
mxSel41 <="00";
MXsel50 <="01";
mxSel51 <="10";
MXsel60 <="10";
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```
mxSel61 <="00";
MXsel70 <="00";
mxSel71 <="00";


wait for 2*clk_Period;


--A0 <="1100" ;A1 <="1101"; A2 <="1011"; A3 <="1010" ;
--B0<="0111" ; B1 <="1011"; B2 <="1110"; B3 <="0010";
--op0 <="00100";
--op1 <="00111";
--op2 <="00010";
--op3 <="10001";
--op4 <="00110";
--op5 <="00100";
--op6 <="10101";
--op7 <="01010";
--MXsel00 <="00";
--mxSel01 <="01";
--MXsel10<="00";
--mxSel11<="00";
--MXsel20<="01";
--mxSel21 <="10";
--MXsel30 <="00";
--mxSel31 <="00";
--MXsel40 <="00";
--mxSel41 <="00";
--MXsel50 <="01";
--mxSel51 <="10";
--MXsel60 <="00";
--mxSel61 <="00";
--MXsel70 <="01";

--mxSel71 <="00";
```

```
--wait for 2*clk_Period;
finish;
end process;

end Behavioral;
```