EENG 5560 HW5

Assigned: March 19, 2024
Due: March 28, 2024
Total points: 50

Contents

1 Question

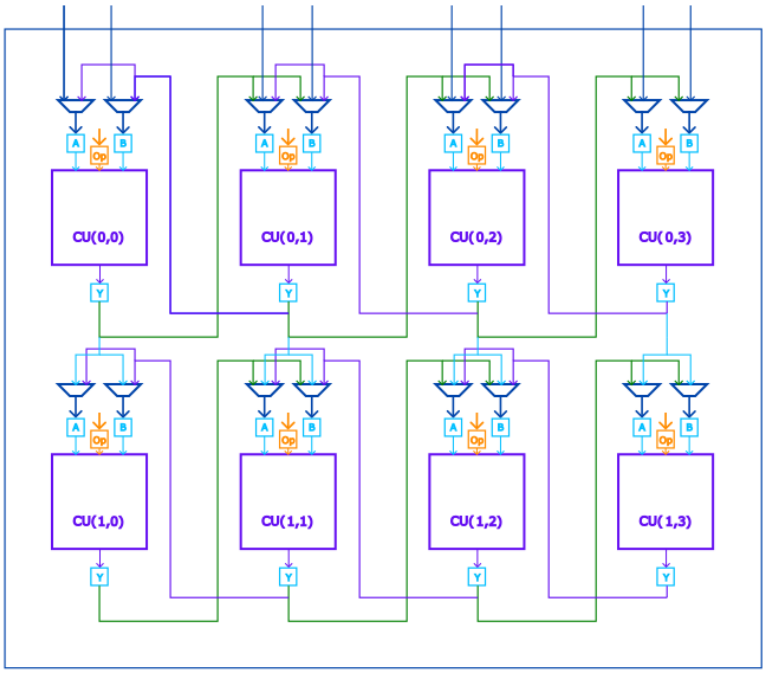

Figure 1: Overall design.

Using the same CU from HW 2 but with a data width parameter set to 4, implement the design shown in Fig. 1. Arrays are also required to be used for all of the ports and signals (but generates are not required). Storage units will be used to store both the data inputs (A, B) and data outputs (Y). The first row of CUs all have the ability to use external data, but also have horizontal connectivity input options, with the left connectivities being in purple and the right connectivities being in green. Appropriately sized muxes must be used to allow for the shown connectivities. Unused data inputs to the muxes must be grounded. The second row of CUs can also obtain data from the output of the CU in the same corresponding column but in the previous row. The overall outputs will be all of the CU outputs from the second row.

2 Test cases

You need to make testbenches for all components used, but you only have to show the calculations and waveforms for the overall design in this assignment. This time, you are required to show the waveforms for the intermediate CU outputs in addition to the overall outputs. The test cases for the overall design are as follows.

2.1 Case 1

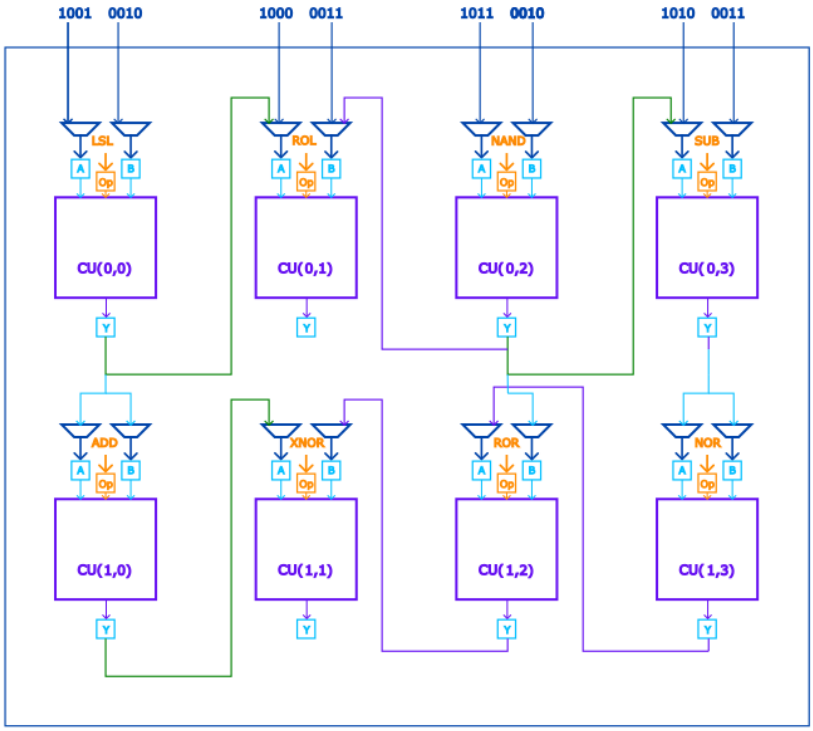

Figure 2: Test Case 1.

Row 0 External Data Inputs

CU#	A	B
CU(0,0)	1001	0010
CU(0,1)	1000	0011
CU(0,2)	1011	0010
CU(0,3)	1010	0011

Connectivity and Operations

CU#	SourceA	SourceB	Oper
CU(0,0)	External	External	LSL
CU(0,1)	CU(0,0)	CU(0,2)	ROL
CU(0,2)	External	External	NAND
CU(0,3)	CU(0,2)	External	SUB
CU(1,0)	CU(0,0)	CU(0,3)	ADD
CU(1,1)	CU(0,1)	CU(0,2)	NAND
CU(1,2)	CU(1,3)	CU(0,2)	ROR
CU(1,3)	CU(0,3)	CU(0,3)	NOR

2.2 Case 2

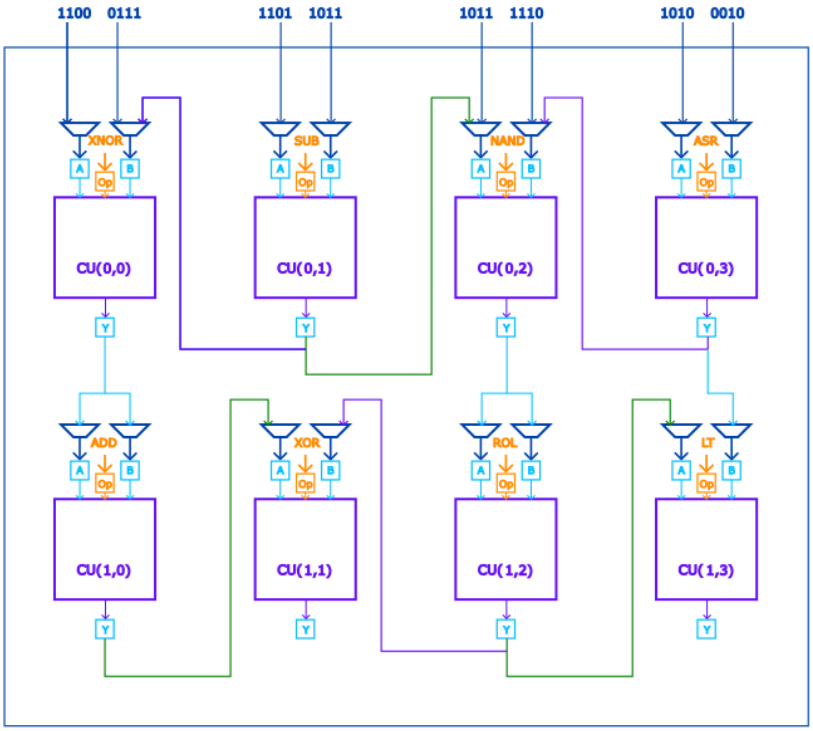

Figure 3: Test Case 2.

Inputs

CU#	A	B
CU(0,0)	1100	0111
CU(0,1)	1101	1011
CU(0,2)	1011	1110
CU(0,3)	1010	0010

Connectivity

CU#	SourceA	SourceB	Oper
CU(0,0)	External	CU(0,1)	XNOR
CU(0,1)	External	External	SUB
CU(0,2)	CU(0,1)	CU(0,3)	NAND
CU(0,3)	External	External	ASR
CU(1,0)	CU(0,0)	CU(0,0)	ADD
CU(1,1)	CU(1,0)	CU(1,2)	XOR
CU(1,2)	CU(0,2)	CU(0,2)	ROL
CU(1,3)	CU(1,2)	CU(0,3)	LT

3 Formatting

3.1 Steps: Printing code to pdf

For each source file (both the design and the simulation VHDL or other HDL language files), print the code to pdf either in Vivado or by opening the code in any other text editor and printing it from there. It is preferable to combine all of the pdfs of the code into a single pdf, you can do so using this website or any other websites/software with that capability. The steps to print the code to a pdf from Vivado are as follows:

1. With the VHDL\source file currently open and being viewed in the text editor, click the file tab at the top and near the bottom select the print option (or press Ctrl + P).

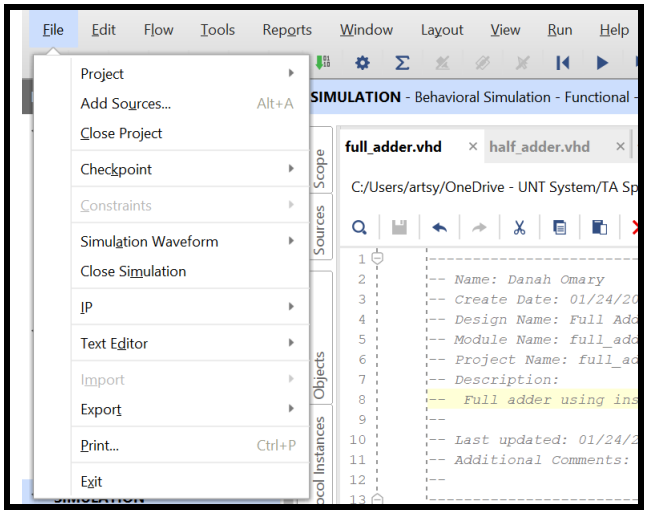

Figure 4: Print button.

2. In the popup, in the dropdown next to the "Name: " text, make sure to select Microsoft Print to PDF. Then click ok.

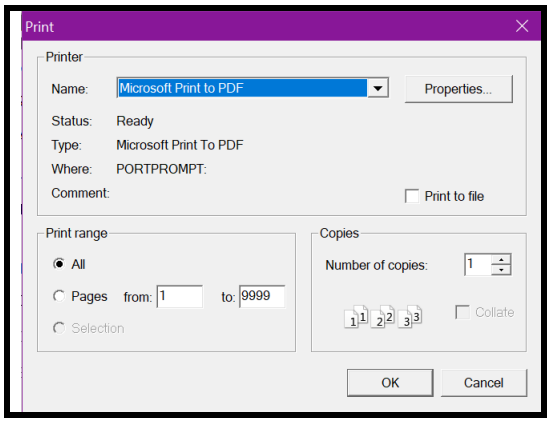

Figure 5: Printing popup with print to pdf chosen.

3. Name the pdf file something clearly indicating what it is and then browse to where you'd like to save the pdf to.

3.2 Source files zipping

In a **separate** **zip file, include the following files (and only these files):**

- **A README text file that includes a list of all the files that should be included and any special instructions needed to run the top level module (in Windows, to create a text file, in the file explorer right click empty space and choose "New - Text Document"). This will help in the case that any files that were supposed to be included ended up missing.**
- **VHDL file for top level component**
- **VHDL files for all subcomponents and any of their testbenches**
- **VHDL file for top level testbench**

Do not include other files from the project or the submission (i.e. the report and pdf of the vhdl code), only the VHDL files are needed.

3.3 Example submission files

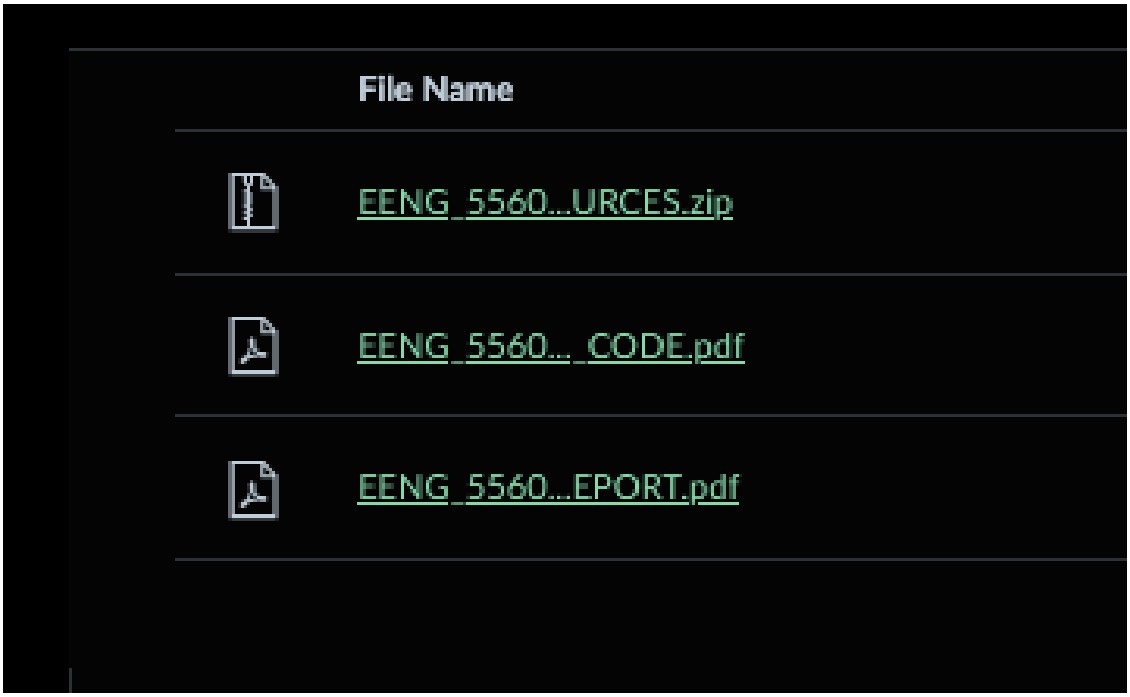

Figure 6: Example showing the file types and good naming conventions of a submission.

In total you will have 3 major parts to your submission:

1. **Report(s): pdf(s)**
2. **Code: pdf(s)**
3. **Source files: zip folder**

As can be seen in the figure, the pdfs for the code and report *NEED TO BE OUTSIDE OF A ZIP FILE*.

3.4 Other formatting notes

If you would like to make a report yourself rather than follow the provided template, please make sure to include all of the things listed out in the checklist below as well as a Table of Contents and page numbers on each page. Do not include all of the VHDL code in the report, please keep it separate from the report.

4 Checklist

Your submission should include (using helpful/distinguishable file names):

- ☐ **Report (either in pdf or .docx file type) including:**
  - ☐ **Design: Block diagrams, design explanation**
  - ☐ **Generated RTL Schematic and verbal comparison (top module only)**
  - ☐ **Simulation waveforms for the test cases, including the overall outputs and relevant intermediate signals (top module only)**
  - ☐ **Table with Calculated outputs vs Simulation outputs for all test cases (top module only)**
- ☐ **PDF(s): VHDL (or verilog or systemverilog) code for the top level component, all subcomponents, and the testbenches (can combine all code pdfs into one pdf overall or include individual pdfs)**
- ☐ **Zip file with all the VHDL source code files needed to run the top level component**