EENG HW 5Report Template

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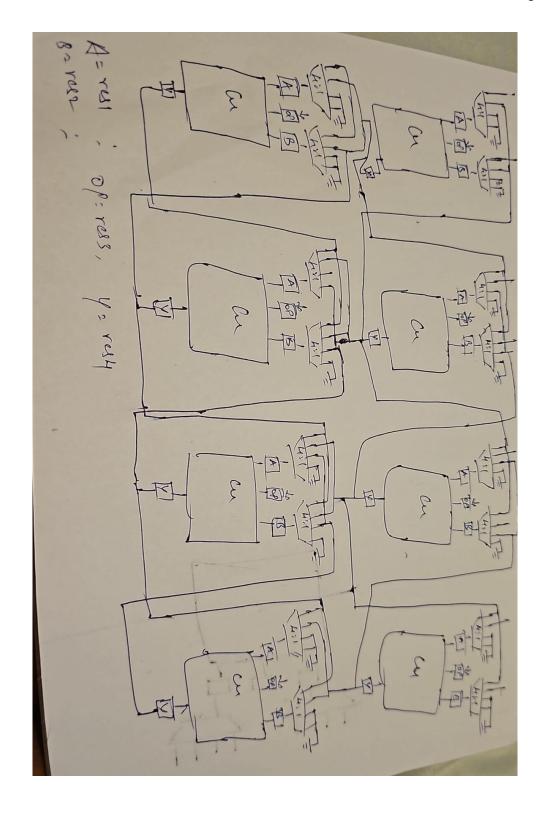
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Design

Block diagrams

Overall design



Overall component: top box

Parameters: d_w - data width (for inputs and outputs)

Input ports:

Port name	Bit width	Purpose
A0, A1, A2,A3, B0, B1, B2, B3	d_w = 4	Data inputs
op0, op1, op2,op3,op4, op5, op6, op7		Selection line for cu
MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30, mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61, MXsel70,mxSel71	2	Mux selection lines
R_en1, R_en2, R_en3, R_en4	1	enable

Output ports:

Port name	Bit width	Purpose
000,001,002,003,	$d_w = 4$	Data output
o10, o11, o12,		
o13		

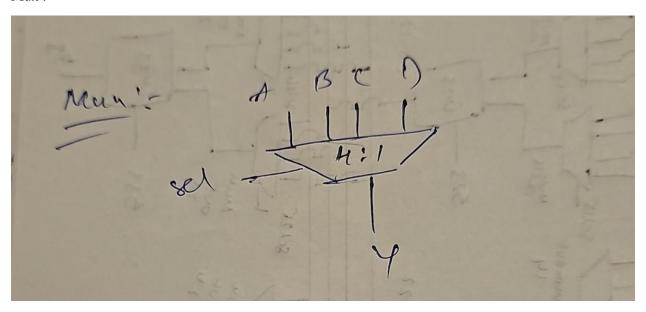
Necessary intermediate signals:

If there are no intermediate signals, you can remove this section name and table

Port name	Bit	Purpose
	width	
Y00,Y01,Y02,Y03,Y10,Y11,Y12,Y13	$d_w = 4$	Intermediate signals

Subcomponents

Mux:



Input ports:

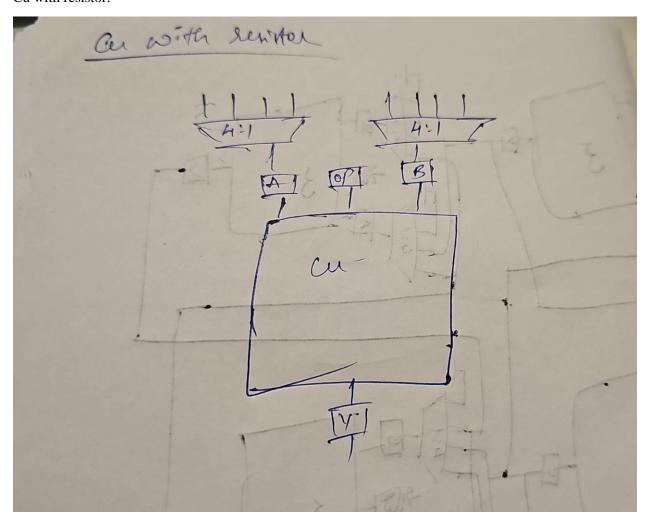
Port name	Bit width	Purpose
A,b,c,d	$d_w = 4$	Data inputs
Sel	1	Select line, selects which of the 2 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
Y	d w = 4	Data output

^{*}Necessary intermediate signals: *

Cu with resistor:



Input ports:

Port name	Bit width	Purpose
I0, I1, I2, I3	$d_w = 4$	Data inputs
Sel	2	Select line, selects which of the 4 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
y	$d_w = 4$	Data output

Design explanation

It is a 2 by 4 architecture pre configurable

Both inputs and outputs are stored units.

The data flow according to design.

A0, A1, A2, A3, B0, B1, B2, B3 are data inputs.

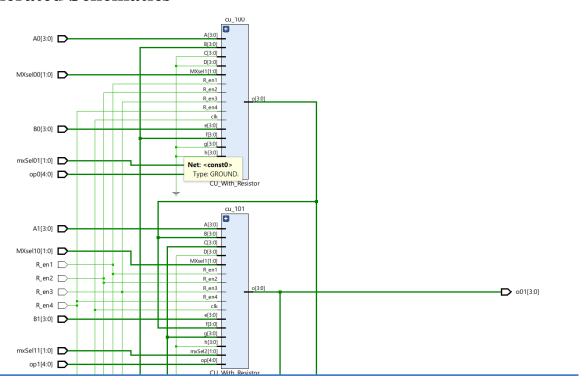
op0, op1, op2,op3,op4, op5, op6, op7 selections lines for cu.

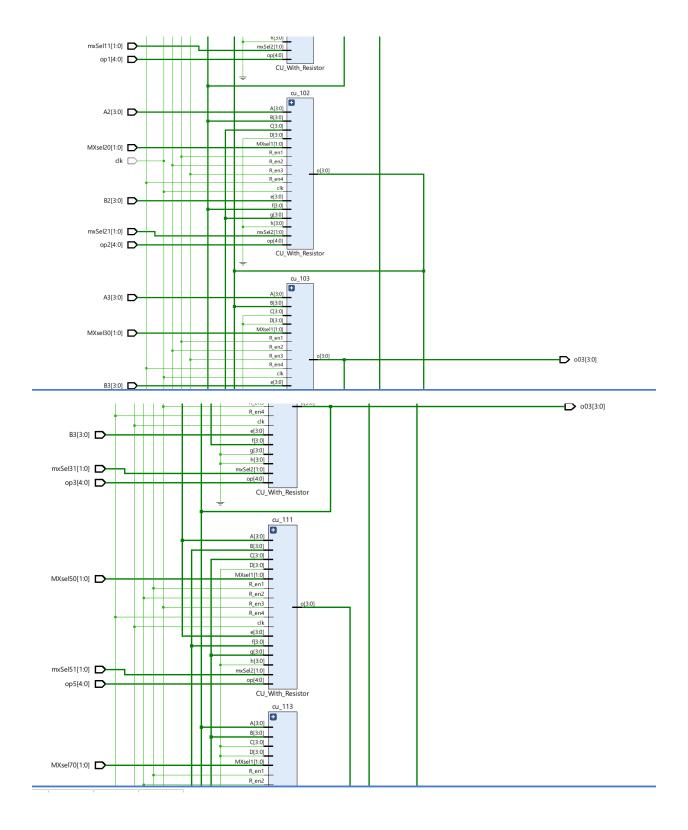
MXsel00,mxSel01, MXsel10, mxSel11, MXsel20, mxSel21, MXsel30, mxSel31, MXsel40, mxSel41, MXsel50, mxSel51, MXsel60, mxSel61, MXsel70,mxSel71 are mux selection lines.

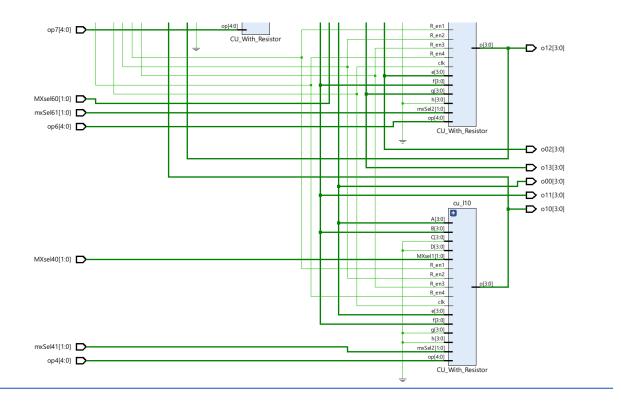
o00,o01,o02,o03, o10, o11, o12, o13 are out puts

Results

Generated Schematics

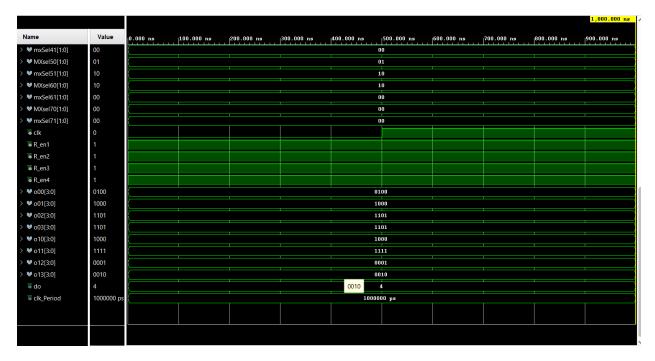






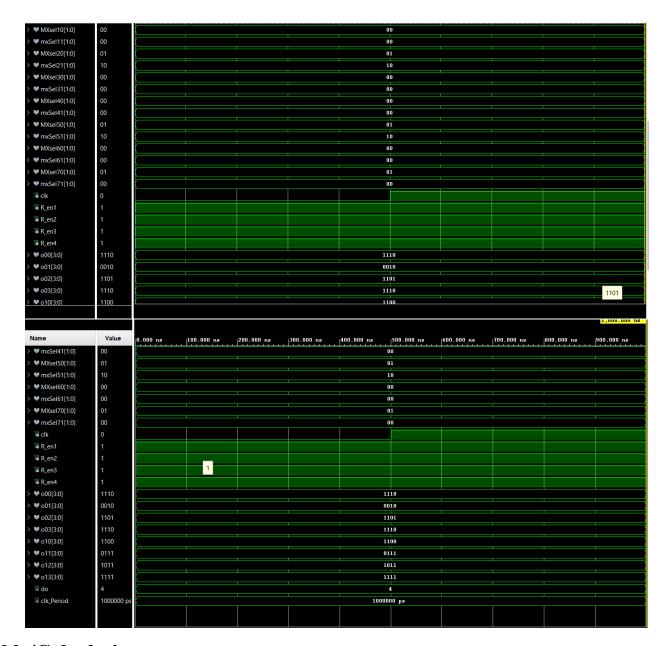
Waveforms

											1,000.000
lame	Value	0.000 ns	100.000 ns	200.000 ns	300.000 ns	400.000 ns	500.000 ns	600.000 ns	700.000 ns	800.000 ns	900.000 ns
M A0[3:0]	1001	<u> </u>					1001				
M A1[3:0]	1000						1000				
A2[3:0]	1011						1011				
A3[3:0]	1010	(1010				
B0[3:0]	0010	(0010				
B1[3:0]	0011	(0011				
B2[3:0]	0010	(0010				
B3[3:0]	0011						0011				
oP0[4:0]	10011						10011				
op1[4:0]	10101						10101				
op2[4:0]	00010						00010				
op3[4:0]	00111						00111				
op4[4:0]	00110						00110				
op5[4:0]	00010						00010				
op6[4:0]	10100						10100				
op7[4:0]	00011						00011				
MXsel00[1:0]	00						00				
mxSel01[1:0]	00	(00				
MXsel10[1:0]	01						01				
mxSel11[1:0]	10						10				
MXsel20[1:0]	00						00				
mxSel21[1:0]	00						00				
MXsel30[1:0]	10						10				
mxSel31[1:0]	00						nn				
op7[4:0]	00011						00011				
MXsel00[1:0]	00	(00				
mxSel01[1:0]	00						00				
MXsel10[1:0]	01						01				
mxSel11[1:0]	10						10				
MXsel20[1:0]	00		1				00				
mxSel21[1:0]	00						00				
MXsel30[1:0]	10						10				
mxSel31[1:0]	00						00				
MXsel40[1:0]	00						00				
mxSel41[1:0]	00						00				
MXsel50[1:0]	01						01				
mxSel51[1:0]	10						10				
MXsel60[1:0]	10						10				
mxSel61[1:0]	00						00				
MXsel70[1:0]	00						00				
mxSel71[1:0]	00						00				
clk	0										
R_en1	1										
R_en2	1										
R_en3	1										
R_en4	1										
							0100				
							ULLUU				
000[3:0]	0100 1000	<u> </u>					1000				



• Test case 2

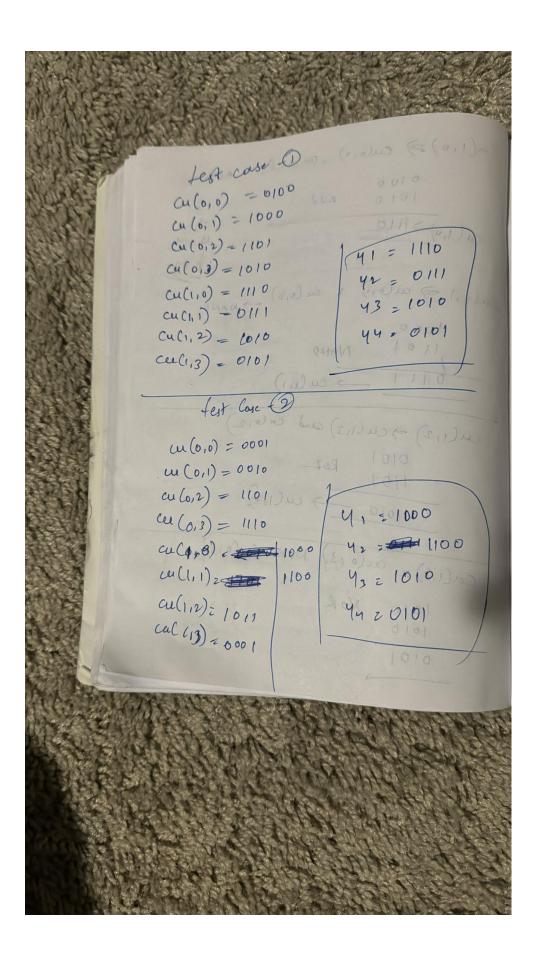
> W A0[3:0]	1100	1100
> W A1[3:0]	1101	1101
> W A2[3:0]	1011	1011
> W A3[3:0]	1010	1010
> W B0[3:0]	0111	0111
> W B1[3:0]	1011	1011
> W B2[3:0]	1110	1110
> W B3[3:0]	0010	0010
> W oP0[4:0]	00100	00100
> W op1[4:0]	00111	00111
> W op2[4:0]	00010	00010
> W op3[4:0]	10001	10001
> W op4[4:0]	00110	00110
> ♥ op5[4:0]	00100	00100
> № op6[4:0]	10101	10101
> ₩ op7[4:0]	01010	01010
> W MXsel00[1:0]	00	00
> W mxSel01[1:0]	01	01
> W MXsel10[1:0]	00	00
> ₩ mxSel11[1:0]	00	00
> W MXsel20[1:0]	01	01
> W mxSel21[1:0]	10	10
> W MXsel30[1:0]	00	00
> W mxSel31[1:0]	00	<u> </u>



Table/Calculations

Overall Design;

Due to insufficient time I am unable to do table calculation so I am putting hand calculations.please consider atleast for partial mark for this.



Test Case # (*0ns to 5ns*):

CU#	SourceA	SourceB	А	В	Oper	Calculated Op	Simulated Op	Match
CU1	Α	В	0011	0010	MULT	0110	0110	Yes
CU2	С	D	0101	0100	ADD	1001	1001	Yes
CU3	CU1	CU2	0110	1001	LT	1111	1111	Yes
•••								

Test Case # (*5ns to 10ns*):

CU#	SourceA	SourceB	А	В	Oper	Calculated Op	Simulated Op	Match
CU1	Α	В	0011	0010	MULT	0110	0110	Yes
CU2	С	D	0101	0100	ADD	1001	1001	Yes
CU3	CU1	CU2	0110	1001	LT	1111	1111	Yes

Subcomponent test cases

Test Case # (*0ns to 5ns*):

Α	В	Oper	Calculated Op	Simulated Op	Match
0011	0010	MULT (000)	0110	0110	Yes
0101	0100	ADD (001)	1001	1001	Yes
0110	1001	LT (010)	1111	1111	Yes

Test Case # (*5ns to 10ns*):

Α	В	Oper	Calculated Op	Simulated Op	Match
0011	0010	MULT (000)	0110	0110	Yes
0101	0100	ADD (001)	1001	1001	Yes
0110	1001	LT (010)	1111	1111	Yes
