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-- Company:
-- Engineer:
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-- Create Date: 02/08/2024 01:14:49 AM
-- Design Name:
-- Module Name: Top_Box - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top_Box is
generic(dw: integer:=4);
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  Port (a1, a2, a3, a4, a5, a6, a7, a8, b1, b2, b3, b4, b5, b6, b7,
b8: in std_logic_vector(dw-1 downto 0);
  s11, s12, s13, s14, s15, s16, s17, s18, s21, s22, s23, s24, s25,
s26, s27, s28: in std_logic_vector(dw downto 0);
  sel1,sel2,sel3, sel4,sel13, sel14, sel15, sel16: in
std_logic_vector(dw-3 downto 0);
  sel5, sel6, sel7, sel8, sel9,sel10,sel11, sel12: in
std_logic_vector(dw-2 downto 0);
  y1, y2, y3, y4, y5, y6, y7, y8: out std_logic_vector(dw-1 downto
0) );
end Top_Box;

 architecture Behavioral of Top_Box is
 --Below signal lines for establishing connection between output of
CU and input of muxes
signal cuout1, cuout2, cuout3, cuout4, cuout5, cuout6, cuout7,
cuout8: std_logic_vector(dw-1 downto 0);
 -- signal lines for establishing connection between  outputs of
muxes and inputs of CU
signal
muxout1,muxout2,muxout3,muxout4,muxout5,muxout6,muxout7,muxout8,
muxout9,muxout10,muxout11,muxout12,muxout13,muxout14,muxout15,muxou
t16: std_logic_vector(dw-1 downto 0);
begin
-- construction of 8*2 reconfigurable architecture.
--row 1
cu11: entity work.compunit(Behavioral)
 port map(a => a1, b =>B1, S => S11 ,O =>CUOUT1);
cu12: entity work.compunit(Behavioral)
 port map(a => a2, b =>B2, S => S12 ,O =>CUOUT2);
 cu13: entity work.compunit(Behavioral)
 port map(a => a3, b =>B3, S => S13 ,O =>CUOUT3);
cu14: entity work.compunit(Behavioral)
 port map(a => a4, b =>B4, S => S14 ,O =>CUOUT4);
 cu15: entity work.compunit(Behavioral)
 port map(a => a5, b =>B5, S => S15 ,O =>CUOUT5);
cu16: entity work.compunit(Behavioral)
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 port map(a => a6, b =>B6, S => S16 ,O =>CUOUT6);
 cu17: entity work.compunit(Behavioral)
 port map(a => a7, b =>B7, S => S17 ,O =>CUOUT7);
cu18: entity work.compunit(Behavioral)
 port map(a => a8, b =>B8, S => S18 ,O =>CUOUT8);
-- row 2
mx1:entity work.MUX4_1(behavioral)
port map(a=>cuout1,b=> cuout2, c => cuout3,d => cuout4, sel =>
sel1, y => muxout1);
mx2:entity work.MUX4_1(behavioral)
port map(a=>cuout1,b=> cuout2, c => cuout3,d => cuout4, sel =>
sel2, y => muxout2);
cu21: entity work.compunit(Behavioral)
port map(a => muxout1, b =>muxout2, S => S21 ,O =>y1);

mx3:entity work.MUX4_1(behavioral)
port map(a=>cuout2,b=> cuout3, c => cuout4,d => cuout5, sel =>
sel3, y => muxout3);
mx4:entity work.MUX4_1(behavioral)
port map(a=>cuout2,b=> cuout3, c => cuout4,d => cuout5, sel =>
sel4, y => muxout4);
cu22: entity work.compunit(Behavioral)
port map(a => muxout3, b =>muxout4, S => S22 ,O =>y2);

mx5:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel5, y =>
muxout5);
mx6:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel6, y =>
muxout6);
cu23: entity work.compunit(Behavioral)
port map(a => muxout5, b =>muxout6, S => S23 ,O =>y3);



mx7:entity work.MUX8_1(behavioral)
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port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel7, y =>
muxout7);
mx8:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel8, y =>
muxout8);
cu24: entity work.compunit(Behavioral)
port map(a => muxout7, b =>muxout8, S => S24 ,O =>y4);

mx9:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel9, y =>
muxout9);
mx10:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel10, y =>
muxout10);
cu25: entity work.compunit(Behavioral)
port map(a => muxout9, b =>muxout10, S => S25 ,O =>y5);

mx11:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel11, y =>
muxout11);
mx12:entity work.MUX8_1(behavioral)
port map(a=>cuout1, b=> cuout2, c => cuout3, d => cuout4,
e=>cuout5, f=> cuout6, g => cuout7, h => cuout8, sel => sel12, y =>
muxout12);
cu26: entity work.compunit(Behavioral)
port map(a => muxout11, b =>muxout12, S => S26 ,O =>y6);

mx13:entity work.MUX4_1(behavioral)
port map(a=>cuout4,b=> cuout5, c => cuout6,d => cuout7, sel =>
sel13, y => muxout13);
mx14:entity work.MUX4_1(behavioral)
port map(a=>cuout4,b=> cuout5, c => cuout6,d => cuout7, sel =>
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sel14, y => muxout14);
cu27: entity work.compunit(Behavioral)
port map(a => muxout13, b =>muxout14, S => S27 ,O =>y7);

mx15:entity work.MUX4_1(behavioral)
port map(a=>cuout5,b=> cuout6, c => cuout7,d => cuout8, sel =>
sel15, y => muxout15);
mx16:entity work.MUX4_1(behavioral)
port map(a=>cuout5,b=> cuout6, c => cuout7,d => cuout8, sel =>
sel16, y => muxout16);
cu28: entity work.compunit(Behavioral)
port map(a => muxout15, b =>muxout16, S => S28 ,O =>y8);


end Behavioral;
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