```
----------------------------------------------------------------------
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-- Company:
-- Engineer:
--
-- Create Date: 02/14/2024 01:43:59 PM
-- Design Name:
-- Module Name: Mux8_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux8_1 is
generic( dw: integer:=4);
```

```
Port (a, b, c, d, e, f, g, h: in std_logic_vector(dw-1 downto 0);
sel: in std_logic_vector(dw-2 downto 0);
y: out std_logic_vector(dw-1 downto 0) );
end Mux8_1;

architecture Behavioral of Mux8_1 is

begin
process(a,b,c,d,sel)
begin
case sel is
when "000" => y <= a;
when "001" => y <= b;
when "010" => y <= c;
when "011" => y <= d;
when "100" => y <= e;
when "101" => y <= f;
when "110" => y <= g;
when "111" => y <= h;
when others => y <= (others => '0');
end case;
end process;
end Behavioral;
```