```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/14/2024 01:47:11 PM
-- Design Name:
-- Module Name: Mux8_1_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux8_1_tb is
```

```
--  Port ( );
generic( dw: integer:=4);
end Mux8_1_tb;

architecture Behavioral of Mux8_1_tb is
signal a, b, c, d, e, f, g, h : std_logic_vector ( dw-1 downto 0);
signal sel: std_logic_vector(dw-2 downto 0);
signal y: std_logic_vector (dw-1 downto 0);
begin
test: entity work.MUX8_1(Behavioral)
port map(a => a,b => b,c => c, d => d, e => e,f => f,g => g, h =>
h, sel => sel, y=>y);

tp:process
 begin
a <= "1110";b<= "1101"; c<= "1101";d<= "1101";e <= "1110";f<=
"1101"; g<= "1101";h<= "1101";
sel <= "000";wait for 30ns;
sel <= "001";wait for 30ns;
sel <= "010";wait for 30ns;
sel <= "011";wait for 30ns;
sel <= "100";wait for 30ns;
sel <= "101";wait for 30ns;
sel <= "110";wait for 30ns;
sel <= "111";wait for 30ns;
finish;
end process;

end Behavioral;
```