EENG 5560HW 3 Report Template

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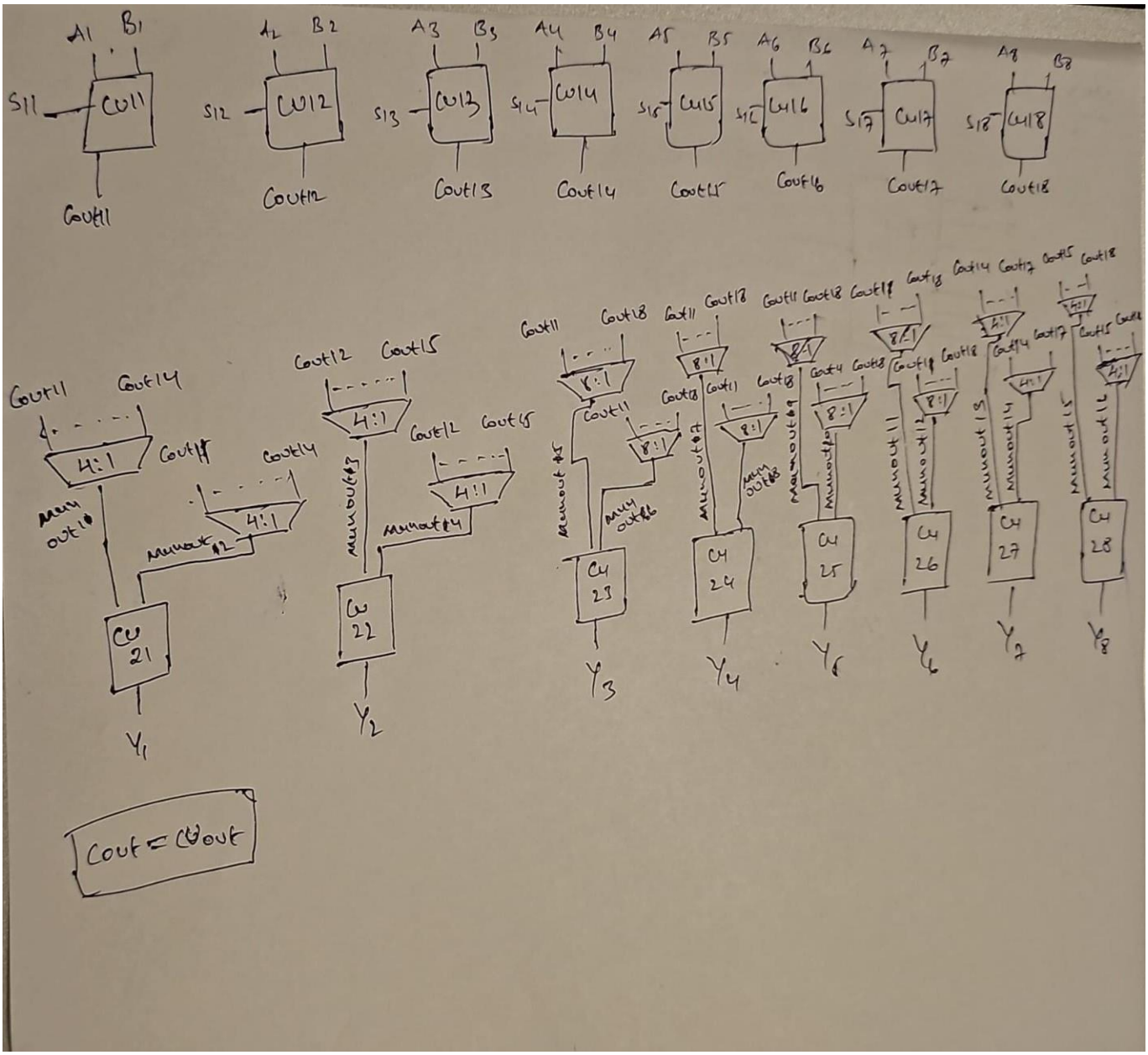
Design

Block diagrams

Overall design



Overall component: top box

Parameters: dw – data width (for inputs and outputs)

Input ports:

Port name	Bit width	Purpose
A1,A2,A3,A4,A5,A6,A7,A8 B1,B2,B3,B4,B5,B6,B7,B8	dw = 4	Data inputs
S11,S12,S13,S14,S15,S16,S17,S18 S21,S22,S23,S24,S25,S26,S27,S28	5	Selection line, selects data input to send to output

Output ports:

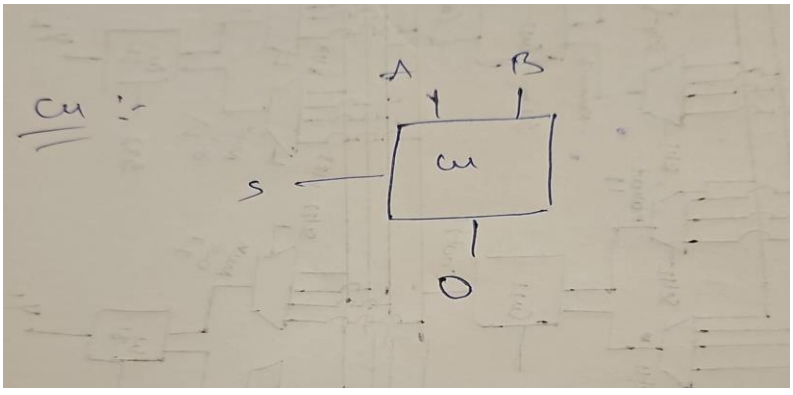
Port name	Bit width	Purpose
Y1,Y2,Y3,Y4, Y5,Y6,Y7,Y8	dw = 4	Data output

Necessary intermediate signals:

Port name	Bit width	Purpose
Cuout11-Cuout18, Cuout21-cuout28,	4	Connection between CUs output and Mux input
Muxout 1-muxout16	4	Connection between mux out put and cu's input

Subcomponents

Subcomponent: Computational Unit (CU)



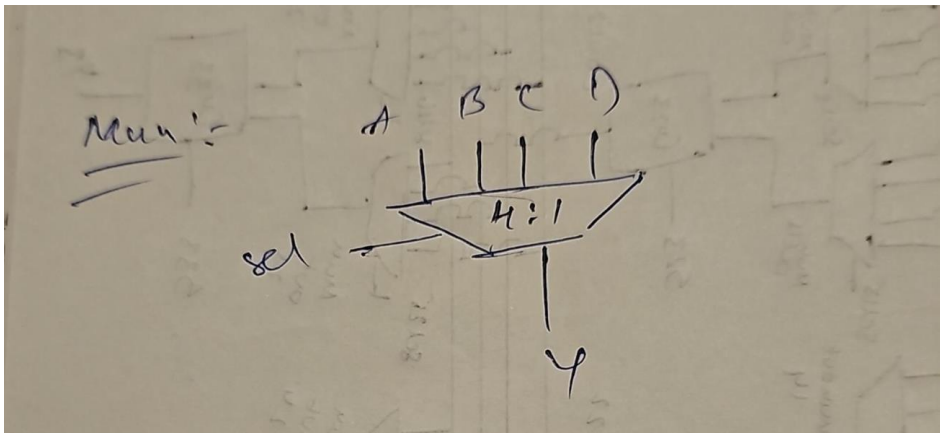
Input ports:

Port name	Bit width	Purpose
A	4	DATA INPUTS
B	4	DATA INPUTS
S	5	Selection line

Output ports:

Port name	Bit width	Purpose
O	dw = 4	Data output

Subcomponent: 4 to 1mux:



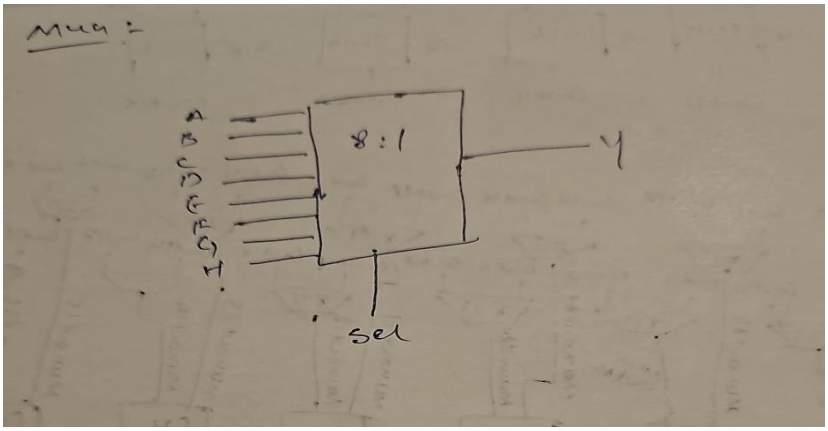
input

Port name	Bit width	Purpose
A,B,C,D	dw = 4	Data inputs
Sel	2	Select line, selects which of the 4 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
Y	dw = 4	Data output

SUB COMPONENT : 8 to 1 mux:



Port name	Bit width	Purpose
A,B,C,D,E,F,G,H	dw = 4	Data inputs
Sel	2	Select line, selects which of the 4 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
Y	dw = 4	Data output

Design explanation

Functionality

Top box is designed in 8:2 matrix form.

A1 to A8 &B1 to B8 are initial inputs for the CUs in the first row .the output of the CUs send through intermediate signal (cuout 11to cuout18) to muxs.

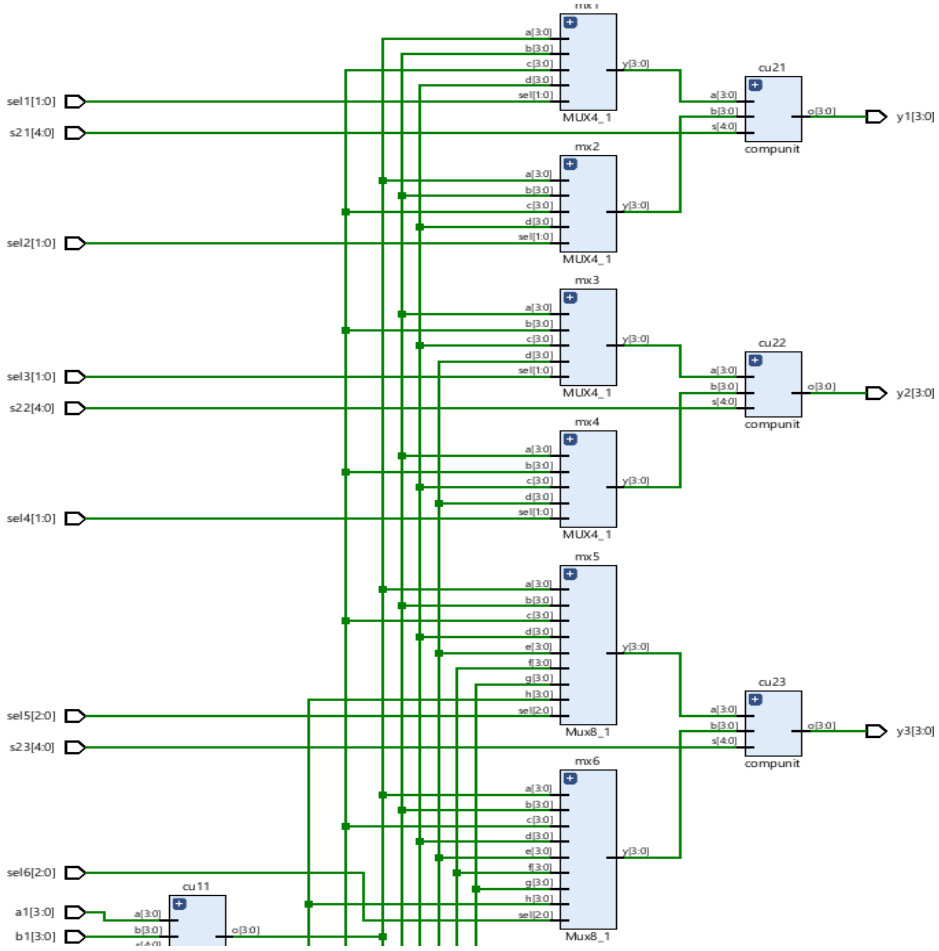
We are using 4 to 1 and 8 to 1 mux . The outputs of the 1st row CU's are connected to the inputs of the muxes.Output of the muxes are connected as the inputs of the cu's in 2nd row.

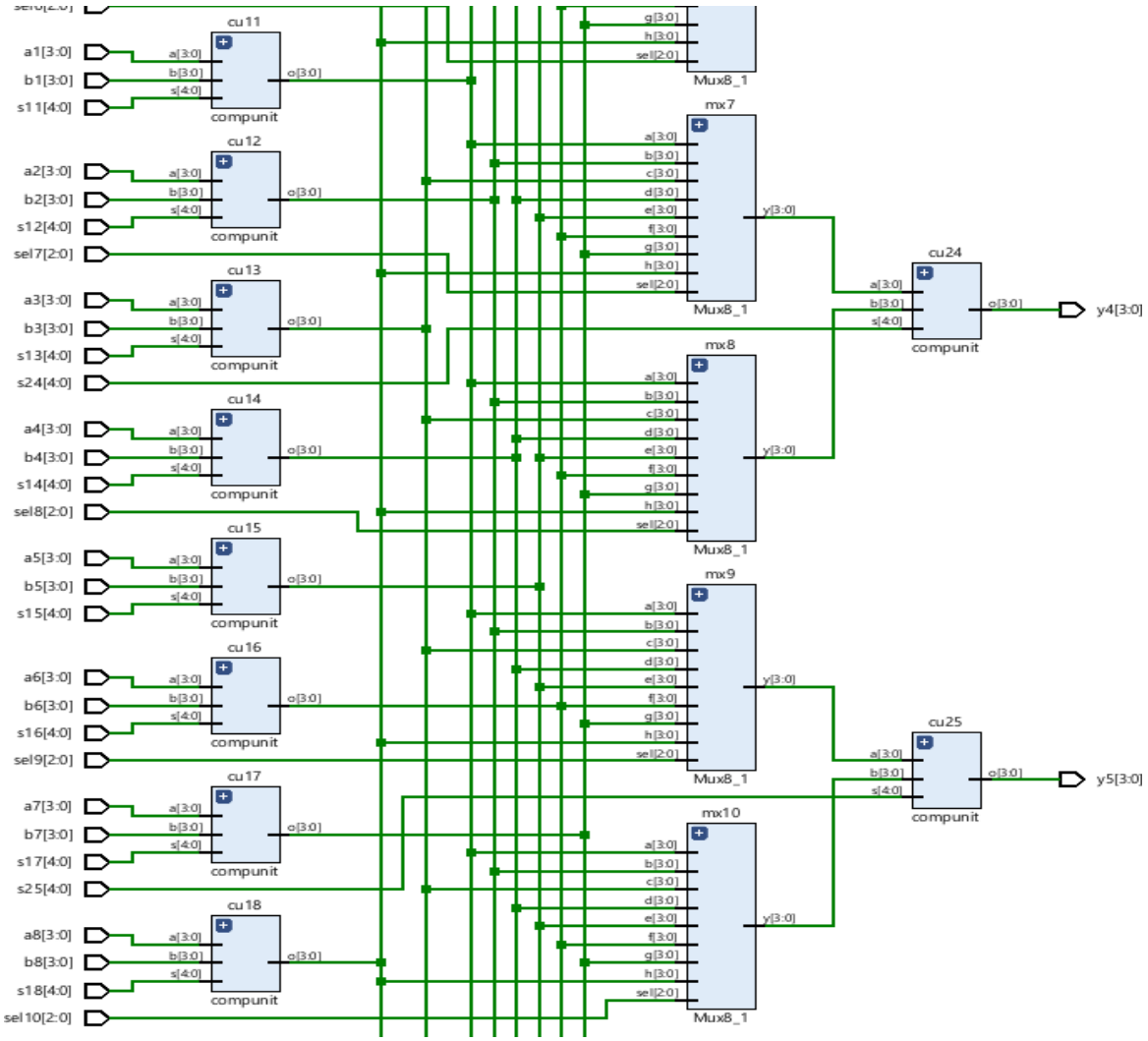
Output of the cu's in the 2nd row as main output.

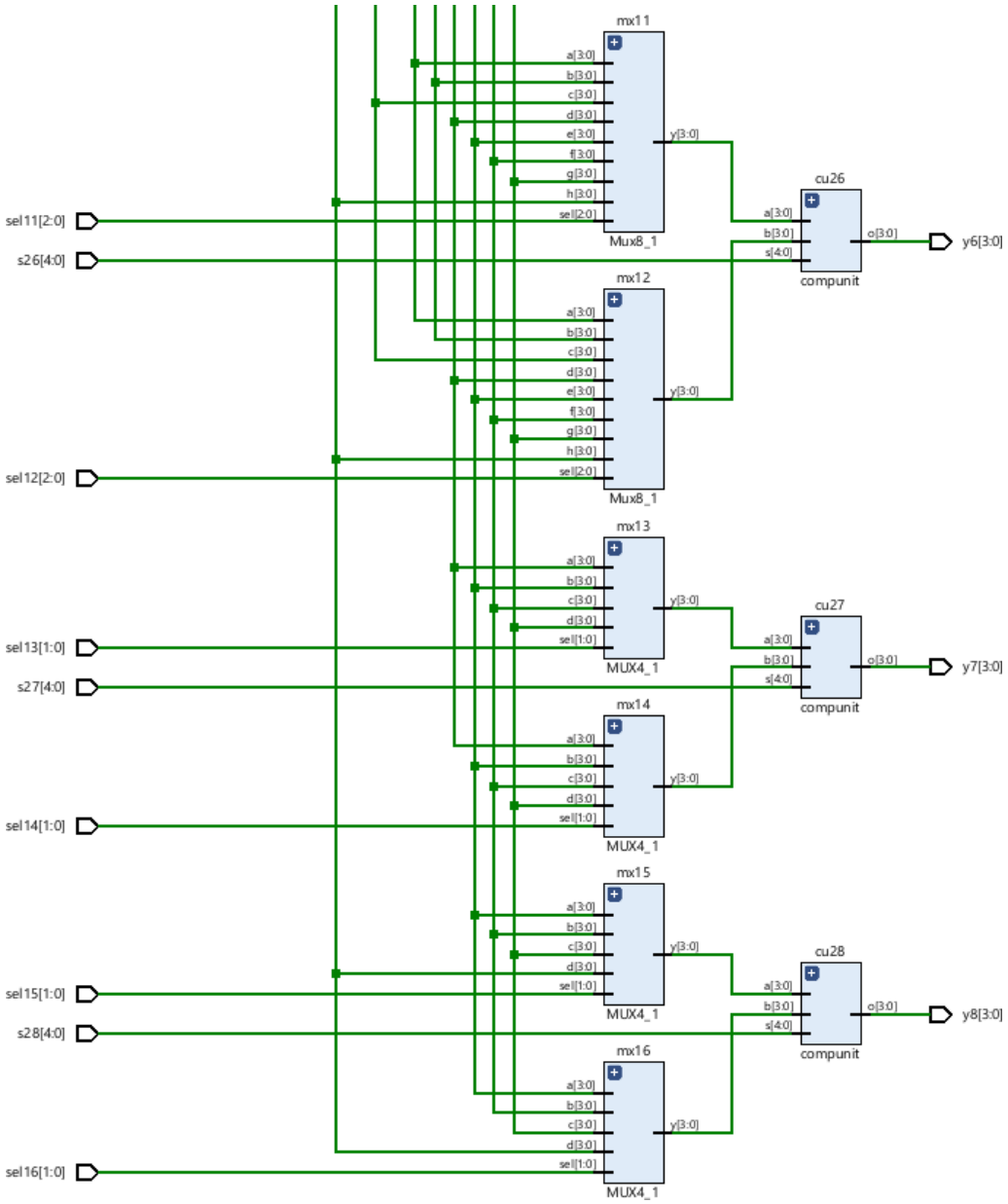
Results

Generated Schematics

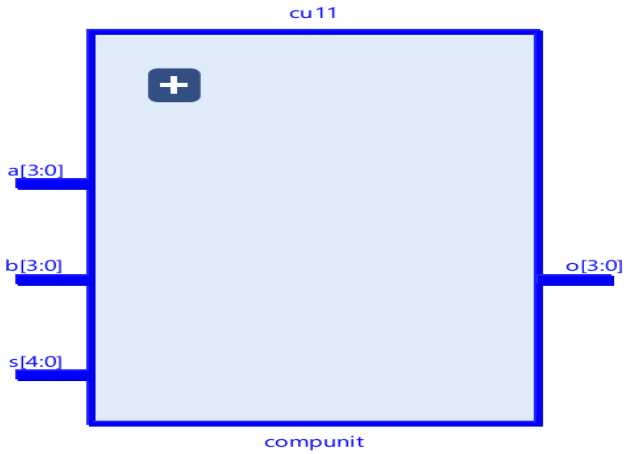
Top box:



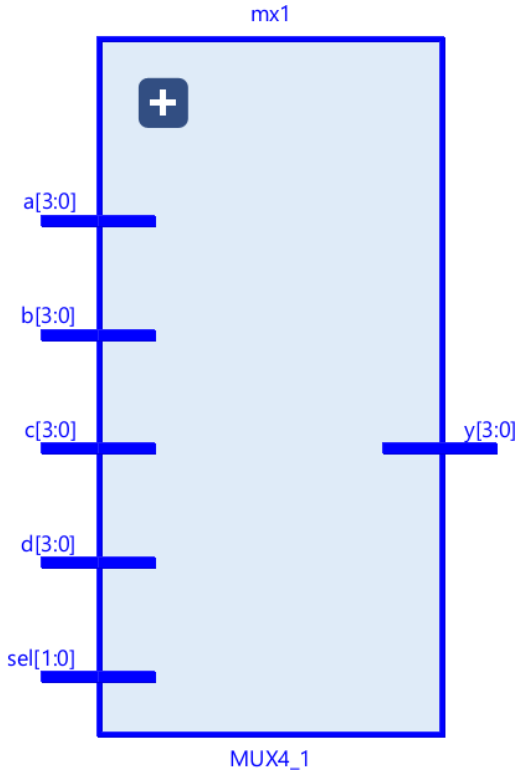

cu11
a1[3:0]
b1[3:0]
s11[4:0]
a[3:0]
b[3:0]
s[4:0]
o[3:0]
compunit
cu12
a2[3:0]
b2[3:0]
s12[4:0]
sel7[2:0]
cu13
a3[3:0]
b3[3:0]
s13[4:0]
s24[4:0]
cu14
a4[3:0]
b4[3:0]
s14[4:0]
sel8[2:0]
cu15
a5[3:0]
b5[3:0]
s15[4:0]
cu16
a6[3:0]
b6[3:0]
s16[4:0]
sel9[2:0]
cu17
a7[3:0]
b7[3:0]
s17[4:0]
s25[4:0]
cu18
a8[3:0]
b8[3:0]
s18[4:0]
sel10[2:0]
g[3:0]
h[3:0]
sel[2:0]
Mux8_1
mx7
c[3:0]
d[3:0]
e[3:0]
f[3:0]
y[3:0]
mx8
mx9
mx10
cu24
cu25
y4[3:0]
y5[3:0]


mx11
a[3:0]
b[3:0]
c[3:0]
d[3:0]
e[3:0]
f[3:0]
g[3:0]
h[3:0]
sel[2:0]
y[3:0]
Mux8_1
cu26
a[3:0]
b[3:0]
s[4:0]
o[3:0]
compunit
y6[3:0]
sel11[2:0]
s26[4:0]
mx12
Mux8_1
sel12[2:0]
mx13
sel[1:0]
MUX4_1
cu27
y7[3:0]
sel13[1:0]
s27[4:0]
mx14
sel14[1:0]
mx15
cu28
y8[3:0]
sel15[1:0]
s28[4:0]
mx16
sel16[1:0]

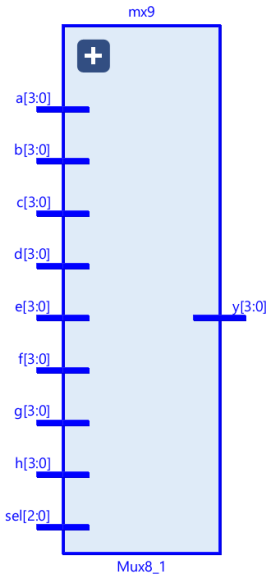
RTL for CU:



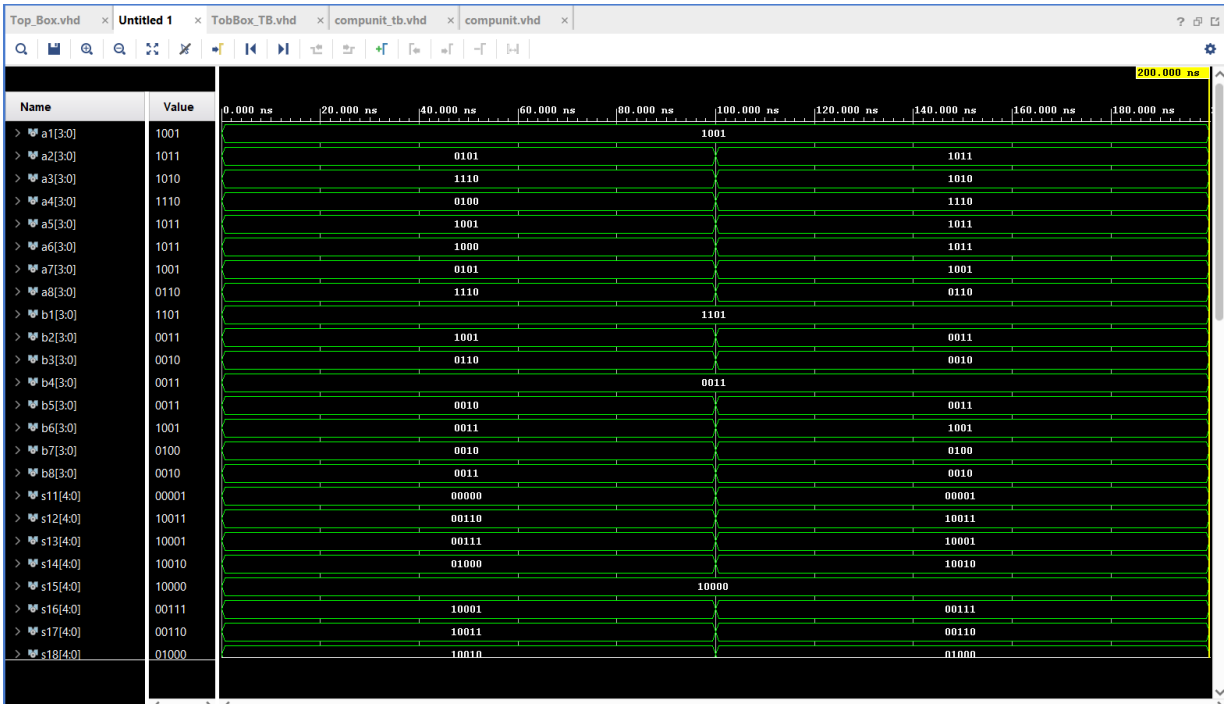
RTL for 4 to1 mux:

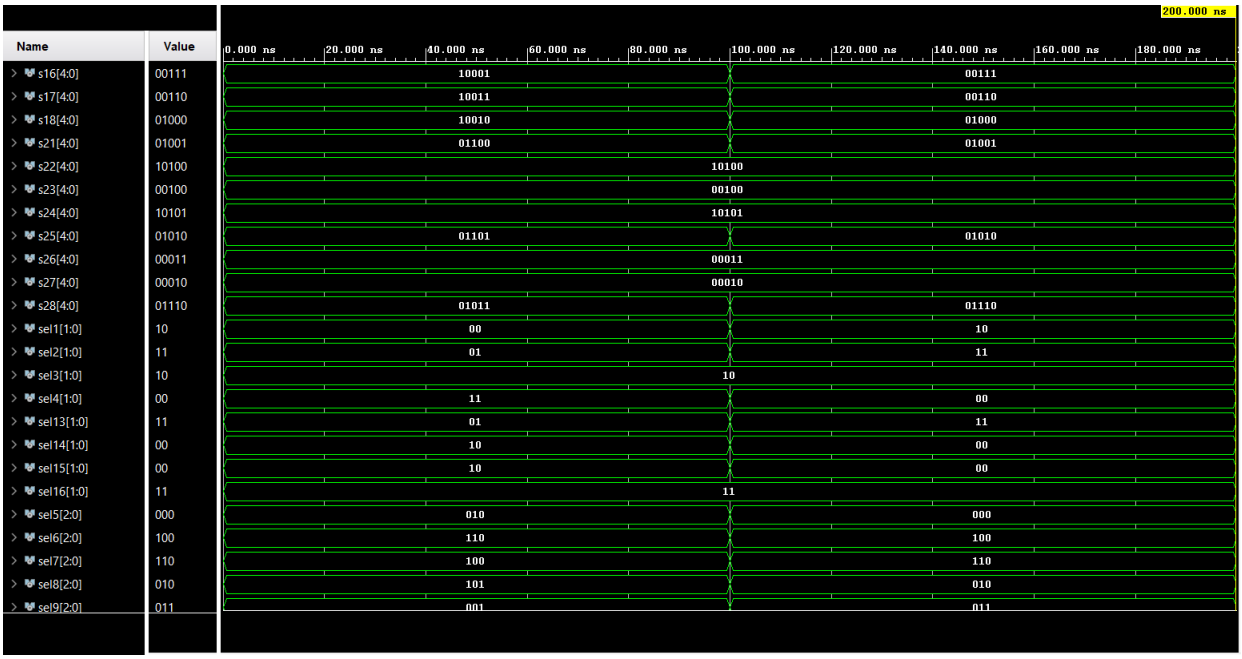


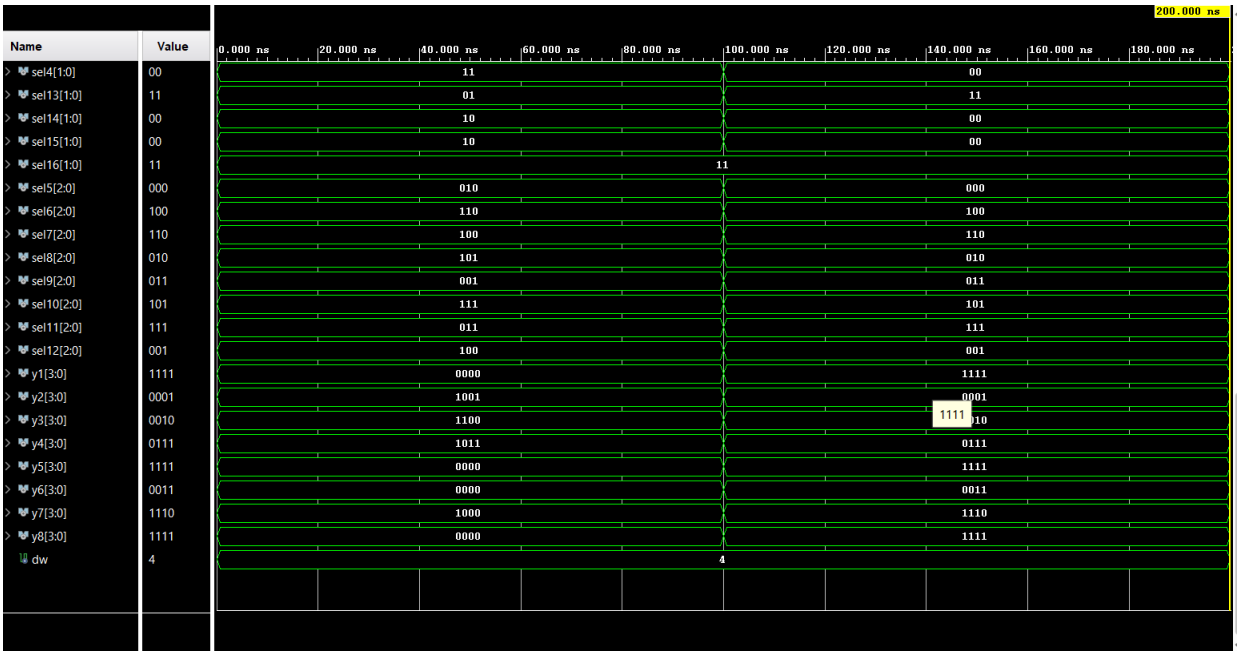
RTL for 8 to 1 mux:



Waveforms




Name
Value
s16[4:0] 00111
s17[4:0] 00110
s18[4:0] 01000
s21[4:0] 01001
s22[4:0] 10100
s23[4:0] 00100
s24[4:0] 10101
s25[4:0] 01010
s26[4:0] 00011
s27[4:0] 00010
s28[4:0] 01110
sel1[1:0] 10
sel2[1:0] 11
sel3[1:0] 10
sel4[1:0] 00
sel13[1:0] 11
sel14[1:0] 00
sel15[1:0] 00
sel16[1:0] 11
sel5[2:0] 000
sel6[2:0] 100
sel7[2:0] 110
sel8[2:0] 010
sel9[2:0] 011
200.000 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
10001
00111
10011
00110
10010
01000
01100
01001
10100
00100
10101
01101
01010
00011
00010
01011
01110
00
10
01
11
10
11
00
01
11
10
00
10
00
11
010
000
110
100
100
110
101
010
001
011


Name
Value
sel4[1:0] 00
sel13[1:0] 11
sel14[1:0] 00
sel15[1:0] 00
sel16[1:0] 11
sel5[2:0] 000
sel6[2:0] 100
sel7[2:0] 110
sel8[2:0] 010
sel9[2:0] 011
sel10[2:0] 101
sel11[2:0] 111
sel12[2:0] 001
y1[3:0] 1111
y2[3:0] 0001
y3[3:0] 0010
y4[3:0] 0111
y5[3:0] 1111
y6[3:0] 0011
y7[3:0] 1110
y8[3:0] 1111
dw 4
200.000 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
11
00
01
11
10
00
10
00
11
010
000
110
100
100
110
101
010
001
011
111
101
011
111
100
001
0000
1111
1001
0001
1100
0010
1011
0111
0000
1111
0000
0011
1000
1110
0000
1111
4
1111

Table/Calculations

Overall Design

Test Case 1 (*0ns to 100ns*):

CU	source a	source b	operation	calculated output	simulated output	matched
CU11	1001	1101	AND	1001	1001	YES
CU12	0101	1001	ADD	1110	1110	YES
CU13	1110	0110	SUB	1000	1000	YES
CU14	0100	0011	MULT	1100	1100	YES
CU15	1001	0010	ASL	0111	0111	YES
CU16	1000	0011	ASR	1111	1111	YES
CU17	0101	0010	LSL	0100	0100	YES
CU18	1110	0011	LSR	0001	0001	YES
CU21	CU11	CU12	GTE	0000	0000	YES
CU22	CU14	CU15	ROR	1001	1001	YES
CU23	CU13	CU17	XOR	1100	1100	YES
CU24	CU15	CU16	ROL	1011	1011	YES
CU25	CU12	CU18	LTE	0000	0000	YES
CU26	CU14	CU15	NOR	0000	0000	YES
CU27	CU15	CU16	NAND	1000	1000	YES
CU28	CU17	CU18	EQ	0000	0000	YES

Test Case # (*100ns to 200ns*):

CU	source a	source b	operation	calculated output	simulated output	matched
CU11	1001	1101	OR	1101	1101	YES
CU12	1011	0011	LSL	1000	1000	YES
CU13	1010	0010	ASR	1110	1110	YES
CU14	1110	0011	LSR	0001	0001	YES
CU15	1011	0011	ASR	1111	1111	YES
CU16	1011	1001	SUB	0010	0010	YES
CU17	1001	0100	ADD	1101	1101	YES
CU18	0110	0010	MULT	1100	1100	YES
CU21	CU13	CU14	GT	1111	1111	YES
CU22	CU14	CU12	ROR	0001	0001	YES
CU23	CU11	CU15	XOR	0010	0010	YES
CU24	CU17	CU13	ROL	0111	0111	YES
CU25	CU14	CU16	LT	1111	1111	YES
CU26	CU18	CU12	NOR	0011	0011	YES
CU27	CU17	CU14	NAND	1110	1110	YES
CU28	CU15	CU18	NEQ	1111	1111	YES