```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/08/2024 03:57:22 PM
-- Design Name:
-- Module Name: TobBox_TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TobBox_TB is
--  Port ( );
```

```
generic(dw: integer:=4);
end TobBox_TB;

architecture Behavioral of TobBox_TB is
  signal a1, a2, a3, a4, a5, a6, a7, a8, b1, b2, b3, b4, b5, b6,
b7, b8:  std_logic_vector(dw-1 downto 0);
  signal s11, s12, s13, s14, s15, s16, s17, s18, s21, s22, s23,
s24, s25, s26, s27, s28:  std_logic_vector(dw downto 0);
  signal sel1,sel2,sel3, sel4,sel13, sel14, sel15, sel16:
std_logic_vector(dw-3 downto 0);
  signal sel5, sel6, sel7, sel8, sel9,sel10,sel11, sel12:
std_logic_vector(dw-2 downto 0);
  signal y1, y2, y3, y4, y5, y6, y7, y8:  std_logic_vector(dw-1
downto 0);
begin
box: entity work.Top_Box(behavioral)
port map(a1 =>a1, a2 =>a2, a3 =>a3, a4 =>a4, a5 =>a5, a6 =>a6, a7
=>a7, a8 =>a8,
b1 =>b1,b2 =>b2,b3 =>b3,b4 =>b4,b5 =>b5,b6 =>b6,b7 =>b7,b8 =>b8,
s11=>s11,s12=>s12,s13 =>s13,s14 =>s14,s15 =>s15,s16 => s16, s17
=>s17,s18 =>s18,
s21=>s21,s22=>s22,s23 =>s23,s24 =>s24,s25 =>s25,s26=> s26, s27
=>s27,s28 =>s28,
sel1 => sel1,sel2 => sel2,sel3 => sel3, sel4 => sel4,sel5 => sel5,
sel6 => sel6,
sel7 => sel7, sel8 => sel8,sel9 => sel9,sel10 => sel10,sel11 =>
sel11, sel12 => sel12,
sel13 => sel13, sel14 => sel14, sel15 => sel15, sel16 => sel16,y1
=> y1,y2 => y2,y3 => y3,y4 => y4,
y5 => y5,y6 => y6,y7 => y7,y8 => y8);
ts:process
begin

--testcase1
a1<="1001";b1<= "1101";
a2<="0101";b2<= "1001";
a3<="1110";b3<= "0110";
```

```
a4<="0100";b4<= "0011";
a5<="1001";b1<= "0010";
a6<="1000";b2<= "0011";
a7<="0101";b3<= "0010";
a8<="1110";b4<= "0011";


s11<="00000";s12<= "00110";s13<="00111";s14<=
"01000";s15<="10000";s16<= "10001";s17<="10011";s18<= "10010";
s21<="01100";s22<= "10100";s23<="00100";s24<=
"10101";s25<="01101";s26<= "00011";s27<="00010";s28<= "01011";
sel1<="00";sel2<="01";sel3<="10";sel4<="11";
sel5<="100";sel6<="101";sel7<="001";sel8<="111";sel9<="011";
sel10<="100"; sel11<="100"; sel12<="101";
sel13<="00"; sel14<="01"; sel15<="10"; sel16<="11";

wait for 100ns;

--testcase2
a1<="1001";b1<= "1101";
a2<="1011";b2<= "0011";
a3<="1010";b3<= "0010";
a4<="1110";b4<= "0011";
a5<="1011";b5<= "0011";
a6<="1011";b6<= "1001";
a7<="1001";b7<= "0100";
a8<="0110";b8<= "0010";


s11<="00001";s12<= "10011";s13<="10001";s14<=
"10010";s15<="10000";s16<= "00111";s17<="00110";s18<= "01000";
s21<="01001";s22<= "10100";s23<="00100";s24<=
"10101";s25<="01010";s26<= "00011";s27<="00010";s28<= "01110";
sel1<="10";sel2<="11";sel3<="10";sel4<="00";
sel5<="000";sel6<="100";sel7<="110";sel8<="010";sel9<="011";
sel10<="101"; sel11<="111"; sel12<="001";
 sel13<="11"; sel14<="00"; sel15<="00"; sel16<="11";
```

```
wait for 100ns;

finish;
end process;
end Behavioral;
```