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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 02/08/2024 03:04:32 PM
-- Design Name:
-- Module Name: MUX4_1_TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity MUX4_1_TB is
```

```
--  Port ( );
end MUX4_1_TB;

architecture Behavioral of MUX4_1_TB is
signal a ,b,c,d : std_logic_vector ( 5 downto 0);
signal sel: std_logic_vector(1 downto 0);
signal y: std_logic_vector (5 downto 0);
begin
test: entity work.MUX4_1(Behavioral)
port map(a => a,b => b,c => c, d => d,sel => sel, y=>y);

tp:process
 begin
a <= "111001";b<= "110101"; c<= "110100";d<= "110101";
sel <= "00";wait for 30ns;
sel <= "01";wait for 30ns;
sel <= "10";wait for 30ns;
sel <= "11";wait for 30ns;
finish;
end process;

end Behavioral;
```