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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/08/2024 12:55:42 AM
-- Design Name:
-- Module Name: MUX4_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity MUX4_1 is
Port (a,b,c,d: in std_logic_vector(5 downto 0);
```

```
sel: in std_logic_vector(1 downto 0);
y: out std_logic_vector(5 downto 0) );
end MUX4_1;

architecture Behavioral of MUX4_1 is

begin
process(a,b,c,d,sel)
begin
case sel is
when "00" => y <= a;
when "01" => y <= b;
when "10" => y <= c;
when "11" => y <= d;
when others => y <= (others => '0');
end case;
end process;
end Behavioral;
```