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-- Company:
-- Engineer:
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-- Create Date: 02/08/2024 01:14:49 AM
-- Design Name:
-- Module Name: Top_Box - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top_Box is
  Port (a1,a2,a3,a4,b1,b2,b3,b4: in std_logic_vector(5 downto 0);
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  s11,s12,s13,s14,s21,s22,s23,s24,s31,s32,s33,s34: in
std_logic_vector(4 downto 0);
  sel11,sel12,sel13, sel14,sel15, sel16, sel17, sel18,
  sel21,sel22,sel23, sel24,sel25, sel26, sel27, sel28: in
std_logic_vector(1 downto 0);
  y1,y2,y3,y4: out std_logic_vector(5 downto 0) );
end Top_Box;

 architecture Behavioral of Top_Box is
 --Below signal lines for establishing connection between output of
CU and input of muxes
signal cuout11,cuout12,cuout13, cuout14,cuout21,cuout22,cuout23,
cuout24: std_logic_vector(5 downto 0);
 -- signal lines for establishing connection between  outputs of
muxes and inputs of CU
signal
muxout11,muxout12,muxout13,muxout14,muxout15,muxout16,muxout17,muxo
ut18,
muxout21,muxout22,muxout23,muxout24,muxout25,muxout26,muxout27,muxo
ut28: std_logic_vector(5 downto 0);
begin
-- construction of 4*3 reconfigurable architecture.
--row 1
cu11: entity work.compunit(Behavioral)
 port map(a => a1, b =>B1, S => S11 ,O =>CUOUT11);
cu12: entity work.compunit(Behavioral)
 port map(a => a2, b =>B2, S => S12 ,O =>CUOUT12);
 cu13: entity work.compunit(Behavioral)
 port map(a => a3, b =>B3, S => S13 ,O =>CUOUT13);
cu14: entity work.compunit(Behavioral)
 port map(a => a4, b =>B4, S => S14 ,O =>CUOUT14);

-- row 2
mx11:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel11, y => muxout11);
mx12:entity work.MUX4_1(behavioral)
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port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel12, y => muxout12);
cu21: entity work.compunit(Behavioral)
port map(a => muxout11, b =>muxout12, S => S21 ,O =>CUOUT21);

mx13:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel13, y => muxout13);
mx14:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel14, y => muxout14);
cu22: entity work.compunit(Behavioral)
port map(a => muxout13, b =>muxout14, S => S22 ,O =>CUOUT22);

mx15:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel15, y => muxout15);
mx16:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel16, y => muxout16);
cu23: entity work.compunit(Behavioral)
port map(a => muxout15, b =>muxout16, S => S23 ,O =>CUOUT23);

mx17:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel17, y => muxout17);
mx18:entity work.MUX4_1(behavioral)
port map(a=>cuout11,b=> cuout12, c => cuout13,d => cuout14, sel =>
sel18, y => muxout18);
cu24: entity work.compunit(Behavioral)
 port map(a => muxout17, b =>muxout18, S => S24 ,O =>CUOUT24);

--row3
mx21:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel21, y => muxout21);
mx22:entity work.MUX4_1(behavioral)
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port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel22, y => muxout22);
cu31: entity work.compunit(Behavioral)
port map(a => muxout21, b =>muxout22, S => S31 ,O =>y1);

mx23:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel23, y => muxout23);
mx24:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel24, y => muxout24);
cu32: entity work.compunit(Behavioral)
port map(a => muxout23, b =>muxout24, S => S32 ,O =>y2);

mx25:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel25, y => muxout25);
mx26:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel26, y => muxout26);
cu33: entity work.compunit(Behavioral)
port map(a => muxout25, b =>muxout26, S => S33 ,O =>y3);

mx27:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel27, y => muxout27);
mx28:entity work.MUX4_1(behavioral)
port map(a=>cuout21,b=> cuout22, c => cuout23,d => cuout24, sel =>
sel28, y => muxout28);
cu34: entity work.compunit(Behavioral)
 port map(a => muxout27, b =>muxout28, S => S34 ,O =>y4);

end Behavioral;
```