EENG 5560 HW 2 Report

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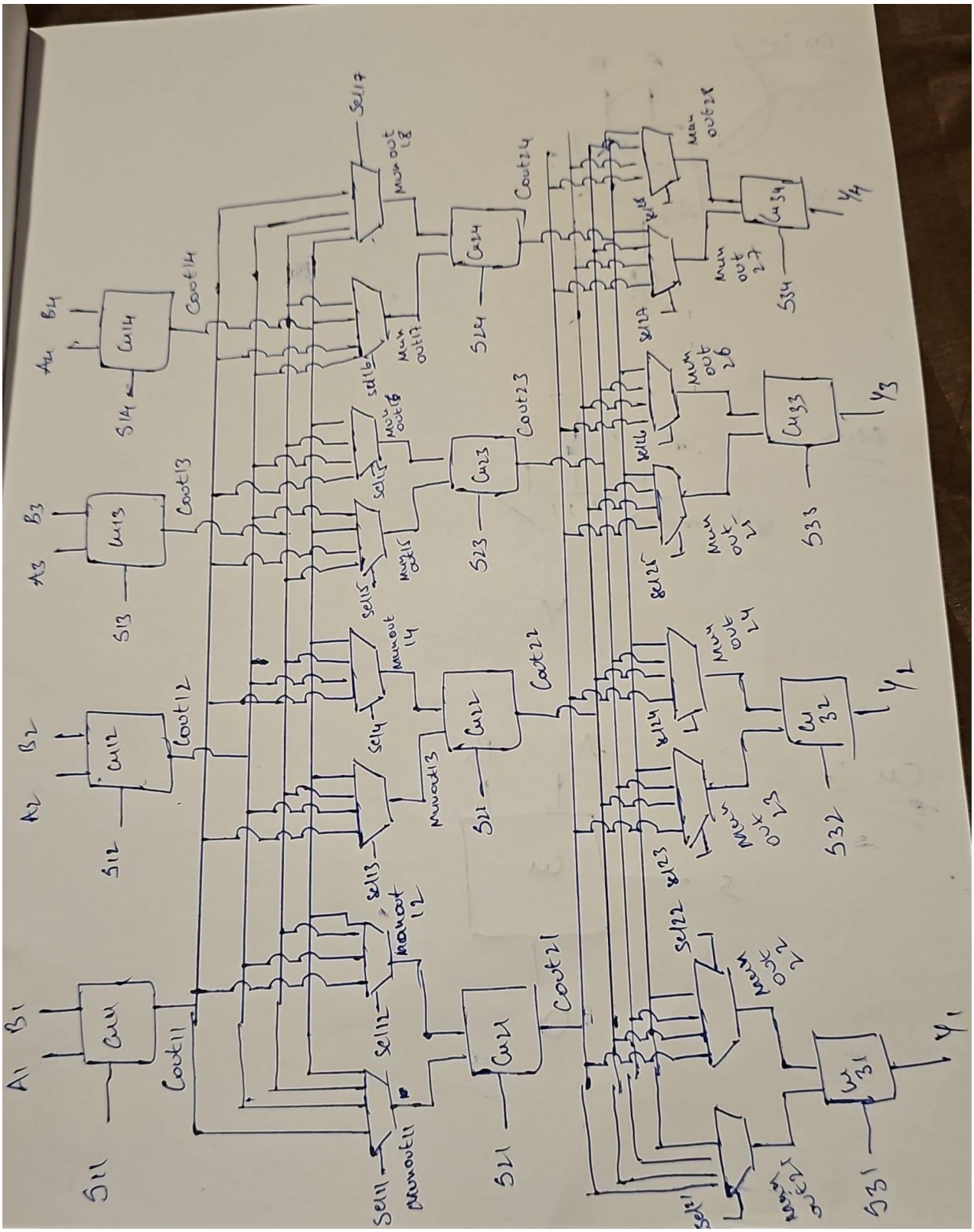
Design

Block diagram



Overall component: top box

Input ports:

Port name	Bit width	Purpose
A1 B1 ,A2 B2 ,A3 B3,A4 B4	6	Operand 1-operand 8
S11-S14, S21- S24, S31-s34	5	Cu selection lines
Sel11- Sel18 Sel21- Sel28	2	Mux selection lines

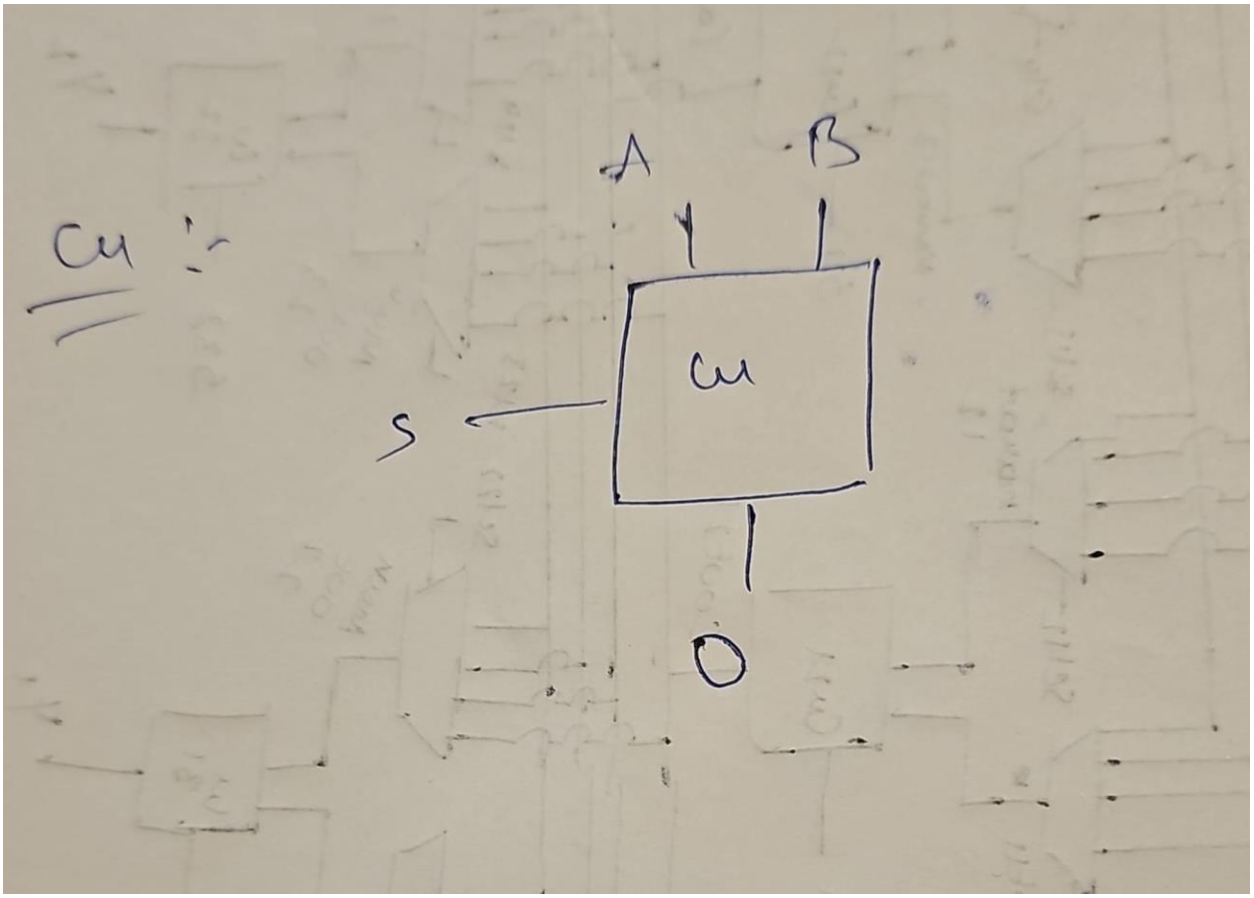
Output ports:

Port name	Bit width	Purpose
Y1, Y2,Y3,Y4	6	Out put

Necessary intermediate signals:

Port name	Bit width	Purpose
Cuout11-Cuout14, Cuout21-cuout24, Cuout31-cuout34	6	Connection between CUs output and Mux input
Muxout 11-muxout18, Muxout21-muxout28	6	Connection between mux out put and cu’s input

Subcomponent: Computational Unit (CU)



Input ports:

Port name	Bit width	Purpose
A	6	Operand 1
B	6	Operand 2
S	5	Selection line

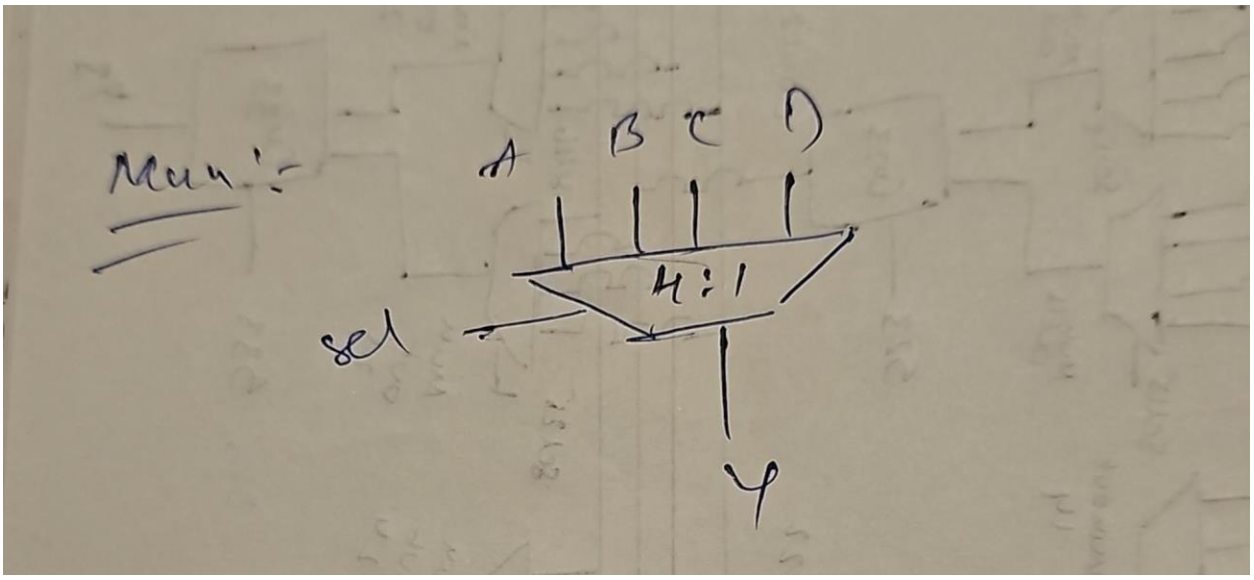
Output ports:

Port name	Bit width	Purpose
O	6	Out put

Necessary intermediate signals:

No intermediate signals used.

Subcomponent: mux:



Input ports:

Port name	Bit width	Purpose
A	6	Operand 1
B	6	Operand 2
C	6	Operand 3
D	6	Operand 4
S	2	Selection line

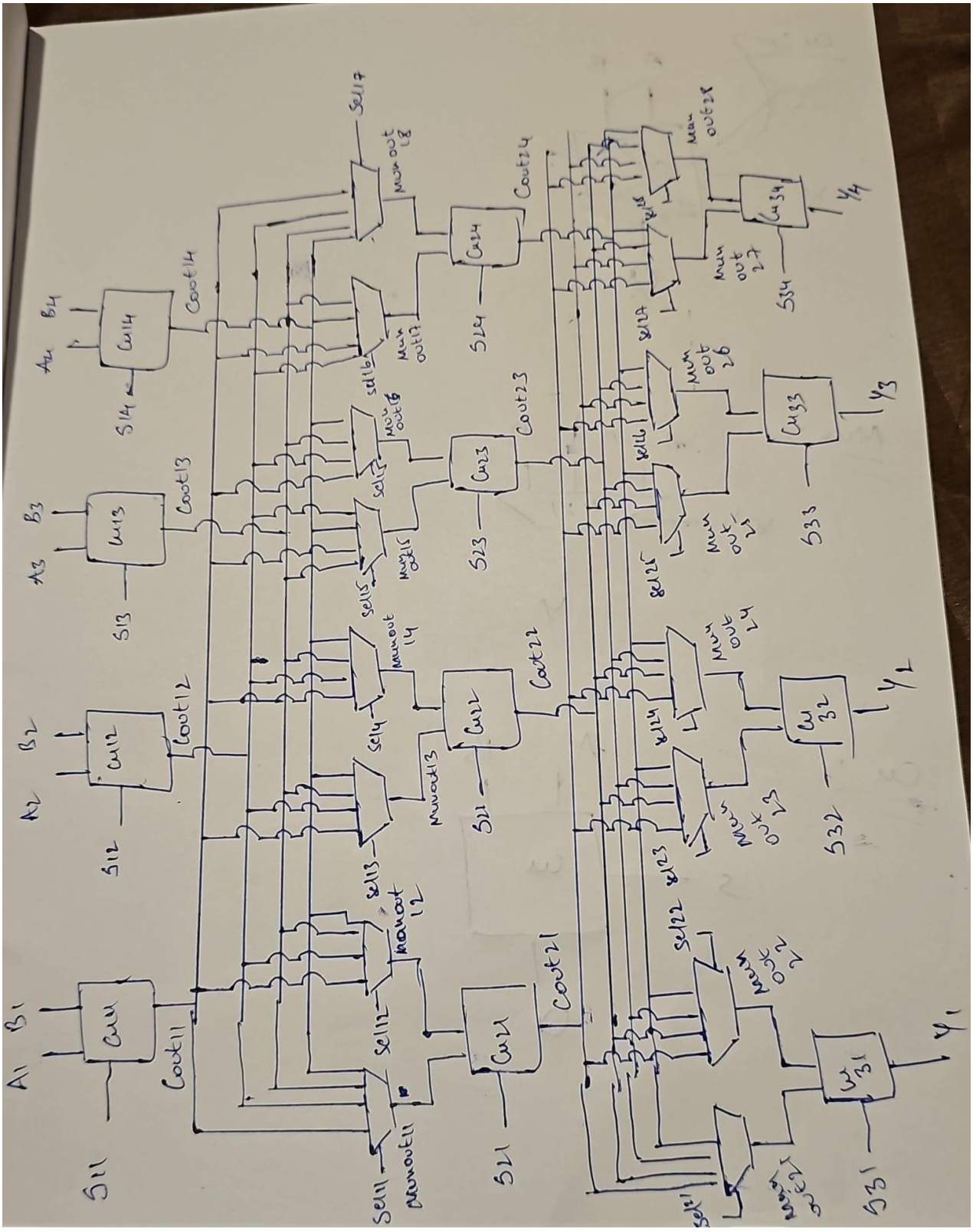
Output ports:

Port name	Bit width	Purpose
O	6	Out put

Necessary intermediate signals:

No intermediate signals used.

Design



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A1,B1 are inputs for CU11

A2,B2 are inputs for CU12

A3,B3 are inputs for CU13

A4,B4 are inputs for CU14

Operations in the cu:

00000 = AND

00001 = OR

00010 =NAND

00011 = N0R

00100 =XOR

00101 = XNOR

00110 = ADD

00111 = SUB

01000 = MUL

01001 = GREATER THAN

01010 =LESS THAN

01011 = EQUAL TOO

01100 = GREATHER THAN OR EQUALTOO

01101 = LESS THAN OR EQUAL TOO

01110 = NOT EQUAL TOO

01111 = GRND

10000 = arithmetic shift left

10001 = arithmetic shift right

10010 =logical shift right

10011 =logical shift left

10100 =rotation shift right

10101 =rotation shift left

Design explanation:

a1,a2,a3,a4,b1,b2,b3,b4 are the inputs to the cu's of the 1st row.

The 4 outputs of the 1st row CU's are connected to the inputs of the muxes.

Output of the muxes are connected as the inputs of the cu's in 2nd row.

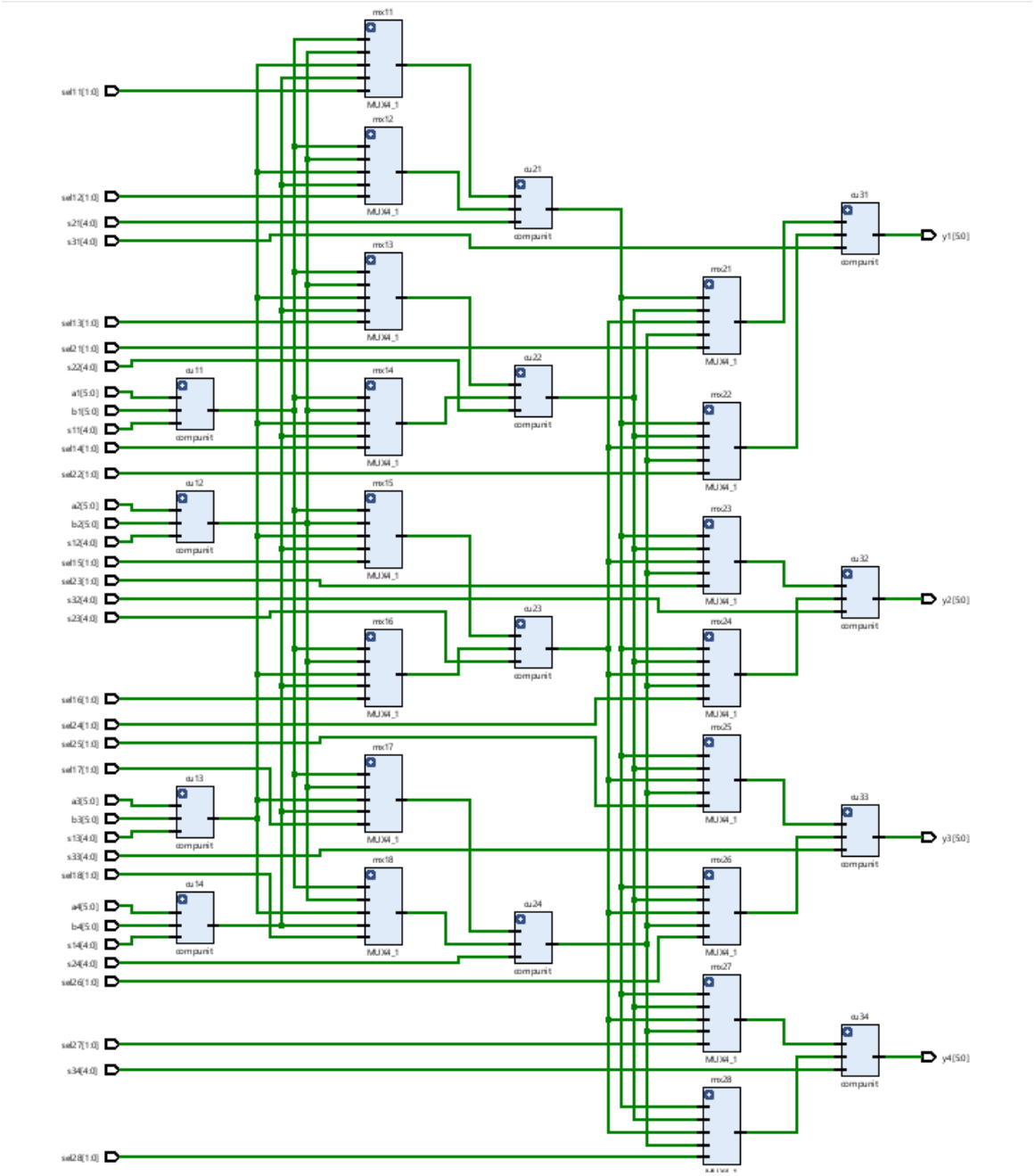
The 4 outputs of the 2st row CU's are connected to the inputs of the muxes.

Output of the muxes are connected as the inputs of the cu's in 3nd row.

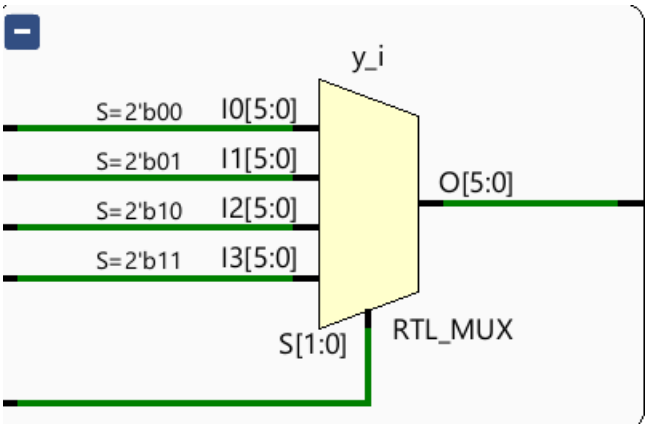
Output of the cu's as main output.

Results

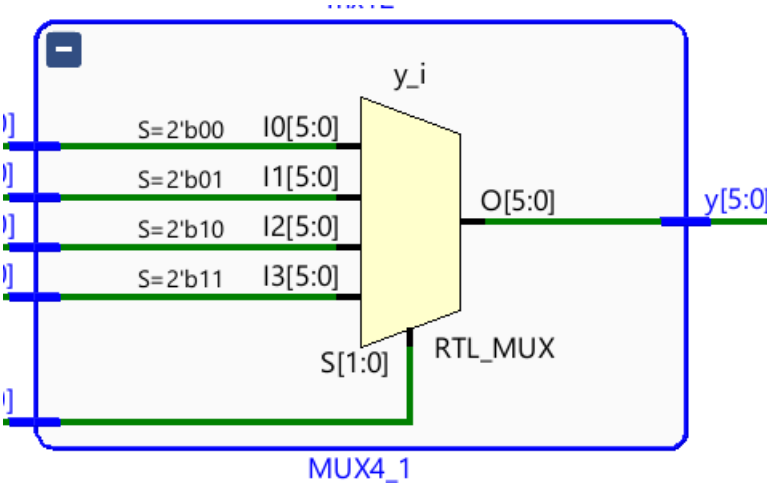
Generated Schematic



Sub component: mux

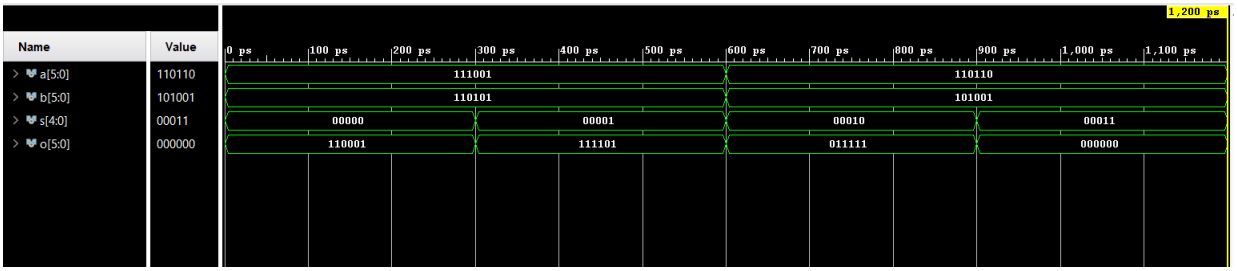


CU

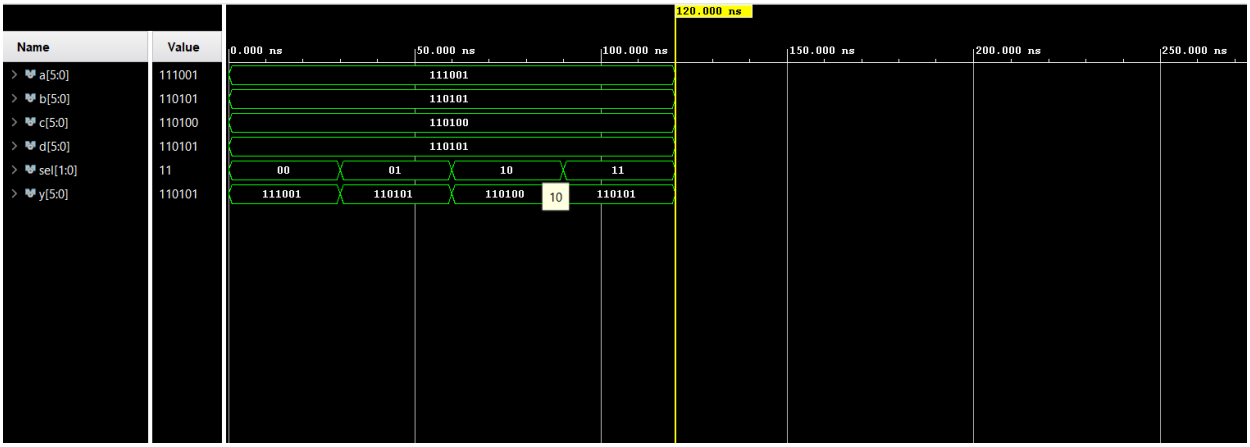


Waveforms

CU waveform



Mux waveform



Topbox waveform :

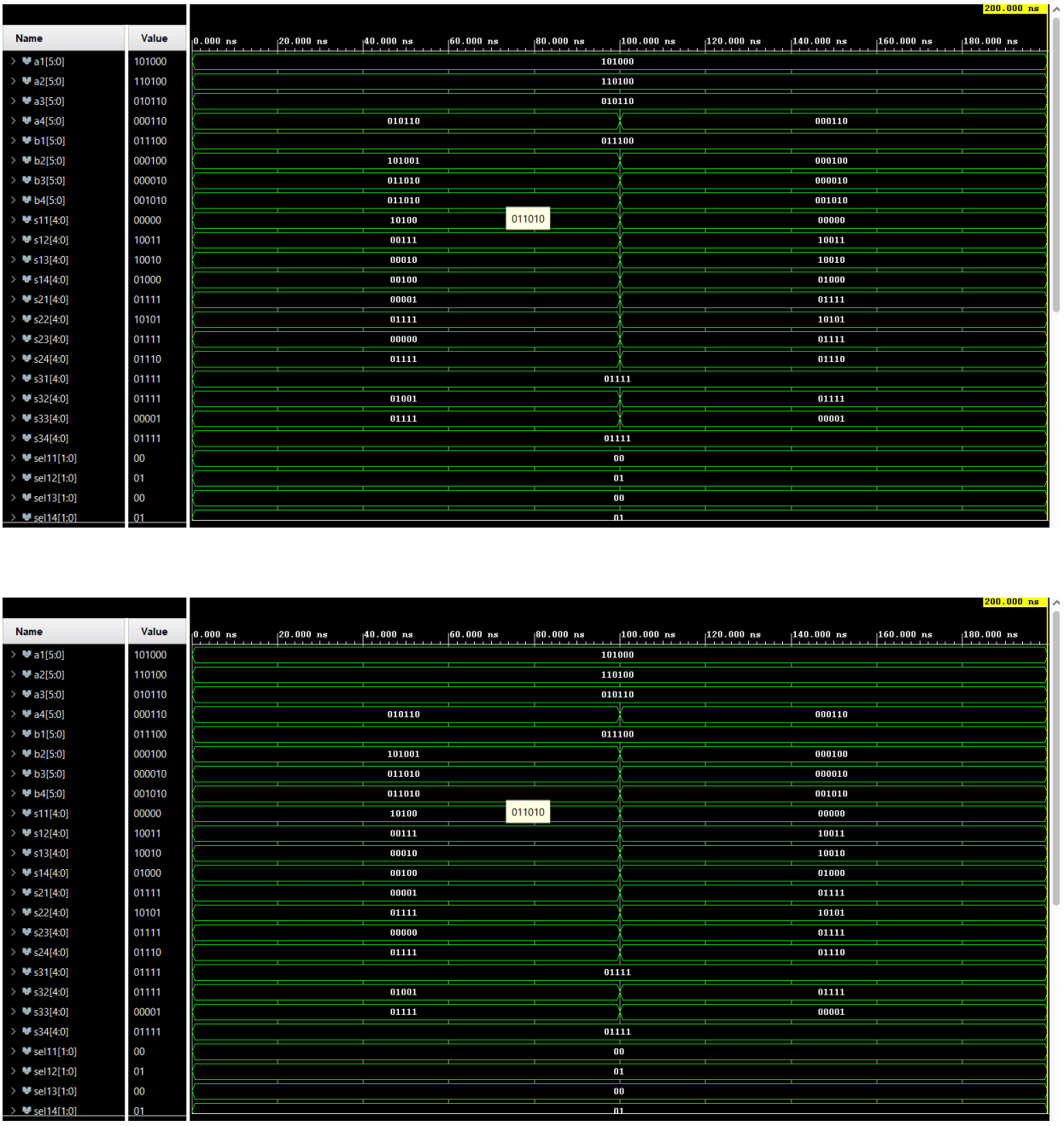


Figure 1 - Waveforms

Table/Calculations:

Case 1:

CU#	SourceA	SourceB	Oper	Calculated Op	Simulated Op	Match	
CU11	101000	11100	ror	10	10	Yes	
CU12	110100	101001	sub	10000	10000	Yes	
CU13	10110	11010	nand	101101	101101	Yes	
Cu14	10110	11010	xor	001100	1100	yes	
Cu21	(Cu11)	(cu12)	or	10010	10010	yes	
Cu22	(Cu11)	(cu12)	gnd	SHUTDOWN	SHUTDOWN	yes	
Cu23	(Cu13)	(cu14)	add	111001	111001	yes	
Cu24	(Cu13)	(cu14)	gnd	0	0	yes	
Cu31	Cu21	cu22	gnd	0	0	yes	
Cu32	Cu21	Cu23	gt	0	0	yes	OUT PUT
Cu33	Cu21	cu22	gnd	0	0	yes	
Cu34	Cu21	cu22	gnd	0	0	yes	

Case 2:

CU#	SourceA	SourceB	Oper	Calculated Op	Simulated Op	Match	
CU11	101000	011100	AND	001000	001000	Yes	
CU12	110100	000100	LSL	0	0	Yes	
CU13	010110	000010	LSR	101	101	Yes	
Cu14	000110	001010	MULT	111100	111100	yes	
Cu21	CU14	CU12	GRND	0	0	yes	
Cu22	Cu11	Cu12	ROL	1000	1000	yes	
Cu23	CU11	CU12	GRND	0	0	yes	
Cu24	Cu13	Cu14	NE	111111	111111	yes	
Cu31	CU21	CU22	GRND	0	0	yes	
Cu32	CU21	CU21	GRND	0	0	yes	
Cu33	Cu21	Cu23	OR	111111	111111	yes	output
Cu34	CU21	CU22	GRND	0	0	yes	