```
----------------------------------------------------------------------
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-- Company:
-- Engineer:
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-- Create Date: 04/29/2023 10:33:34 PM
-- Design Name:
-- Module Name: Registor - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Registor is
generic(dw:integer);
```

```
Port (a: in std_logic_vector(dw-1 downto 0);
clk: in std_logic;
R_en: in std_logic;
z: out std_logic_vector(dw-1 downto 0));
end Registor;

architecture Behavioral of Registor is
signal storage_unit: std_logic_vector(dw-1 downto 0);
begin
    process(clk, R_en,a)
    begin
        if (clk = '1') then
            if R_en = '0' then
                storage_unit<= a;
             else
             z <= storage_unit;
          end if;
          end if;
     end process;
end Behavioral;
```