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-- Company:
-- Engineer:
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-- Create Date: 03/27/2024 04:50:45 PM
-- Design Name:
-- Module Name: Top_Box - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.custom_pack.all;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top_Box is
--  Port ( );
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generic(do:integer:=4);
Port (input: in ARR_2D (0 to do -3,0 to do -1)(do-1 downto 0);
op: in ARR_2D (0 to do-1,0 to do-1)(do downto 0);
clk: in std_logic;
MxSel: in ARR_2D (0 to (do)-1,0 to 2*do-1)(do-3 downto 0);
R_en_a,R_en_b,R_en_op,R_en_o:  in array_2D (0 to do-1,0 to do-1);
output: out ARR_2D (0 to do-1,0 to do-1)(do-1 downto 0));
end Top_Box;

architecture Behavioral of Top_Box is
signal buss: ARR_2D (0 to do -1,0 to do -1)(do-1 downto 0);
begin
cu_00: entity work.CU_With_Resistor (Behavioral)
port map( A => input(0,0), B => buss(3,0), C => "0000", D =>
"0000",
e =>input(1,0) , f =>buss(3,0) ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(0,0),op => op(0,0),mxSel2 => mxSel(0,1), clk =>
clk,
 R_en_a => R_en_a(0,0),
  R_en_b => R_en_b(0,0),R_en_op => R_en_op(0,0),R_en_o =>
R_en_o(0,0),o => buss(0,0));

cu_01: entity work.CU_With_Resistor (Behavioral)
port map( A => input(0,1), B => buss(3,1), C => buss(0,0), D =>
"0000",e =>input(1,1), f =>buss(3,1) ,g => buss(0,0),h => "0000" ,
 MXsel1 => Mxsel(0,2),op => op(0,1),mxSel2 => mxSel(0,3), clk =>
clk,R_en_a => R_en_a(0,1),  R_en_b => R_en_b(0,1),R_en_op =>
R_en_op(0,1),R_en_o => R_en_o(0,1),o => buss(0,1));

cu_02: entity work.CU_With_Resistor (Behavioral)
port map( A => input(0,2), B => buss(3,2), C => buss(0,0), D =>
"0000",e =>input(1,2), f =>buss(3,2) ,g => buss(0,0),h => "0000" ,
 MXsel1 => Mxsel(0,4),op => op(0,2),mxSel2 => mxSel(0,5), clk =>
clk,R_en_a => R_en_a(0,2),  R_en_b => R_en_b(0,2),R_en_op =>
R_en_op(0,2),R_en_o => R_en_o(0,2),
o => buss(0,2));
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cu_03: entity work.CU_With_Resistor (Behavioral)
port map( A => input(0,3), B => buss(3,3), C => buss(0,0), D =>
"0000",e =>input(1,3), f =>buss(3,3) ,g => buss(0,0),h => "0000" ,
 MXsel1 => Mxsel(0,6),op => op(0,3),mxSel2 => mxSel(0,7), clk =>
clk,R_en_a => R_en_a(0,3),  R_en_b => R_en_b(0,3),R_en_op =>
R_en_op(0,3),R_en_o => R_en_o(0,3),
o => buss(0,3));

cu_10: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(0,0), B => "0000", C => "0000", D => "0000",e
=>buss(0,0) , f =>"0000" ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(1,0),op => op(1,0),mxSel2 => mxSel(1,1), clk =>
clk,R_en_a => R_en_a(1,0),  R_en_b => R_en_b(1,0),R_en_op =>
R_en_op(1,0),R_en_o => R_en_o(1,0),
o => buss(1,0));

cu_11: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(0,1), B => buss(1,0), C => "0000", D =>
"0000",e =>buss(0,1) , f =>buss(1,0) ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(1,2),op => op(1,1),mxSel2 => mxSel(1,3), clk =>
clk,R_en_a => R_en_a(1,1),  R_en_b => R_en_b(1,1),R_en_op =>
R_en_op(1,1),R_en_o => R_en_o(1,1),
o => buss(1,1));

cu_12: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(0,2), B => buss(1,0), C => "0000", D =>
"0000",e =>buss(0,2) , f =>buss(1,0) ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(1,4),op => op(1,2),mxSel2 => mxSel(1,5), clk =>
clk,R_en_a => R_en_a(1,2),  R_en_b => R_en_b(1,2),R_en_op =>
R_en_op(1,2),R_en_o => R_en_o(1,2),
o => buss(1,2));

cu_13: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(0,3), B => buss(1,0), C => "0000", D =>
"0000",e =>buss(0,3) , f =>buss(1,0) ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(1,6),op => op(1,3),mxSel2 => mxSel(1,7), clk =>
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clk,R_en_a => R_en_a(1,3),  R_en_b => R_en_b(1,3),R_en_op =>
R_en_op(1,3),R_en_o => R_en_o(1,3),
o => buss(1,3));

cu_20: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(1,0), B => buss(0 ,0), C => "0000", D =>
"0000",
e =>buss(1,0) , f =>buss(0,0) ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(2,0),op => op(2,0),mxSel2 => mxSel(2,1), clk =>
clk,R_en_a => R_en_a(2,0),  R_en_b => R_en_b(2,0),R_en_op =>
R_en_op(2,0),R_en_o => R_en_o(2,0),
o => buss(2,0));

cu_21: entity work.CU_With_Resistor (Behavioral)
port map(  A => buss(1,1), B => buss(0,1), C => buss(2,0), D =>
"0000",
e =>buss(1,1) , f =>buss(0,1) ,g => buss(2,0),h => "0000" ,
 MXsel1 => Mxsel(2,2),op => op(2,1),mxSel2 => mxSel(2,3), clk =>
clk,R_en_a => R_en_a(2,1),  R_en_b => R_en_b(2,1),R_en_op =>
R_en_op(2,1),R_en_o => R_en_o(2,1),
o => buss(2,1));

cu_22: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(1,2), B => buss(0,2), C => buss(2,0), D =>
"0000",
e =>buss(1,2) , f =>buss(0,2) ,g => buss(2,0),h => "0000" ,
 MXsel1 => Mxsel(2,4),op => op(2,2),mxSel2 => mxSel(2,5), clk =>
clk,R_en_a => R_en_a(2,2),  R_en_b => R_en_b(2,2),R_en_op =>
R_en_op(2,2),R_en_o => R_en_o(2,2),
o => buss(2,2));

cu_23: entity work.CU_With_Resistor (Behavioral)
port map(  A => buss(1,3), B => buss(0,3), C => buss(2,0), D =>
"0000",
e =>buss(1,3) , f =>buss(0,3) ,g => buss(2,0),h => "0000" ,
 MXsel1 => Mxsel(2,6),op => op(2,3),mxSel2 => mxSel(2,7), clk =>
clk,R_en_a => R_en_a(2,3),  R_en_b => R_en_b(2,3),R_en_op =>
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R_en_op(2,3),R_en_o => R_en_o(2,3),
o => buss(2,3));


cu_30: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(2,0), B => buss(1,0), C => "0000", D =>
"0000",e =>buss(2,0) , f =>buss(1,0) ,g => "0000",h => "0000" ,
 MXsel1 => Mxsel(3,0),op => op(3,0),mxSel2 => mxSel(3,1), clk =>
clk,R_en_a => R_en_a(3,0),  R_en_b => R_en_b(3,0),R_en_op =>
R_en_op(3,0),R_en_o => R_en_o(3,0),
o => buss(3,0));

cu_31: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(2,1), B => buss(1,1), C => buss(3,0), D =>
"0000",
e =>buss(2,1) , f =>buss(1,1) ,g => buss(3,0),h => "0000" ,
 MXsel1 => Mxsel(3,2),op => op(3,1),mxSel2 => mxSel(3,3), clk =>
clk,R_en_a => R_en_a(3,1),  R_en_b => R_en_b(3,1),R_en_op =>
R_en_op(3,1),R_en_o => R_en_o(3,1),
o => buss(3,1));

cu_32: entity work.CU_With_Resistor (Behavioral)
port map( A => buss(2,2), B => buss(1,2), C => buss(3,0), D =>
"0000",
e =>buss(2,2) , f =>buss(1,2) ,g => buss(3,0),h => "0000" ,
 MXsel1 => Mxsel(3,4),op => op(3,2),mxSel2 => mxSel(3,5), clk =>
clk,R_en_a => R_en_a(3,2),  R_en_b => R_en_b(3,2),R_en_op =>
R_en_op(3,2),R_en_o => R_en_o(3,2),
o => buss(3,2));

cu_33: entity work.CU_With_Resistor (Behavioral)
port map(  A => buss(2,3), B => buss(1,3), C => buss(3,0),
D => "0000",e =>buss(2,3), f =>buss(1,3) ,g => buss(3,0),h =>
"0000" ,
 MXsel1 => Mxsel(3,6),op => op(3,3),mxSel2 => mxSel(3,7), clk =>
clk,R_en_a => R_en_a(3,3),  R_en_b => R_en_b(3,3),R_en_op =>
R_en_op(3,3),R_en_o => R_en_o(3,3),
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o => buss(3,3));


output <= buss;
end Behavioral;
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