EENG 5560 project Report

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Design

Block diagrams

Overall design

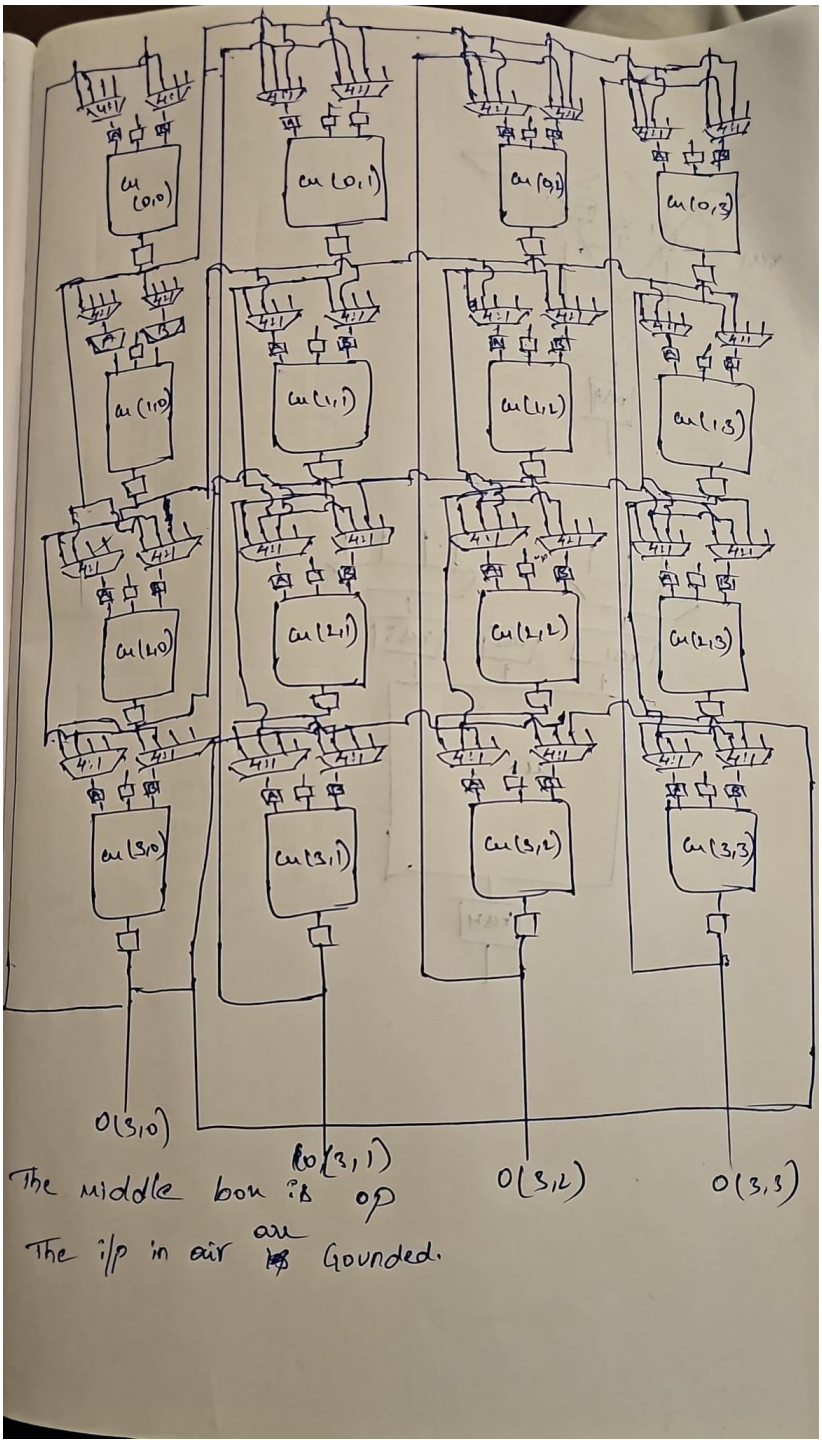


Figure 1

Overall component: top box

Parameters: do – data width (for inputs and outputs)

Input ports:

Port name	Bit width	Purpose
Input(2*4 array)	4	Data inputs
op	5	Selection line of cu
MxSel(4*8 array)	4	Selection line of mux
R_en_a,R_en_b,R_en_op,R_en_o(4*4 array)	4	enable for of registor

Output ports:

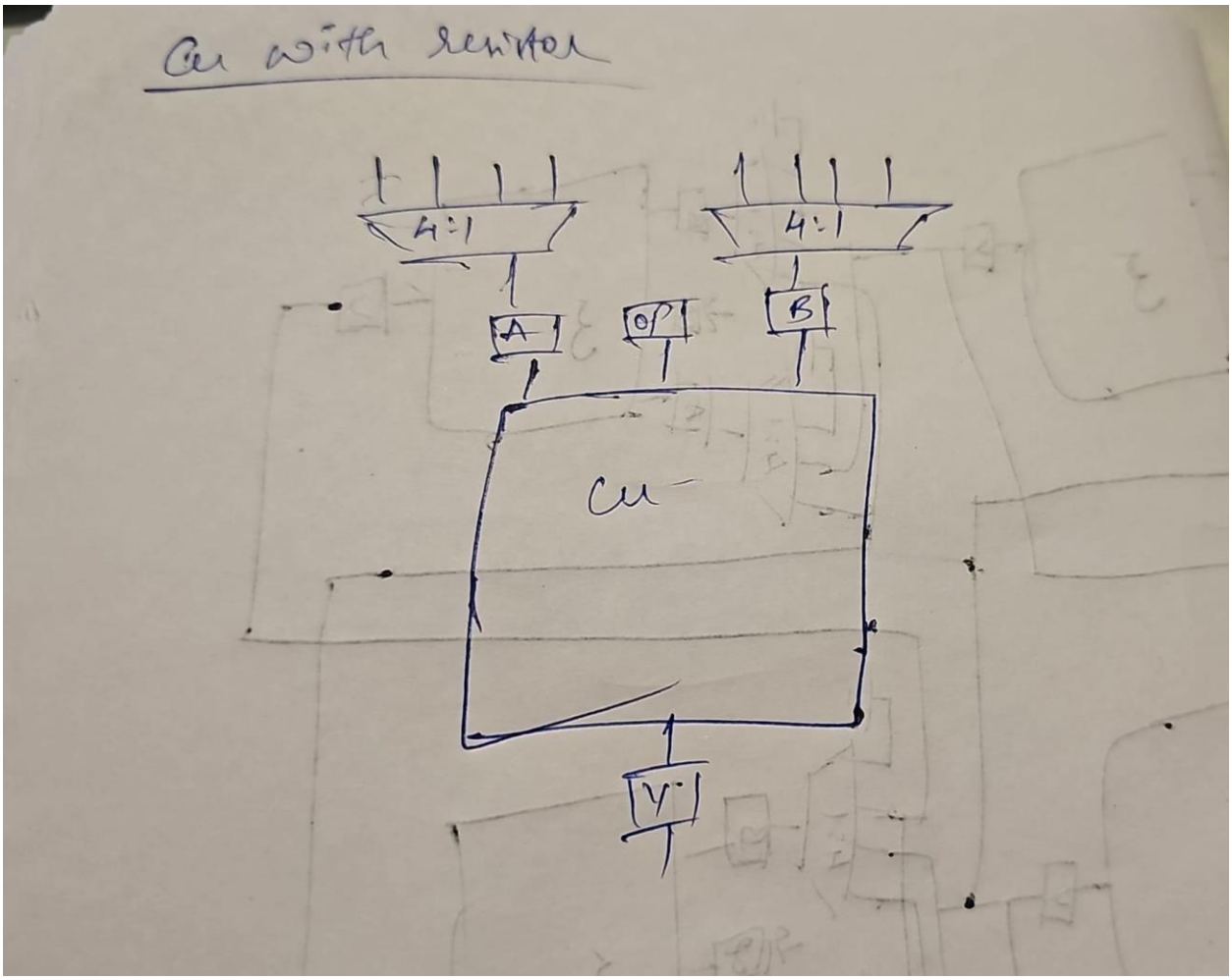
Port name	Bit width	Purpose
Output(4*4 array)	d_w = 4	Data output

Necessary intermediate signals:

Port name	Bit width	Purpose
Buss(4*4 array)	d_w = 4	Outputs of previous cu's, inputs to next cu's

Subcomponents:

Cu with resistor:



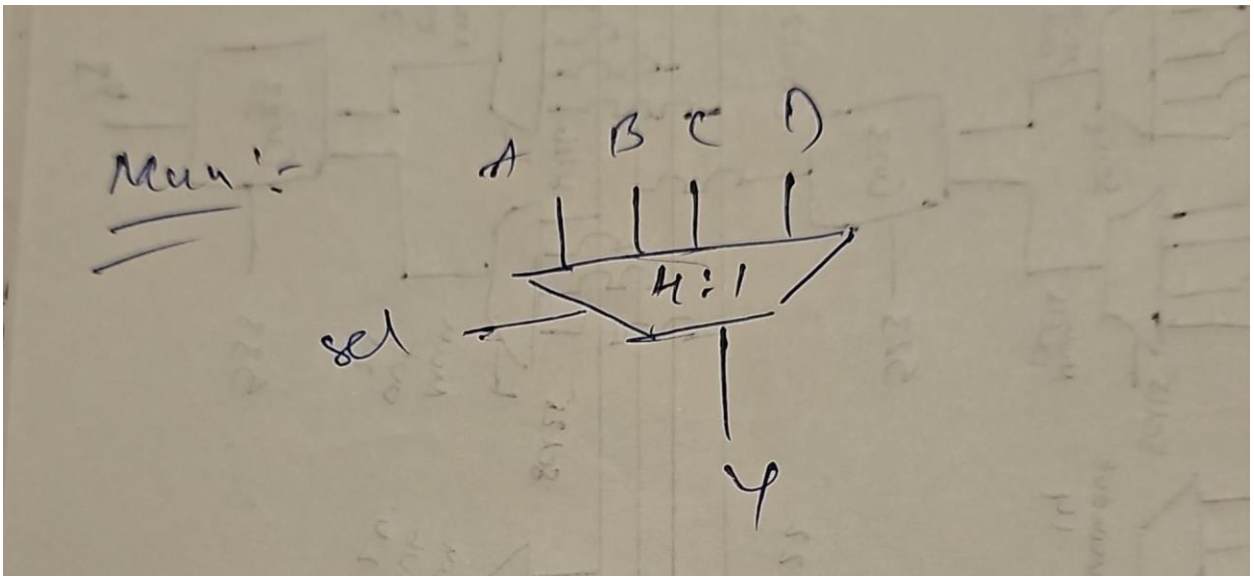
Input ports:

Port name	Bit width	Purpose
I0, I1, I2, I3	4	Data inputs
Sel	5	Select line, selects which of the 4 data inputs to send to data output
MXsel	2	Mux selection line
R_en	1	Enable signal

Output ports:

Port name	Bit width	Purpose
y	4	Data output

Mux :



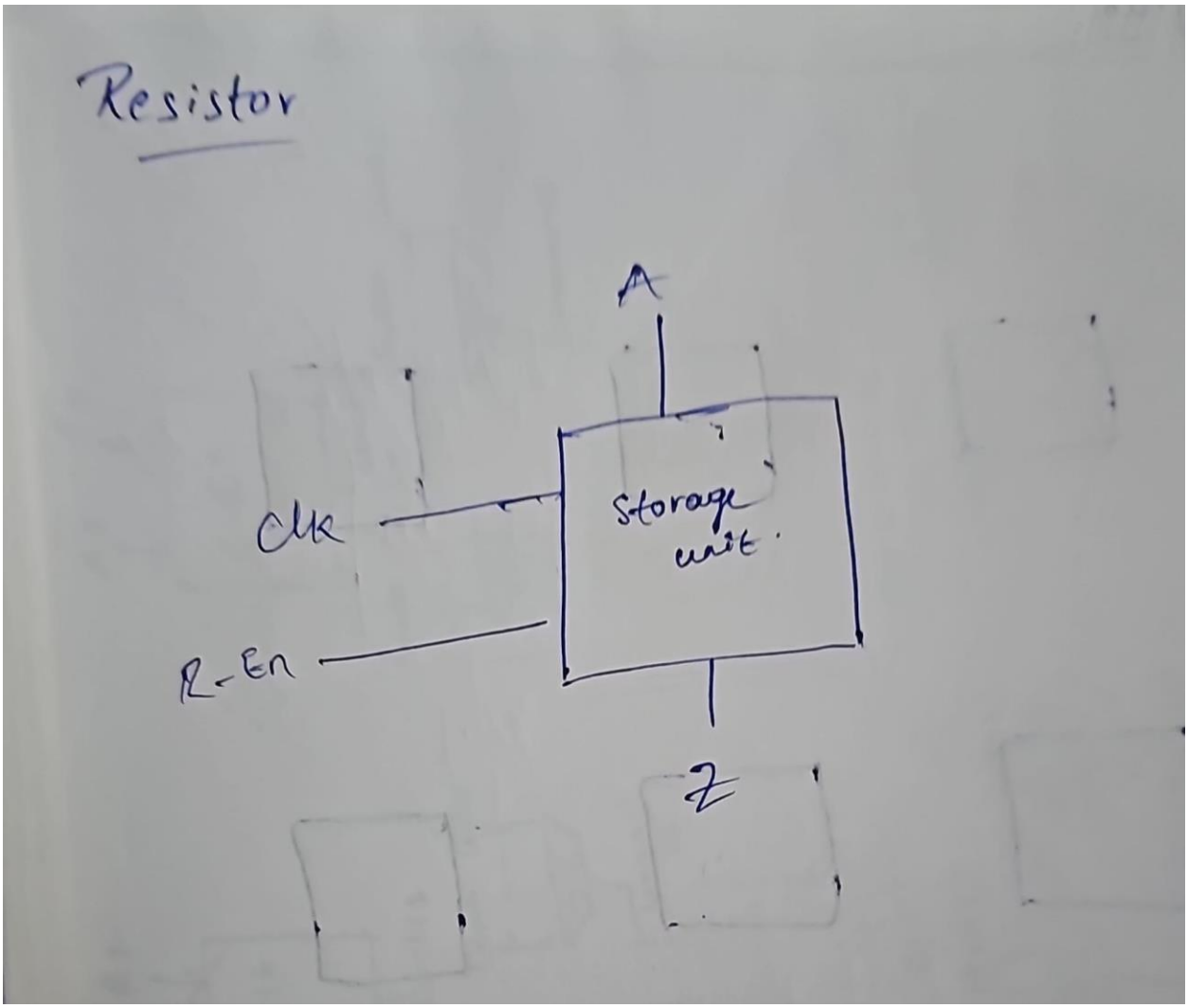
Input ports:

Port name	Bit width	Purpose
A,b,c,d	4	Data inputs
Sel	1	Select line, selects which of the 2 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
Y	4	Data output

Resistor:



Input ports:

Port name	Bit width	Purpose
A	Parameterized	Data inputs
clk	1	Clock input
R-En	1	Enable input

Output ports:

Port name	Bit width	Purpose
z	parameterized	Data output

Functionality

Design explanation

Functionality

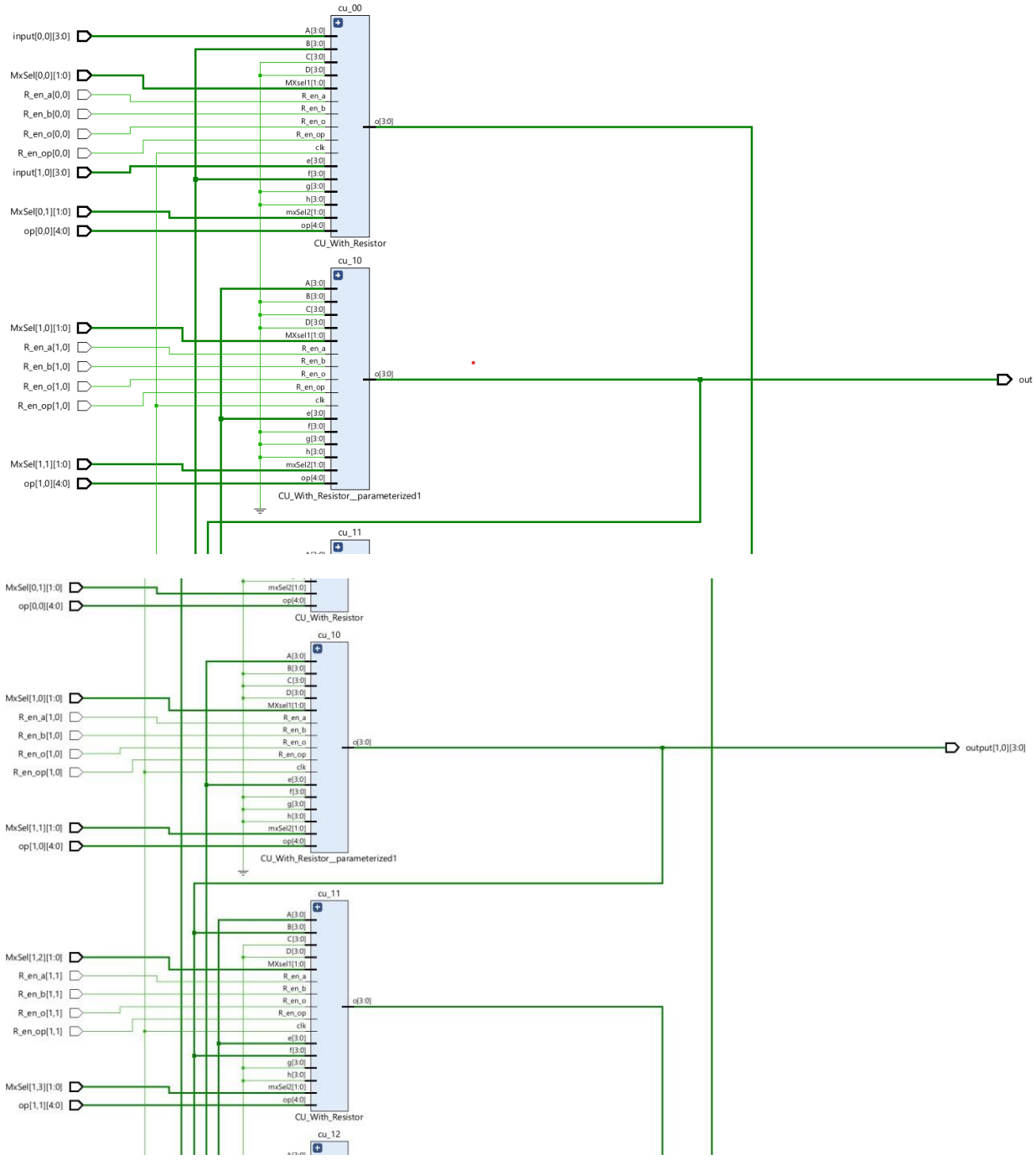
I have created 4 by 4 fabric design where we can perform 4 by 8 fabric logic. Here basically the top box is performing the 2 runs in the circuit, where in the 1st run the external are given as input to the circuit and the output of the run is given as the input to the circuit using intermediate signals and the data sent to the circuit then we take the output in the 2nd run. In the fabric we are for the 1st and 2nd cycle the inputs are manipulated by muxes and the storage units. We have used array for the input and output and intermediate data. And we parameterized the circuit. I have created 2d and 1d dynamical array for std logic and logic vectors.

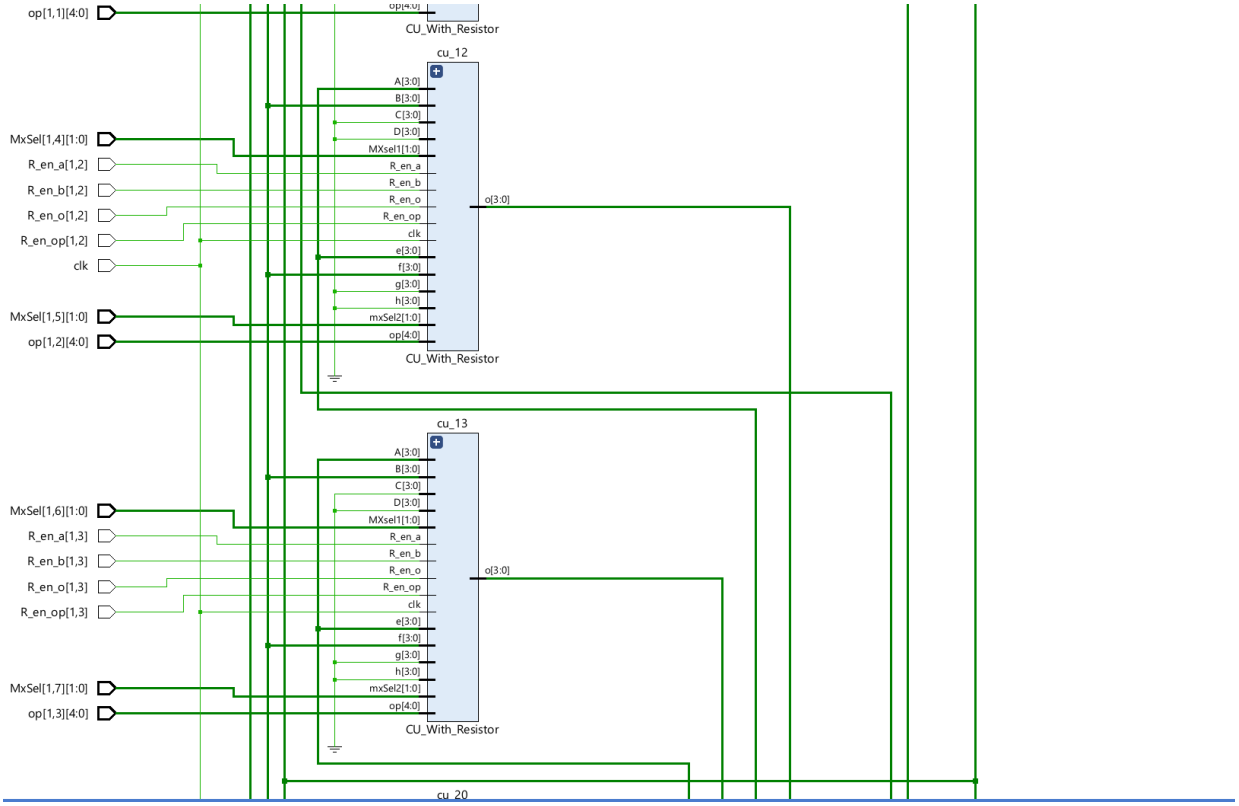
Design Choices

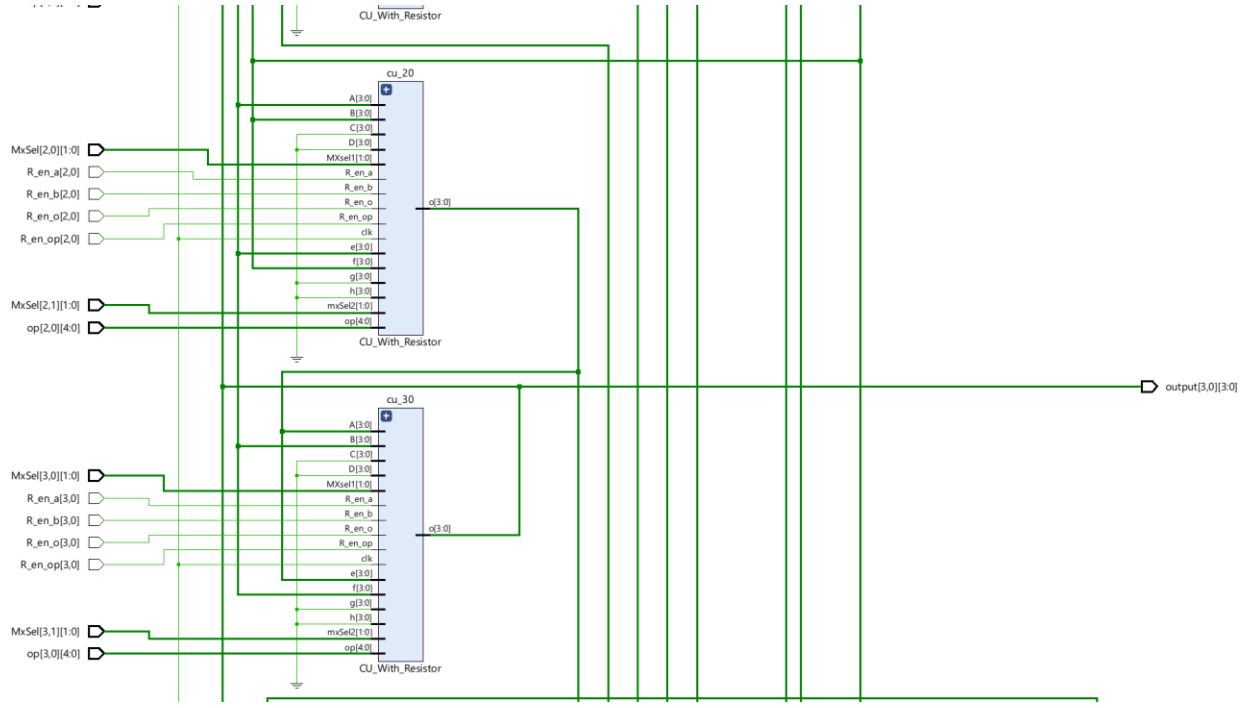
We have 4 by 4 fabric to perform 8 by 4 circuit. For the looping i have used 4 to 1 muxes to so i can select external input for the 1st run and for the 2nd run input i give output of the 1st run. After selecting the data from the muxes we are using storage units to read and write the functions. Then the data has sent to the cu and the output of the cu is stored in the storage unit..the data will send to the array by intermideate signal and it's continues to next cu . then i can store the 1st run data in the output storage unit the then i can perform second run and and i can overwrite the data in the output storage unit then i can take the output.

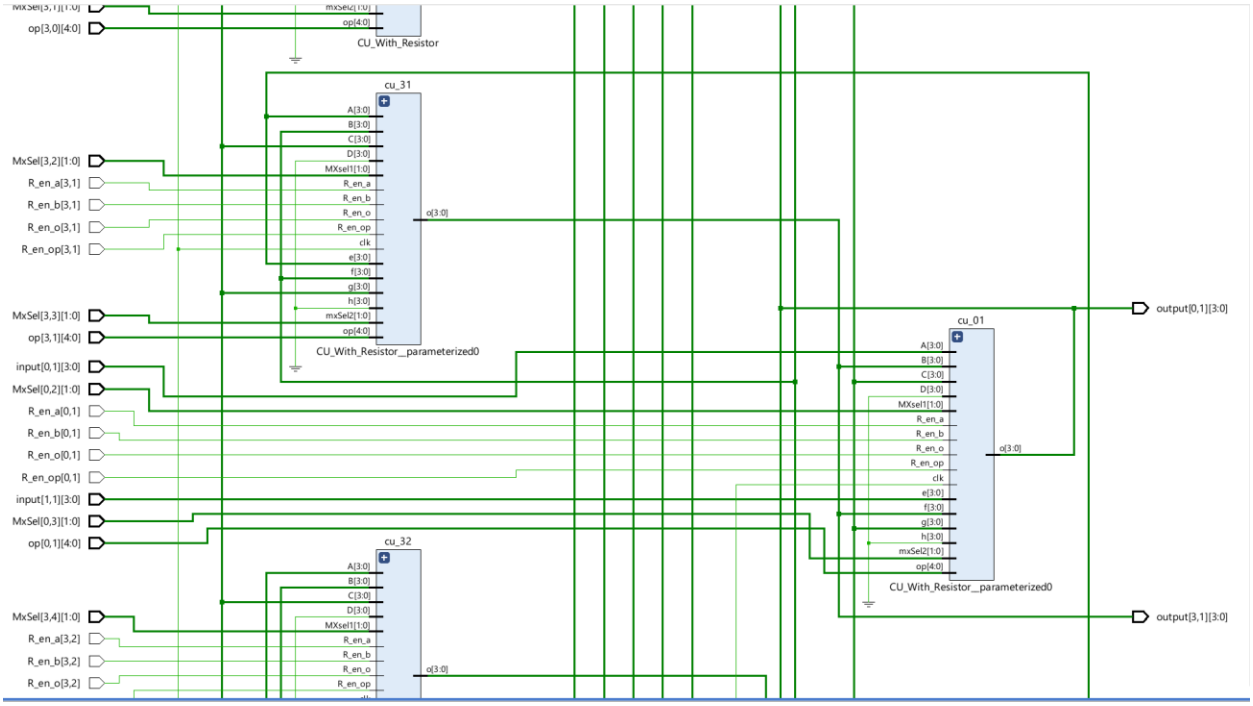
Results

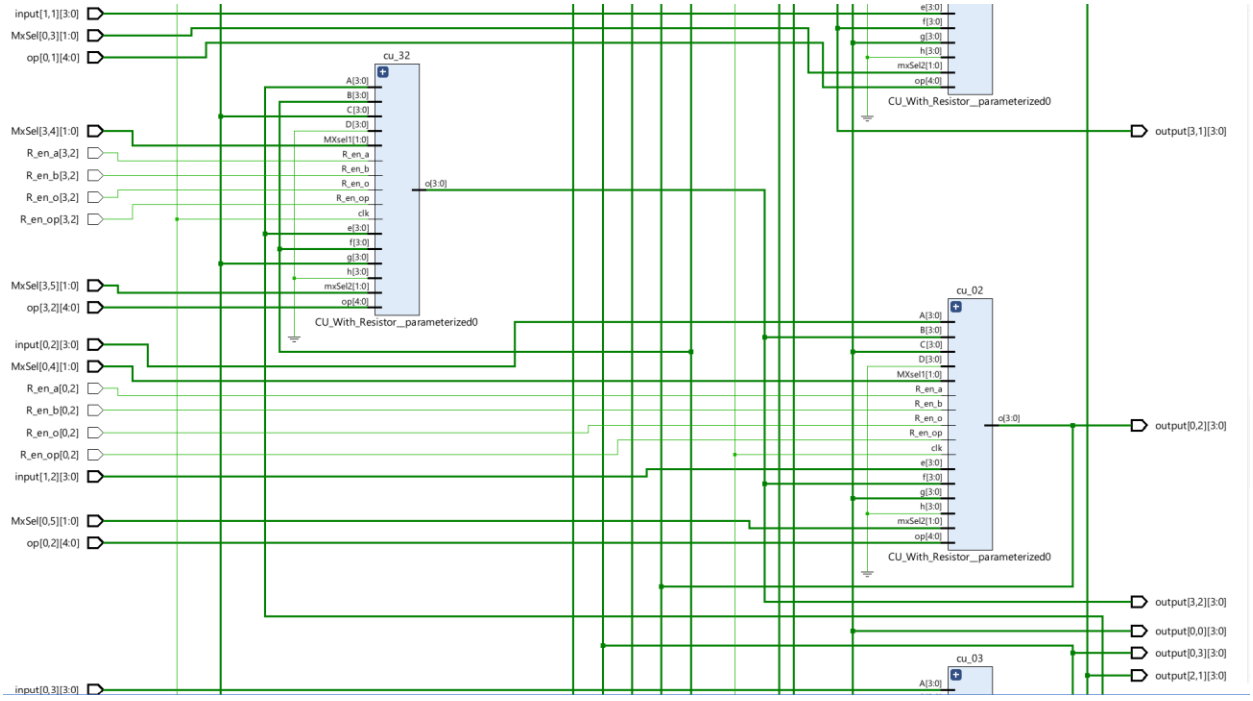
Generated Schematics:

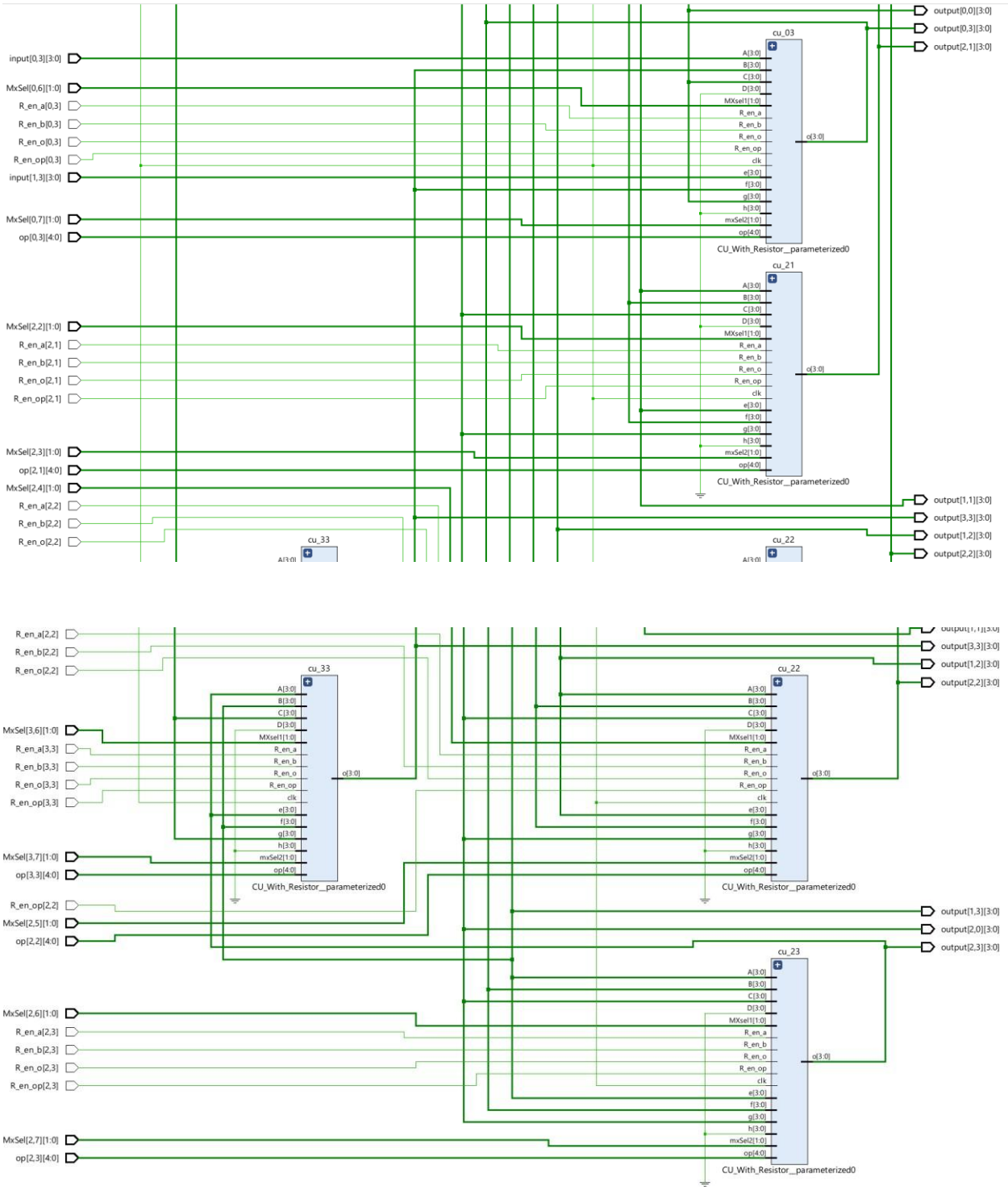

cu_00
input[0,0][3:0]
MxSel[0,0][1:0]
R_en_a[0,0]
R_en_b[0,0]
R_en_o[0,0]
R_en_op[0,0]
input[1,0][3:0]
MxSel[0,1][1:0]
op[0,0][4:0]
A[3:0]
B[3:0]
C[3:0]
D[3:0]
MXsel1[1:0]
R_en_a
R_en_b
R_en_o
R_en_op
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
CU_With_Resistor
cu_10
MxSel[1,0][1:0]
R_en_a[1,0]
R_en_b[1,0]
R_en_o[1,0]
R_en_op[1,0]
MxSel[1,1][1:0]
op[1,0][4:0]
CU_With_Resistor__parameterized1
out
cu_11
MxSel[0,1][1:0]
op[0,0][4:0]
CU_With_Resistor
cu_10
MxSel[1,0][1:0]
R_en_a[1,0]
R_en_b[1,0]
R_en_o[1,0]
R_en_op[1,0]
MxSel[1,1][1:0]
op[1,0][4:0]
CU_With_Resistor__parameterized1
output[1,0][3:0]
cu_11
MxSel[1,2][1:0]
R_en_a[1,1]
R_en_b[1,1]
R_en_o[1,1]
R_en_op[1,1]
MxSel[1,3][1:0]
op[1,1][4:0]
CU_With_Resistor
cu_12


op[1,1][4:0]
CU_With_Resistor
cu_12
A[3:0]
B[3:0]
C[3:0]
D[3:0]
MXsel1[1:0]
R_en_a
R_en_b
R_en_o
R_en_op
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
MxSel[1,4][1:0]
R_en_a[1,2]
R_en_b[1,2]
R_en_o[1,2]
R_en_op[1,2]
clk
MxSel[1,5][1:0]
op[1,2][4:0]
CU_With_Resistor
cu_13
MxSel[1,6][1:0]
R_en_a[1,3]
R_en_b[1,3]
R_en_o[1,3]
R_en_op[1,3]
MxSel[1,7][1:0]
op[1,3][4:0]
CU_With_Resistor
cu_20


CU_With_Resistor
cu_20
A[3:0]
B[3:0]
C[3:0]
D[3:0]
MXsel1[1:0]
R_en_a
R_en_b
R_en_o
R_en_op
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
MxSel[2,0][1:0]
R_en_a[2,0]
R_en_b[2,0]
R_en_o[2,0]
R_en_op[2,0]
MxSel[2,1][1:0]
op[2,0][4:0]
CU_With_Resistor
output[3,0][3:0]
cu_30
MxSel[3,0][1:0]
R_en_a[3,0]
R_en_b[3,0]
R_en_o[3,0]
R_en_op[3,0]
MxSel[3,1][1:0]
op[3,0][4:0]
CU_With_Resistor

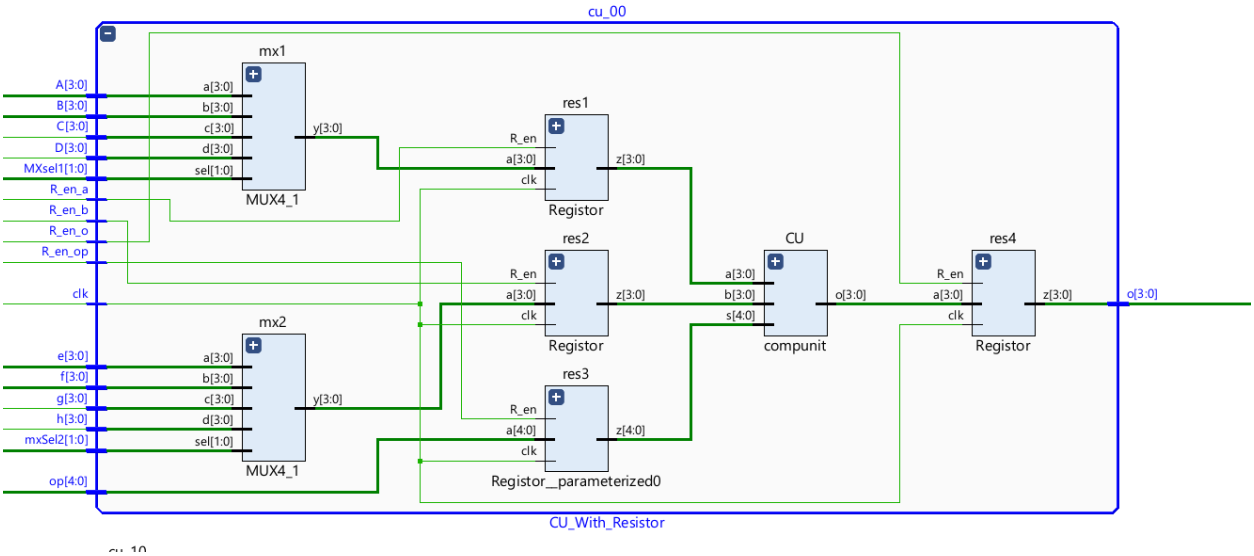

op[3,0][4:0]
CU_With_Resistor
cu_31
A[3:0]
B[3:0]
C[3:0]
D[3:0]
MXsel1[1:0]
R_en_a
R_en_b
R_en_o
R_en_op
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
CU_With_Resistor__parameterized0
MxSel[3,2][1:0]
R_en_a[3,1]
R_en_b[3,1]
R_en_o[3,1]
R_en_op[3,1]
MxSel[3,3][1:0]
op[3,1][4:0]
input[0,1][3:0]
MxSel[0,2][1:0]
R_en_a[0,1]
R_en_b[0,1]
R_en_o[0,1]
R_en_op[0,1]
input[1,1][3:0]
MxSel[0,3][1:0]
op[0,1][4:0]
cu_32
MxSel[3,4][1:0]
R_en_a[3,2]
R_en_b[3,2]
R_en_o[3,2]
cu_01
output[0,1][3:0]
output[3,1][3:0]


input[1,1][3:0]
MxSel[0,3][1:0]
op[0,1][4:0]
cu_32
A[3:0]
B[3:0]
C[3:0]
D[3:0]
MXsel1[1:0]
R_en_a
R_en_b
R_en_o
R_en_op
clk
e[3:0]
f[3:0]
g[3:0]
h[3:0]
mxSel2[1:0]
op[4:0]
o[3:0]
CU_With_Resistor__parameterized0
MxSel[3,4][1:0]
R_en_a[3,2]
R_en_b[3,2]
R_en_o[3,2]
R_en_op[3,2]
MxSel[3,5][1:0]
op[3,2][4:0]
input[0,2][3:0]
MxSel[0,4][1:0]
R_en_a[0,2]
R_en_b[0,2]
R_en_o[0,2]
R_en_op[0,2]
input[1,2][3:0]
MxSel[0,5][1:0]
op[0,2][4:0]
input[0,3][3:0]
output[3,1][3:0]
cu_02
output[0,2][3:0]
output[3,2][3:0]
output[0,0][3:0]
output[0,3][3:0]
output[2,1][3:0]
cu_03



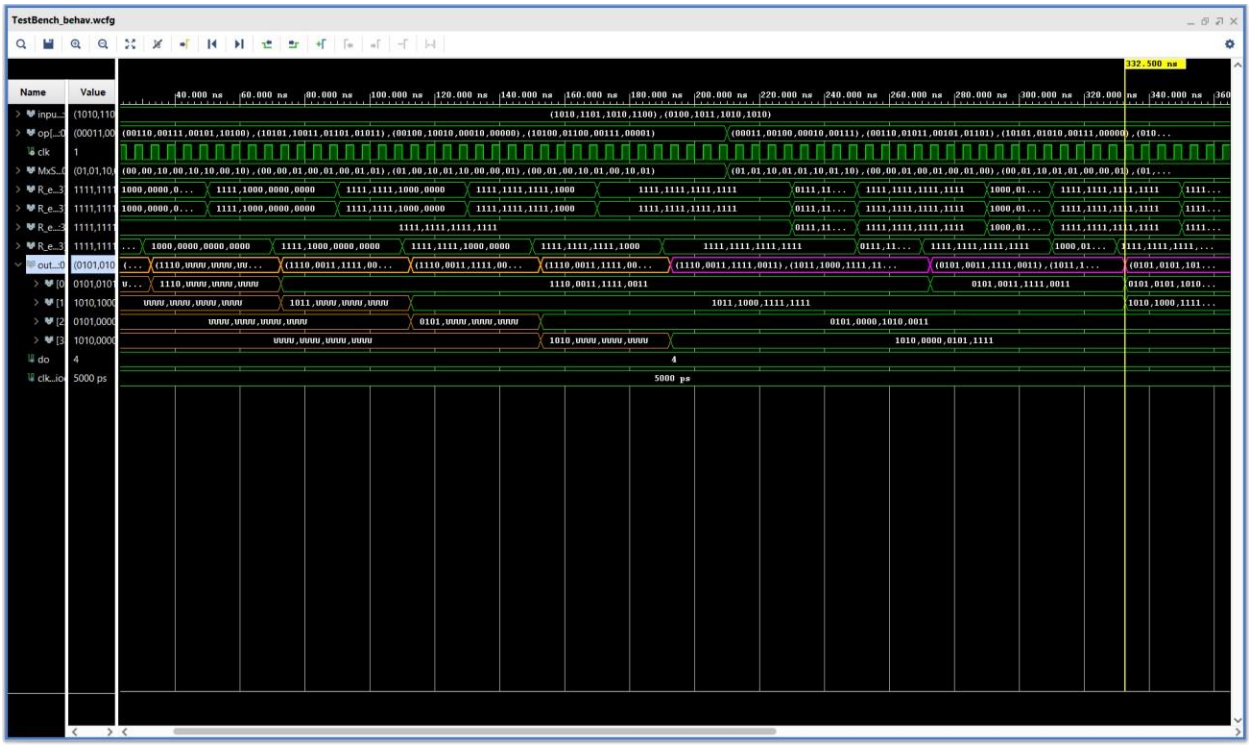
Here We have created 4 by 4 fabric where cu0,0 to cu3,3 is “cu with register” box. This cu wit register contains has computational unit, 4to 1 mux and storage unit (register)as shown below. The inputs are given to cu 0,0 to cu 0.3. and the output are taken from cu 3,0 to cu 3,3. And the runs the data manipulated by muxes and storage units.

Cu with resistor:



Waveforms:

1st cycle output:



2nd cycle output:

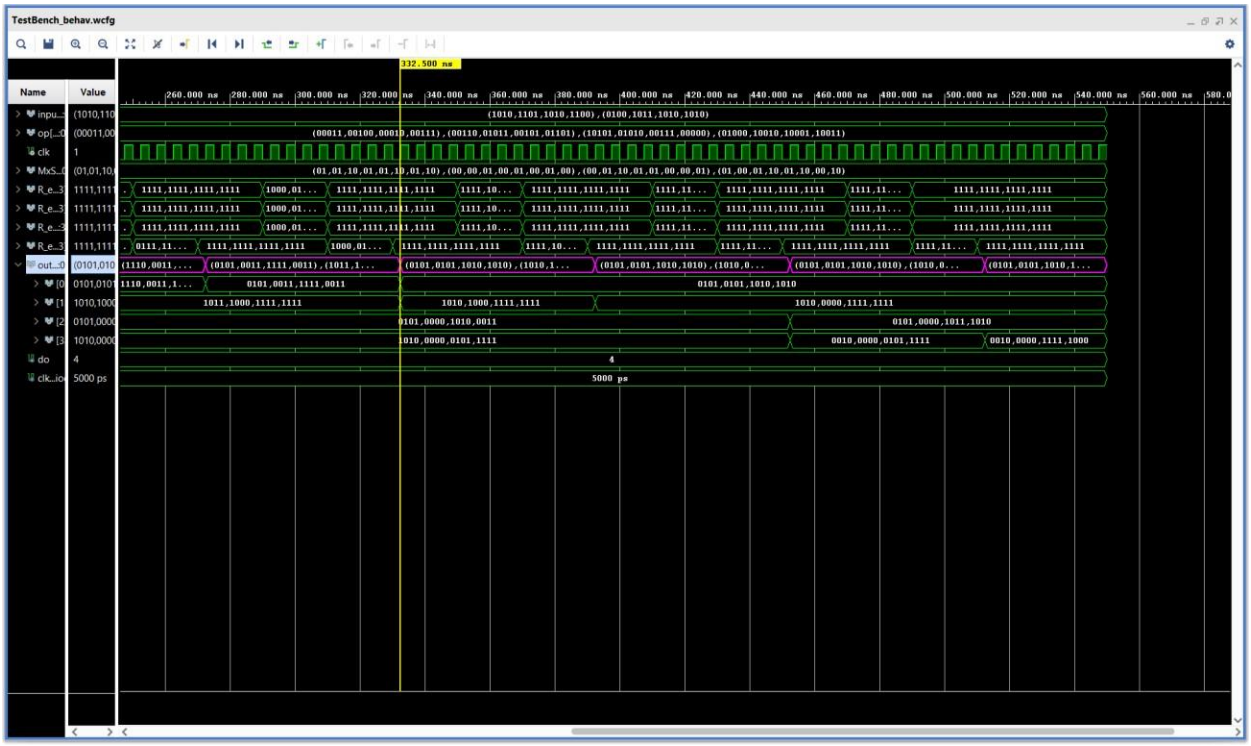


Figure 2 – Overall Waveforms

Table/Calculations

Overall Design

(*0ns to 275.5ns*):

cu	Source A(port name)	Source A	Source B(port name)	Source B	Operation	Calcuclated output	Waveform output	Matched
cu0,0	External	1010	External	0100	ADD	1110	1110	yes
cu0,1	CU(0,0)	1110	External	1011	SUB	0011	0011	yes
cu 0,2	CU(0,0)	1110	CU(0,0)	1110	XNOR	1111	1111	yes
cu 0,3	External	1100	CU(0,0)	1110	ROR	0011	0011	yes
cu1,0	CU(0,0)	1100	CU(0,0)	1110	ROL	1011	1011	yes
cu 1,1	CU(1,0)	1011	CU(0,1)	0011	LSL	1000	1000	yes
cu 1,2	CU(1,0)	1011	CU(0,2)	1111	LTE	1111	1111	yes
cu 1,3	CU(1,0)	1011	CU(1,0)	1011	EQ	1111	1111	yes
cu 2,0	CU(0,0)	1110	CU(1,0)	1011	XOR	0101	0101	yes
cu 2,1	CU(2,0)	0101	CU(0,1)	0011	LSR	0000	0000	yes
cu 2,2	CU(2,0)	0101	CU(1,2)	1111	NAND	1010	1010	yes
cu 2,3	CU(1,3)	1111	CU(0,3)	0011	AND	0011	0011	yes
cu 3,0	CU(2,0)	0101	CU(1,0)	1011	ROR	1010	1010	yes
cu 3,1	CU(2,1)	0000	CU(3,0)	1010	GTE	0000	0000	yes
cu 3,2	CU(1,2)	1111	CU(2,2)	1010	SUB	0101	0101	yes
cu 3,3	CU(3,0)	1010	CU(1,3)	1111	OR	1111	1111	yes

Test Case # (*275.5ns to 550ns*):

cu	Source A(port name)	Source A	Source B(port name)	Source B	Operation	Calcuclated output	Waveform output	Matched
CU(0,0)	CU(3,0)	1010	CU(3,0)	1010	NOR	0101	0101	yes
CU(0,1)	CU(0,0)	0101	CU(3,1)	0000	XOR	0101	0101	yes
CU(0,2)	CU(3,2)	0101	CU(0,0)	0101	NAND	1010	1010	yes
CU(0,3)	CU(3,3)	1111	CU(0,0)	0101	SUB	1010	1010	yes
CU(1,0)	CU(0,0)	0101	CU(0,0)	0101	ADD	1010	1010	yes
CU(1,1)	CU(1,0)	1010	CU(0,1)	0101	EQ	0000	0000	yes
CU(1,2)	CU(1,0)	1010	CU(0,2)	1010	XNOR	1111	1111	yes
CU(1,3)	CU(1,0)	1010	CU(0,3)	1010	LTE	1111	1111	yes
CU(2,0)	CU(1,0)	1010	CU(0,0)	0101	ROL	0101	0101	yes
CU(2,1)	CU(2,0)	0101	CU(0,1)	0101	LT	0000	0000	yes
CU(2,2)	CU(0,2)	1010	CU(1,2)	1111	SUB	1011	1011	yes
CU(2,3)	CU(1,3)	1111	CU(0,3)	1010	AND	1010	1010	yes
CU(3,0)	CU(1,0)	1010	CU(2,0)	0101	MULT	0010	0010	yes
CU(3,1)	CU(1,1)	0000	CU(3,0)	0010	LSR	0000	0000	yes
CU(3,2)	CU(1,2)	1111	CU(3,0)	0010	ASR	1111	1111	yes
CU(3,3)	CU(2,3)	1010	CU(3,0)	0010	LSL	1000	1000	yes

The calculated output and wave form output are matched.

Note:

1.the number of clock cycles for 1st run is 77 .and the number of clock cycles for second run is 205.i said wrong answer in demo please consider partial credit for this one.