```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 01.04.2024 21:49:08
-- Design Name:
-- Module Name: Custom_Pack - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

package custom_pack is
type gate_oper is (ANDo, ORo, XORo, XNORo, NORo, NANDo);
```

```
type gate_arr_1d is array(natural range<>) of gate_oper;
type gate_arr_2d is array(natural range<>) of gate_arr_1d;

subtype dim1 is std_logic_vector;
type arr_1d is array(natural range<>) of dim1;
type arr_2d is array(natural range<>,natural range<>) of dim1;

end package custom_pack;
```