EENG HW 6 Report

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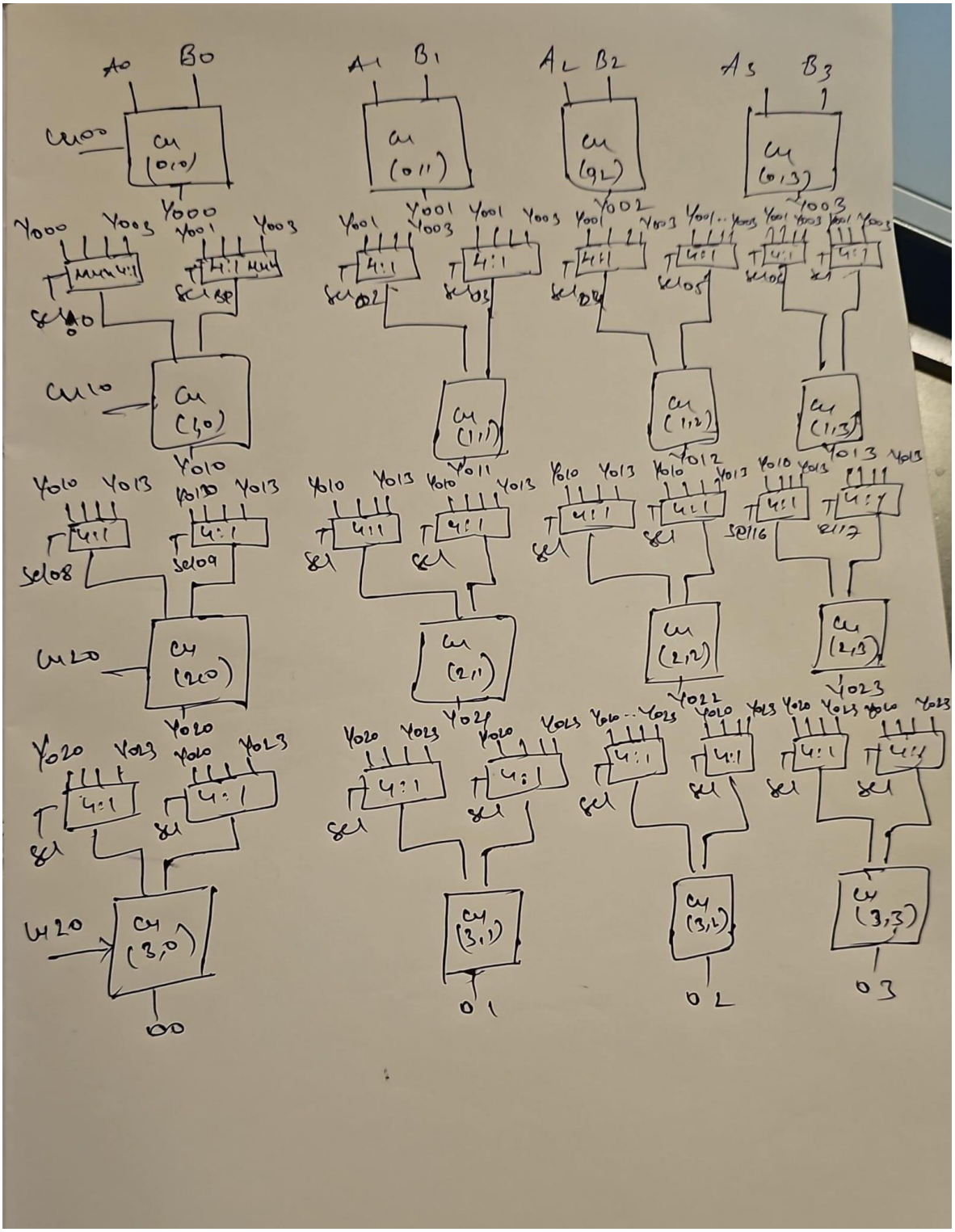
Block diagram:



Overall component: top box

Parameters: d_w – data width (for inputs and outputs)

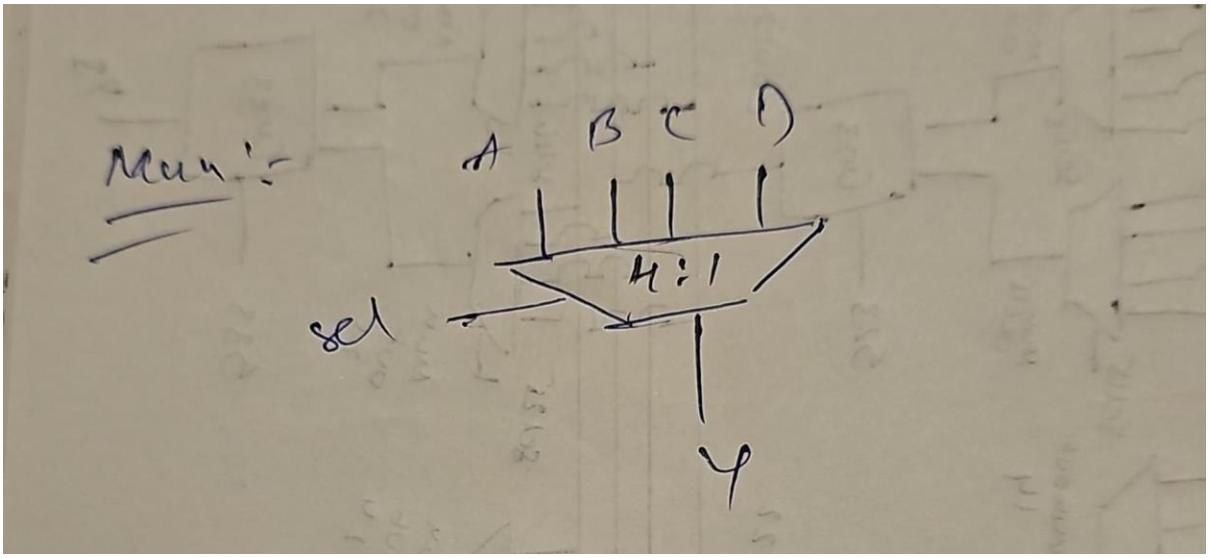
Input ports:

Port name	Bit width	Purpose
A0,a1,a2,a3,b0,b1,b2,b3	d_w = 4	Data inputs
Cu00,cu01,cu02,cu03,cu04,….. Upto cu23	3	Selection lines for cu

Output ports:

Port name	Bit width	Purpose
O0,o1,o2,o3	d_w = 4	Data output

Subcomponents



Subcomponent: 4x1 mux

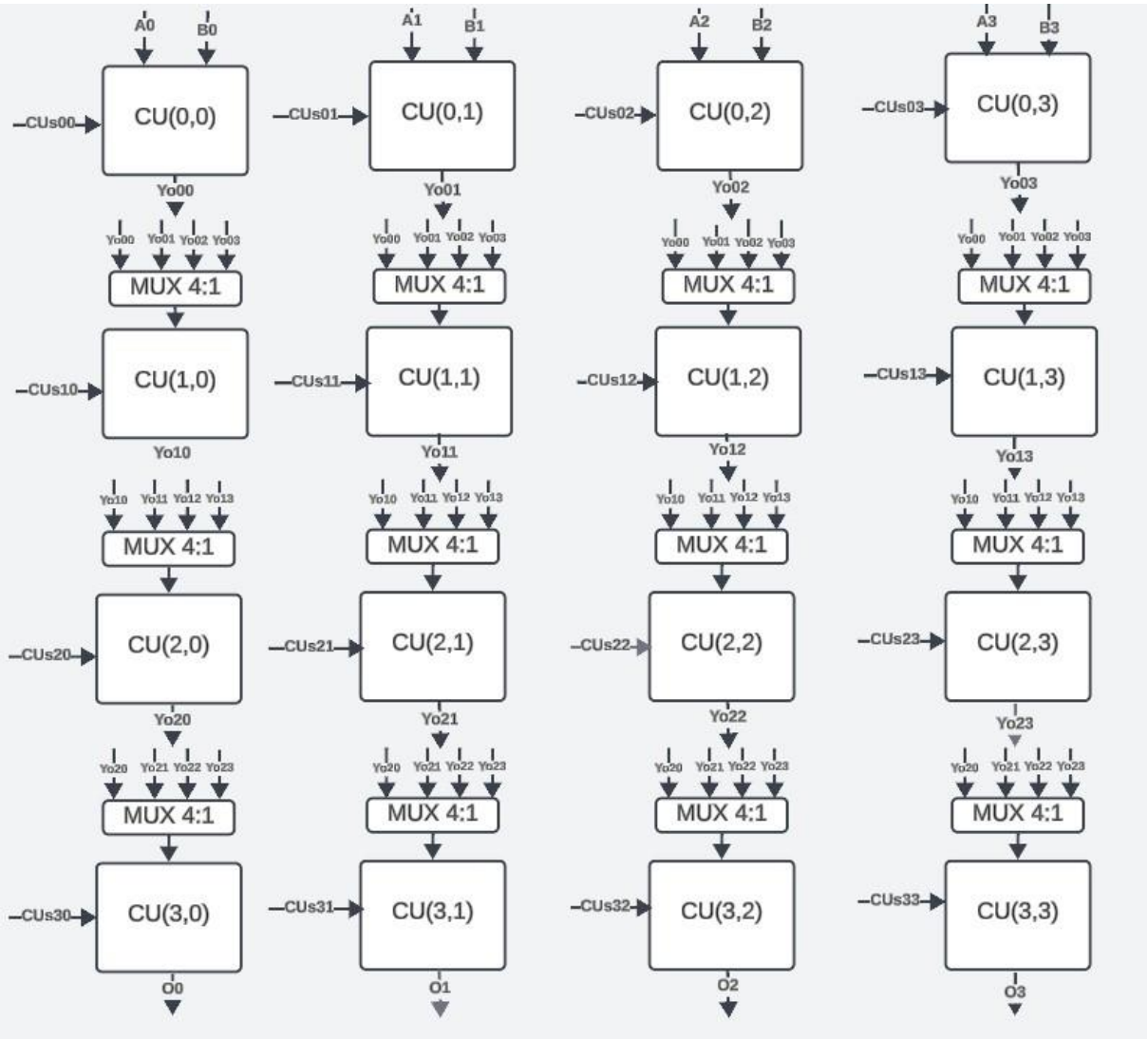
Input ports:

Port name	Bit width	Purpose
A,b,c,d	d_w = 4	Data inputs
Sel	1	Select line, selects which of the 2 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
Y	d_w = 4	Data output

Design Explanation:



From the above diagram the interconnects are taken same 4*1 Multiplexer (MUX) for the input A and B. So, I have showed only 1 MUX as interconnect for each CU.

1-dimensional and 2-dimensional arrays are used to develop the overall fabric.

Row 0 to 3 and Columns 0 to 3 are used to generate 16 CUs (Computational Unit) with 4*4 matrix and the inputs and outputs are taken as per the following.

Inputs:

A, B are 1-dimensional array from 0 to 3 which are external inputs given to the row 0 CUs correspondingly. Which are capable of 4-bit.

CUs is a 2-dimensional array which can generate rows from 0 to 3 and columns from 0 to 3 of 5-bit operation selection input is given each CU accordingly.

SELA and SELB are 2-dimensional array which can generate rows from 0 to 2 and columns from 0 to 2 of 2-bit selection input for 4:1 MUX which are used as interconnects to the CUs

from row 1 to 3. SELA is used for MUXes to select which output of the above row CUs that feeds input to A for each CU. SELB is used for MUXes to select which output of the above row CUs that feeds input to B for each CU.

Outputs:

O is a 1-dimensional array from 0 to 3 which are the external outputs for the overall design.

Interconnects:

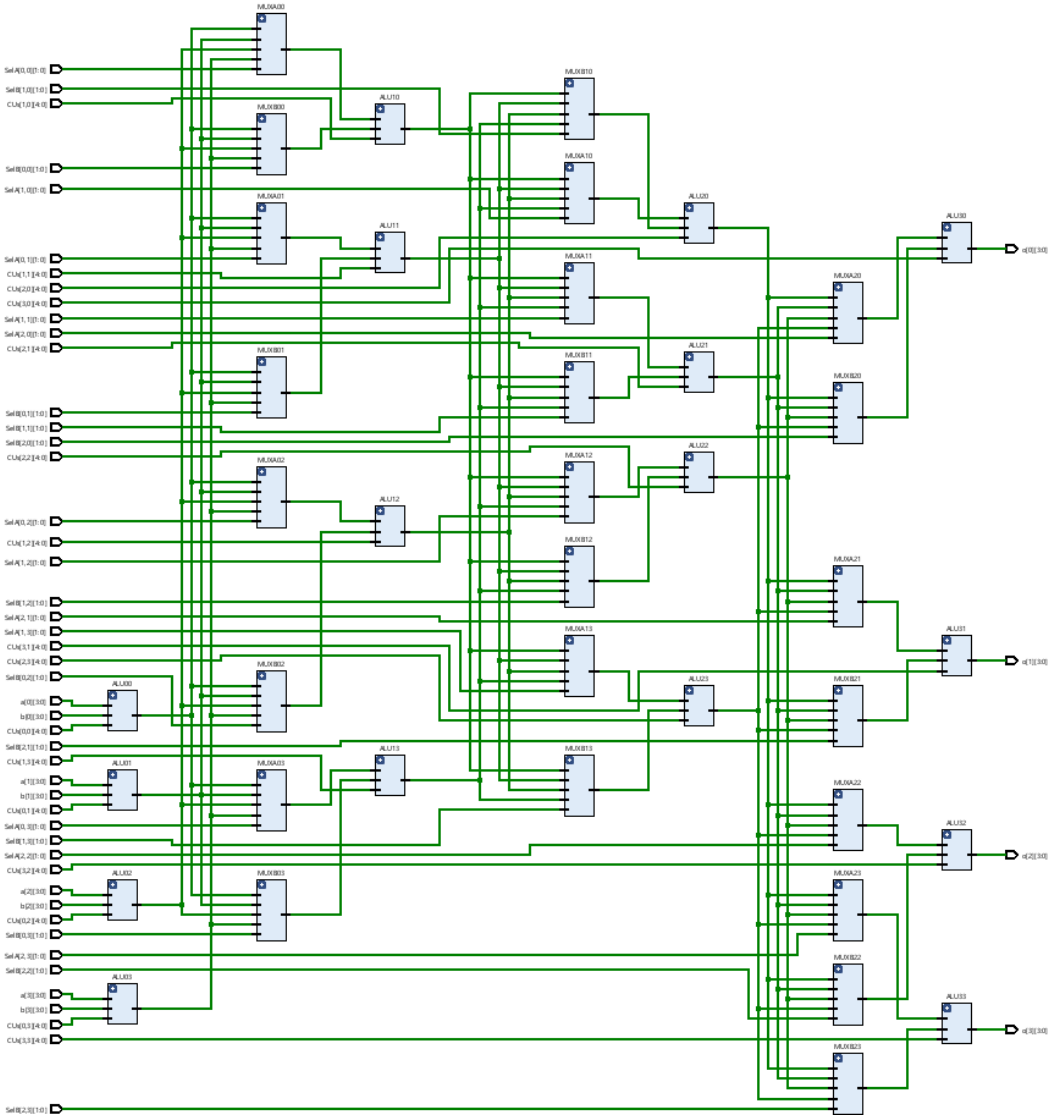
Yo is a 2-dimensional array which can generate rows from 0 to 2 and columns from 0 to 2. It is a 4-bit output from CU of row 1 and 2.

MAo and MBo are 2-dimensional array which can generate rows from 0 to 2 and columns from 0 to 2. It is a 4-bit output from each MUX. And given MAo to the A input of CU and MBo to the B input of CU.

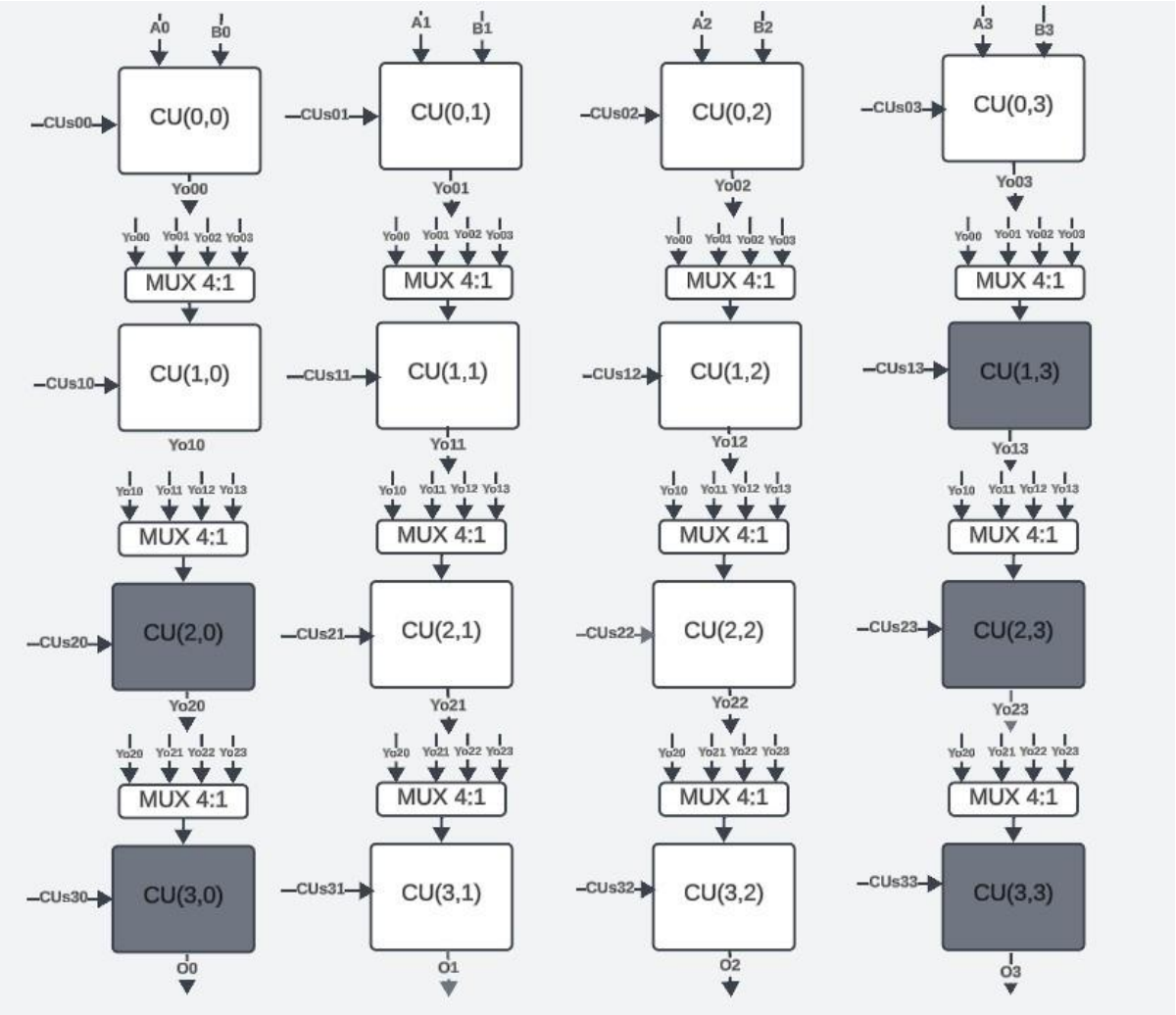
Arthematic Logic Unit:

S.No:	OP Code(CUs)	Operation
0	00000	No Operation (NO OP)
1	00001	AND
2	00010	OR
3	00011	NAND
4	00100	NOR
5	00101	XOR
6	00110	XNOR
7	00111	Addition (ADD)
8	01000	Subtraction (SUB)
9	01001	Multiplication (MUL)
10	01010	Greater Than (GT)
11	01011	Less Than (LT)
12	01100	Equal To (ET)
13	01101	Greater Than or Equal To (GTE)
14	01110	Less Than or Equal To (LTE)
15	01111	Not Equal To (NET)
16	10000	Arithmetic Shift Left (ASL)
17	10001	Arithmetic Shift Right (ASR)
18	10010	Rotate Shift Left (ROL)
19	10011	Rotate Shift Right (ROR)
20	10100	Logical Shift Left (LSL)
21	10101	Logical Shift Right (LSR)
22	10110	PASS A
23	10111	PASS B
24	11000-11111	00000

Schematic:



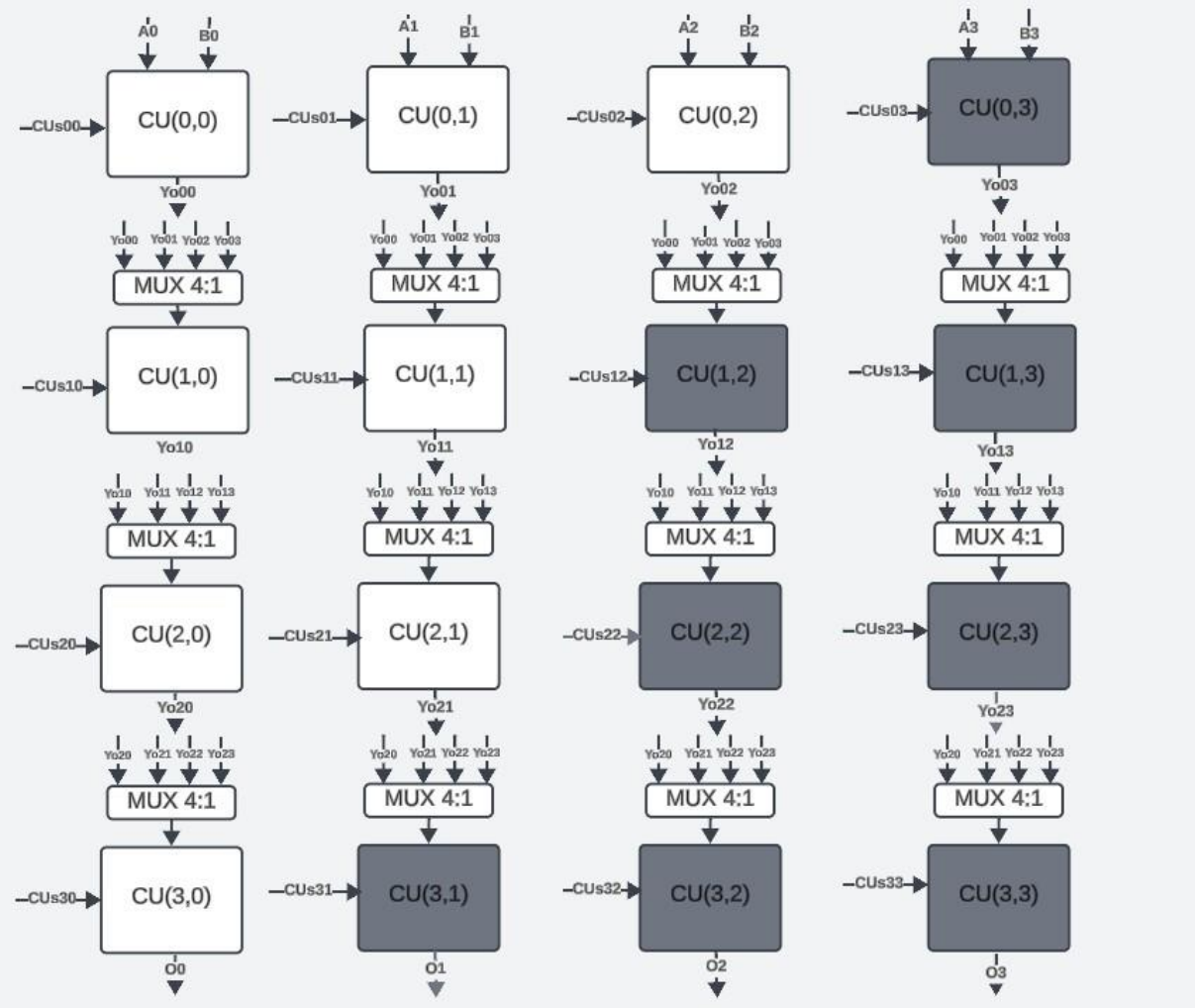
Case 1:



CU	Input A	Input B	Operation	Output
CU(0,0)	1001	0011	ADD	1100
CU(0,1)	1111	0110	SUB	1001
CU(0,2)	0111	0010	MULT	1110
CU(0,3)	1101	0010	LSL	0100
CU(1,0)	CU(0,2) 1110	CU(0,3) 0100	ROL	1110
CU(1,1)	CU(0,0) 1100	CU(0,2) 1110	XOR	0010
CU(1,2)	CU(0,1) 1001	CU(0,3) 0100	NAND	1111
CU(2,1)	CU(1,0) 1110	CU(1,1) 0010	GT	1111
CU(2,2)	CU(1,1) 0010	CU(1,2) 1111	OR	1111
CU(3,1)	CU(2,1) 1111	CU(2,1) 1111	GT	1111
CU(3,2)	CU(2,2) 1111	CU(2,2) 1111	OR	1111

CU(1,3), CU(2,0), CU(2,3), CU(3,0), and CU(3,3) are not used for simulating the DFG1. So, OP Code was 00000 No Operation was done by all the mentioned CUs.

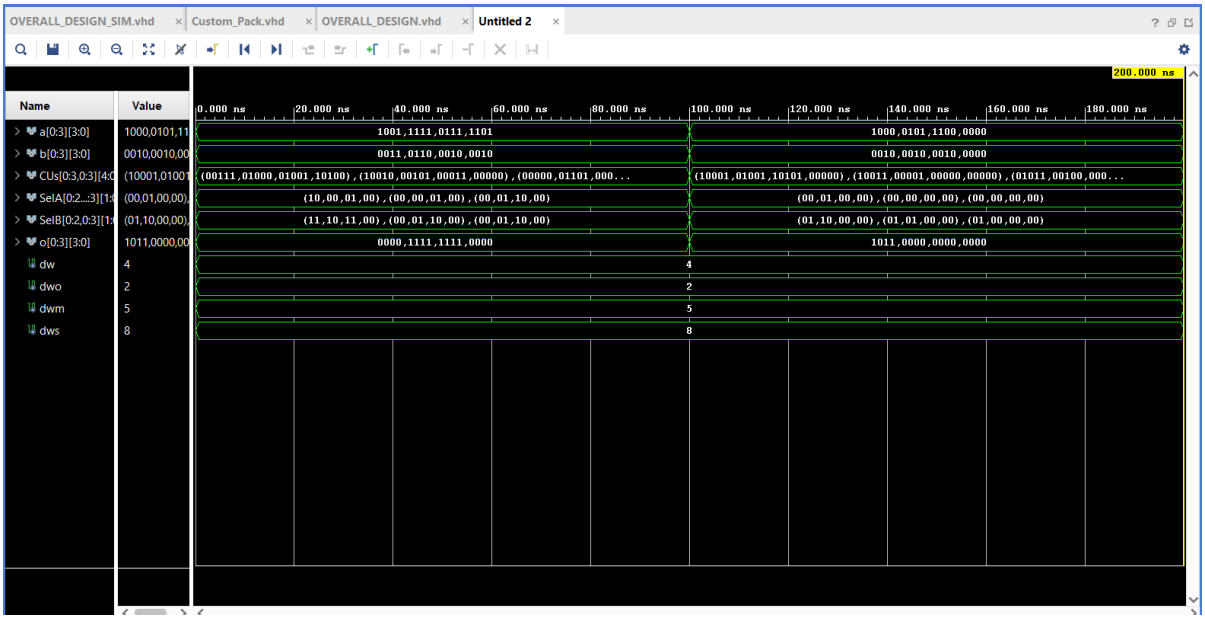
Case 2:



CU	Input A	Input B	Operation	Output
CU(0,0)	1000	0010	ASR	1110
CU(0,1)	0101	0010	MULT	1010
CU(0,2)	1100	0010	LSR	0011
CU(1,0)	CU(0,0) 1110	CU(0,1) 1010	ROR	1011
CU(1,1)	CU(0,1) 1010	CU(0,2) 0011	AND	0010
CU(2,0)	CU(1,0) 1011	CU(1,1) 0010	LT	0000
CU(2,1)	CU(1,0) 1011	CU(1,1) 0010	NOR	0100
CU(3,0)	CU(2,0) 0000	CU(2,1) 0100	XNOR	1011

CU(0,3), CU(1,2), CU(1,3), CU(2,2), CU(2,3), CU(3,1), CU(3,2), and CU(3,3) are not used for simulating the DFG2. So, OP Code was 00000 No Operation was done by all the mentioned CUs.

Output Waveforms:



Case 1:

CU	Input A	Input B	Operation	Expected Output	Actual Output	Matched
CU(0,0)	1001	0011	ADD	1100	1100	Yes
CU(0,1)	1111	0110	SUB	1001	1001	Yes
CU(0,2)	0111	0010	MULT	1110	1110	Yes
CU(0,3)	1101	0010	LSL	0100	0100	Yes
CU(1,0)	CU(0,2) 1110	CU(0,3) 0100	ROL	1110	1110	Yes
CU(1,1)	CU(0,0) 1100	CU(0,2) 1110	XOR	0010	0010	Yes
CU(1,2)	CU(0,1) 1001	CU(0,3) 0100	NAND	1111	1111	Yes
CU(2,1)	CU(1,0) 1110	CU(1,1) 0010	GT	1111	1111	Yes
CU(2,2)	CU(1,1) 0010	CU(1,2) 1111	OR	1111	1111	Yes
CU(3,1)	CU(2,1) 1111	CU(2,1) 1111	GT	1111	1111	Yes
CU(3,2)	CU(2,2) 1111	CU(2,2) 1111	OR	1111	1111	Yes

Case 2:

CU	Input A	Input B	Operation	Expected Output	Actual Output	Matched
CU(0,0)	1000	0010	ASR	1110	1110	Yes
CU(0,1)	0101	0010	MULT	1010	1010	Yes

CU(0,2)	1100	0010	LSR	0011	0011	Yes
CU(1,0)	CU(0,0) 1110	CU(0,1) 1010	ROR	1011	1011	Yes
CU(1,1)	CU(0,1) 1010	CU(0,2) 0011	AND	0010	0010	Yes
CU(2,0)	CU(1,0) 1011	CU(1,1) 0010	LT	0000	0000	Yes
CU(2,1)	CU(1,0) 1011	CU(1,1) 0010	NOR	0100	0100	Yes
CU(3,0)	CU(2,0) 0000	CU(2,1) 0100	XNOR	1011	1011	Yes