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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02.04.2024 00:54:52
-- Design Name:
-- Module Name: OVERALL_DESIGN_SIM - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.custom_pack.all;
use std.env.finish;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity OVERALL_DESIGN_SIM is
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--  Port ( );
end OVERALL_DESIGN_SIM;

architecture Behavioral of OVERALL_DESIGN_SIM is
constant dw: integer:=4;
constant dwo: integer:=2;
constant dwm: integer:=5;
constant dws:integer:=8;

signal a,b: ARR_1D (0 to dw-1)(dw-1 downto 0);
signal  CUs:  ARR_2D (0 to dw-1,0 to dw-1)(dw downto 0);
signal SelA,SelB:  ARR_2D (0 to dw-2,0 to dw-1)(1 downto 0);
signal  o:  ARR_1D (0 to dw-1)(dw-1 downto 0);

begin
UUT: entity work.OVERALL_DESIGN(Behavioral)
generic map(dw=>dw,dwo=>dwo,dwm=>dwm,dws=>dws)
port map(a=>a,b=>b,CUs=>CUs,SelA=>SelA,SelB=>SelB, o=>o);
stim: process
begin
-----------------DFG-1-----------------------
a<=("1001","1111","0111","1101");
b<=("0011","0110","0010","0010");
CUs<=(("00111","01000","01001","10100"),
        ("10010","00101","00011","00000"),
        ("00000","01101","00010","00000"),
        ("00000","10110","10110","00000"));
SelA<=(("10","00","01","00"),
       ("00","00","01","00"),
       ("00","01","10","00"));
SelB<=(("11","10","11","00"),
       ("00","01","10","00"),
       ("00","01","10","00"));

wait for 100ns;
---------------DFG-2-----------------------
a<=("1000","0101","1100","0000");
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b<=("0010","0010","0010","0000");
CUs<=(("10001","01001","10101","00000"),
        ("10011","00001","00000","00000"),
        ("01011","00100","00000","00000"),
        ("00110","00000","00000","00000"));
SelA<=(("00","01","00","00"),
       ("00","00","00","00"),
       ("00","00","00","00"));
SelB<=(("01","10","00","00"),
       ("01","01","00","00"),
       ("01","00","00","00"));
wait for 100ns;
-----------------------------------------
finish;
end process;
end Behavioral;
```