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-- Company:  
-- Engineer:  
--  
-- Create Date: 01.04.2024 21:43:50  
-- Design Name:  
-- Module Name: OVERALL_DESIGN - Behavioral  
-- Project Name:  
-- Target Devices:  
-- Tool Versions:  
-- Description:  
--  
-- Dependencies:  
--  
-- Revision:  
-- Revision 0.01 - File Created  
-- Additional Comments:  
--  
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```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;  
use work.custom_pack.all;
```

```
-- Uncomment the following library declaration if using  
-- arithmetic functions with Signed or Unsigned values  
--use IEEE.NUMERIC_STD.ALL;
```

```
-- Uncomment the following library declaration if instantiating  
-- any Xilinx leaf cells in this code.  
--library UNISIM;  
--use UNISIM.VComponents.all;
```

```
entity OVERALL_DESIGN is
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generic( dw: integer:=4;
         dwo: integer:=2;
         dwm: integer:=5;
         dws:integer:=8
        );
Port (a,b:in ARR_1D (0 to dw-1)(dw-1 downto 0);
      CUs: in ARR_2D (0 to dw-1,0 to dw-1)(dw downto 0);
      SelA,SelB: in ARR_2D (0 to dw-2,0 to dw-1)(1 downto 0);
      o: out ARR_1D (0 to dw-1)(dw-1 downto 0));
end OVERALL_DESIGN;

architecture Behavioral of OVERALL_DESIGN is
signal MAo,MBo:ARR_2D(0 to dw-1,0 to dw-1)(dw-1 downto 0);
signal Yo: ARR_2D(0 to dw-2,0 to dw-1)(dw-1 downto 0);
begin

-----ROW=0-----
--
ALU00: entity work.ALU_6(Behavioral)
port map(a=>a(0),b=>b(0),s=>CUs(0,0),o=>Yo(0,0));
ALU01: entity work.ALU_6(Behavioral)
port map(a=>a(1),b=>b(1),s=>CUs(0,1),o=>Yo(0,1));
ALU02: entity work.ALU_6(Behavioral)
port map(a=>a(2),b=>b(2),s=>CUs(0,2),o=>Yo(0,2));
ALU03: entity work.ALU_6(Behavioral)
port map(a=>a(3),b=>b(3),s=>CUs(0,3),o=>Yo(0,3));
-----MUXES
ROW=0-----
MUXA00: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelA(0,0),y=>MAo(0,0));
MUXB00: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelB(0,0),y=>MBo(0,0));

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MUXA01: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelA(0,1),y=>MAo(0,1));

MUXB01: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelB(0,1),y=>MBo(0,1));

MUXA02: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelA(0,2),y=>MAo(0,2));

MUXB02: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelB(0,2),y=>MBo(0,2));

MUXA03: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelA(0,3),y=>MAo(0,3));

MUXB03: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(0,0),b=>Yo(0,1),c=>Yo(0,2),d=>Yo(0,3),sel=>SelB(0,3),y=>MBo(0,3));

-----ROW=1-----
--

ALU10: entity work.ALU_6(Behavioral)
port map(a=>MAo(0,0),b=>MBo(0,0),s=>CUs(1,0),o=>Yo(1,0));
ALU11: entity work.ALU_6(Behavioral)
port map(a=>MAo(0,1),b=>MBo(0,1),s=>CUs(1,1),o=>Yo(1,1));
ALU12: entity work.ALU_6(Behavioral)
port map(a=>MAo(0,2),b=>MBo(0,2),s=>CUs(1,2),o=>Yo(1,2));
ALU13: entity work.ALU_6(Behavioral)
port map(a=>MAo(0,3),b=>MBo(0,3),s=>CUs(1,3),o=>Yo(1,3));

```

-----MUXES
ROW=1-----

```
MUXA10: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelA(1,0),y=>M
Ao(1,0));
```

```
MUXB10: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelB(1,0),y=>M
Bo(1,0));
```

```
MUXA11: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelA(1,1),y=>M
Ao(1,1));
```

```
MUXB11: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelB(1,1),y=>M
Bo(1,1));
```

```
MUXA12: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelA(1,2),y=>M
Ao(1,2));
```

```
MUXB12: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelB(1,2),y=>M
Bo(1,2));
```

```
MUXA13: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelA(1,3),y=>M
Ao(1,3));
```

```
MUXB13: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(1,0),b=>Yo(1,1),c=>Yo(1,2),d=>Yo(1,3),sel=>SelB(1,3),y=>M
Bo(1,3));
```

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-----ROW=2-----
--
ALU20: entity work.ALU_6(Behavioral)
port map(a=>MAo(1,0),b=>MBo(1,0),s=>CUs(2,0),o=>Yo(2,0));
ALU21: entity work.ALU_6(Behavioral)
port map(a=>MAo(1,1),b=>MBo(1,1),s=>CUs(2,1),o=>Yo(2,1));
ALU22: entity work.ALU_6(Behavioral)
port map(a=>MAo(1,2),b=>MBo(1,2),s=>CUs(2,2),o=>Yo(2,2));
ALU23: entity work.ALU_6(Behavioral)
port map(a=>MAo(1,3),b=>MBo(1,3),s=>CUs(2,3),o=>Yo(2,3));
-----MUXES
ROW=2-----
MUXA20: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelA(2,0),y=>M
Ao(2,0));
MUXB20: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelB(2,0),y=>M
Bo(2,0));

MUXA21: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelA(2,1),y=>M
Ao(2,1));
MUXB21: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelB(2,1),y=>M
Bo(2,1));

MUXA22: entity work.MUX4_1(Behavioral)
port
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelA(2,2),y=>M
Ao(2,2));
MUXB22: entity work.MUX4_1(Behavioral)
port

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```
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelB(2,2),y=>MBo(2,2));
```

```
MUXA23: entity work.MUX4_1(Behavioral)
```

```
port
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```
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelA(2,3),y=>MAo(2,3));
```

```
MUXB23: entity work.MUX4_1(Behavioral)
```

```
port
```

```
map(a=>Yo(2,0),b=>Yo(2,1),c=>Yo(2,2),d=>Yo(2,3),sel=>SelB(2,3),y=>MBo(2,3));
```

```
-----ROW=3-----
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ALU30: entity work.ALU_6(Behavioral)
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```
port map(a=>MAo(2,0),b=>MBo(2,0),s=>CUs(3,0),o=>o(0));
```

```
ALU31: entity work.ALU_6(Behavioral)
```

```
port map(a=>MAo(2,1),b=>MBo(2,1),s=>CUs(3,1),o=>o(1));
```

```
ALU32: entity work.ALU_6(Behavioral)
```

```
port map(a=>MAo(2,2),b=>MBo(2,2),s=>CUs(3,2),o=>o(2));
```

```
ALU33: entity work.ALU_6(Behavioral)
```

```
port map(a=>MAo(2,3),b=>MBo(2,3),s=>CUs(3,3),o=>o(3));
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end Behavioral;
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