EENG 5560 HW6

Assigned: March 26, 2024
Due: April 4, 2024
Total points: 50

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1 Question

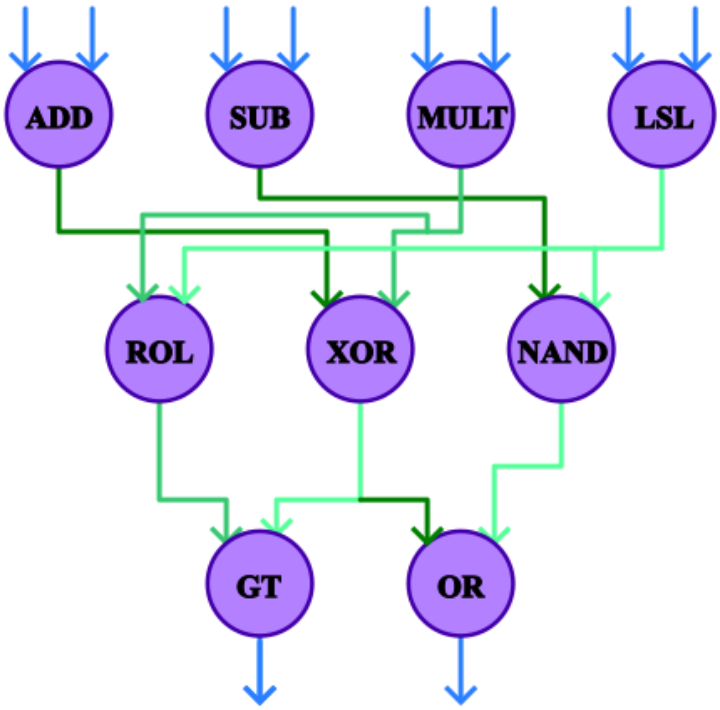

Figure 1: Dataflow graph 1.

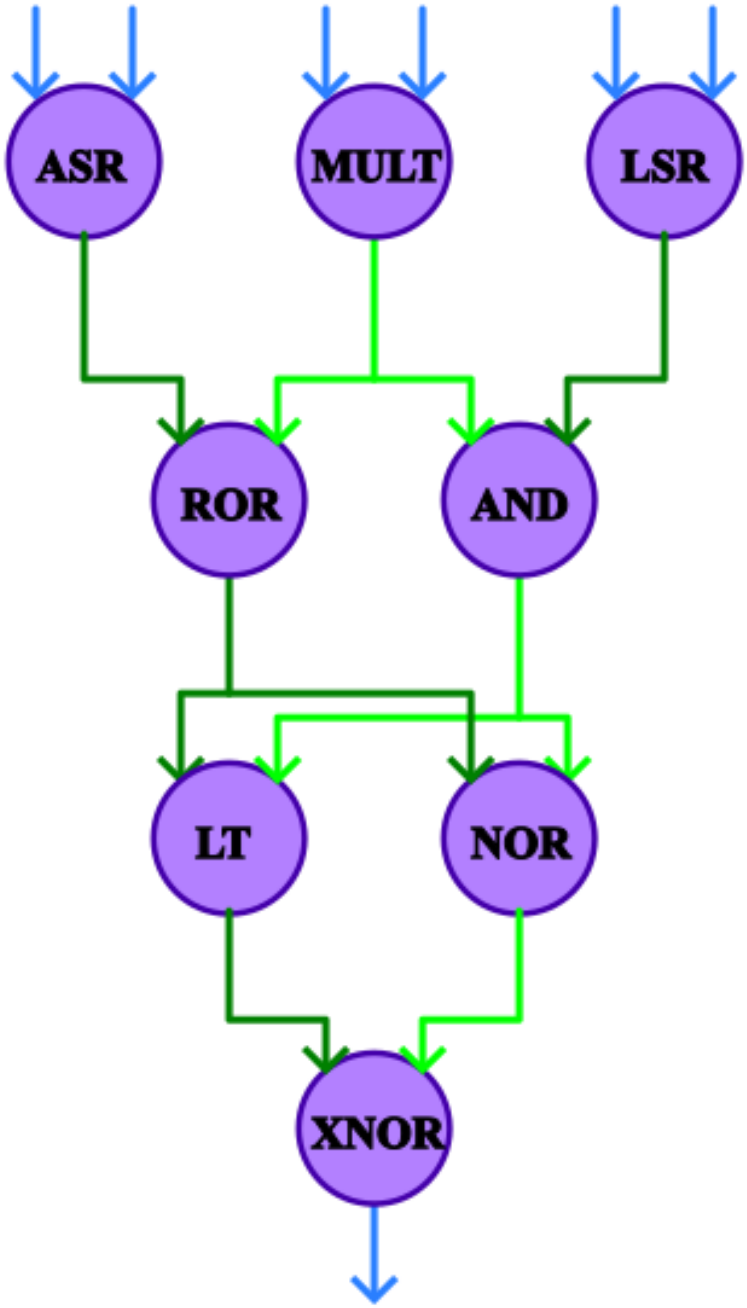

Figure 2: Dataflow graph 2.

Implement the above 2 dataflow graphs (DFGs) on the same fabric. You will need to create a CU that only supports the operations required by the combined required operations, but has a data width parameter set to 4. You will need to decide on the overall fabric size, each interconnect connectivity. Once you decide a fabric size, you will need to pick the arrangement and placement of the CUs on the decided fabric for each DFG. Each dataflow graph is a "test case" with the external data input values listed in the next section.

2 Test case Data Inputs

You need to make testbenches for all components used, but you only have to show the calculations and waveforms for the overall design in this assignment. This time, you are required to show the waveforms for the intermediate CU outputs in addition to the overall outputs. The external data input values for each DFG are as follows.

2.1 DFG 1

Row 0 External Data Inputs

CU#	A	B
CU(0,0)	1001	0011
CU(0,1)	1111	0110
CU(0,2)	0111	0010
CU(0,3)	1101	0010

2.2 DFG 2

Row 0 External Data Inputs

CU#	A	B
CU(0,0)	1000	0010
CU(0,1)	0101	0010
CU(0,2)	1100	0010

3 Formatting

3.1 Steps: Printing code to pdf

For each source file (both the design and the simulation VHDL or other HDL language files), print the code to pdf either in Vivado or by opening the code in any other text editor and printing it from there. It is preferable to combine all of the pdfs of the code into a single pdf, you can do so using this website

or any other websites/software with that capability. The steps to print the code to a pdf from Vivado are as follows:

1. With the VHDL\source file currently open and being viewed in the text editor, click the file tab at the top and near the bottom select the print option (or press Ctrl + P).

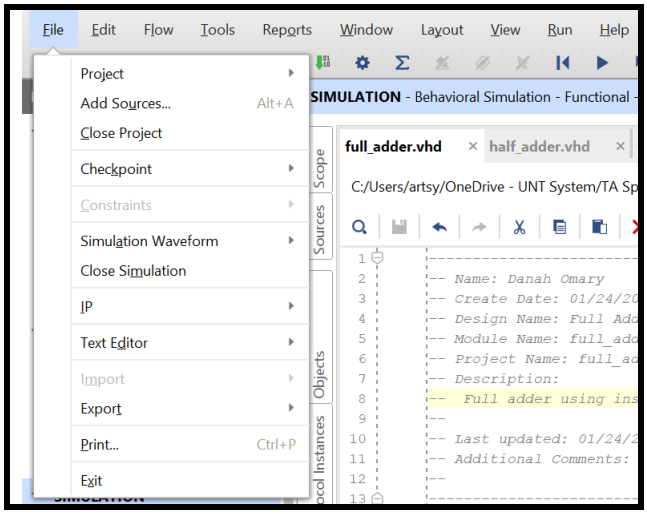

Figure 3: Print button.

2. In the popup, in the dropdown next to the “Name: ” text, make sure to select Microsoft Print to PDF. Then click ok.

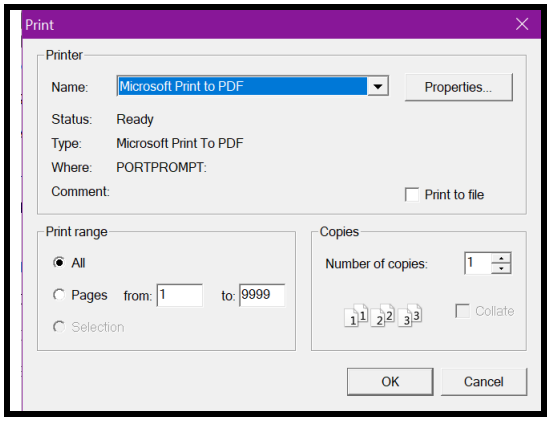

Figure 4: Printing popup with print to pdf chosen.

3. Name the pdf file something clearly indicating what it is and then browse to where you'd like to save the pdf to.

3.2 Source files zipping

In a **separate** **zip file, include the following files (and only these files):**

- **A README text file that includes a list of all the files that should be included and any special instructions needed to run the top level module (in Windows, to create a text file, in the file explorer right click empty space and choose "New - Text Document"). This will help in the case that any files that were supposed to be included ended up missing.**
- **VHDL file for top level component**
- **VHDL files for all subcomponents and any of their testbenches**
- **VHDL file for top level testbench**

Do not include other files from the project or the submission (i.e. the report and pdf of the vhdl code), only the VHDL files are needed.

3.3 Example submission files

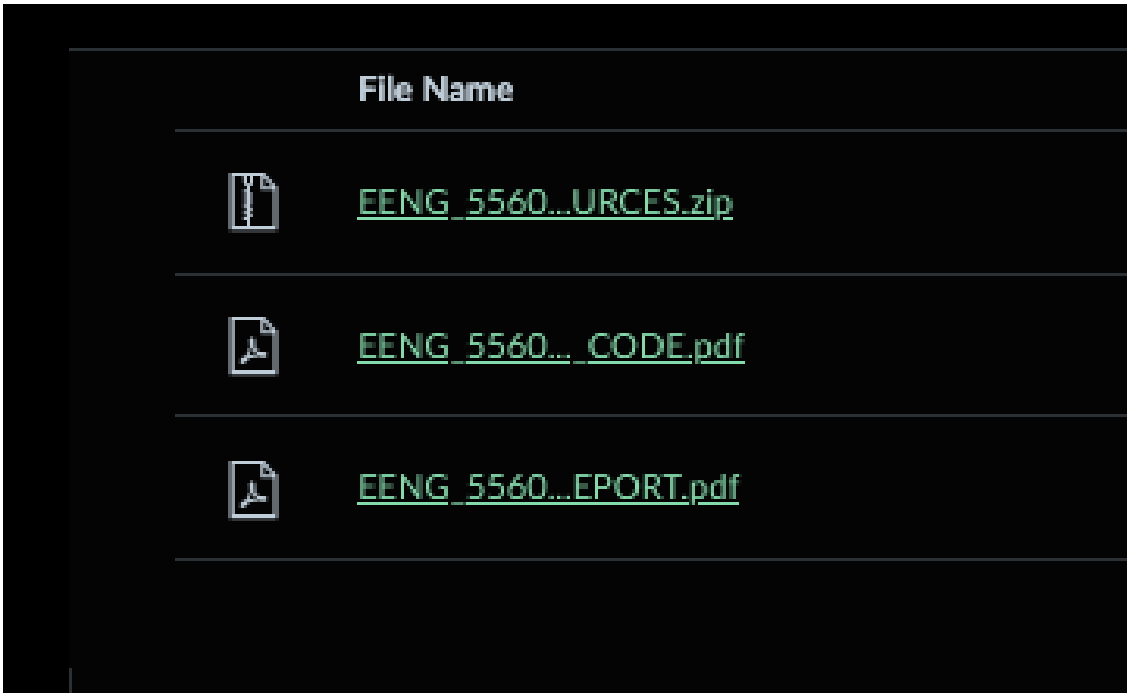

Figure 5: Example showing the file types and good naming conventions of a submission.

In total you will have 3 major parts to your submission:

1. **Report(s): pdf(s)**
2. **Code: pdf(s)**
3. **Source files: zip folder**

As can be seen in the figure, the pdfs for the code and report *NEED TO BE OUTSIDE OF A ZIP FILE*.

3.4 Other formatting notes

If you would like to make a report yourself rather than follow the provided template, please make sure to include all of the things listed out in the checklist below as well as a Table of Contents and page numbers on each page. Do not include all of the VHDL code in the report, please keep it separate from the report.

4 Checklist

Your submission should include (using helpful/distinguishable file names):

- ☐ **Report (either in pdf or .docx file type) including:**
  - ☐ **Design: Block diagrams, design explanation**
  - ☐ **Generated RTL Schematic and verbal comparison (top module only)**
  - ☐ **Simulation waveforms for the test cases, including the overall outputs and relevant intermediate signals (top module only)**
  - ☐ **Table with Calculated outputs vs Simulation outputs for all test cases (top module only)**
- ☐ **PDF(s): VHDL (or verilog or systemverilog) code for the top level component, all subcomponents, and the testbenches (can combine all code pdfs into one pdf overall or include individual pdfs)**
- ☐ **Zip file with all the VHDL source code files needed to run the top level component**