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-- Company:  
-- Engineer:  
--  
-- Create Date: 02/01/2024 03:47:50 PM  
-- Design Name:  
-- Module Name: Topbox_tb - Behavioral  
-- Project Name:  
-- Target Devices:  
-- Tool Versions:  
-- Description:  
--  
-- Dependencies:  
--  
-- Revision:  
-- Revision 0.01 - File Created  
-- Additional Comments:  
--  
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```

```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;  
use std.env.finish;  
-- Uncomment the following library declaration if using  
-- arithmetic functions with Signed or Unsigned values  
--use IEEE.NUMERIC_STD.ALL;  
  
-- Uncomment the following library declaration if instantiating  
-- any Xilinx leaf cells in this code.  
--library UNISIM;  
--use UNISIM.VComponents.all;  
  
entity Topbox_tb is  
-- Port ( );
```

```
end Topbox_tb;
```

architecture Behavioral of Topbox\_tb is

```
signal a ,b, c, d: std_logic_vector ( 7 downto 0);
```

```
signal s1, s2, s3: std_logic_vector(3 downto 0);
```

```
signal o: std_logic_vector (7 downto 0);
```

```
begin
```

```
test: entity work.Topbox(Behavioral)
```

```
port map(a => a,b => b,c => c, d => d, s1 => s1, s2 => s2, s3 =>
```

```
s3, o=>o);
```

```
ut: process
```

```
begin
```

```
a<= "10101011";b<= "01011100";c <= "11011001";d <= "10010011";
```

```
s1<= "0001";s2<= "0110";s3<= "1001";
```

```
wait for 300ns;
```

```
a<= "11011011";b<= "11001100";c <= "10111001";d <= "10010011";
```

```
s1<= "0000";s2<= "1010";s3<= "0111";
```

```
wait for 300ns;
```

```
finish;
```

```
end process;
```

```
end Behavioral;
```