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-- Company:
-- Engineer:
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-- Create Date: 02/01/2024 02:16:51 PM
-- Design Name:
-- Module Name: compunit_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

use std.env.finish;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity compunit_tb is
```

```
end compunit_tb;

architecture Behavioral of compunit_tb is
signal a ,b: std_logic_vector ( 7 downto 0);
signal s: std_logic_vector(3 downto 0);
signal o: std_logic_vector (7 downto 0);

begin
test: entity work.compunit(Behavioral)
port map(a => a,b => b,s => s, o=>o);

ut: process
begin
a<= "11111111";b<= "01101100";
--c <= "11011001";d <= "10010011";
s<= "1001";
wait for 300ns;
finish;
end process;



end Behavioral;
```