EENG 5560 HW1

Assigned: January 23, 2024
Due: February 1, 2024
Total points: 50

Contents

1 Question

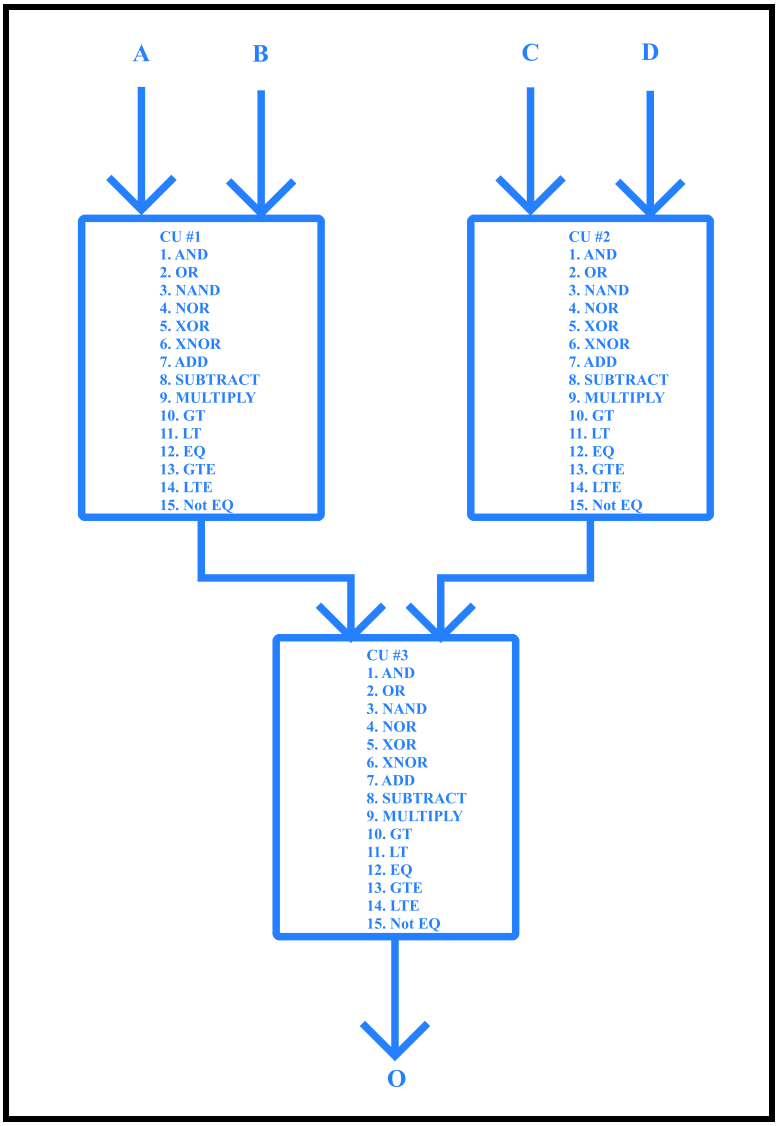

Figure 1: Design.

Create a computational unit that can compute the following operations on 8 bit operands:

1. AND
2. OR
3. NAND
4. NOR
5. XOR
6. XNOR
7. Addition
8. Subtraction
9. Multiplication
10. Greater than
11. Less than
12. Equal to
13. Greater than or equal to
14. Less than or equal to
15. Not equal to

First test the computation unit for all operations. After verifying the unit works properly for all operations, then instantiate the component 3 times in the arrangement shown in Fig. 1. Make sure to use the same input and output names shown in Fig. 1, but note that the figure is representational and does not show all inputs and signals you might need to implement the design.

2 Test cases

To test the computation unit, use the inputs “1011 1001” and “0111 0101” for the first test case and “0101 0110” and “1100 1001” for the second test case. Calculate the expected values and then record the simulated outputs in a table for comparison to verify that they match.

To test the overall design, use the following test cases and similarly record the calculated vs simulated outputs in a separate table for comparison.
Case 1:

- A: “1010 1011”, B: “0101 1100”, C: “1101 1001”, D: “1001 0011”
- CU #1: OR, CU #2: ADD, CU#3: GREATER THAN

Case 2:

- A: 1101 1011, B: 1100 1100, C: 1011 1001, D: 1001 0011
- CU #1: AND, CU #2: LESS THAN, CU#3: SUBTRACT

3 Formatting

3.1 Steps: Printing code to pdf

For each source file (both the design and the simulation VHDL or other HDL language files), print the code to pdf either in Vivado or by opening the code in any other text editor and printing it from there. The steps to print the code to a pdf from Vivado are as follows:

1. With the VHDL\source file currently open and being viewed in the text editor, click the file tab at the top and near the bottom select the print option (or press Ctrl + P).

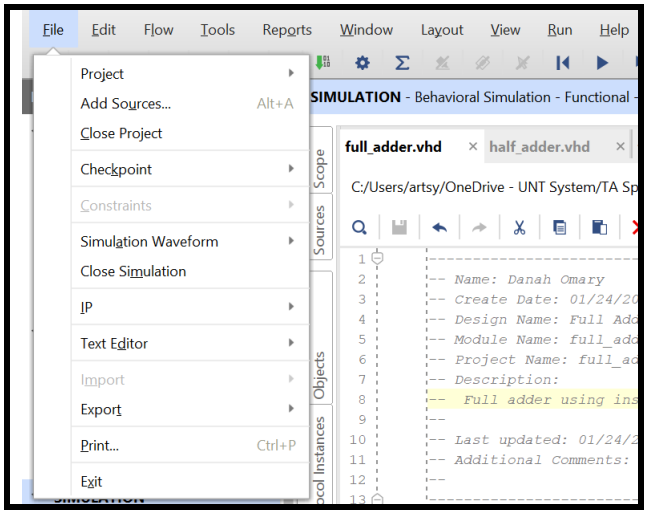

Figure 2: Print button.

2. In the popup, in the dropdown next to the "Name: " text, make sure to select Microsoft Print to PDF. Then click ok.

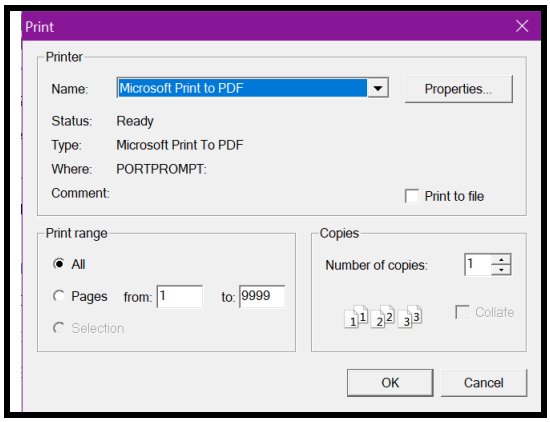

Figure 3: Printing popup with print to pdf chosen.

3. Name the pdf file something clearly indicating what it is and then browse to where you'd like to save the pdf to.

3.2 Source files zipping

In a separate zip file, include the following files (and only these files):

- A README text file that includes a list of all the files that should be included and any special instructions needed to run the top level module (in Windows, to create a text file, in the file explorer right click empty space and choose "New - Text Document"). This will help in the case that any files that were supposed to be included ended up missing.
- VHDL file for top level component
- VHDL files for all subcomponents and any of their testbenches
- VHDL file for top level testbench

Do not include other files from the project or the submission (i.e. the report and pdf of the vhdl code), only the VHDL files are needed.

3.3 Other formatting notes

If you would like to make a report yourself rather than follow the provided template, please make sure to include all of the things listed out in the checklist below as well as a Table of Contents and page numbers on each page. Do not include all of the VHDL code in the report, please keep it separate from the report.

4 Checklist

Your submission should include (using helpful/distinguishable file names):

- ☐ **Report (either in pdf or .docx file type) including:**
  - ☐ **Block diagrams\design explanations**
  - ☐ **Generated RTL Schematic\Block diagram**
  - ☐ **Simulation outputs\waveforms for the test cases**
  - ☐ **Manual calculations for the test cases**
  - ☐ **Table with Calculated outputs vs Simulation outputs for both calculated test cases**
- ☐ **PDF(s): VHDL (or verilog or systemverilog) code for the top level component, all subcomponents, and the testbenches (can combine all code pdfs into one pdf overall or include individual pdfs)**
- ☐ **Zip file with all the VHDL source code files needed to run the top level component**