(\*EENG 5560\*) Final Project Report Template

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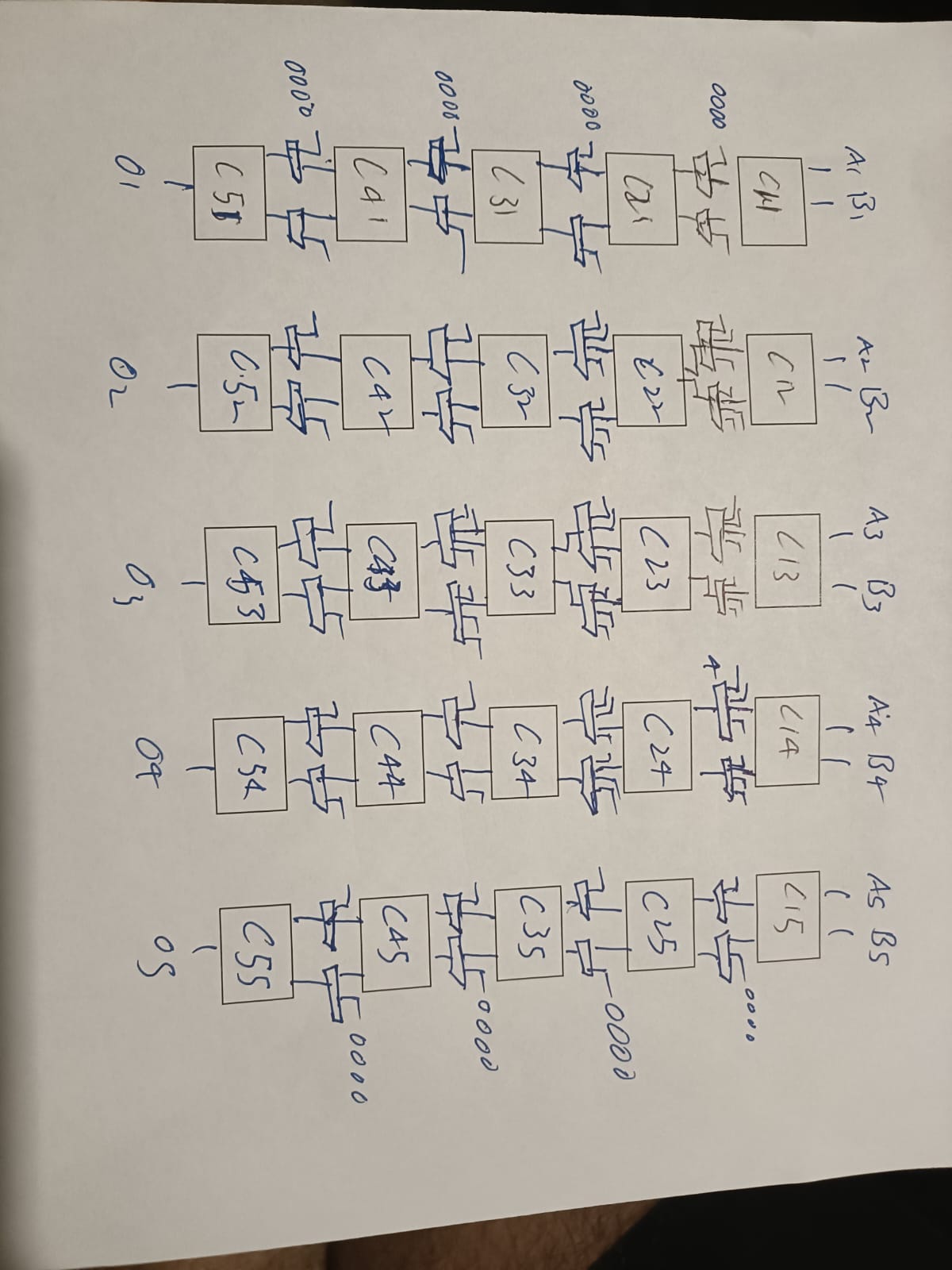
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# Specifications

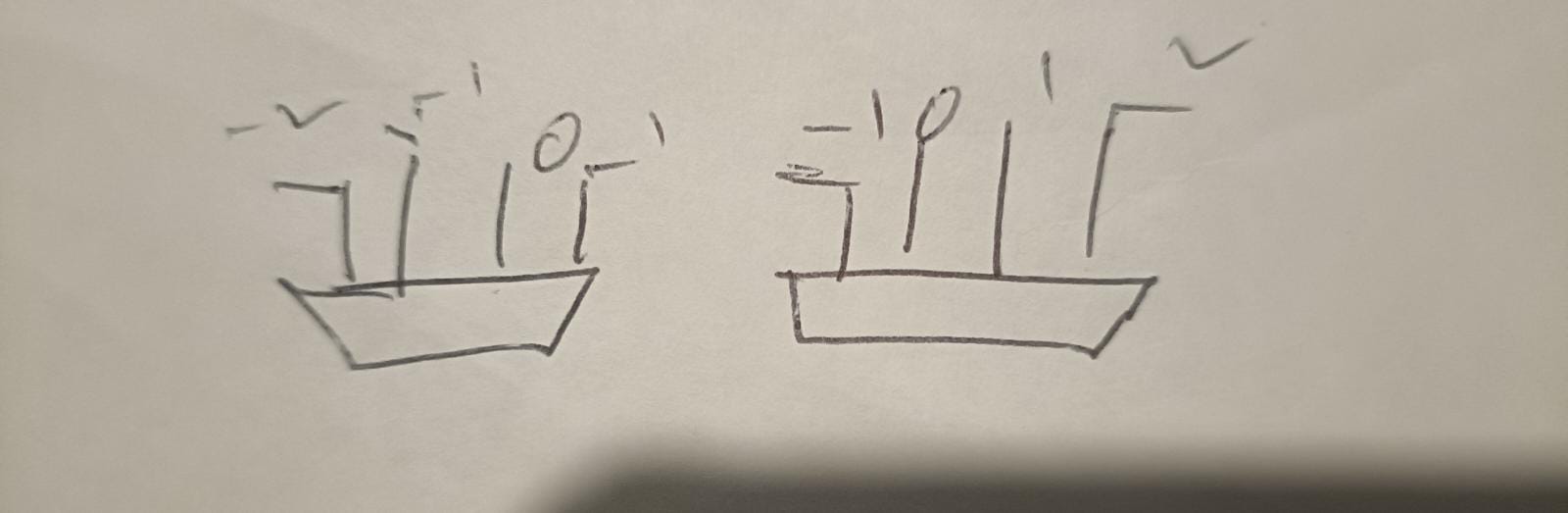
|  |  |
| --- | --- |
| Requirement | Design Follows Requirement |
| Input data width: 4 bits | Yes |
| Homogeneous Computational Units (CUs) | Yes |
| Heterogeneous Interconnects | Yes |
| Interconnects with mirroring | Yes |
| Pass and No Op operation support | Yes |
| Support for all of the DFGs on the Super-architecture | Yes |

# Design

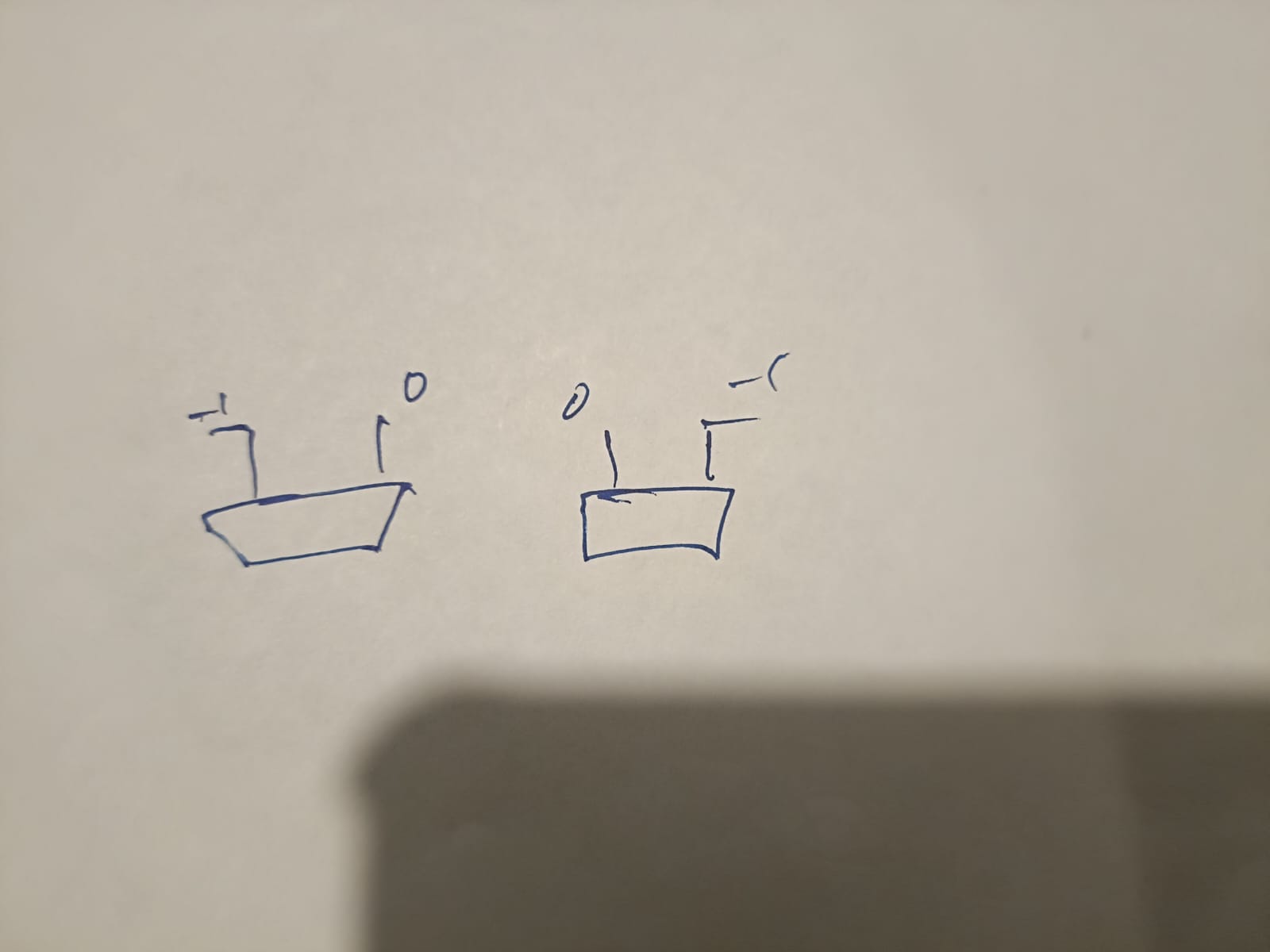
## Block diagram



1.1 )5 CROSS 5 ARCHITECTURE



1.2) 4 TO 1 MIRROR MUXES



1.3) 2 TO 1 MIRROR MUXES

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Figure 2- Computational Unit

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Figure 3- Mux 2x1

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Figure 4- Mux 4x1

Here the We use Homogenious Computational unit, Mirror muxes (2 to 1) and 4 to 1 with Hetroginity

We designed 5 cross 5 size architecture it contains 25 Computational units and 40 muxes . We are giving 10 inputs and taking 5 outputs.

Overall Component: (5x 5) Fabric

* Overall ports:
  + Inputs:
    - A1,A2,A3,A4,A5,B1,B2,B3,B4,B5: data inputs (4 bits wide)
  + Inputs:

CU\_SEL11 ,CU\_SEL12, CU\_SEL 13,CU\_SEL14, CU\_SEL15,

CU\_SEL21, CU\_SEL22, CU\_SEL23, CU\_SEL24, CU\_SEL25,

CU\_SEL31, CU\_SEL32, CU\_SEL33, CU\_SEL34, CU\_SEL35,

CU\_SEL41, CU\_SEL42, CU\_SEL43, CU\_SEL44, CU\_SEL45,

CU\_SEL51, CU\_SEL52, CU\_SEL53, CU\_SEL54, CU\_SEL55: (5 bits wide)

M\_Sel11, M\_Sel12, M\_Sel19, M\_Sel110, M\_Sel21, M\_Sel22, M\_Sel29, M\_Sel210, M\_Sel31, M\_Sel32,M\_Sel39, M\_Sel310, M\_Sel41, M\_Sel42, M\_Sel49, M\_Sel410 ,M\_Sel33, M\_Sel34, M\_Sel37, M\_Sel38, M\_Sel43, M\_Sel44, M\_Sel45, M\_Sel46, M\_Sel47, M\_Sel48(1 BIT) - **2 TO 1 MUX**  **SELECTION LINE**

M\_Sel13, M\_Sel14,M\_Sel15, M\_Sel16,M\_Sel17, M\_Sel18,M\_Sel23,

M\_Sel24,M\_Sel25, M\_Sel26,M\_Sel27, M\_Sel28, M\_Sel35,M\_Sel36

-(2 BIT) **4 BIT SELECTION LINE**

* + Outputs:
    - O1,O2,O3,O4,O5: data output (ex: 4 bits wide)
* Subcomponents:
  + (14) 4:1 muxes
  + (26) 2:1 mux
  + (25) ALU
* Necessary intermediate signals:
  + c11, c12, c13, c14, c15, c21, c22, c23 , c24,c25,c31, c32, c33 , c34,c35,

c41, c42, c43 ,c44, c45 (4 BIT) -- Signal Lines for CU's

* + m11 ,m12 ,m13 ,m14 ,m15 ,m16,m17 ,m18,m19 ,m110,m21, m22 ,m23 ,m24 , m25 ,m26, m27 ,m28 ,m29 , m210,m31 ,m32 ,m33 ,m34 ,m35 ,m36,m37 ,m38 ,m39 ,m310,

m41 ,m42 ,m43 ,m44 ,m45 ,m46,m47 ,m48 ,m49 ,m410 (4 BIT)-- Signal Lines for Mux's

**Description (top\_bOX):**

This code is an implementation of a digital circuit design called "Top\_Box".

It consists of multiple components, such as computational units (CU), 2x1 and 4x1 multiplexers (mux), and signal lines that connect them. The input ports of this design are the signal vectors A1-A5 and B1-B5, which have a size of 4 bits. These signals are used as inputs to the computational units (CU) in the data flow graphs.

The selection lines of the CUs are represented by the signals CU\_SEL11 to CU\_SEL55. The signal M\_Sel33 to M\_Sel48 are selection lines for the 2x1 mux, and M\_Sel11 to M\_Sel410 are also selection lines for 2x1 mux.

The signal vectors M\_Sel13 to M\_Sel36 are selection lines for the 4x1 mux. The output ports of this design are the signal vectors O1-O5, which also have a size of 4 bits.

These signals are the outputs of the CUs in the data flow graphs. The architecture of the Top\_Box design is implemented using signal lines and component instantiations. The CUs and muxes are instantiated as separate entities, and their input and output ports are connected using signals. The first row of CUs consists of five CU blocks, and each CU block has its own set of input ports (A and B) and selection lines (CU\_SEL11 to CU\_SEL15).

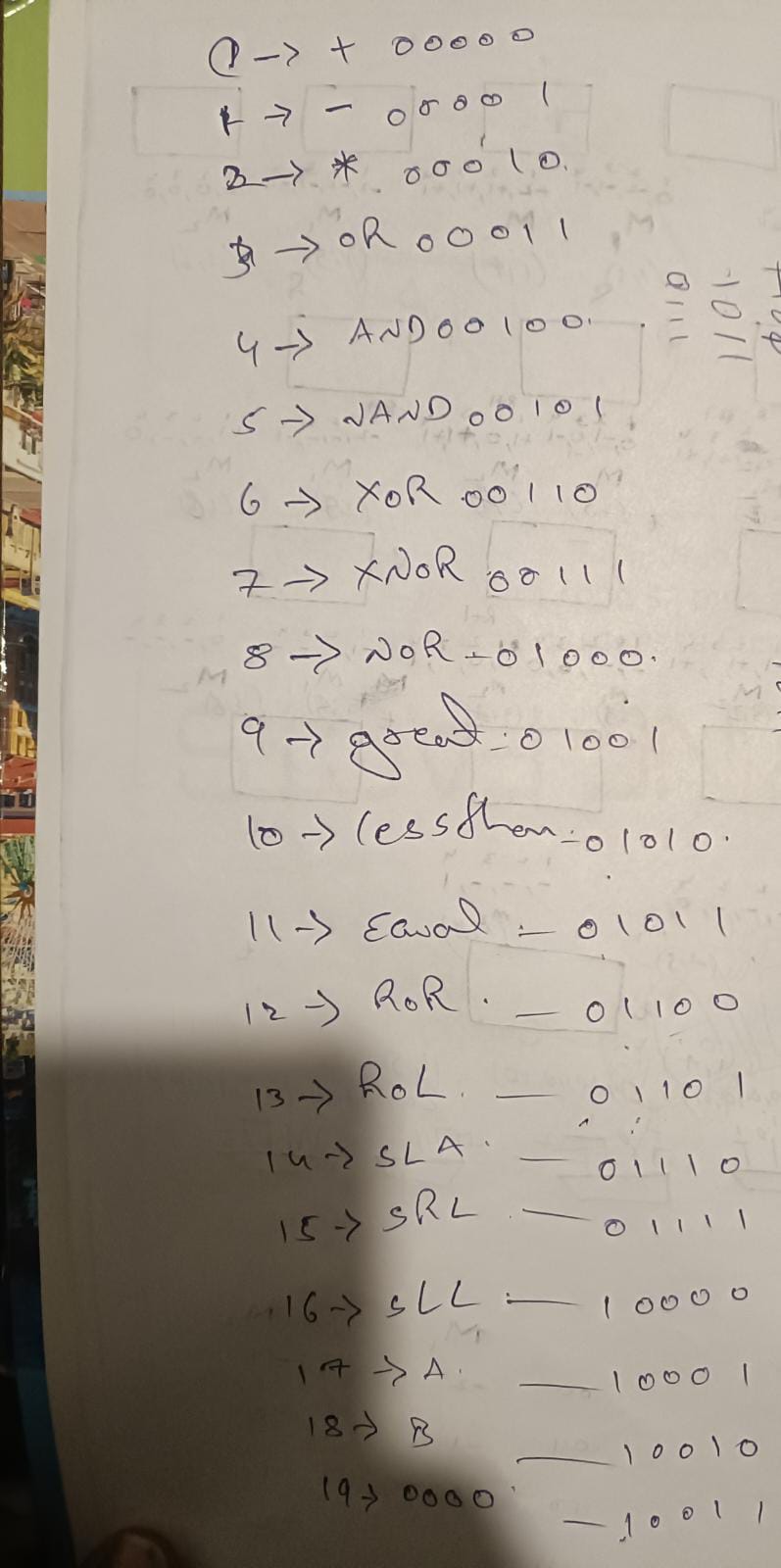
The output of each CU is connected to the input of a 2x1 mux block. The second row of the design consists of four CU blocks, and each block has its own set of input ports that are connected to the output of the 2x1 muxes. The output of each CU is connected to the input of a 4x1 mux block.

Finally, the output of each 4x1 mux is connected to one of the output ports of the Top\_Box design (O1-O5). The design is flexible enough to accommodate different data flow graphs by changing the selection lines of the CUs and muxes. Overall, this design is suitable for implementing complex data flow graphs and digital signal processing applications

Subcomponent: Computational Unit (CU)

* Overall ports:
  + Inputs:
    - a, b (ex: 4 bits wide)
    - Sel: data input select line (5 bits wide)
  + Outputs:
    - Z: data output (ex: 4 bits wide)
* Subcomponents (mux):
  + (2) 4:1 muxes
  + Inputs:
    - x1, x2, X3, X4(4 bits wide)
    - f: data input select line (2 bits wide)
  + Outputs:
    - o: data output (ex: 4 bits wide)
  + (1) 2:1 mux
  + (2) 4:1 muxes
  + Inputs:
    - x1, x2(4 bits wide)
    - t: data input select line (2 bits wide)
  + Outputs:
    - o: data output (ex: 4 bits wide)

Opcode table:



## Design explanation:

This is a VHDL code for a behavioral model of a control unit (CU).

The CU takes two 4-bit inputs A and B, a 5-bit selection input SEL, and generates a 4-bit output Z based on the selected operation.

The entity CU declares the input and output ports.

Inputs A, B, and SEL are of type std\_logic\_vector(3 downto 0)

The process block contains a case statement that selects one of the 18 operations based on the input selection signal SEL. The result of the selected operation is stored in a temporary variable temp, which is then assigned to the output Z.

### Arithmetic handling:

We used a library to “ieee.std\_logic\_unsigned.all” , “ieee.numeric\_std.all” to manage the arithmetic operations. For multiplication we used “std\_logic\_vector(to\_unsigned(to\_integer(unsigned(a)) \* to\_integer(unsigned(b)),4))” to truncate the extra bits.

### Shift Operations:

For shift operations we are shifting the first input by the second input number of bits

### Comparison operations:

When the conditions (<, >, =) are true then the output is 1111 else 0000

# Results

## Generated RTL Schematic

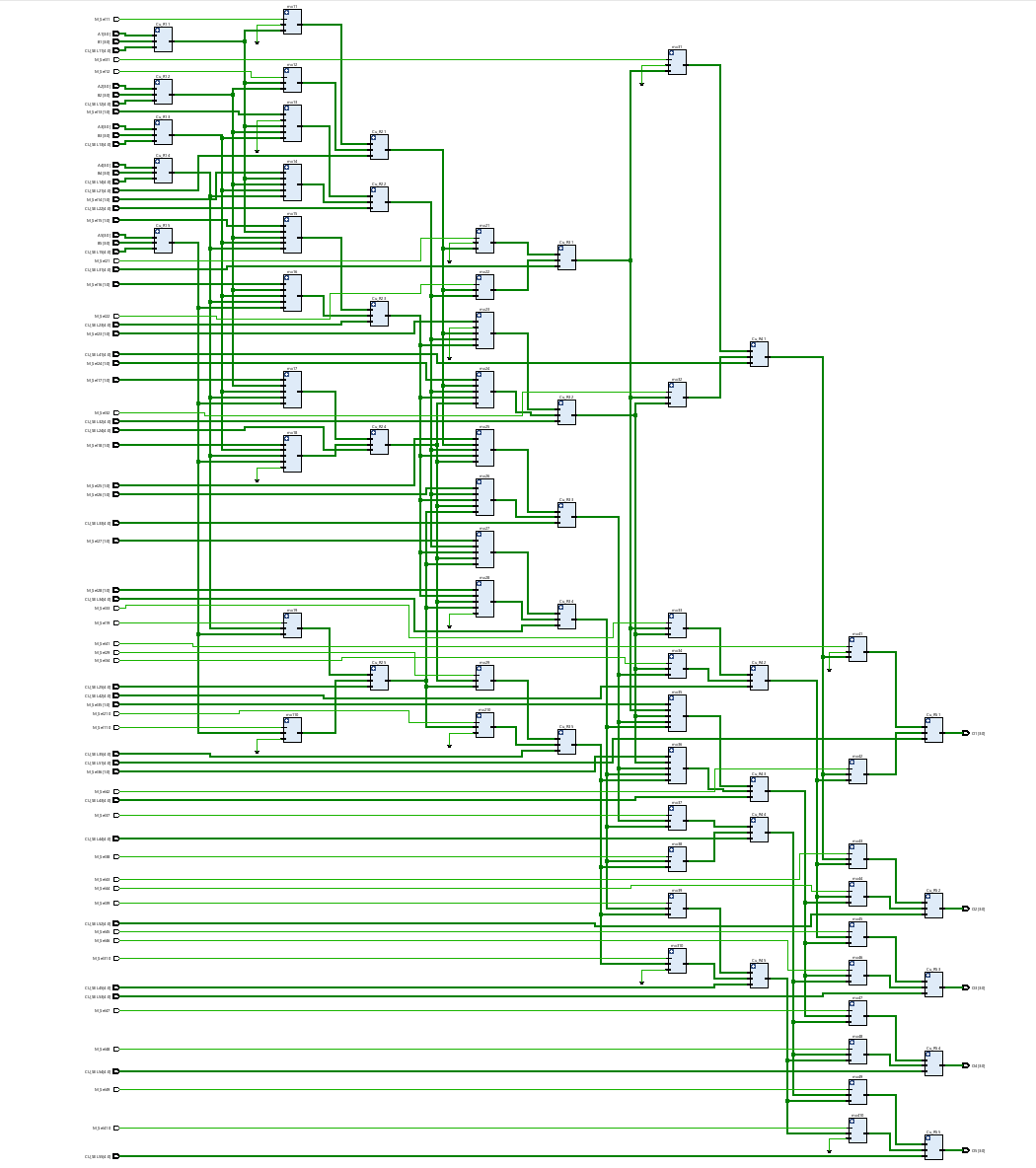


Figure 5 – Top Box generated RTL schematic

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Figure 6 – CU generated RTL schematic

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Figure – Mux 2x1 generated RTL schematic

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Figure – Mux 4x1 generated RTL schematic

## Waveforms

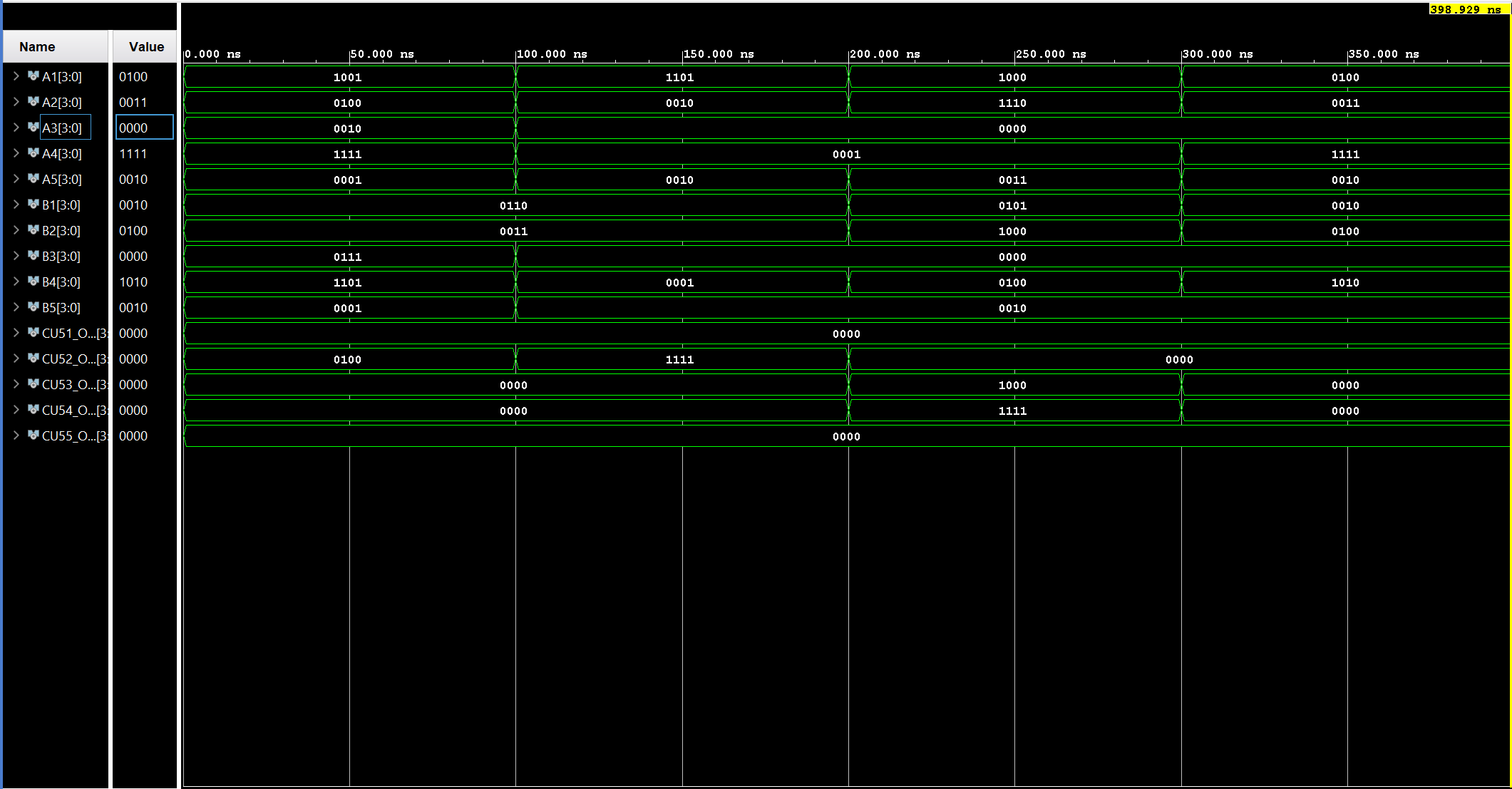


Figure 4 - Waveforms

## Table/Calculations

**Dataflow1(100ns)**

OUTPUT1 z2 : 0100 Output2: Z4:0000

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| STORAGE | SOURCE A | SOURCE B | A | B | OPERATION | CALCULATED OUTPUT | SIMULATED OUTPUT | MATCH |
| Cu11 | A1 | B1 | 1001 | 0110 | ADD | 1111 | 1111 | YES |
| Cu12 | A2 | B2 | 0100 | 0011 | MULTI | 1100 | 1100 | YES |
| Cu13 | A3 | B3 | 0010 | 0111 | ADD | 1001 | 1001 | YES |
| Cu14 | A4 | B4 | 1111 | 1101 | SUB | 0010 | 0010 | YES |
| Cu15 | A5 | B5 | 0001 | 0001 | MULTI | 0001 | 0001 | YES |
| Cu21 | Cu11 | Cu12 | 1111 | 1100 | No Op | 0000 | 0000 | YES |
| Cu22 | CU11 | Cu13 | 1111 | 1001 | SUB | 0110 | 0110 | YES |
| Cu23 | Cu13 | Cu15 | 1001 | 0001 | ADD | 1010 | 1010 | YES |
| Cu24 | Cu12 | Cu14 | 1100 | 0010 | SUB | 1010 | 1010 | YES |
| Cu25 | Cu15 | Cu15 | 0001 | 0001 | Pass A | 0001 | 0001 | YES |
| Cu31 | Cu21 | Cu21 | 0000 | 0000 | No Op | 0000 | 0000 | YES |
| Cu32 | Cu22 | Cu23 | 0110 | 1010 | OR | 1110 | 1110 | YES |
| Cu33 | Cu23 | Cu24 | 1010 | 1010 | AND | 1010 | 1010 | YES |
| Cu34 | Cu22 | Cu15 | 0110 | 0001 | NAND | 0111 | 0111 | YES |
| Cu35 | Cu24 | Cu25 | 1010 | 0001 | No Op | 0000 | 0000 | YES |
| Cu41 | Cu31 | Cu31 | 0000 | 0000 | No Op | 0000 | 0000 | YES |
| Cu42 | Cu32 | Cu33 | 1110 | 1010 | XOR | 0100 | 0100 | YES |
| Cu43 | Cu33 | Cu34 | 1010 | 1111 | No Op | 0000 | 0000 | YES |
| Cu44 | Cu33 | Cu34 | 1010 | 0111 | NOR | 0000 | 0000 | YES |
| Cu45 | Cu34 | Cu35 | 1111 | 0000 | No Op | 0000 | 0000 | YES |
| Cu51 | Cu41 | Cu41 | 0000 | 0000 | No Op | 0000 | 0000 | YES |
| Cu52 | Cu42 | Cu42 | 0100 | 0100 | Pass A | 0100 | 0100 | YES |
| Cu53 | Cu42 | Cu43 | 0100 | 0000 | No Op | 0000 | 0000 | YES |
| Cu54 | Cu44 | Cu44 | 0000 | 0000 | Pass A | 0000 | 0000 | YES |
| Cu55 | Cu44 | Cu45 | 0000 | 0000 | No Op | 0000 | 0000 | YES |

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**Dataflow2(100ns)**

OUTPUT1 z2: 1111 Output2: Z3:0000

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| STORAGE | SOURCE A | SOURCE B | A | B | OPERATION | CALCULATED OUTPUT | SIMULATED OUTPUT | MATCH |
| Cu11 | A1 | B1 | 1101 | 0110 | SUB | 0111 | 0111 | YES |
| Cu12 | A2 | B2 | 0010 | 0011 | MULTI | 0110 | 0110 | YES |
| Cu13 | Ground | Ground | 0000 | 0000 | No Op | 0000 | 0000 | YES |
| Cu14 | A4 | B4 | 0001 | 0001 | ADD | 0010 | 0010 | YES |
| Cu15 | A5 | B5 | 0010 | 0010 | MULTI | 0100 | 0100 | YES |
| Cu21 | C11 | C11 | 0111 | 0111 | Pass A | 0111 | 0111 | YES |
| Cu22 | Cu11 | Cu14 | 0111 | 0010 | ADD | 1001 | 1001 | YES |
| Cu23 | Cu11 | Cu15 | 0111 | 0100 | SUB | 0011 | 0011 | YES |
| Cu24 | Cu12 | Cu15 | 0110 | 0100 | ADD | 1010 | 1010 | YES |
| Cu25 | Cu14 | Cu15 | 0011 | 0100 | Pass A | 0010 | 0010 | YES |
| Cu31 | Cu21 | Cu21 | 0111 | 0111 | No Op | 0000 | 0000 | YES |
| Cu32 | Cu11 | Cu24 | 0111 | 1010 | ROR | 1101 | 1101 | YES |
| Cu33 | Cu22 | Cu14 | 1001 | 0010 | LSL | 0100 | 100 | YES |
| Cu34 | Cu23 | Cu24 | 0011 | 0010 | Pass A | 0011 | 0011 | YES |
| Cu35 | Cu24 | Cu25 | 1010 | 0010 | No Op | 0000 | 0000 | YES |
| Cu41 | Cu31 | Cu31 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu42 | Cu32 | Cu33 | 1101 | 0100 | GREATER | 1111 | 1111 | YES |
| Cu43 | Cu32 | Cu23 | 1101 | 0011 | EQUAL TO | 0000 | 0000 | YES |
| Cu44 | Cu33 | Cu34 | 0100 | 0011 | NO Op | 0000 | 0000 | YES |
| Cu45 | Cu34 | Cu35 | 0011 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu51 | Cu41 | Cu42 | 0000 | 1111 | No OP | 0000 | 0000 | YES |
| Cu52 | Cu42 | Cu42 | 1111 | 1111 | Pass A | 1111 | 1111 | YES |
| Cu53 | Cu43 | Cu43 | 0000 | 0000 | Pass A | 0000 | 0000 | YES |
| Cu54 | Cu44 | Cu44 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu55 | Cu44 | Cu45 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |

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**Dataflow3(100ns)**

OUTPUT1 z3: 1000 Output2: Z4:1111

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| STORAGE | SOURCE A | SOURCE B | A | B | OPERATION | CALCULATED OUTPUT | SIMULATED OUTPUT | MATCH |
| Cu11 | A1 | B1 | 1000 | 0101 | ADD | 1101 | 1101 | YES |
| Cu12 | A2 | B2 | 1110 | 1000 | SUB | 0110 | 0110 | YES |
| Cu13 | Ground | Ground | 0000 | 0000 | No Op | 0000 | 0000 | YES |
| Cu14 | A4 | B4 | 0001 | 0100 | MULTI | 0100 | 0100 | YES |
| Cu15 | A5 | B5 | 0011 | 0010 | MULTI | 0110 | 0110 | YES |
| Cu21 | Cu11 | Cu11 | 1101 | 1101 | NO Op | 0000 | 0000 | YES |
| Cu22 | Cu11 | Cu12 | 1101 | 0110 | SUB | 0111 | 0111 | YES |
| Cu23 | Cu12 | Cu15 | 0110 | 0110 | ADD | 1100 | 1100 | YES |
| Cu24 | Cu12 | Cu15 | 0110 | 0110 | SUB | 0000 | 0000 | YES |
| Cu25 | Cu14 | Cu15 | 0100 | 0110 | Pass A | 0100 | 0100 | YES |
| Cu31 | Cu21 | Cu21 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu32 | Cu21 | Cu22 | 0000 | 0111 | NO Op | 0000 | 0000 | YES |
| Cu33 | Cu22 | Cu14 | 0111 | 0100 | NOR | 1000 | 1000 | YES |
| Cu34 | Cu23 | Cu24 | 1100 | 0000 | NAND | 1111 | 1111 | YES |
| Cu35 | Cu24 | Cu25 | 0000 | 0100 | NO Op | 0000 | 0000 | YES |
| Cu41 | Cu31 | Cu31 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu42 | Cu32 | Cu32 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu43 | Cu33 | Cu33 | 1000 | 1000 | Pass A | 1000 | 1000 | YES |
| Cu44 | Cu34 | Cu34 | 1111 | 1111 | Pass A | 1111 | 1111 | YES |
| Cu45 | Cu34 | Cu35 | 1111 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu51 | Cu41 | Cu42 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu52 | Cu42 | Cu42 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu53 | Cu43 | Cu43 | 1000 | 1000 | Pass A | 1000 | 1000 | YES |
| Cu54 | Cu44 | Cu44 | 1111 | 1111 | Pass A | 1111 | 1111 | YES |
| Cu55 | Cu44 | Cu45 | 1111 | 0000 | NO Op | 0000 | 0000 | YES |

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**Dataflow4(100ns)**

OUTPUT1 z2: 0000

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| STORAGE | SOURCE A | SOURCE B | A | B | OPERATION | CALCULATED OUTPUT | SIMULATED OUTPUT | MATCH |
| Cu11 | A1 | B1 | 0100 | 0010 | MULTI | 1000 | 1000 | YES |
| Cu12 | A2 | B2 | 0011 | 0100 | ADD | 0111 | 0111 | YES |
| Cu13 | Ground | Ground | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu14 | A4 | B4 | 1111 | 1010 | SUB | 0101 | 0101 | YES |
| Cu15 | A5 | B5 | 0010 | 0010 | MULTI | 0100 | 0100 | YES |
| Cu21 | Cu11 | Cu11 | 1000 | 1000 | NO Op | 0000 | 0000 | YES |
| Cu22 | Cu11 | Cu14 | 1000 | 0101 | ADD | 1101 | 1101 | YES |
| Cu23 | Cu12 | Cu15 | 0111 | 0100 | ADD | 1011 | 1011 | YES |
| Cu24 | Cu14 | Cu15 | 0101 | 0100 | SUB | 0001 | 0001 | YES |
| Cu25 | Cu14 | Cu15 | 0101 | 0110 | NO Op | 0000 | 0000 | YES |
| Cu31 | Cu21 | Cu21 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu32 | Cu22 | Cu23 | 1101 | 1011 | LSR | 0000 | 0000 | YES |
| Cu33 | Cu21 | Cu24 | 1101 | 0001 | ROL | 1011 | 1011 | YES |
| Cu34 | Cu23 | Cu24 | 1011 | 0001 | ASL | 0110 | 0110 | YES |
| Cu35 | Cu24 | Cu25 | 0001 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu41 | Cu31 | Cu32 | 0001 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu42 | Cu32 | Cu33 | 0000 | 1011 | XOR | 1011 | 1011 | YES |
| Cu43 | Cu33 | Cu34 | 1011 | 0110 | XNOR | 0010 | 0010 | YES |
| Cu44 | Cu34 | Cu34 | 0111 | 0111 | NO Op | 0000 | 0000 | YES |
| Cu45 | Cu34 | Cu35 | 0111 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu51 | Cu41 | Cu42 | 0000 | 1011 | NO Op | 0000 | 0000 | YES |
| Cu52 | Cu42 | Cu43 | 1011 | 0010 | LESS THAN | 0000 | 0000 | YES |
| Cu53 | Cu43 | Cu43 | 0011 | 0011 | NO Op | 0000 | 0000 | YES |
| Cu54 | Cu44 | Cu44 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |
| Cu55 | Cu44 | Cu45 | 0000 | 0000 | NO Op | 0000 | 0000 | YES |

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# Contribution: Sandeep has done Computational Unit, Mux’s. Hari Krishna has done Top Box and both together has designed test bench and report.