

EENG 5560 HW 2

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Block diagram for 3x3 reconfigurable computing architecture

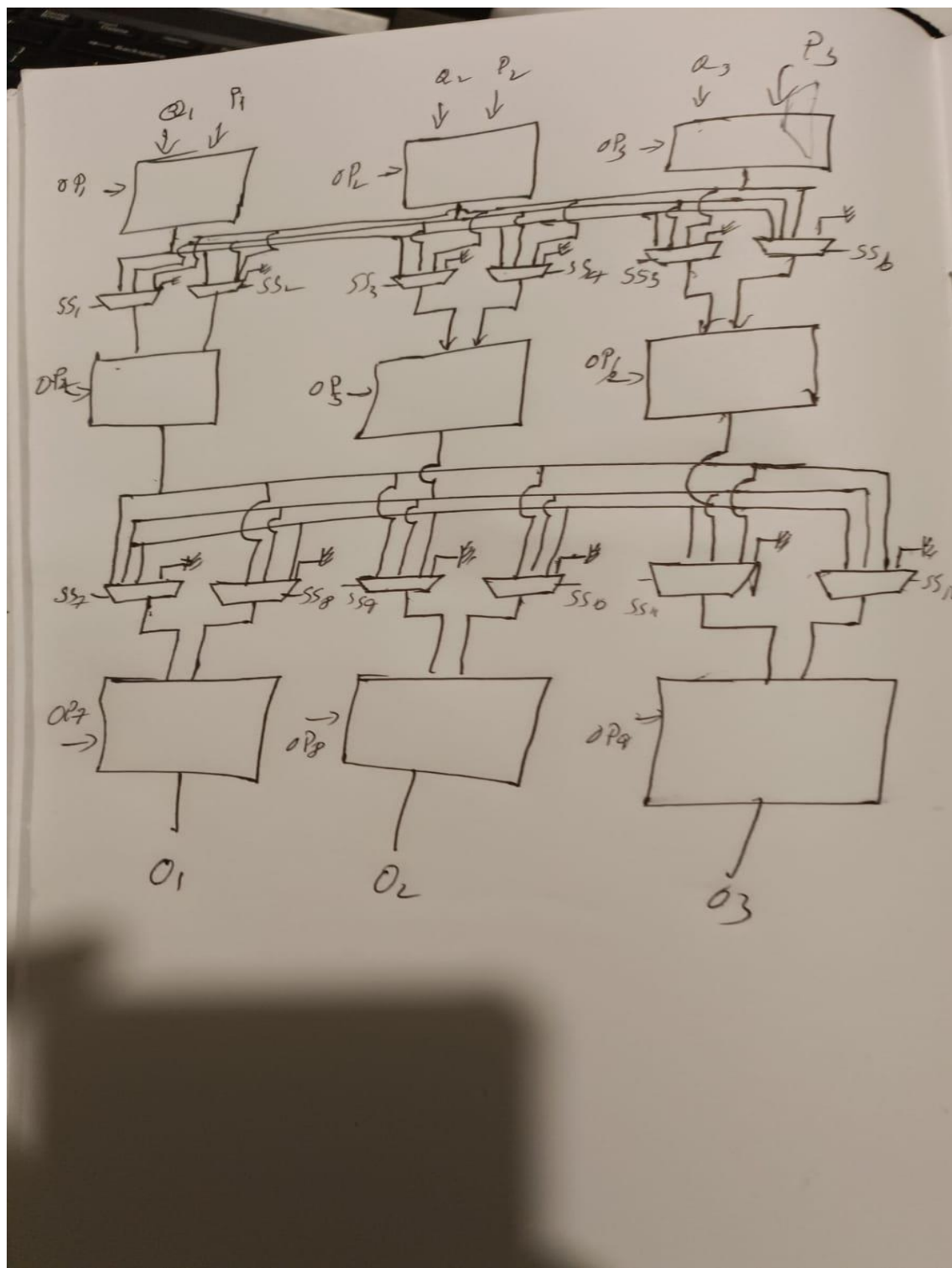


Figure 3x3 reconfigurable computing

- Overall Component: 3x3 reconfigurable computing architecture
- Overall ports:
 - Inputs: Q1, Q2, Q3, P1, P2, P3 – input to computational unit
 - Op1, Op2, Op3, Op4, Op5, Op6, Op7, Op8, Op9 – Selection lines for computational unit.
 - SS1, SS2, SS3, SS4, SS5, SS6, SS7, SS8, SS9, SS10, SS11, SS12 – Selection lines multiplexer.
 - Outputs:
 - O1, O2, O3 – Output.
- **Sub Component:**
 - Computation unit:
 - Q, P – input
 - Op – Selection input
 - O – Output
 - Multiplexer:
 - M1, M2, M3, M4 – Input
 - SS- Selection
 - Mo - Output
- Necessary intermediate signals:
Line11, Line12, Line13, Line21, Line22, Line23, Mo1, Mo2, Mo3, Mo4, Mo5, Mo6, Mo7, Mo8, Mo9, Mo10, Mo11, Mo12.

Design\Algorithm ex:

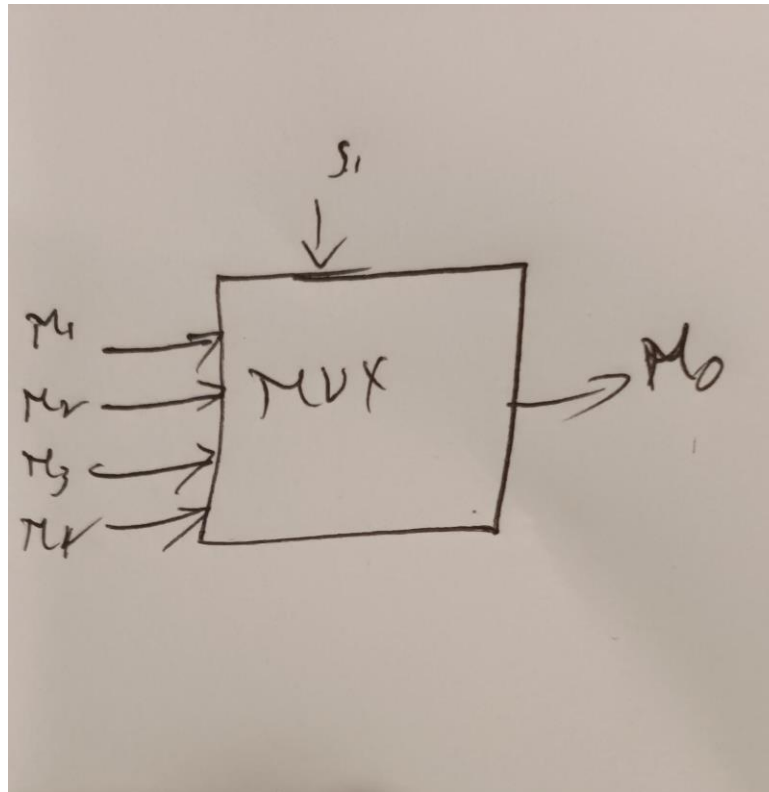


Figure 2– 4 TO 1MUX

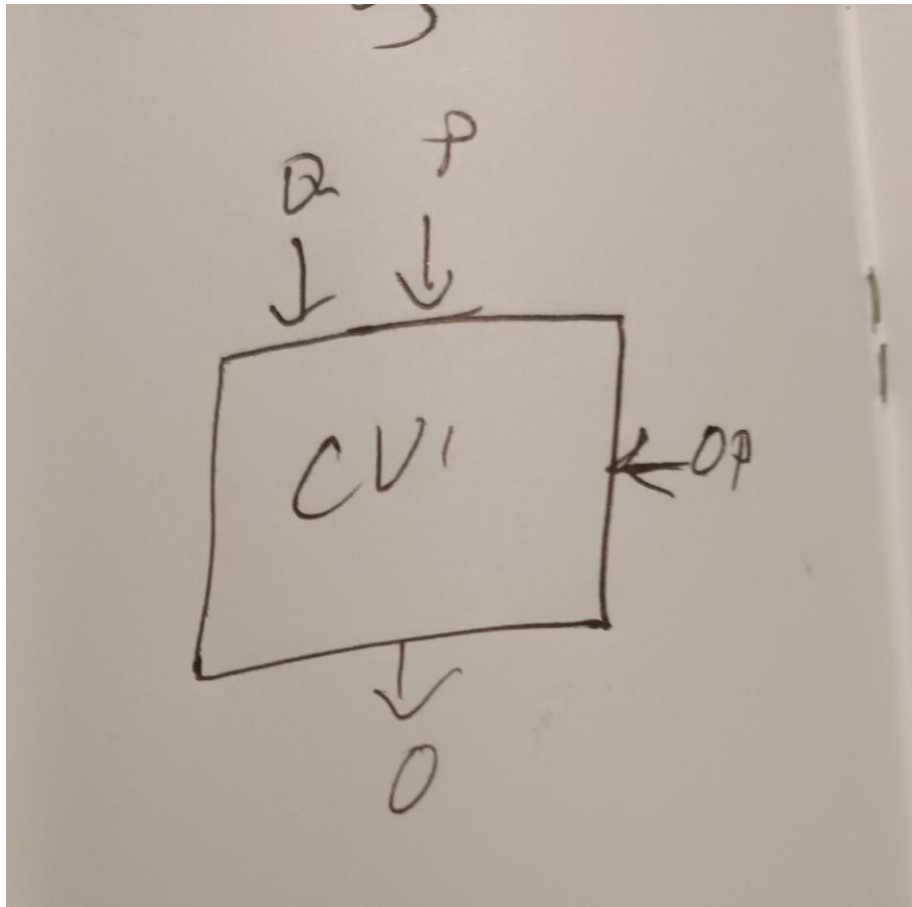


Figure 3 COMPUTATIONAL UNIT

- Overall Component:
- Overall ports:
 - Inputs:
 - Q1, V1: 4 bits
 - Q2, V2: 4 bits
 - Q3, V3: 4 bits
 - Op1, Op2, Op3, Op4, Op5, Op6, Op7, Op8, Op9: 3bits -> select line input
 - S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12: 2 Bit -> Select line input
 - Outputs:
 - :Qout1: 3 bit -> output
 - Qout2: 3 bit -> Output
 - Qout3: 3 bit -> output

Generated RTL Block Diagram/Schematic

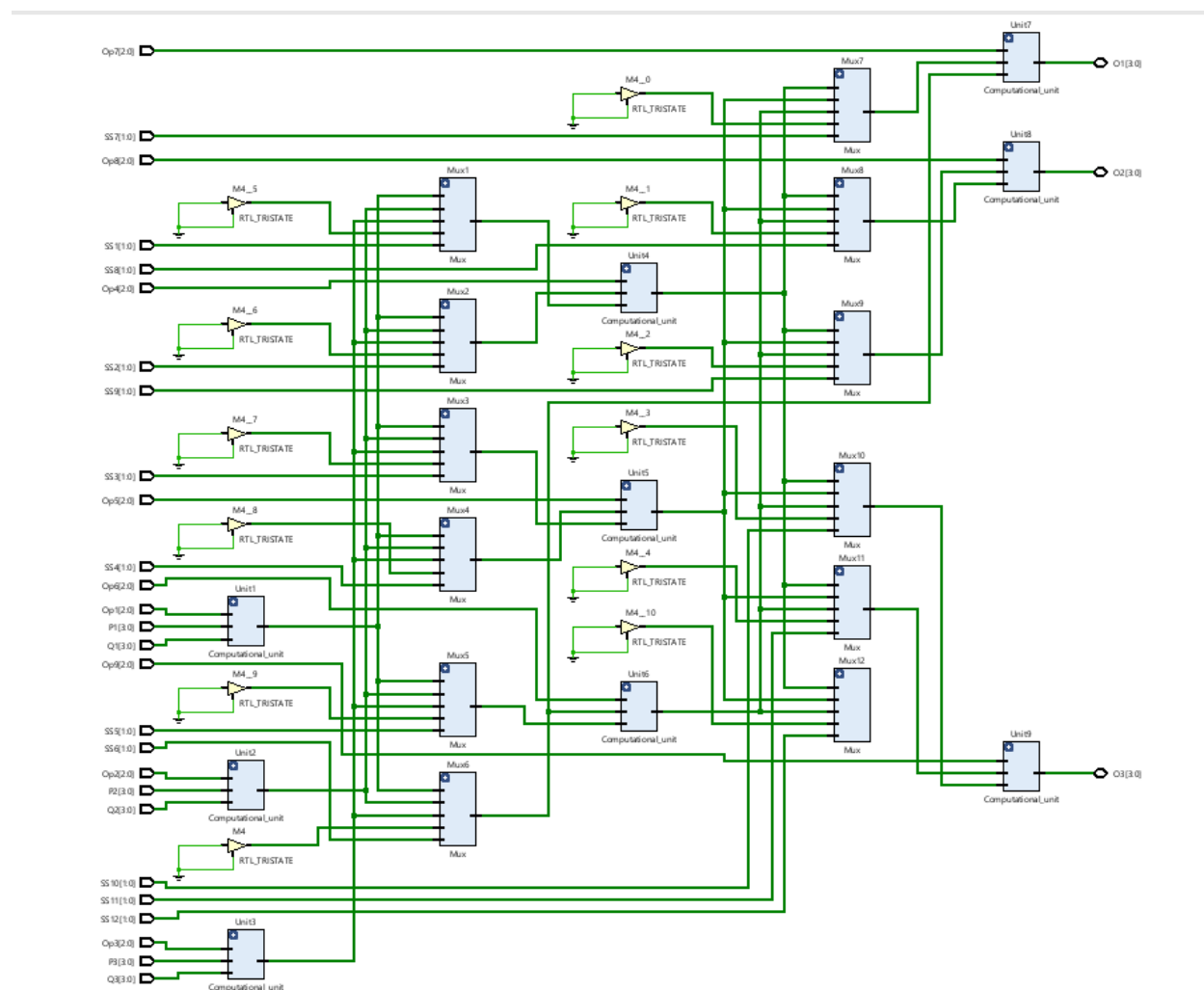
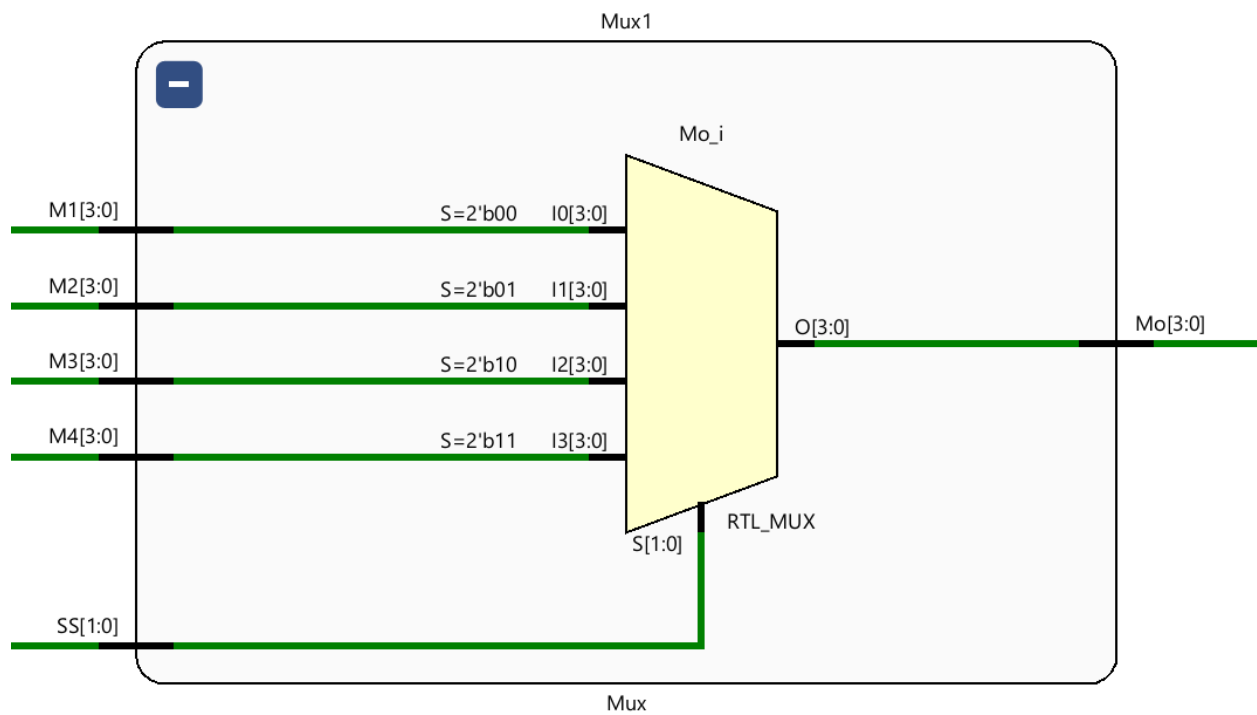
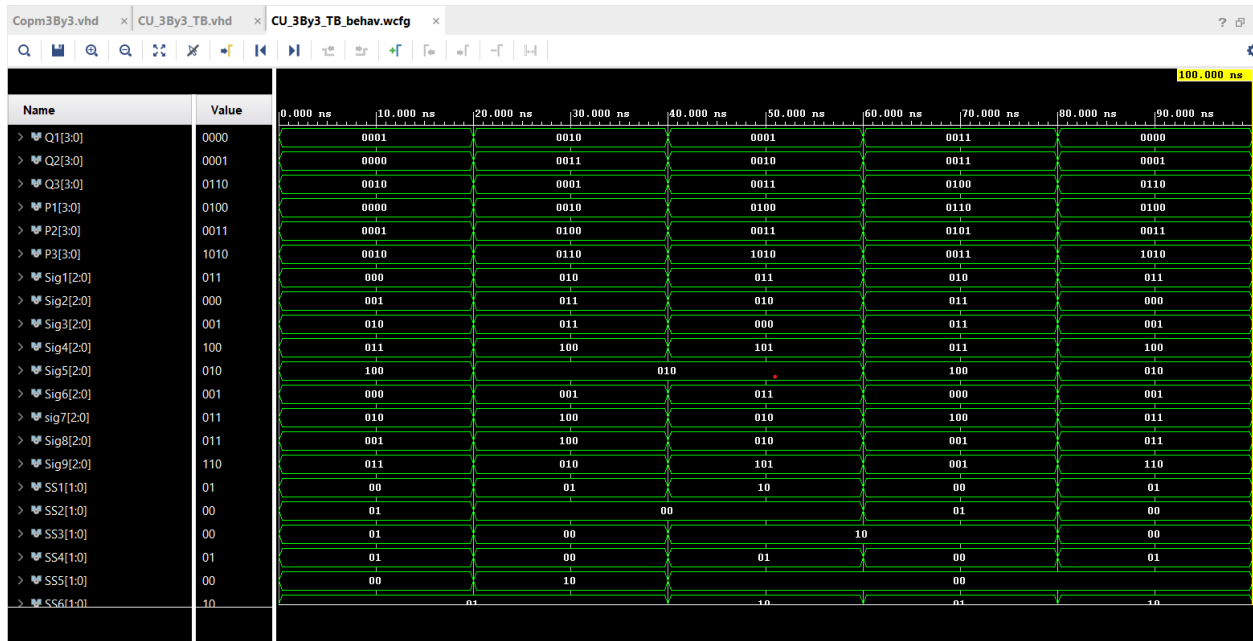


Figure 1 - generated RTL schematic.



Results

Waveforms



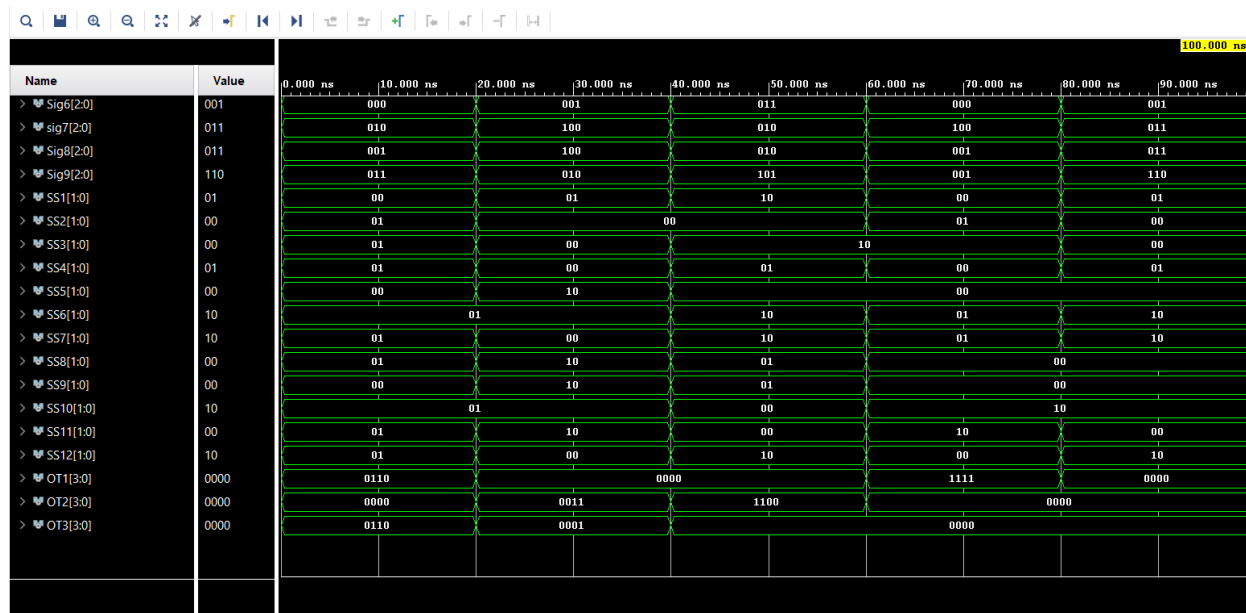


Figure 2 - Waveform

Table

																												calculations			waveforms		
	P1	P2	P3	Q1	Q2	Q3	SIG1	SIG2	SIG3	SIG4	SIG5	SIG6	SIG7	SIG8	SIG9	SS1	SS2	SS3	SS4	SS5	SS6	SS7	SS8	SS9	SS10	SS11	SS12	CT1	CT2	CT3	CT1	CT2	CT3
Testcase1:	0000	0001	0010	0001	0000	0010	0000	0001	0010	0101	0000	0000	0001	0011	0011	0000	0001	0011	0011	0000	0001	0001	0001	0001	0001	0001	0010	0011	0010	0000	0000		
Testcase2:	0001	0010	0010	0011	0001	0001	0001	0011	0101	0000	0001	0000	0000	0000	0000	0001	0000	0000	0000	0000	0001	0000	0000	0000	0001	0000	0000	0000	0001	0000	0001	0000	

