EENG 5560 HW 2

Name: *Hari Krishna *

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Block diagram for 2x2 reconfigurable computing architecture

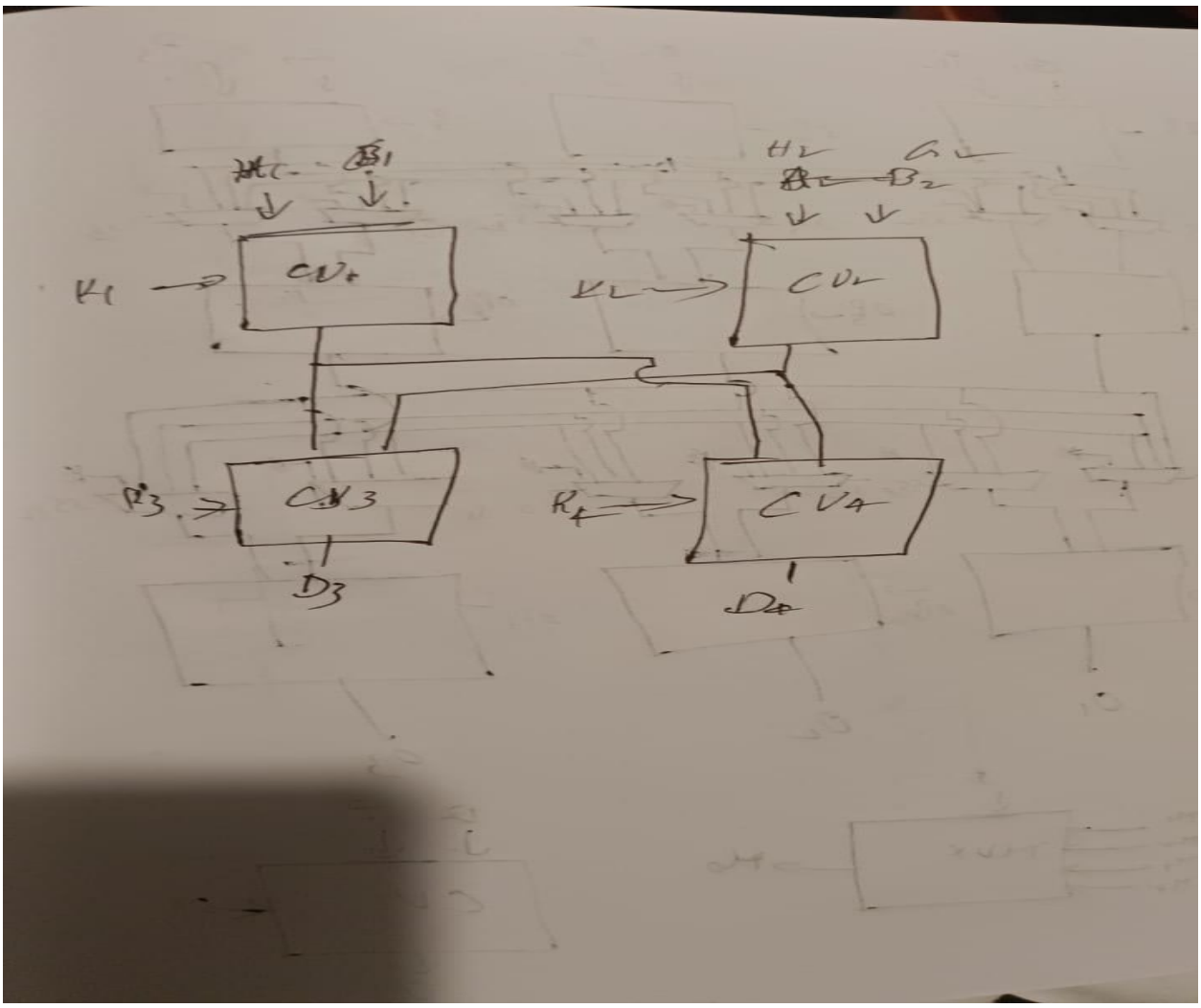

Figure 2x2 reconfigurable computing

- Overall Component: 2x2 reconfigurable computing architecture
- Overall ports:
  - Inputs: H1,H2, G1, G2 – input to computational unit
    - K1, K2, K3, K4– Selection lines for computational unit.
  - Outputs:
    - D3, D4 – Output.
- **Sub Component:**
  - Computation unit:
    - H, G– input
    - K – Selection input
    - D – Output

- Necessary intermediate signals:
    - D1,D2.

Design\Algorithm ex:

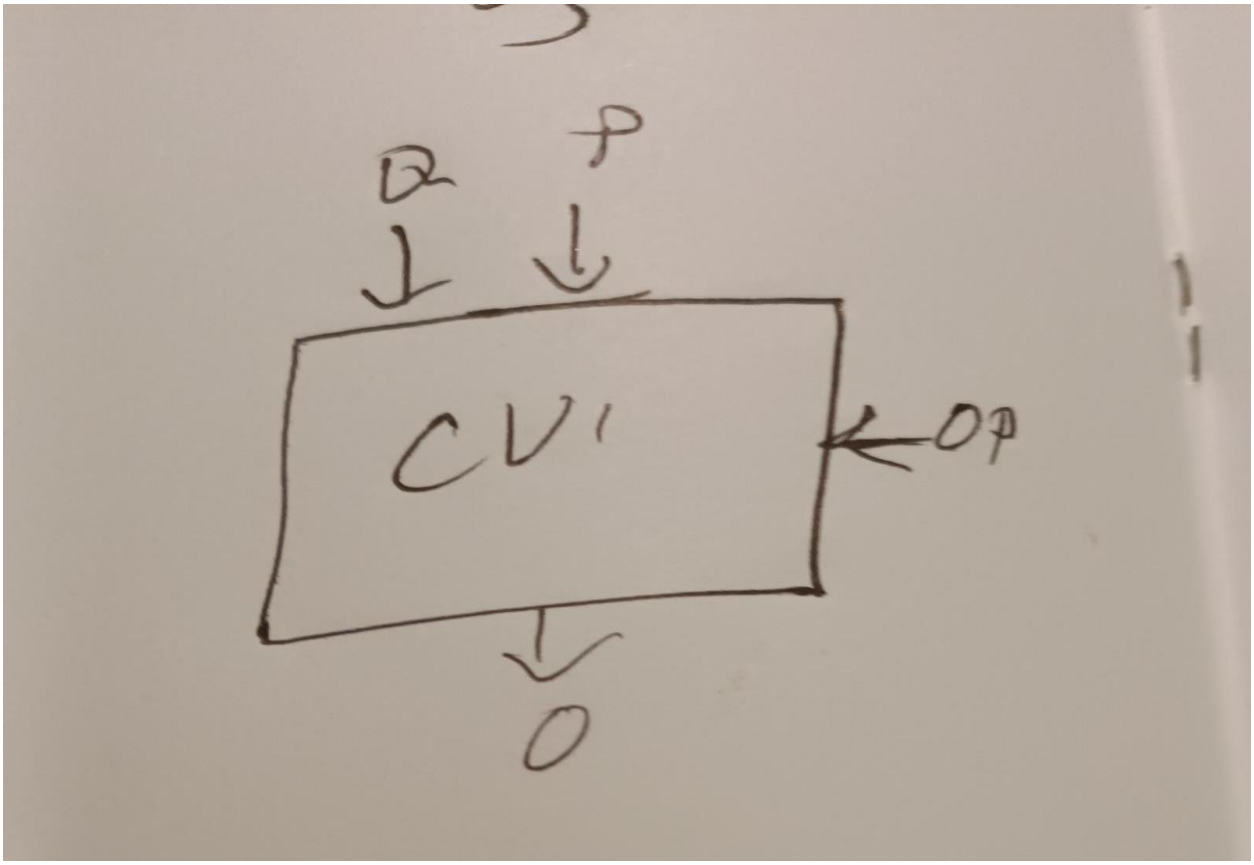

Figure 2– 2x2 reconfigurable computing

- Overall Component:
- Overall ports:
    - Inputs:
        - H1: 4 bits
        - H2: 4 bits
        - G1: 4 bits
        - G2: 4 bits
        - K1, K2, K3, K4: 3bits -> select line input
    - Outputs:
        - D3: 4 bit -> output
        - D4: 4 bit -> Output

Generated RTL Block Diagram\Schematic

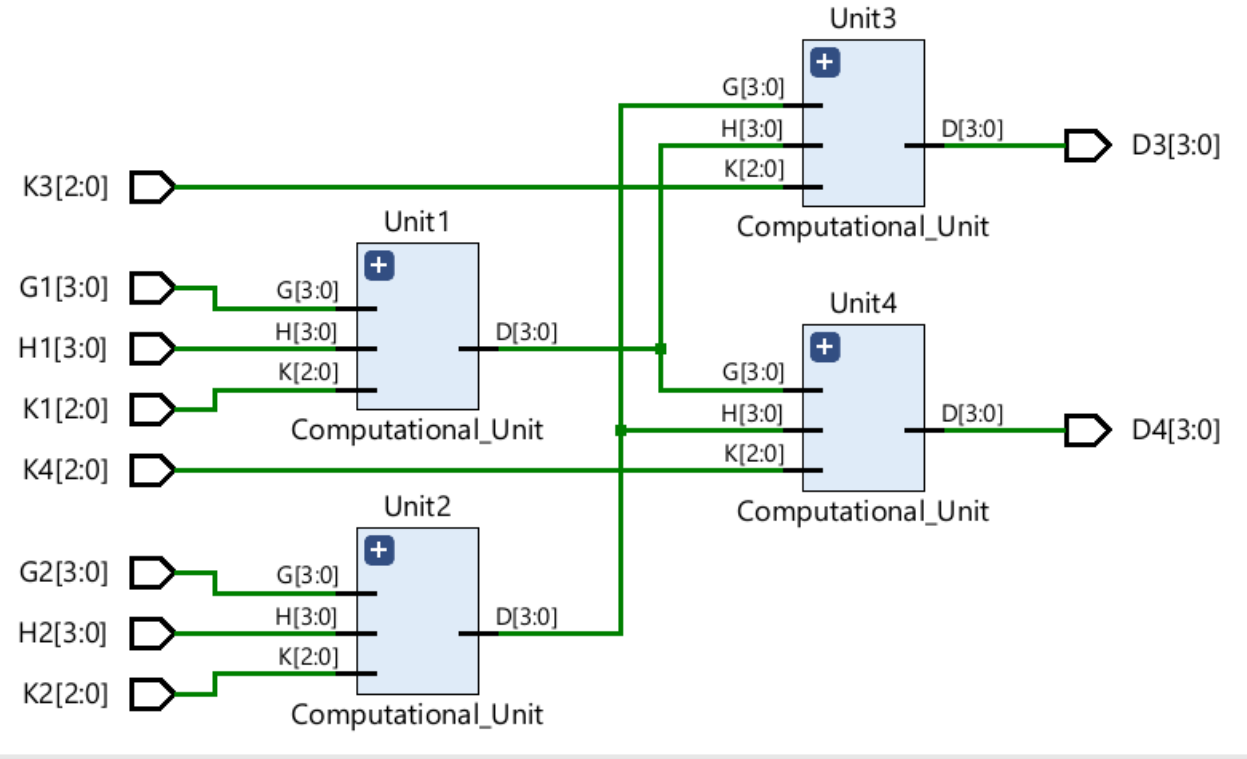

Figure 1 - generated RTL schematic.

Results

Waveforms

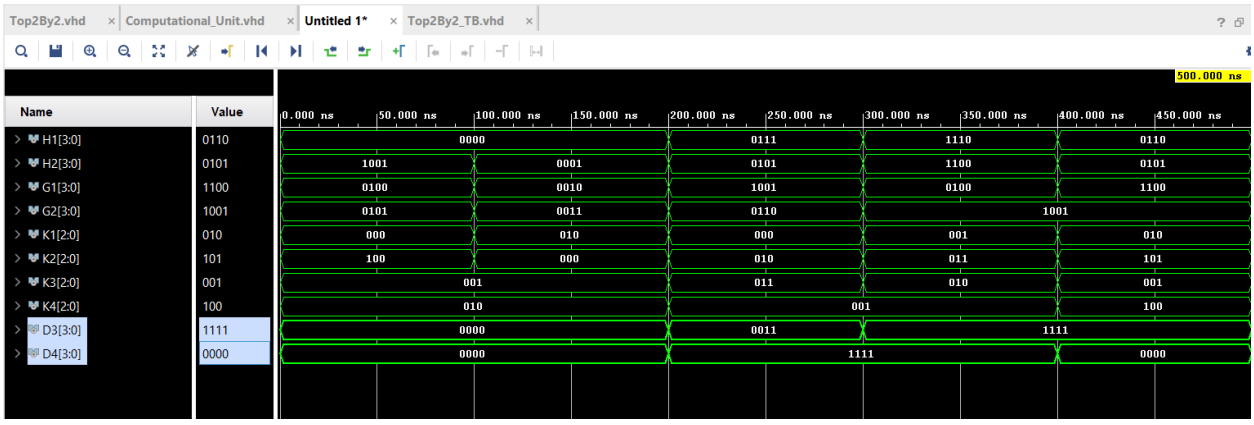

Figure 2 - Waveforms

Table

									calculations		waveforms	
	H1	H2	G1	G2	K1	K2	K3	K4	D1	D2	D1	D2
Test case 1:	0000	0011	0000	0100	000	001	010	010	0000	0000	0000	0000
Test case 2:	0111	0101	1001	0110	000	010	011	010	0000	0011	0000	1111