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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 18.02.2023 01:04:42
-- Design Name:
-- Module Name: Mux - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux is
 Port ( M1,M2,M3, M4: in std_logic_vector (3 downto 0);
```

```
 SS: in std_logic_vector(1 downto 0);
 Mo: INout std_logic_vector(3 downto 0)
--Mo: out std_logic_vector(3 downto 0)

 );
end Mux;

architecture Behavioral of Mux is
--signal temp: std_logic_vector(3 downto 0);
begin
process(M1,M2,M3, M4,SS)
begin
case SS is

-- Mo<= M1 when SS = '0' else M2;
when "00" => Mo <= M1;
when "01" => Mo <= M2;
when "10" => Mo <= M3;
when "11" => Mo <= M4;
when others => Mo <= (others => 'X');
end case;
end process;

end Behavioral;
```

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----------------------------------------------------------------------
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-- Company:
-- Engineer:
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-- Create Date: 14.02.2023 23:20:24
-- Design Name:
-- Module Name: Computational_unit - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Computational_unit is
```

```
  Port (Q, P: in std_logic_vector(3 downto 0);
  Op: in std_logic_vector(2 downto 0);
  Qout: inout std_logic_vector(3 downto 0)
      );
end Computational_unit;

architecture Behavioral of Computational_unit is

begin
process(P,Q,Op)
    begin
        case Op is
        when "000" => Qout <= to_stdlogicvector(to_bitvector(P) sll
to_integer(unsigned(Q))); -- logical shift left
        when "001" => Qout <= to_stdlogicvector(to_bitvector(P) srl
to_integer(unsigned(Q))); -- logical shift right
        when "010" => Qout <= to_stdlogicvector(to_bitvector(P) rol
to_integer(unsigned(Q))); -- Rotate shift left
        when "011" => Qout <= to_stdlogicvector(to_bitvector(P) ror
to_integer(unsigned(Q))); -- Rotate shift right
        When "100" => Qout <=to_stdlogicvector(to_bitvector(P) sla
to_integer(unsigned(Q))); -- Arthemethic shift left
        When "101" => Qout <=to_stdlogicvector(to_bitvector(P) sra
to_integer(unsigned(Q))); -- Arthemethic shift right
         When others => Qout <= P;
end case;
end process;

end Behavioral;
```

```
-- Company:
-- Engineer:
--
-- Create Date: 14.02.2023 23:12:22
-- Design Name:
-- Module Name: Comp3By3 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
--------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Comp3By3 is
Port (Q1, Q2,Q3, P1, P2, P3: in std_logic_vector(3 downto 0);
Op1, Op2,Op3,Op4,Op5, Op6, Op7, Op8, Op9: in std_logic_vector(2
```

```
downto 0);
O1, O2, O3: INout std_logic_vector(3 downto 0);

SS1, SS2, SS3, SS4, SS5, SS6, SS7, SS8, SS9, SS10, SS11, SS12  : in
std_logic_vector(1 downto 0)
);
end Comp3By3;

architecture Behavioral of Comp3By3 is

component Computational_unit is
port(Q,p: IN std_logic_vector( 3 downto 0);
Op: IN std_logic_vector(2 downto 0);
Qout: INout std_logic_vector(3 downto 0)
);
end component;
component Mux is
port ( M1,M2, M3, M4: in std_logic_vector(3 downto 0);
SS: in std_logic_vector(1 downto 0);
Mo: Inout std_logic_vector( 3 downto 0));
end component;
signal Line11, Line12, Line13, Line21,Line22, Line23:
std_logic_vector(3 downto 0);
signal Mo1,Mo2, Mo3, Mo4, Mo5, Mo6,Mo7,Mo8, Mo9, Mo10, Mo11, Mo12 :
 std_logic_vector(3 downto 0);
begin
Unit1: Computational_unit port map(Q => Q1,P=> P1, Op => Op1, Qout
=> Line11);
Unit2: Computational_unit port map(Q => Q2,P => P2,Op => Op2, Qout
=> Line12);
Unit3: Computational_Unit port map(Q => Q3,P => P3, Op => Op3, Qout
=> Line13);
Mux1: Mux port map(M1 => Line11, M2 => Line12, M3 => Line13,M4 =>
"ZZZZ", SS => SS1,Mo => Mo1);
Mux2: Mux port map(M1 => Line11, M2 => Line12, M3 => Line13,M4 =>
"ZZZZ", SS => SS2,Mo => Mo2);
Mux3: Mux port map(M1 => Line11, M2 => Line12, M3 => Line13,M4 =>
```

```
"ZZZZ", SS => SS3,Mo => Mo3);
Mux4: Mux port map(M1 => Line11, M2 => Line12, M3 => Line13,M4 =>
"ZZZZ", SS => SS4,Mo => Mo4);
Mux5: Mux port map(M1 => Line11, M2 => Line12, M3 => Line13,M4 =>
"ZZZZ", SS => SS5,Mo => Mo5);
Mux6: Mux port map(M1 => Line11, M2 => Line12, M3 => Line13,M4 =>
"ZZZZ", SS => SS6,Mo => Mo6);
Unit4: Computational_Unit port map(Q => Mo1,P=> Mo2, Op => Op4,
Qout => Line21);
Unit5: Computational_Unit port map(Q => Mo3,P =>Mo4, Op => Op5,
Qout => Line22);
Unit6: Computational_Unit port map(Q => Mo5, P => Mo6, Op => Op6,
Qout => Line23);
Mux7: Mux port map(M1 => Line21, M2 => Line22,M3 => Line23, M4 =>
"ZZZZ", SS => SS7,Mo => Mo7);
Mux8: Mux port map(M1 => Line21, M2 => Line22,M3 => Line23, M4 =>
"ZZZZ", SS => SS8,Mo => Mo8);
Mux9: Mux port map(M1 => Line21, M2 => Line22,M3 => Line23, M4 =>
"ZZZZ", SS => SS9,Mo => Mo9);
Mux10: Mux port map(M1 => Line21, M2 => Line22,M3 => Line23, M4 =>
"ZZZZ", SS => SS10,Mo => Mo10);
Mux11: Mux port map(M1 => Line21, M2 => Line22,M3 => Line23, M4 =>
"ZZZZ", SS => SS11,Mo => Mo11);
Mux12: Mux port map(M1 => Line21, M2 => Line22,M3 => Line23, M4 =>
"ZZZZ", SS => SS12,Mo => Mo12);

Unit7: Computational_Unit port map(Q => Mo6,P =>Mo7, Op => Op7,
Qout => O1);
Unit8: Computational_Unit port map(Q => Mo8,P =>Mo9, Op => Op8,
Qout => O2);
Unit9: Computational_Unit port map(Q => Mo10,P =>Mo11, Op => Op9,
Qout => O3);

end Behavioral;
```

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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 15.02.2023 14:30:43
-- Design Name:
-- Module Name: CU_3By3_TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity CU_3By3_TB is
```

```
--  Port ( );
end CU_3By3_TB;

architecture Behavioral of CU_3By3_TB is
signal Q1, Q2,Q3,P1,P2,P3,OT1 ,OT2 ,OT3 : std_logic_vector(3 downto
0);
signal Sig1, Sig2, Sig3, Sig4, Sig5, Sig6, sig7, Sig8, Sig9:
std_logic_vector(2 downto 0);
signal SS1, SS2, SS3, SS4, SS5, SS6,SS7, SS8, SS9, SS10, SS11, SS12
 : std_logic_vector (1 downto 0);
begin
Top_Box: entity work.Comp3By3(Behavioral)
port map (P1 =>P1, P2=>P2, P3 => P3, Q1=>Q1 ,Q2 =>Q2, Q3 => Q3, Op1
=> Sig1, Op2 =>Sig2, Op3 =>Sig3, Op4 =>Sig4,Op5 =>Sig5, Op6 =>Sig6,
Op7 =>Sig7,Op8 =>Sig8,Op9 =>Sig9, O1 => OT1, O2 => OT2, O3 =>OT3,
SS1 => SS1, SS2=> SS2, SS3 => SS3, SS4 => SS4, SS5 => SS5, SS6 =>
SS6, SS7 => SS7, SS8=> SS8, SS9 => SS9, SS10 => SS10, SS11 => SS11,
SS12 => SS12);

Stir: process
begin
P1 <= "0000";P2 <= "0001"; P3 <= "0010" ;Q1 <= "0001"; Q2 <=
"0000";Q3 <= "0010"; Sig1 <= "000"; Sig2 <= "001"; Sig3 <= "010";
Sig4 <= "011"; Sig5 <= "100"; Sig6 <= "000"; Sig7 <= "010"; Sig8 <=
"001"; Sig9 <= "011"; SS1 <="00"; SS2 <= "01"; SS3 <= "01"; SS4 <=
"01";SS5 <="00"; SS6 <= "01"; SS7 <= "01"; SS8 <= "01";SS9 <="00";
SS10 <= "01"; SS11 <= "01"; SS12 <= "01";Wait for 20ns;
P1 <= "0010";P2 <= "0100"; P3 <= "0110" ;Q1 <= "0010"; Q2 <=
"0011";Q3 <= "0001"; Sig1 <= "010"; Sig2 <= "011"; Sig3 <= "011";
Sig4 <= "100"; Sig5 <= "010"; Sig6 <= "001"; Sig7 <= "100"; Sig8 <=
"100"; Sig9 <= "010"; SS1 <="01"; SS2 <= "00"; SS3 <= "00"; SS4 <=
"00";SS5 <="10"; SS6 <= "01"; SS7 <= "00"; SS8 <= "10";SS9 <="10";
SS10 <= "01"; SS11 <= "10"; SS12 <= "00";Wait for 20ns;
P1 <= "0100";P2 <= "0011"; P3 <= "1010" ;Q1 <= "0001"; Q2 <=
"0010";Q3 <= "0011"; Sig1 <= "011"; Sig2 <= "010"; Sig3 <= "000";
Sig4 <= "101"; Sig5 <= "010"; Sig6 <= "011"; Sig7 <= "010"; Sig8 <=
"010"; Sig9 <= "101"; SS1 <="10"; SS2 <= "00"; SS3 <= "10";SS4 <=
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```
"01";SS5 <="00"; SS6 <= "10"; SS7 <= "10"; SS8 <= "01";SS9 <="01";
SS10 <= "00"; SS11 <= "00"; SS12 <= "10"; Wait for 20ns;
P1 <= "0110";P2 <= "0101"; P3 <= "0011" ;Q1 <= "0011"; Q2 <=
"0011";Q3 <= "0100"; Sig1 <= "010"; Sig2 <= "011"; Sig3 <= "011";
Sig4 <= "011"; Sig5 <= "100"; Sig6 <= "000"; Sig7 <= "100"; Sig8 <=
"001"; Sig9 <= "001"; SS1 <="00"; SS2 <= "01"; SS3 <= "10";SS4 <=
"00";SS5 <="00"; SS6 <= "01"; SS7 <= "01"; SS8 <= "00";SS9 <="00";
SS10 <= "10"; SS11 <= "10"; SS12 <= "00"; Wait for 20ns;
P1 <= "0100";P2 <= "0011"; P3 <= "1010" ;Q1 <= "0000"; Q2 <=
"0001";Q3 <= "0110"; Sig1 <= "011"; Sig2 <= "000"; Sig3 <= "001";
Sig4 <= "100"; Sig5 <= "010"; Sig6 <= "001"; Sig7 <= "011"; Sig8 <=
"011"; Sig9 <= "110";SS1 <="01"; SS2 <= "00"; SS3 <= "00";SS4 <=
"01"; SS5 <="00"; SS6 <= "10"; SS7 <= "10";SS8 <= "00"; SS9 <="00";
SS10 <= "10"; SS11 <= "00"; SS12 <= "10"; Wait for 20ns;
--W1 <= "0100";W2 <= "0101"; W3 <= "0010" ;Sig1 <= "010"; Sig2 <=
"011"; Sig3 <= "011"; Sig4 <= "011"; Sig5 <= "100"; Sig6 <= "000";
Sig7 <= "100"; Sig8 <= "100"; Sig9 <= "011";SS1 <="1"; SS2 <= "1";
SS3 <= "0";SS4 <= "1"; Wait for 20ns;
finish;
end process;
end Behavioral;
```