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-- Company:
-- Engineer:
--
-- Create Date: 11.02.2023 14:00:59
-- Design Name:
-- Module Name: Computational_Unit - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.ALL;
use IEEE.std_logic_unsigned.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity Computational_Unit is
Port ( H,G : IN std_logic_vector(3 downto 0);
        K: IN std_logic_vector( 2 downto 0);
        D: OUT std_logic_vector(3 downto 0)
--        I: INOUT std_logic_vector(15 downto 0)
);
end Computational_Unit;

architecture Behavioral of Computational_Unit is
signal Line1,Line2: signed(3 downto 0);
signal mult: std_logic_vector(7 downto 0);
begin
Line1 <= signed(H);
Line2 <= signed(G);
mult <= H*G;
process(H,G,K)
    begin
        case K is
        when "000" =>D <= std_logic_vector(Line1 - Line2);
        when "001" => IF( Line1 > Line2) THEN D <= "1111"; else D
<= "0000"; END IF;
        when "010" => IF( Line1 < Line2) THEN D <= "1111"; else D
<= "0000"; END IF;
        when "011" => D <= std_logic_vector(Line1 + Line2);
        when "100" => IF ( Line1 = Line2) THEN D <= "1111"; else D
<= "0000"; end IF;
        when "101" => D <= mult(3 downto 0);
--        D <= I(7 downto 0);
        when others => D <= (others => 'Z');
        end case;
        end process;
end Behavioral;
```

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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 11.02.2023 13:59:29
-- Design Name:
-- Module Name: Top2By2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top2By2 is
Port (H1,H2, G1, G2: IN std_logic_vector(3 downto 0);
```

```
    K1, K2, K3, K4: IN std_logic_vector (2 downto 0);
    D3, D4: OUT std_logic_vector(3 downto 0)

 );

end Top2By2;

architecture Behavioral of Top2By2 is
component Computational_Unit is
    port(H,G: IN std_logic_vector(3 downto 0);
    K: IN std_logic_vector(2 downto 0);
    D: OUT std_logic_vector(3 downto 0));
end component;

--component Mux is
--    port(M1,M2: IN std_logic_vector(3 downto 0);
--    SS: in std_logic_vector(0 downto 0);
--    Mo: out std_logic_vector(3 downto 0));
--    end component;

signal D1,D2: std_logic_vector(3 downto 0);
begin
    Unit1: Computational_Unit port map (H => H1, G => G1, K => K1,
D => D1);
    Unit2: Computational_Unit port map ( H => H2, G => G2, K => K2,
D => D2);
    Unit3: Computational_Unit port map (H => D1, G => D2, K => K3,
D => D3);
    Unit4: Computational_Unit port map (H => D2, G => D1, K => K4,
D => D4);
    End Behavioral;
```

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 11.02.2023 15:12:02
-- Design Name:
-- Module Name: Top2By2_TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top2By2_TB is
```

```
--  Port ( );
end Top2By2_TB;

architecture Behavioral of Top2By2_TB is
signal H1,H2, G1,G2, D3, D4 : std_logic_vector(3 downto 0);
signal K1, K2, K3, K4: std_logic_vector(2 downto 0);

begin
Final_Unit: entity work.Top2By2(Behavioral)
port map (H1 => H1, H2 => H2, G1 => G1, G2 => G2, D3 => D3 , D4 =>
D4, K1 => K1, K2 => K2, K3 => K3, K4 => K4);
STIM: process
begin
H1<= "0000"; H2 <= "1001"; G1 <= "0100";G2 <= "0101"; K1 <= "000";
K2 <= "100"; K3 <= "001"; K4 <= "010"; wait for 100ns;
H1<= "0000"; H2 <= "0001"; G1 <= "0010";G2 <= "0011"; K1 <= "010";
K2 <= "000"; K3 <= "001"; K4 <= "010"; wait for 100ns;
H1<= "0111"; H2 <= "0101"; G1 <= "1001";G2 <= "0110"; K1 <= "000";
K2 <= "010"; K3 <= "011"; K4 <= "001";wait for 100ns;
H1<= "1110"; H2 <= "1100"; G1 <= "0100";G2 <= "1001"; K1 <= "001";
K2 <= "011"; K3 <= "010"; K4 <= "001";wait for 100ns;
H1<= "0110"; H2 <= "0101"; G1 <= "1100";G2 <= "1001"; K1 <= "010";
K2 <= "101"; K3 <= "001"; K4 <= "100";wait for 100ns;
finish;
end process;
end Behavioral;
```