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-- Company:
-- Engineer:
--
-- Create Date: 11.02.2023 14:00:59
-- Design Name:
-- Module Name: Computational_Unit - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.ALL;
use IEEE.std_logic_unsigned.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity Computational_Unit is
Port ( Q,P : IN std_logic_vector(3 downto 0);
        Op: IN std_logic_vector( 2 downto 0);
        Qout: OUT std_logic_vector(3 downto 0)

);
end Computational_Unit;

architecture Behavioral of Computational_Unit is
signal Line1,Line2: signed(3 downto 0);
signal mult: std_logic_vector(7 downto 0);
begin
Line1 <= signed(Q);
Line2 <= signed(P);
mult <= Q*P;
process(Q,P,Op)
    begin
        case Op is
        when "000" =>Qout <= std_logic_vector(Line1 - Line2);
        when "001" => IF( Line1 > Line2) THEN Qout <= "1111"; else
Qout <= "0000"; END IF;
        when "010" => IF( Line1 < Line2) THEN Qout <= "1111"; else
Qout <= "0000"; END IF;
        when "011" => Qout <= std_logic_vector(Line1 + Line2);
        when "100" => IF ( Line1 = Line2) THEN Qout <= "1111"; else
Qout <= "0000"; end IF;
        when "101" => Qout <= mult(3 downto 0);
--        D <= I(7 downto 0);
        when others => Qout <= (others => 'Z');
        end case;
        end process;
end Behavioral;
```

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----------------------------------------------------------------------
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-- Company:
-- Engineer:
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-- Create Date: 18.02.2023 01:04:42
-- Design Name:
-- Module Name: Mux - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------
--------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux is
 Port ( M1,M2,M3, M4, M5, M6,M7,M8: in std_logic_vector (3 downto
```

```
0);
 SS: in std_logic_vector(2 downto 0);
 Mo: INout std_logic_vector(3 downto 0)
 );
end Mux;

architecture Behavioral of Mux is
--signal temp: std_logic_vector(3 downto 0);
begin
process(M1,M2,M3, M4, M5, M6,M7,M8,SS)
begin
case SS is

when "000" => Mo <= M1;
when "001" => Mo <= M2;
when "010" => Mo <= M3;
when "011" => Mo <= M4;
when "100" => Mo <= M5;
when "101" => Mo <= M6;
when "110" => Mo <= M7;
when "111" => Mo <= M8;
when others => Mo <= (others => '0');
end case;
end process;

end Behavioral;
```

```
-- Company:
-- Engineer:
--
-- Create Date: 14.02.2023 23:12:22
-- Design Name:
-- Module Name: Comp3By3 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
--------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Comp3By3 is
Port (Q1,Q2,Q3,Q4,Q6,Q7,Q8, P1, P2, P3, P4, P6, P7,P8: in
std_logic_vector(3 downto 0);
```

```
Op1,Op2,Op3,Op4,Op5, Op6, Op7, Op8, Op9: in std_logic_vector(2
downto 0);
O1: out std_logic_vector(3 downto 0);
SS1, SS2  : in std_logic_vector(2 downto 0)
);
end Comp3By3;

architecture Behavioral of Comp3By3 is

component Computational_unit is
port(Q,p: IN std_logic_vector( 3 downto 0);
Op: IN std_logic_vector(2 downto 0);
Qout: out std_logic_vector(3 downto 0)
);
end component;
component Mux is
port (M1,M2,M3, M4, M5, M6,M7,M8 : in std_logic_vector(3 downto 0);
SS: in std_logic_vector(2 downto 0);
Mo: Inout std_logic_vector( 3 downto 0));
end component;
signal Line11, Line12, Line13, Line21,Line22, Line23, Line31,
Line32: std_logic_vector(3 downto 0);
signal Mx1, Mx2: std_logic_vector(3 downto 0);
begin
Unit1: Computational_unit port map(Q => Q1,P=> P1, Op => Op1, Qout
=> Line11);
Unit2: Computational_unit port map(Q => Q2,P => P2,Op => Op2, Qout
=> Line12);
Unit3: Computational_Unit port map(Q => Q3,P => P3, Op => Op3, Qout
=> Line13);
Unit4: Computational_Unit port map(Q => Q4,P=> P4, Op => Op4, Qout
=> Line21);
MUX1: Mux port map (M1=> Line11, M2=> Line12, M3=> Line13,M4=>
Line21,M5=> Line23,M6=> Line31,M7 => Line32,M8 => "0000",SS =>SS1,
Mo => Mx1 );
MUX2: Mux port map (M1=> Line11, M2=> Line12, M3=> Line13,M4=>
Line21,M5=> Line23,M6=> Line31,M7 => Line32,M8 => "0000",SS =>SS2,
```

```
Mo => Mx2 );
Unit5: Computational_Unit port map(Q =>Mx1 ,P =>Mx2 , Op => Op5,
Qout => Line22);
Unit6: Computational_Unit port map(Q => Q6, P => P6, Op => Op6,
Qout => Line23);
Unit7: Computational_Unit port map(Q => Q7,P =>P7, Op => Op7, Qout
=> Line31);
Unit8: Computational_Unit port map(Q => Q8,P =>P8, Op => Op8, Qout
=> Line32);
Unit9: Computational_Unit port map(Q => Line22,P =>Line22, Op =>
Op9, Qout =>O1 );

end Behavioral;
```

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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 15.02.2023 14:30:43
-- Design Name:
-- Module Name: CU_3By3_TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.finish;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity CU_3By3_TB is
```

```
--  Port ( );
end CU_3By3_TB;

architecture Behavioral of CU_3By3_TB is
signal Q1, Q2,Q3,Q4,Q6,Q7,Q8, P1, P2, P3, P4, P6, P7,P8 :
std_logic_vector(3 downto 0);
signal Op1, Op2,Op3,Op4,Op5, Op6, Op7, Op8, Op9: std_logic_vector(2
downto 0);
signal SS1, SS2 : std_logic_vector (2 downto 0);
Signal O1: std_logic_vector(3 downto 0);
begin
Comp: entity work.Comp3By3(Behavioral)
port map (P1 =>P1, P2=>P2, P3 => P3,P4 =>P4, P6=>P6, P7 => P7,P8
=>P8, Q1=>Q1 ,Q2 =>Q2, Q3 => Q3,Q4=>Q4 ,Q6 =>Q6, Q7 => Q7,Q8 => Q8,
Op1 => Op1, Op2 =>Op2, Op3 =>Op3, Op4 =>Op4,Op5 =>Op5, Op6 =>Op6,
Op7 =>Op7,Op8 =>Op8,Op9 =>Op9,SS1 =>SS1,SS2 =>SS2, O1 => O1 );

Stir: process
begin
P1 <= "0100";P2 <= "0000"; P3 <= "1010" ;P4 <="1000"; P6<="1100";
P7 <="0110";P8 <="0010"; Q1 <= "0000"; Q2 <= "0001"; Q3 <=
"0100";Q4<= "0010" ;Q6 <="0100"; Q7 <="0010";Q8 <="0000"; Op1 <=
"011"; Op2 <="100"; Op3 <="010"; Op4 <="001"; Op5 <="011"; Op6 <=
"001";Op7 <="101";Op8 <="000";Op9 <="011";SS1 <="010";SS2 <="001";
wait for 100ns;
P1 <= "0010";P2 <= "0100"; P3 <= "0110" ;P4 <="1010"; P6<="1000";
P7 <="0111";P8 <="0011"; Q1 <= "0010"; Q2 <= "0011"; Q3 <=
"0011";Q4<= "0011" ;Q6 <="0010"; Q7 <="0100";Q8 <="0100"; Op1
<="001"; Op2 <="001"; Op3 <="000"; Op4 <="011";Op5 <="011"; Op6 <=
"001";Op7 <="011";Op8 <="010";Op9 <="011"; SS1 <="001"; SS2 <=
"000";Wait for 100ns;
P1 <= "0100";P2 <= "0101"; P3 <= "0111" ;P4 <="1000"; P6<="1100";
P7 <="0001";P8 <="0001"; Q1 <= "0100"; Q2 <= "0010"; Q3 <=
"0001";Q4<= "0100" ;Q6 <="0010"; Q7 <="1000";Q8 <="0010"; Op1
<="011"; Op2 <="001"; Op3 <="010"; Op4 <="001";Op5 <="000"; Op6 <=
"101";Op7 <="001";Op8 <="011";Op9 <="011"; SS1 <="010"; SS2 <=
"001";Wait for 100ns;
```

```
P1 <= "0000";P2 <= "0100"; P3 <= "0101" ;P4 <="0100"; P6<="0011";
P7 <="0101";P8 <="0011"; Q1 <= "0010"; Q2 <= "0010"; Q3 <=
"0011";Q4<= "0100" ;Q6 <="0011"; Q7 <="0010";Q8 <="0001"; Op1
<="001"; Op2 <="011"; Op3 <="011"; Op4 <="000";Op5 <="000"; Op6 <=
"001";Op7 <="100";Op8 <="101";Op9 <="001"; SS1 <="110"; SS2 <=
"011";Wait for 100ns;
P1 <= "0010";P2 <= "0110"; P3 <= "0100" ;P4 <="0001"; P6<="1000";
P7 <="1000";P8 <="0100"; Q1 <= "0011"; Q2 <= "0010"; Q3 <=
"0001";Q4<= "0110" ;Q6 <="0001"; Q7 <="0100";Q8 <="0000"; Op1
<="100"; Op2 <="000"; Op3 <="010"; Op4 <="000";Op5 <="001"; Op6 <=
"000";Op7 <="010";Op8 <="001";Op9 <="001"; SS1 <="000"; SS2 <=
"000";Wait for 100ns;
finish;
end process;
end Behavioral;
```