EENG 5560 HW 3

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# Block diagram for 3x3 matrix architecture

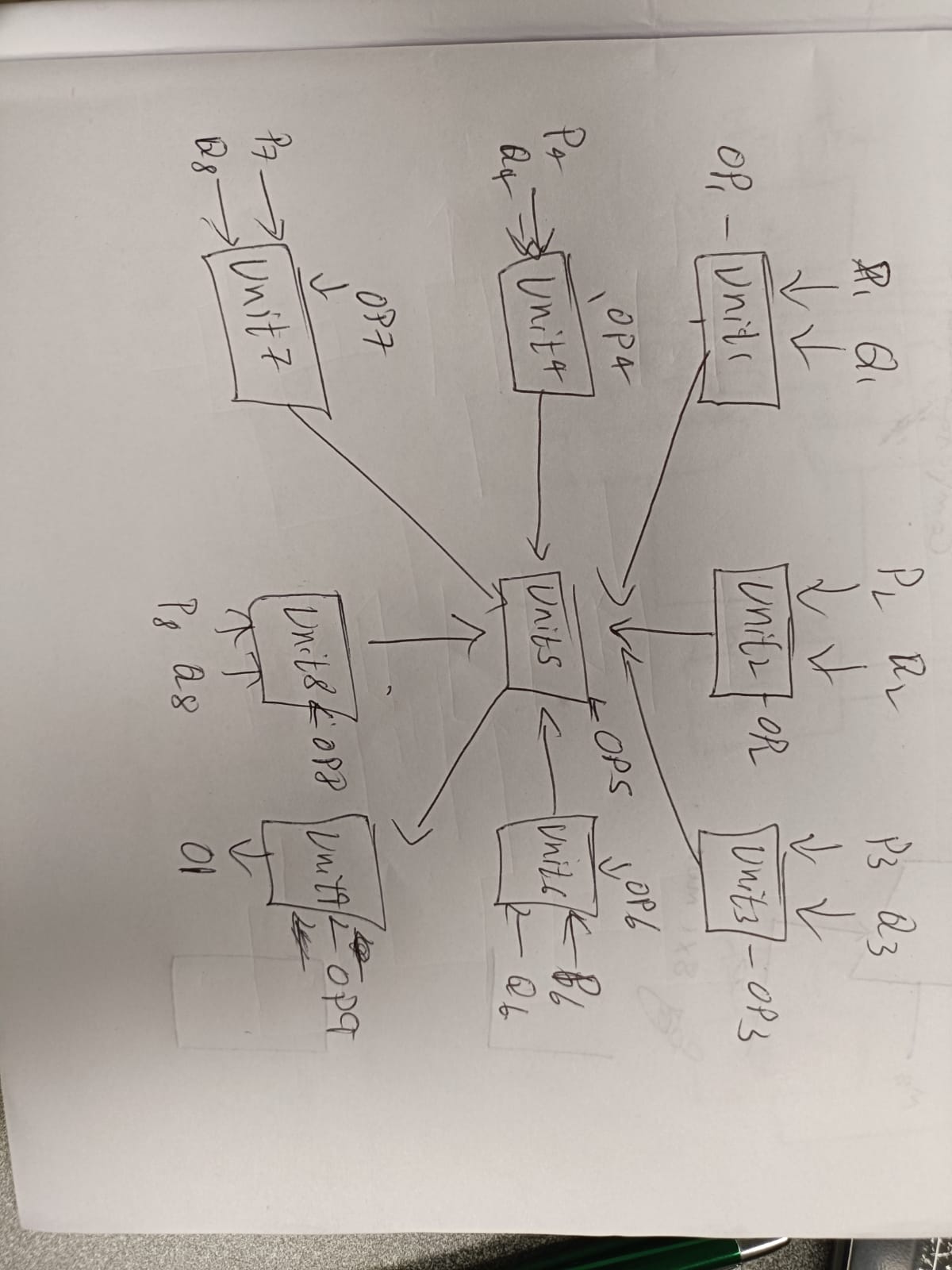


Figure 3x3 matrix

* Overall Component: 3x3 matrix architecture
* Overall ports:
  + Inputs: Q1,Q2,Q3,Q4,Q6,Q7,Q8, P1, P2, P3, P4, P6, P7,P8 – input to computational unit
    - Op1, Op2, Op3, Op4, Op5, Op6, Op7, Op8, Op9 – Selection lines for computational unit.
    - SS1, SS2 - Selection lines multiplexer.
  + Outputs:
    - O1 – Output.
* **Sub Component:**
* Computation unit: 9 computational unit used
  + - P,Q – input
    - Op – Selection input
    - Qout – Output
* Multiplexer: 2 – 8 to 1 mux
  + M1, M2, M3, M4, M5, M6, M7, M8 – Input
  + SS- Selection
  + Mo- Output
* Necessary intermediate signals:
  + Line11, Line12, Line13, Line21,Line22, Line23, Line31, Line32
  + Mx1, Mx2

## Design\Algorithm ex:

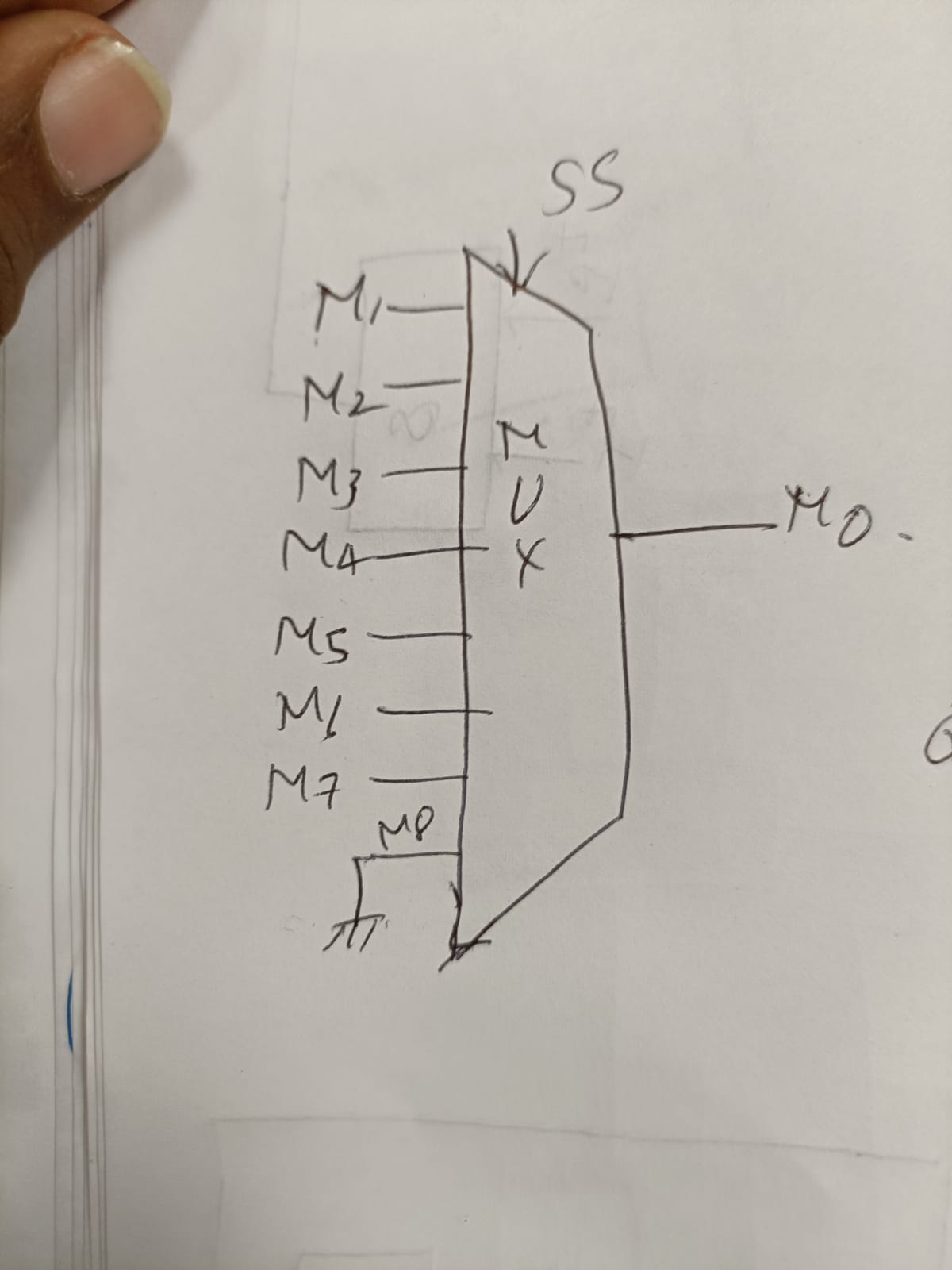


Figure 2– 8 to 1 mux

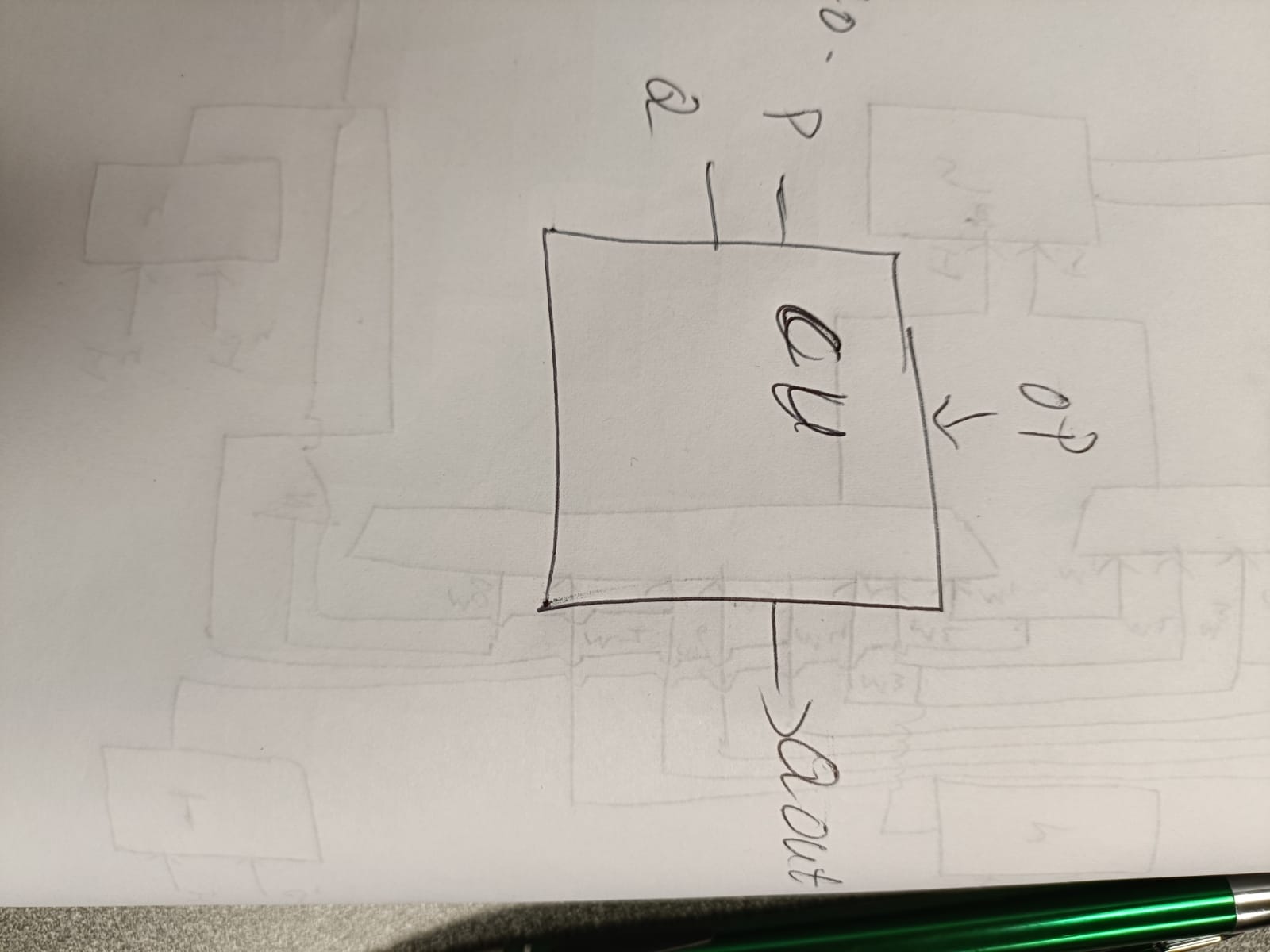


Figure 3– 2 COMPUTATIONAL UNIT

* Overall Component:
* Overall ports:
  + Inputs:
    - Q1,Q2,Q3,Q4,Q6,Q7,Q8, P1, P2, P3, P4, P6, P7,P8: 4 bits
    - Op1, Op2, Op3, Op4, Op5, Op6, Op7, Op8, Op9: 3bits -> select line input
    - SS1, SS2: 3 bit-> select line
  + Outputs:
    - o1: 4 bit -> output(Unit 9)

# Generated RTL Block Diagram\Schematic

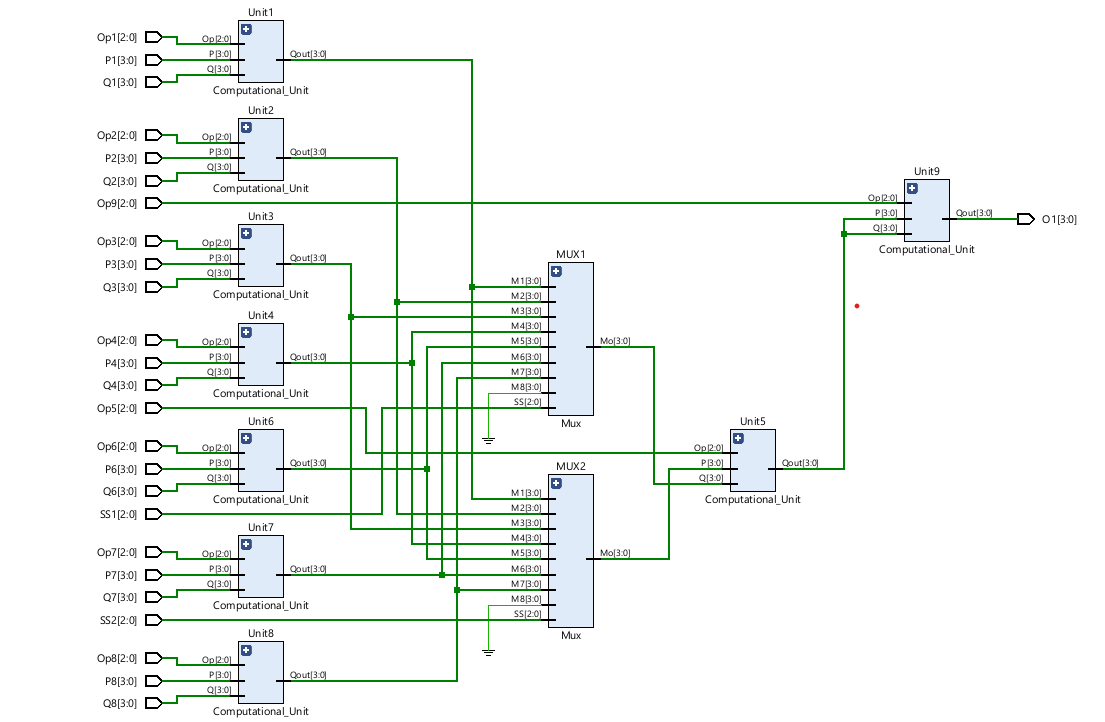


Figure 4 - generated RTL schematic.

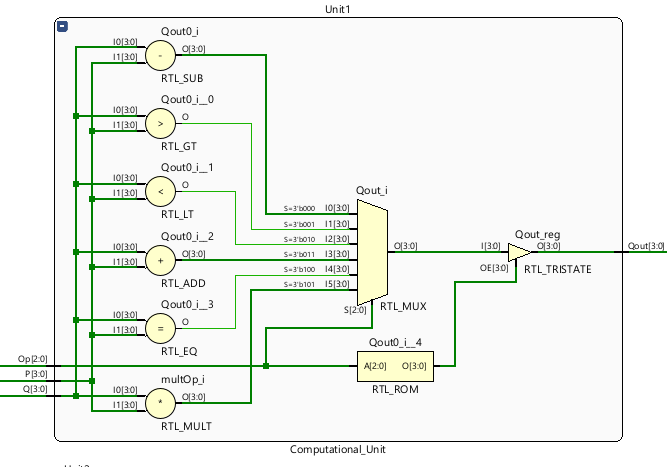


Figure 5- generated RTL schematic.

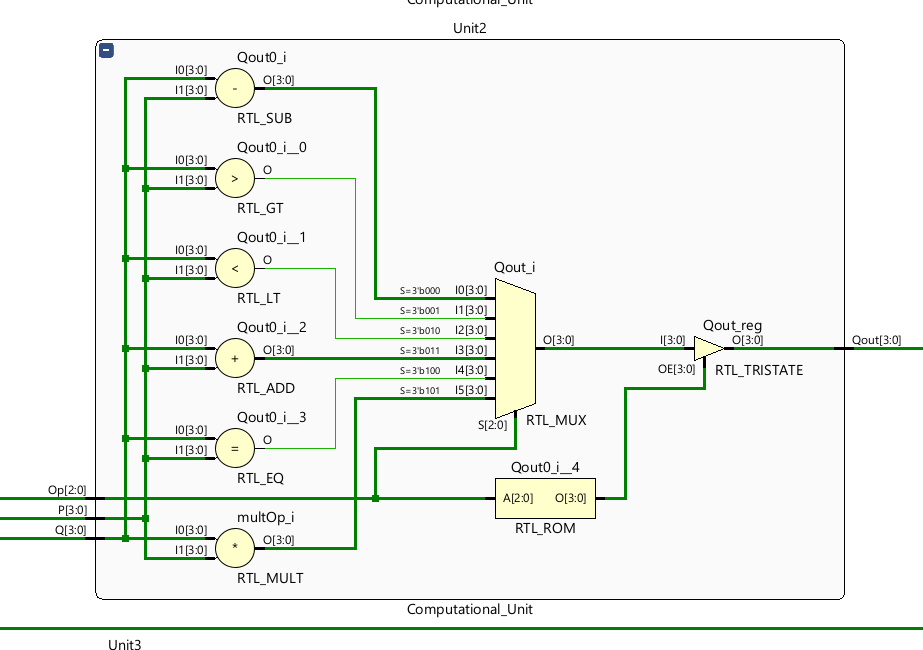


Figure 6- generated RTL schematic.

# Results

## Waveforms

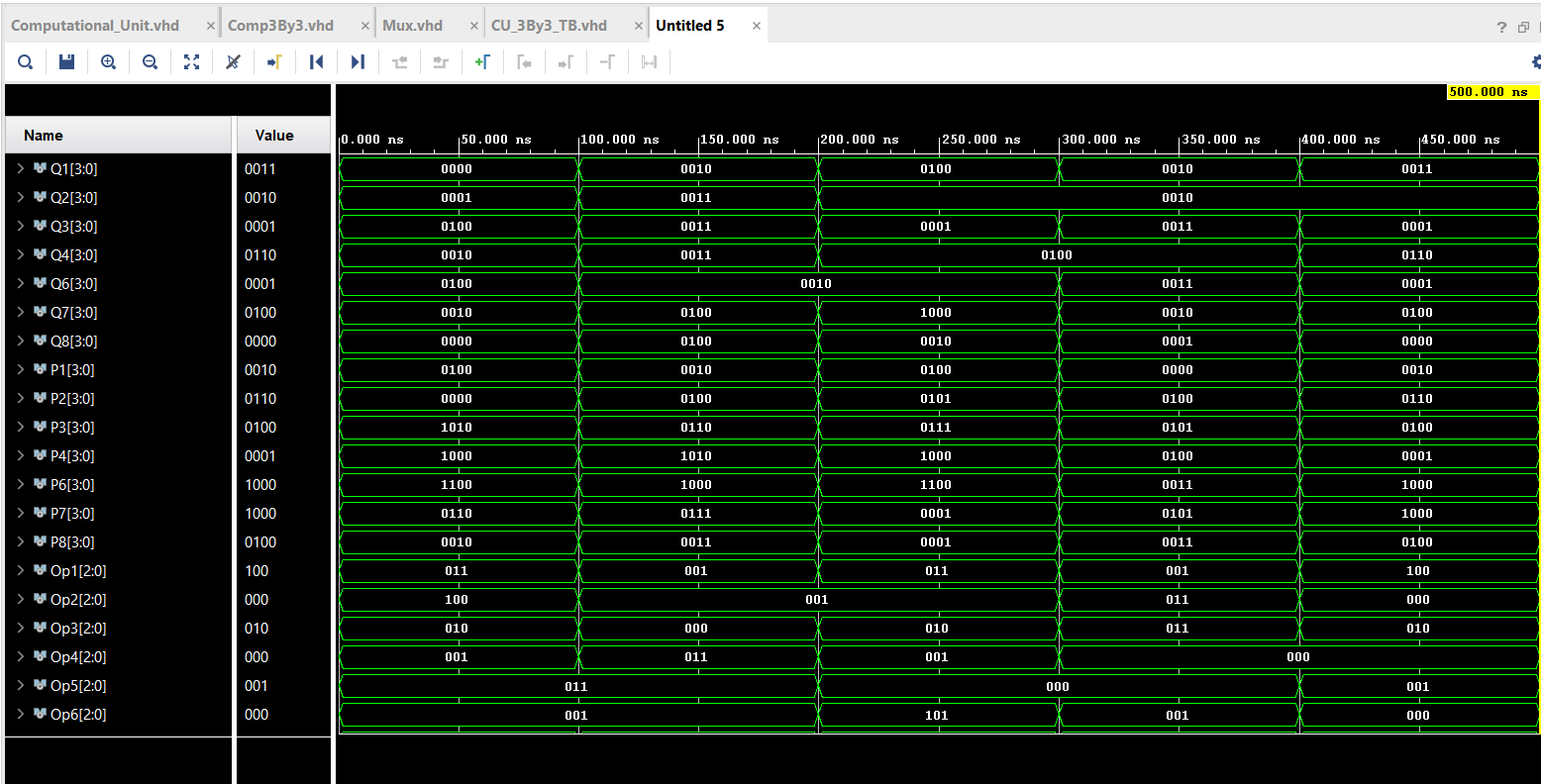


Figure 6 - Waveforms

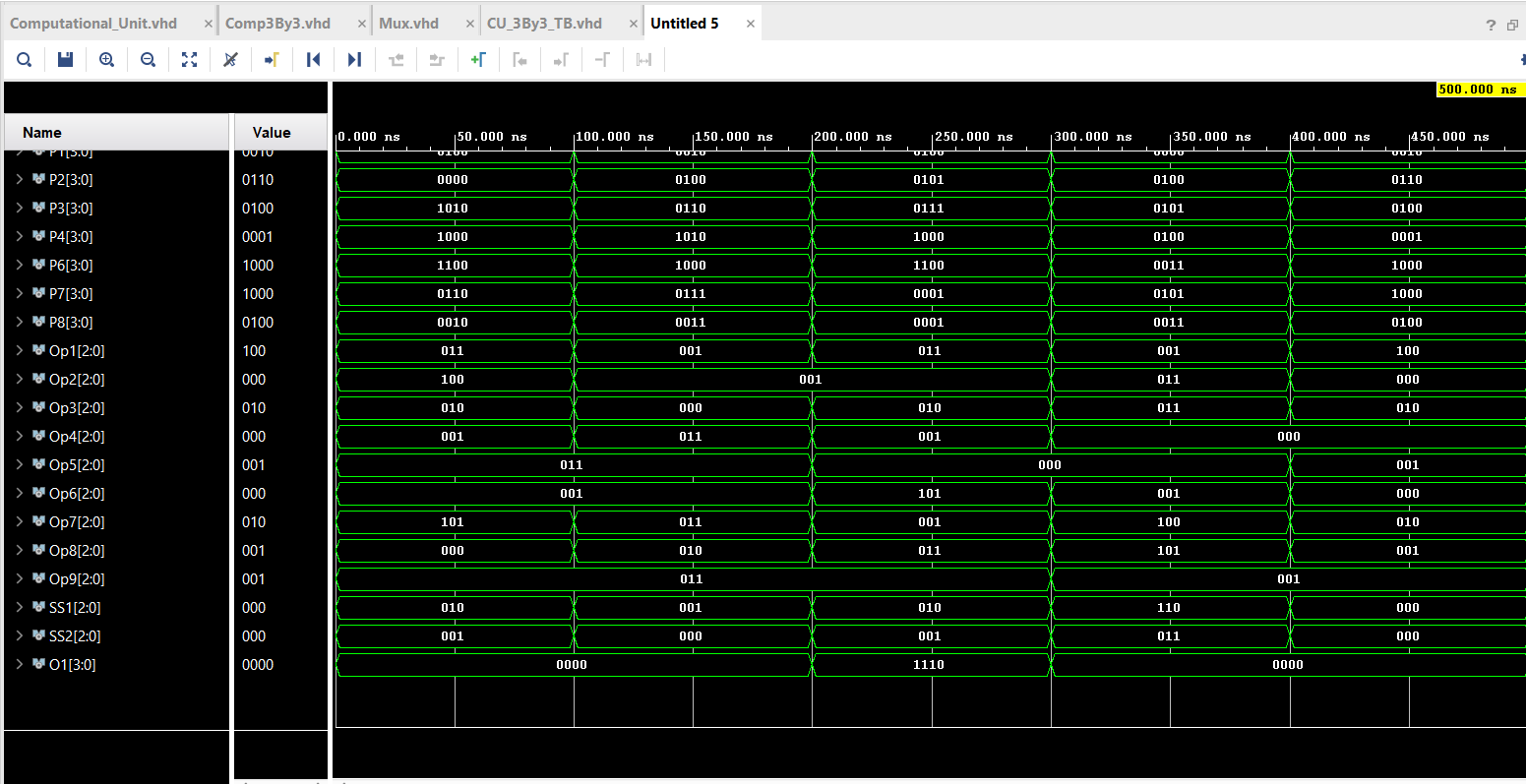


Figure 7 - Waveforms

## Table

**Test case1**

**Input :**

CU

P1 = 0100, Q1 = 0000, Op1 = 011(+)

P2 = 0000, Q2 = 0001, Op2 =100(=)

P3 = 1010, Q3 = 0100, Op3 =010 (<)

P4 =1000, Q4= 0010, Op4 <=001(>)

P6 =1100, Q6 =0100, Op6 =001(>)

P7 =0110, Q7 =0010, Op7 =101(\*)

P8 =0010, Q8 =0000 , Op8 =000(-)

Mux1 – m1= Line1, m2= Line2, m3= Line3, m4= Line4, m5= Line6, m6= Line7, m7 = line8, m8 = 0000 SS1 =010

Mux1 – m1= Line1, m2= Line2, m3= Line3, m4= Line4, m5= Line6, m6= Line7, m7 = line8, m8 = 0000, SS1 =001

P5 =mx1, q5 = mx2, Op5 =011(+)

P9= op5, q9 = op5, Op9 =011(+)

**Output**

O1 = 0000

**Test case3**

**Input :**

CU

P1 = 0101, Q1 = 0100, Op1 = 011(+)

P2 = 0100, Q2 = 0010, Op2 =001(>)

P3 = 0111, Q3 = 0001, Op3 =010(<)

P4 =1000, Q4= 0100, Op4 <=001(>)

P6 = 1100, Q6 =0010, Op6 =101(\*)

P7 = 1100, Q7 =1000, Op7 =001(>)

P8 = 0001, Q8 =0010, Op8 =011(+)

Mux1 – m1= Line1, m2= Line2, m3= Line3, m4= Line4, m5= Line6, m6= Line7, m7 = line8, m8 = 0000 SS1 =010

Mux1 – m1= Line1, m2= Line2, m3= Line3, m4= Line4, m5= Line6, m6= Line7, m7 = line8, m8 = 0000, SS1 =001

P5 =mx1, q5 = mx2, Op5 =000(-)

P9= op5, q9 = op5, Op9 =011(+)

**Output**

O1 = 1110