Harinath B

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Professional Summary

Highly Motivated Electronics and Communication Engineering graduate with strong skills in digital design, embedded systems, and IoT. Effective problem solver and team player, ready to apply academic knowledge to real-world projects and contribute to engineering goals.

Skills

Effective Communication, Problem Solving, Leadership Potential, Project Support, Strategic Planning, Digital Design, Analog Electronics, Embedded & IoT Platforms, Prototype Design, Time Management, Xilinx Vivado, Quartus Prime, Robotics Programming

Experience

- **Intern Trainee | Native Engineering | Apr 2025 – May 2025 | Bangalore | Certificate**

- Simulated complete IoT and robotics projects to verify circuit and code functionality.
- Analyzed cost-effective components based on performance and simulation results.
- Wrote and tested embedded code for sensors and actuators, improving system control.
- Documented circuit diagrams, code logic, and simulation results for easy project tracking.

- **Intern Trainee | Bharat Electronics Limited (BEL) | Jul 2024 – Aug 2024 | Bangalore | Certificate**

- Explored secure communication and unmanned tech within the Strategic Business Unit (SBU).
- Supported feasibility studies for integrating UAVs with defense communication systems.
- Assisted in cost analysis and performance evaluation of real-time subsystems.
- Drafted technical documentation outlining system architecture and key specs.
- Maintained professionalism through punctuality and active engagement.

Project

- **A Comprehensive Approach to Power Optimization in VLSI through Clock Gating | Sep 2024 – May 2025 | Presidency University, Bangalore | Publication**

- Engineered a modular 8-bit ALU and 4-bit ALU in Verilog HDL with operations like ADD, SUB, AND, OR, XOR, NOT, left and right shift controlled via a 3-bit opcode.
- Integrated latch-based clock gating logic to disable inactive modules and reduce unnecessary switching activity.
- Simulated and synthesized the design using Xilinx Vivado and implemented it on an FPGA Nexys A7 Board to validate functional correctness.
- Conducted comparative power analysis, demonstrating a significant reduction in dynamic power usage with minimal area overhead.
- Optimized RTL logic for low-power applications, making it suitable for embedded and battery-operated devices.

Education

- B.Tech in Electronics & Communication Engineering | Presidency University, Bangalore | May 2025 | 7.42/10 CGPA
- PUC in Science (Electronics) | Reva Independent PU College, Bangalore | July 2021 | 79.33%
- 10^{th} | SVN English High School, Bangalore | April 2019 | 89.76%