



Tutorial Altium Designer version 15.1

Status: Draft

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1 Introduction

The goal of the tutorial is to introduce you to the software package Altium Designer (Altium). Altium Designer is a computer-aid design (CAD) software. The software is used to design and layout printed circuit boards (PCB) and generate the necessary files for production or simulation. Altium designer is huge software package containing plug-ins, wizards, tools, and scripting. Altium designer is not a high-end CAD program it can be counted as mid-level and is wide spread over multiple continents, figure .

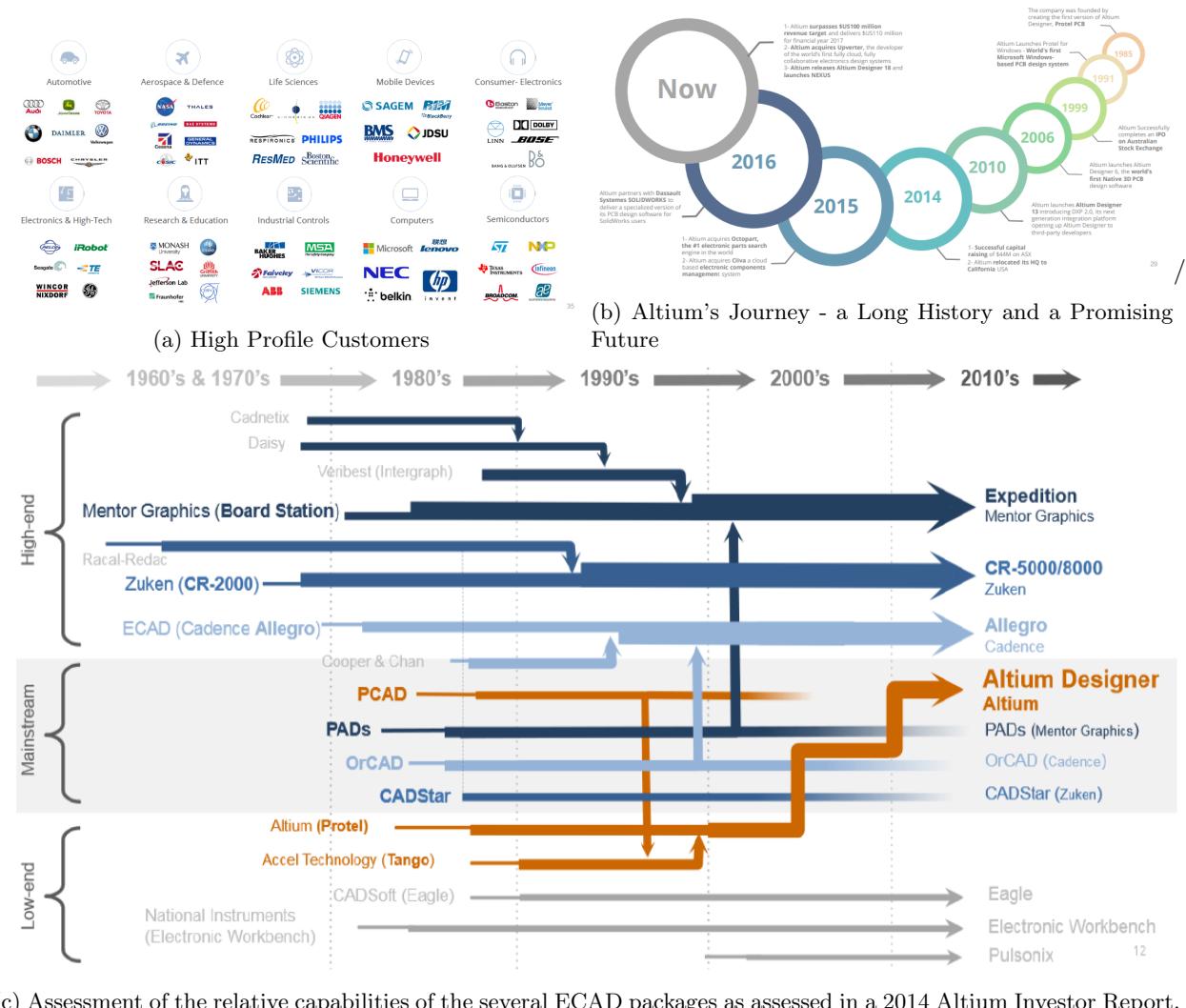


Figure 1: Additional information to Altium out of EGR680 PCB Design Winter 2018 and the ALTIUM HALF YEAR INVESTOR PRESENTATION [AltiumMirkazemi]

2 GVSU Engineering Blade Server

Describes how to access a blade server which provides a virtual user personalized desktop environment. The assumption is made that the student either uses his own personal computer (PC) or a computer provided by GVSU in an engineering laboratory.

The author of this section used his PC and Google Chrome browser on date 09/19/2018.

1. Open your web browser, preferred Google Chrome and use the following link <https://stratus.hpc.gvsu.edu>. A login screen should appear that allows you to login with your engineering network credentials, as shown in figure 2.

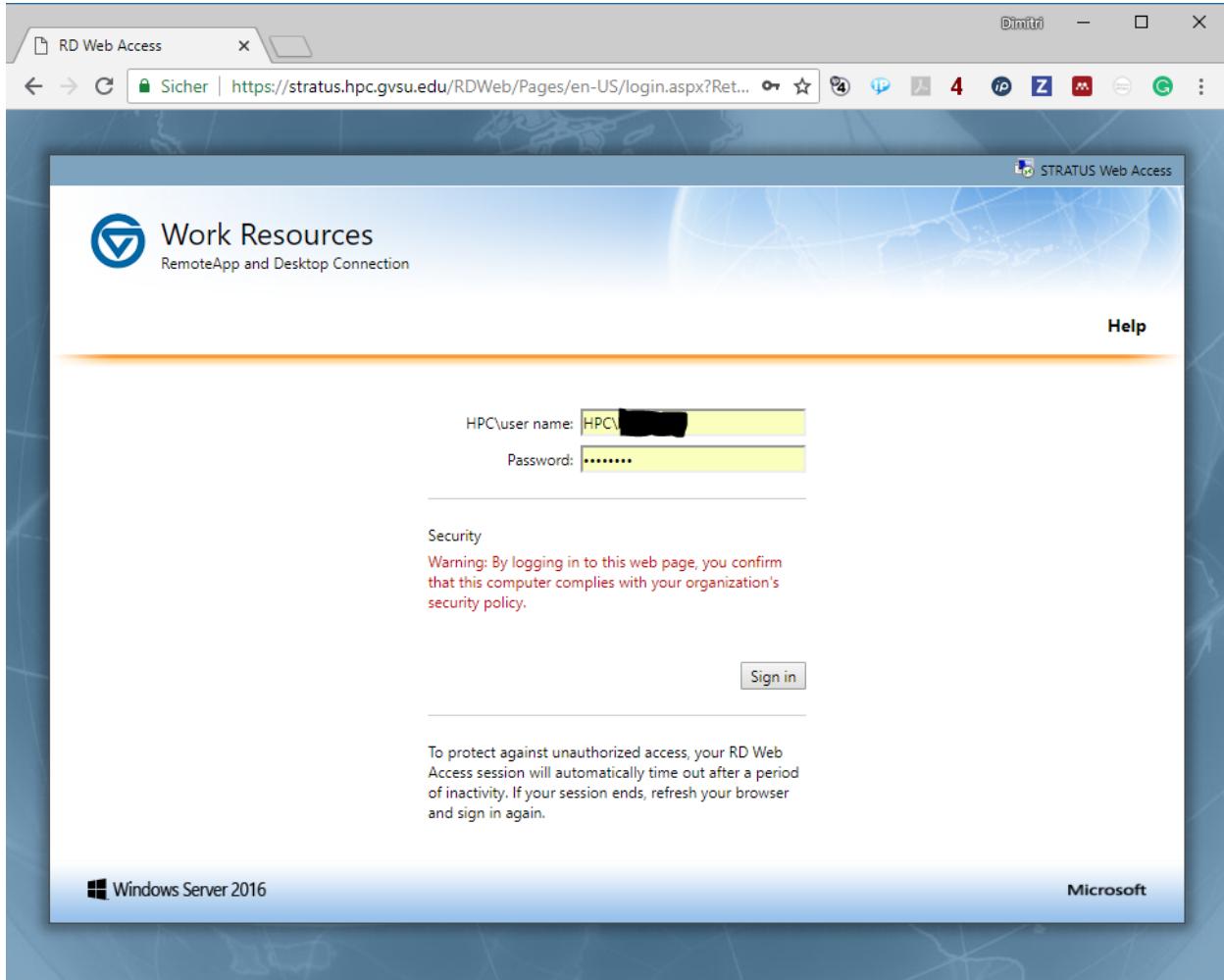


Figure 2: Stratus login for blade server access.

2. After a successful login use the EGR-EE-CE blade icon which is circled red by one left clicking on it which will download a remote desktop connection file type that can be used to start a remote connection to the EGR-EE-CE blade server as shown in figure 3. For further questions a link to Microsoft support website is provided <https://support.microsoft.com/en-us/help/17463/windows-7-connect-to-another-computer-remote-desktop-connection>. Most likely if you open the desktop connection for the first time, you will be asked again to enter your engineering network credentials they are the same as used in the previous step.

IMPORTANT: As of Fall2018 all students must use hpc\username, if you have trouble with login try hpc\username.

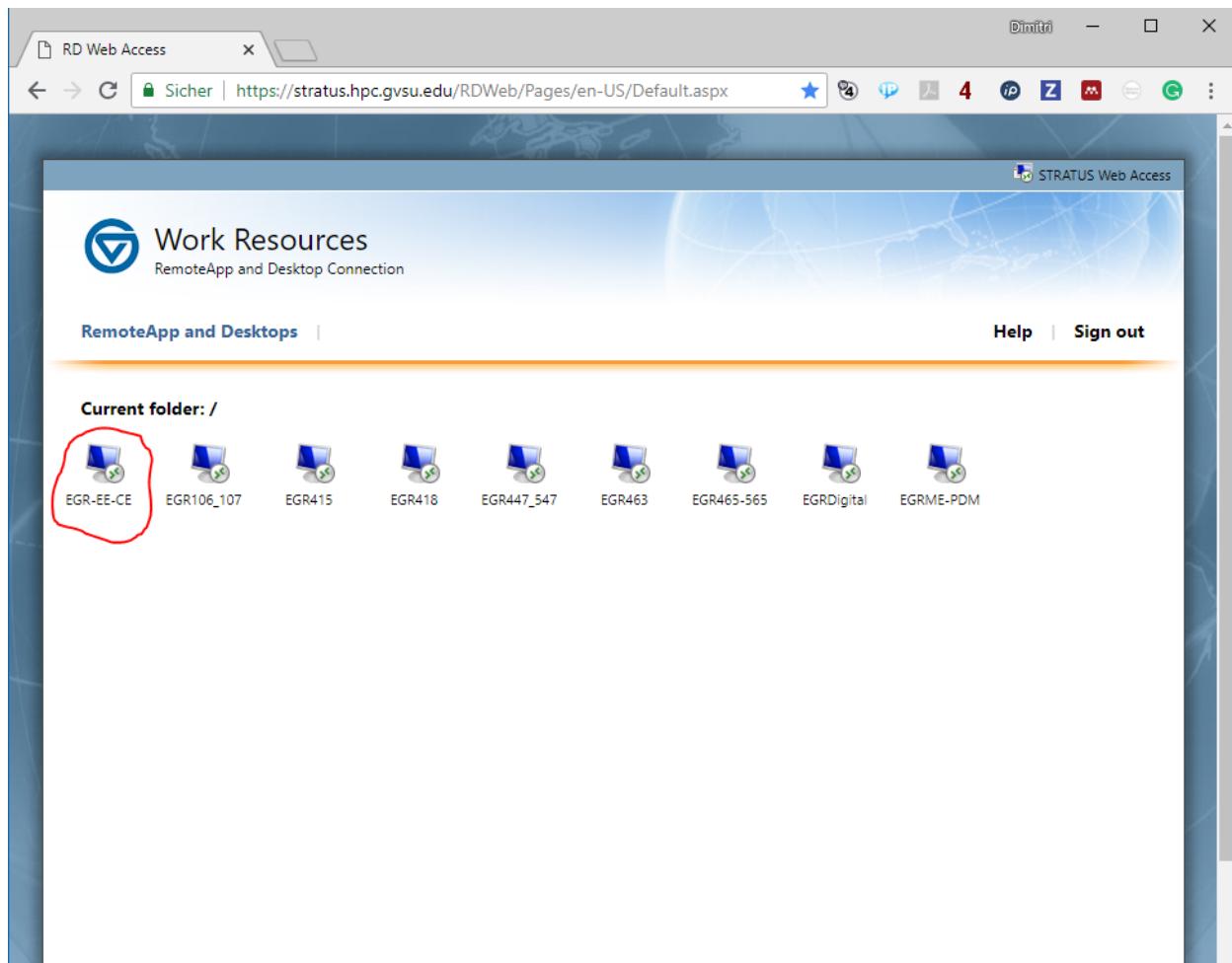


Figure 3: Stratus download blade server remote desktop connection file EGR-EE-CE.

3. If everything worked out as expected the blade screen shown in figure 4 appears. In this figure the Altium Desktop Icon is the third from upper left corner.

To open the software package Altium Designer left double click on the Altium Designer desktop icon. Altium should start up as shown in figure 5

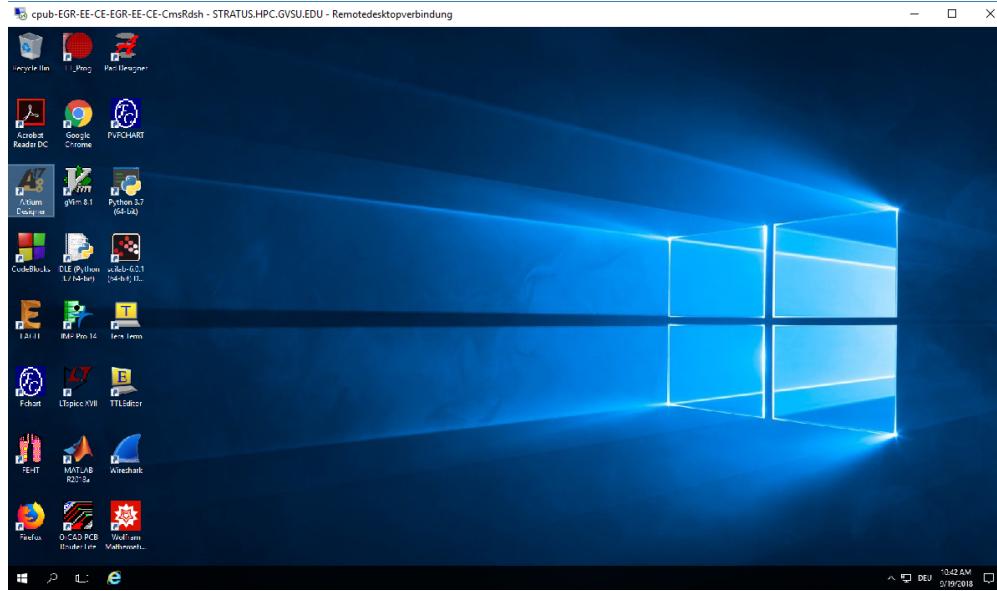


Figure 4: EGR-EE-CE blade server empty Windows Server 2016 desktop, with 46.0 GB RAM.

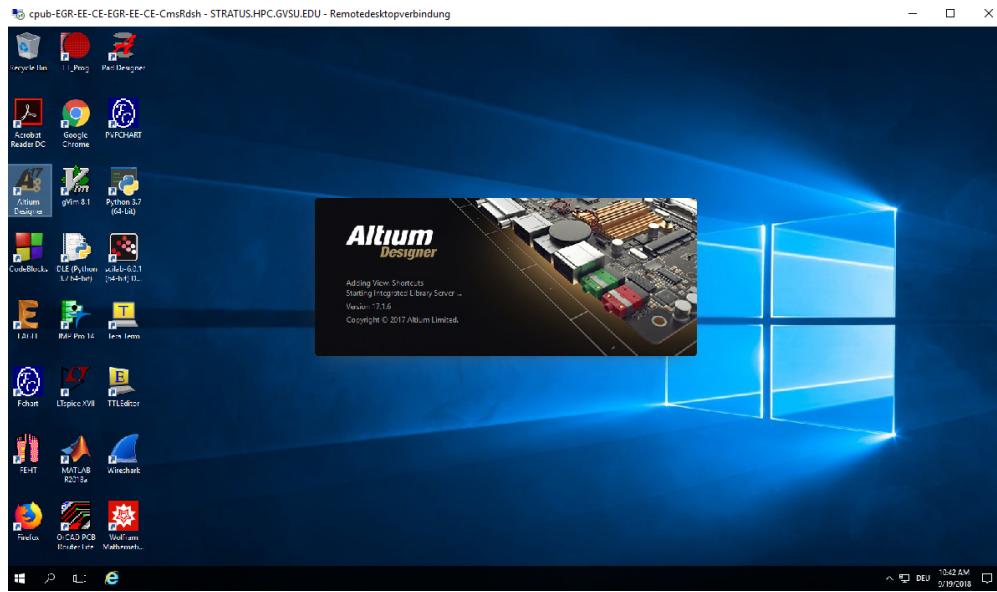


Figure 5: Altium Designer 17.1 start up window.

4. After Altium Designer start up process is finished and you are using Altium for the first time, your screen should look similar to figure 6. Choose the highlighted bullet point that says "No, I don't want to participate in the program" and click OK button.

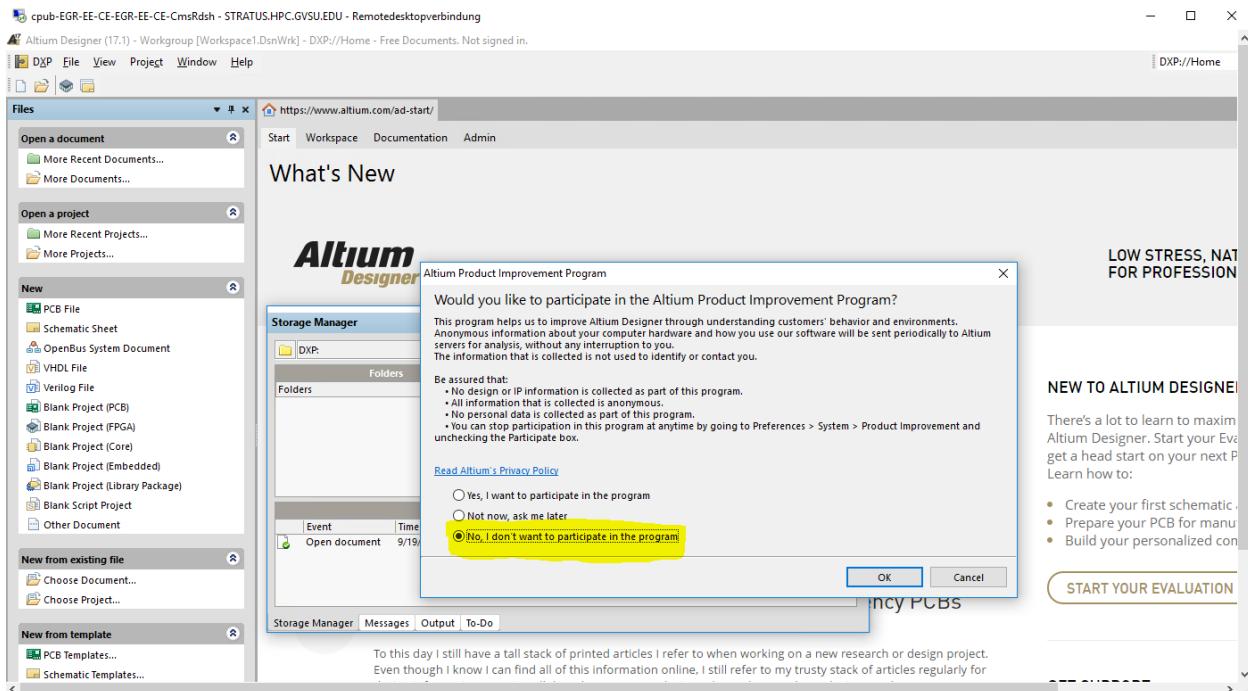


Figure 6: Altium Designer 17.1 Altium Product Improvement Program.

5. Now, to start with Altium Designer, it is recommended to close the Storage Manager dialog by a single left click on the highlighted cross. Then close the window <http://altium.com/ad-start/> by right clicking on it and chose Close All Documents. Then close the file dialog at the lower left corner by right clicking on it and chose Close 'Files'. Figure 7 shows the highlighted spots to click on.

Your screen should look now similar to what is shown in Figure 8. If so, proceed to the Section 3, if not ask the course/class instructor.

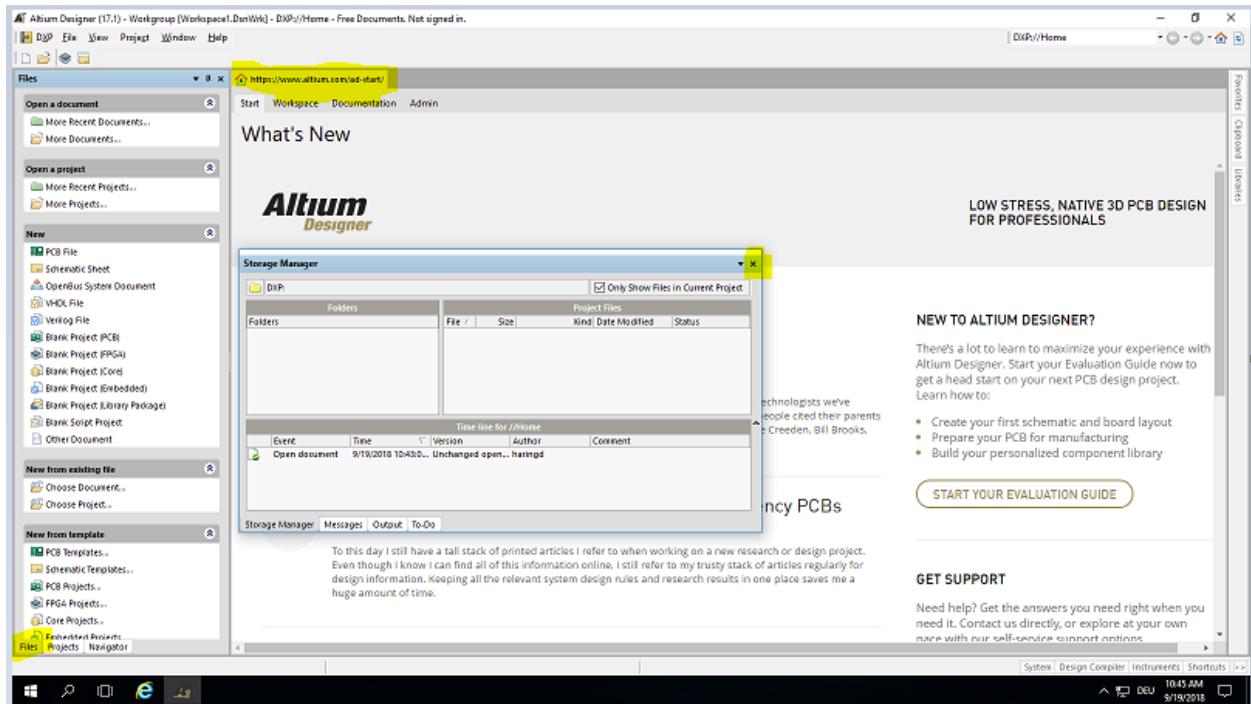


Figure 7: Altium Designer 17.1 screen shot first time started.

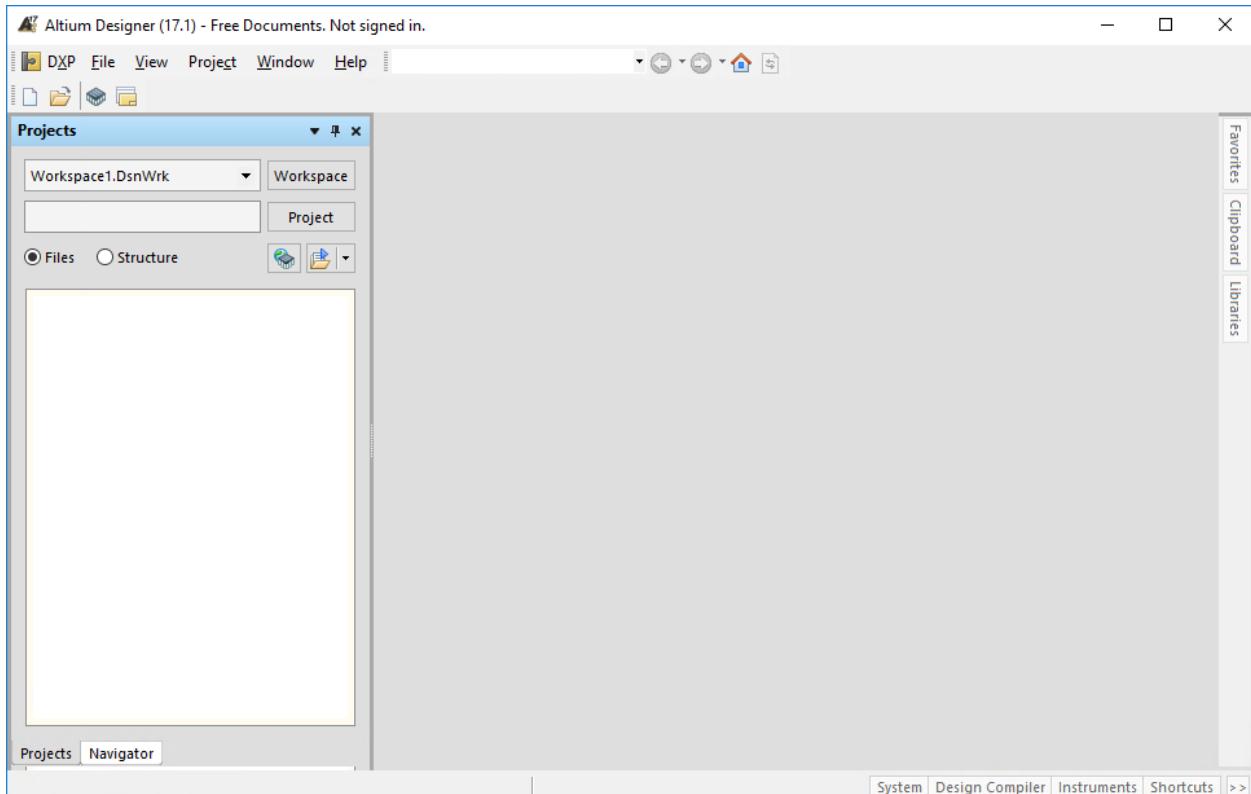


Figure 8: Stratus login for blade server access.

3 Altium Designer v15.1

This is an Altium Designer (Altium), tutorial that shall guide the user through the most common steps of Altium.

It is assumed that Altium is installed on your PC or you have access to it through the GVSU School of Engineering software.

1. Press Windows key on keyboard and type "Altium" and press enter or double click on Altium Icon, shown in Figure 9.



Figure 9: Altium Icon.

2. Altium starts and if no project is open the screen should look like the one in Figure 10.

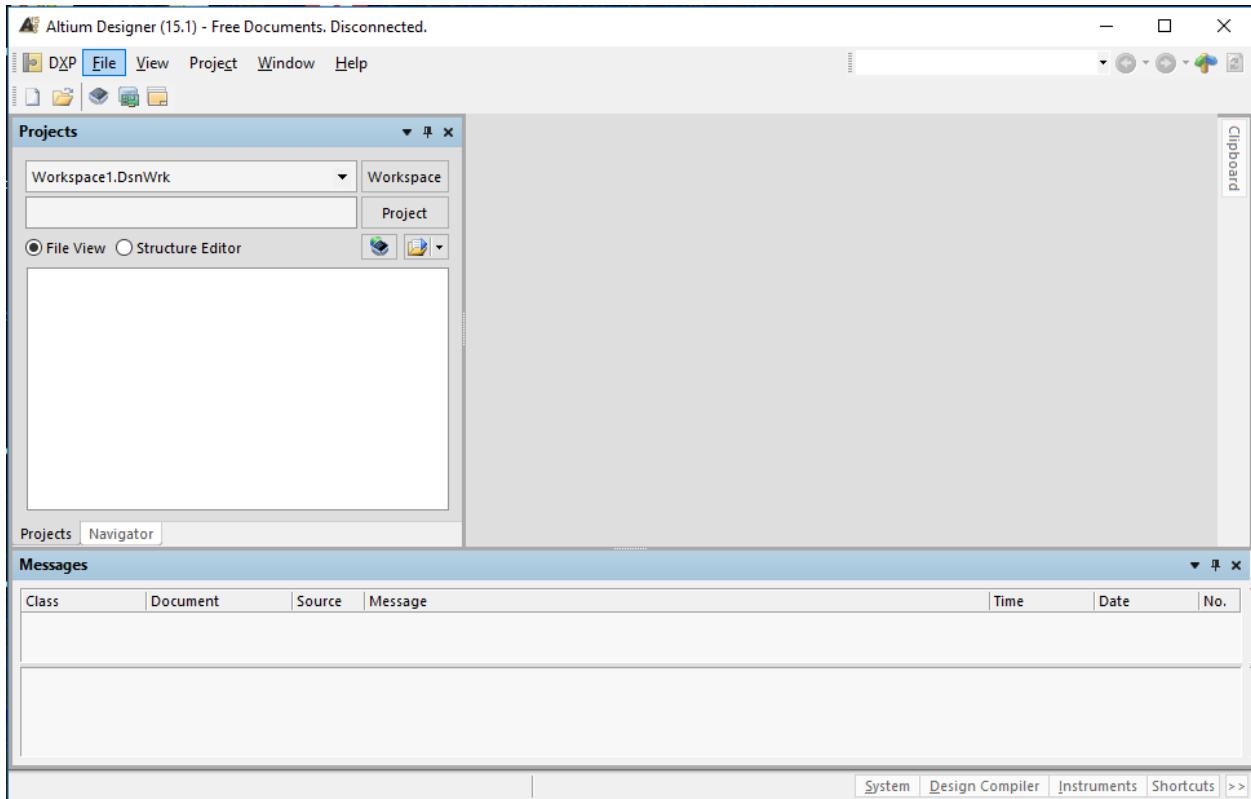


Figure 10: Altium No Project open.

3. To start a new project select in menu bar "File" → "New" → "Project" as shown in Figure 11.

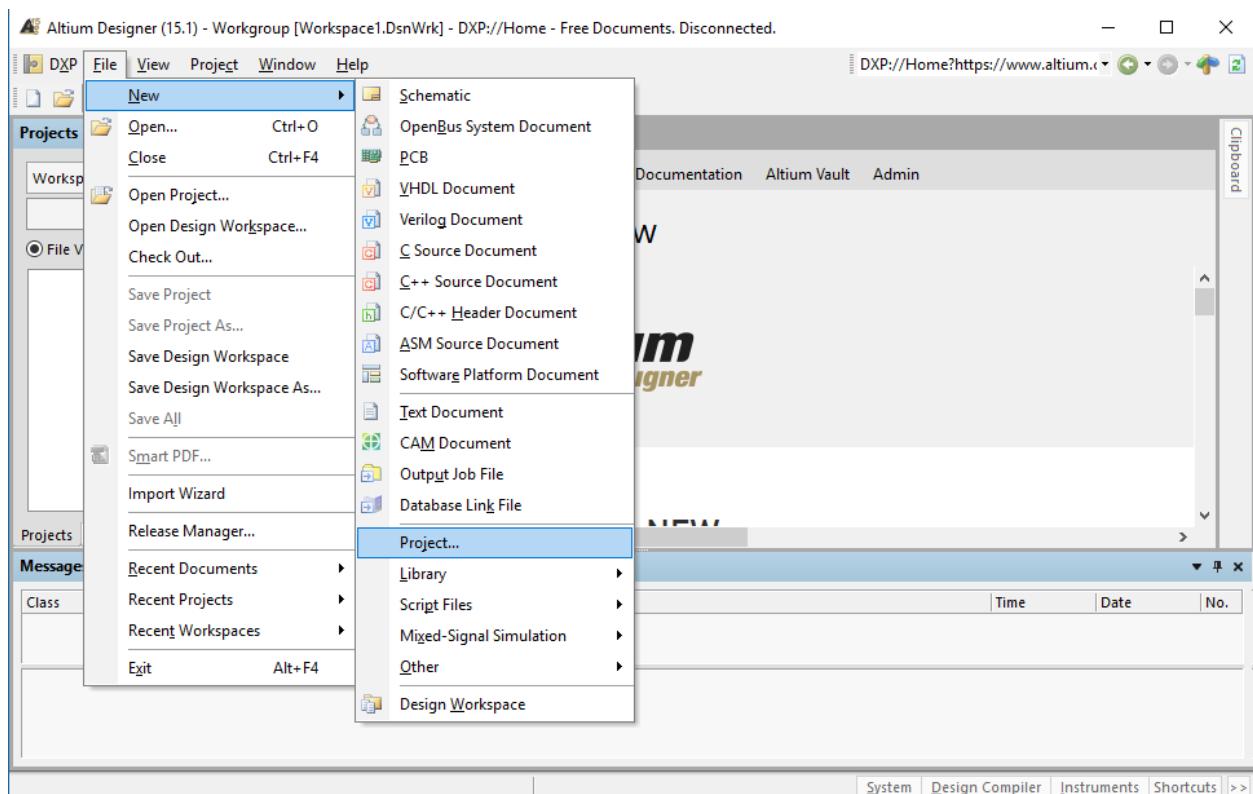


Figure 11: Altium new Project.

4. The Altium new project dialog appears. Select "PCB Project" in the first column and default in the second one.

In the field Name type an appropriate project name like "EMC_Filter" as example. In the field Location choose an appropriate folder to store the project. On your own personal computer (PC) it is beneficial if it is on the C: drive, on a GVSU blade server on the W: drive. The version control box is as well as the Managed Project box should be unchecked. **Note:** In the naming and location instead of spaces use underscores this avoids unwanted magic errors.

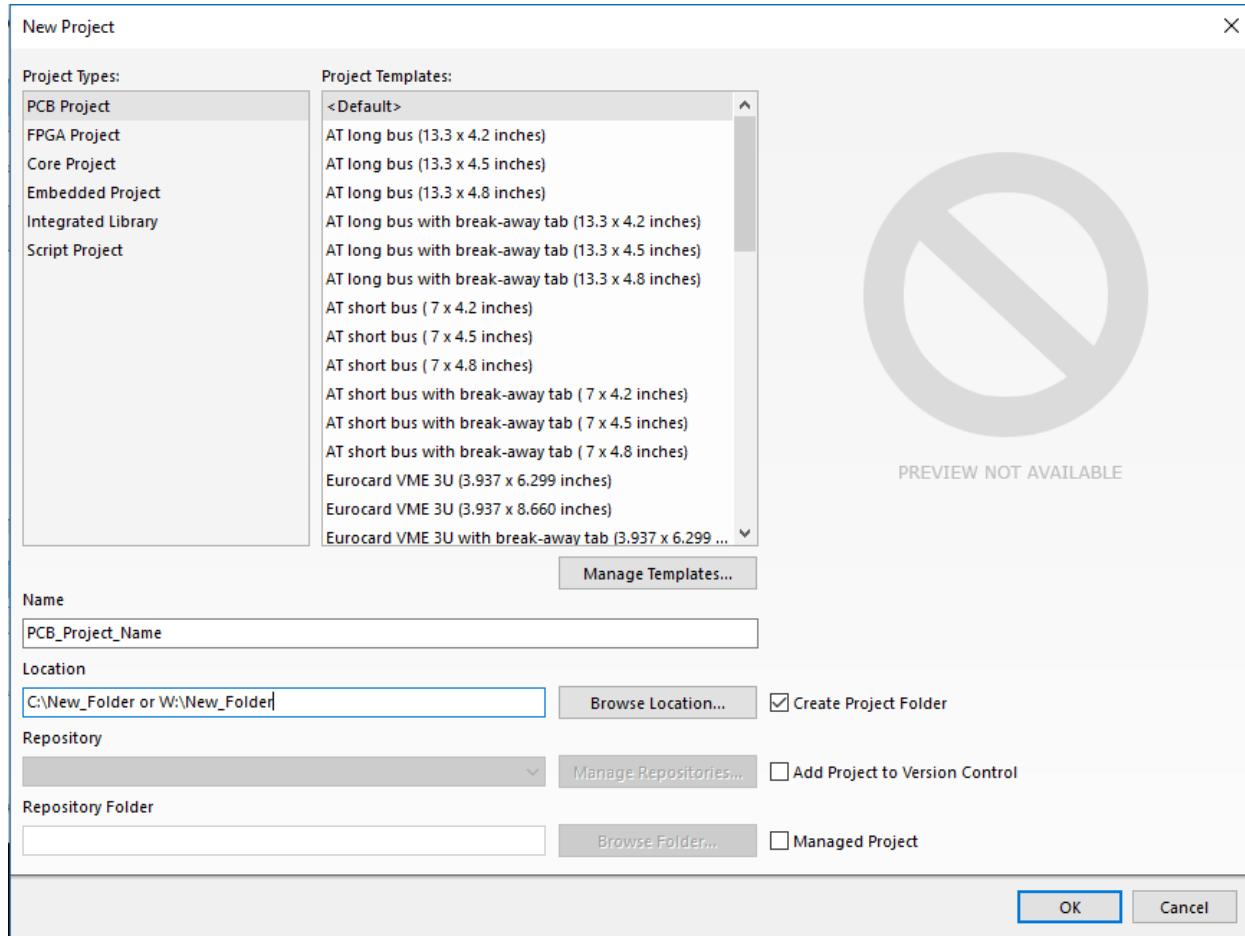


Figure 12: Altium new Project dialog.

5. The Altium generated now an empty project which appears in the Project view bar on the left side as shown in Figure 13. The project does not contain any documents yet.

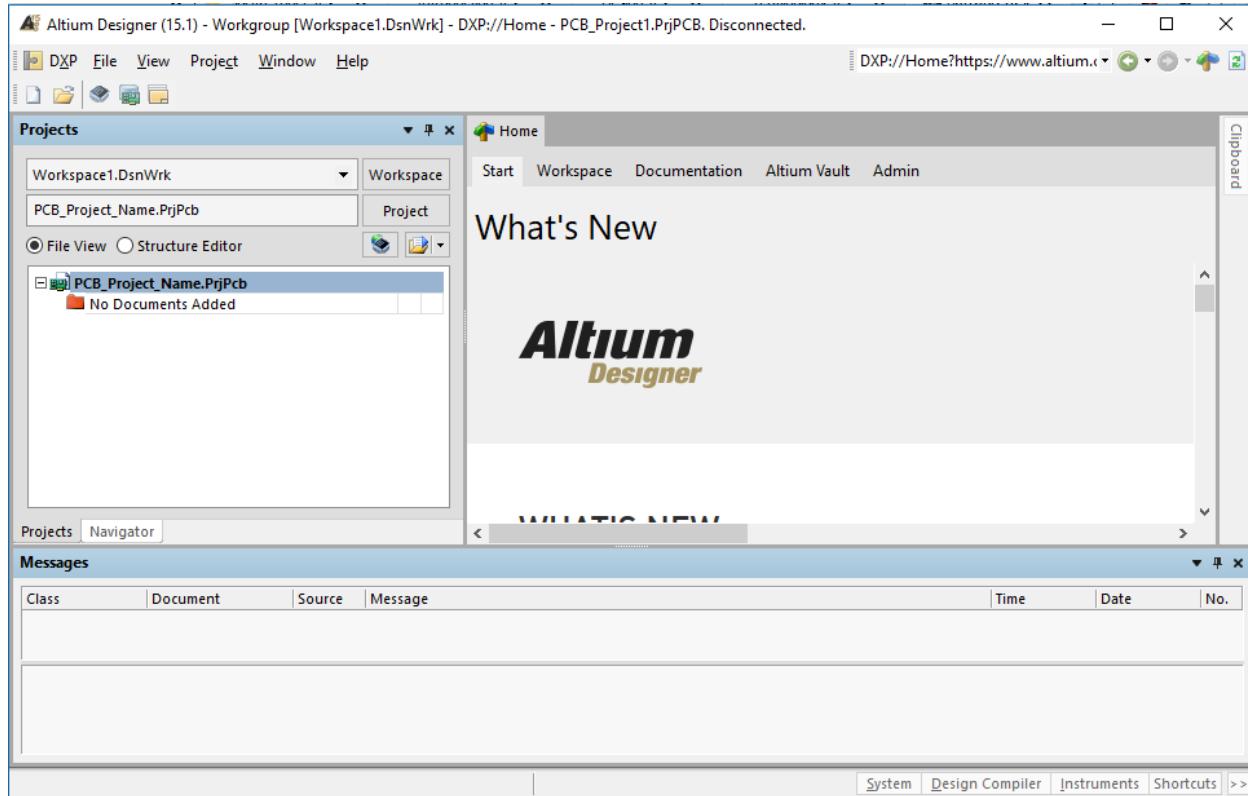


Figure 13: Altium empty Project.

6. The first thing is to add a schematic sheet which allows to draw a circuit. To add a schematic **right click on the empty project** → **Add New to Project** → **Schematic**. It is possible to do the same step in menu bar "File" → **New...** → **Schematic**. If the latter approach is used be aware that if you have multiple projects the new schematic sheet will be added to the selected project in project view window.

Note: That a new document called "Sheet1.SchDoc" has been created under "Source Documents" in the left window named Project.

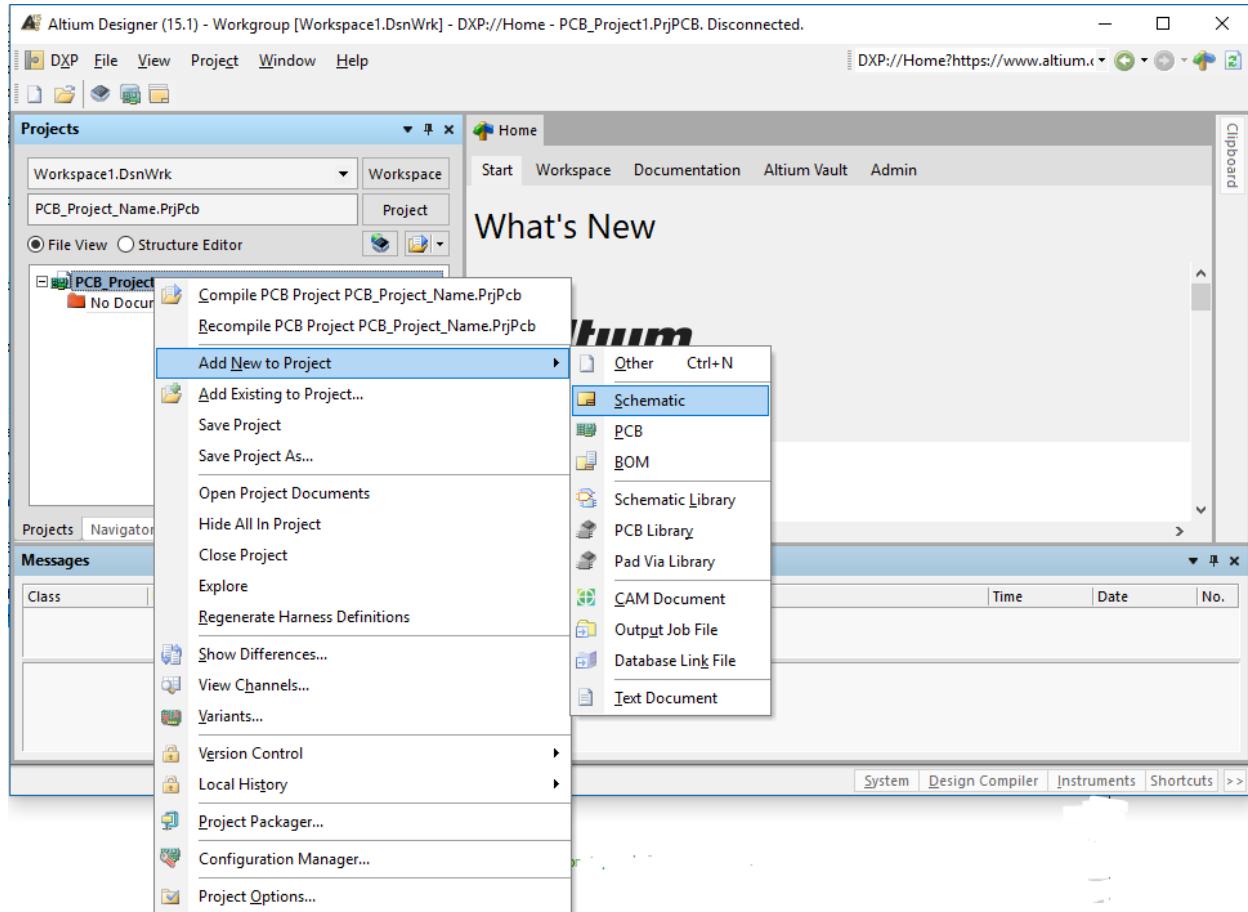


Figure 14: Altium add Schematic sheet.

7. Press **CTRL+S** to save the new generated sheet and name it circuit_1", as shown in Figure 15.

Hint: After a document is generated it is good practice to save it. Choose a more descriptive name for the sheet, and keep in mind that Altium allows you to build an hierarchical sheet structure with top level and multiple sheets. Furthermore, Altium is a huge software package which results in complexity, so it can crash a lot, save often! The short cut to save is **CTRL+S**

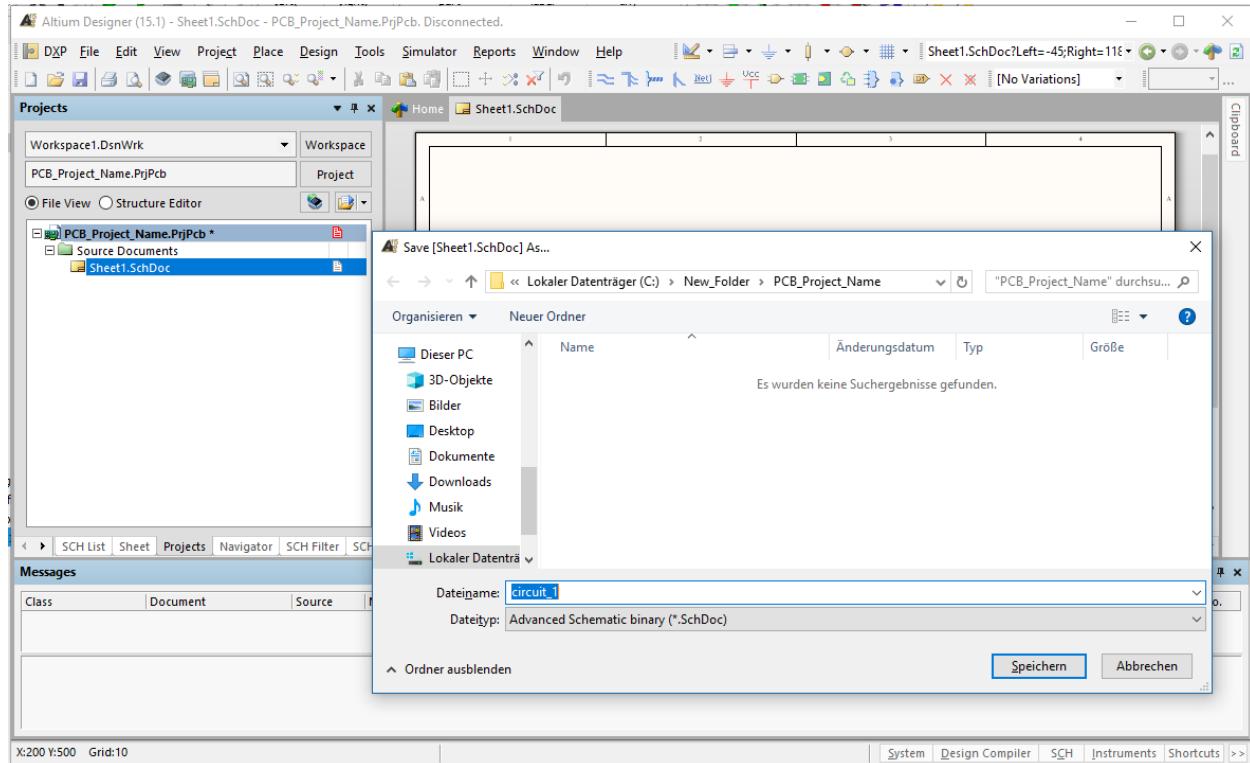


Figure 15: Altium save schematic sheet with an expressive name.

8. In the generated document which is a schematic sheet the Document options have to be set. Right click mostly anywhere on the schematic sheet then follow **Options...** → **Document Options...**, as shown in Figure 16.

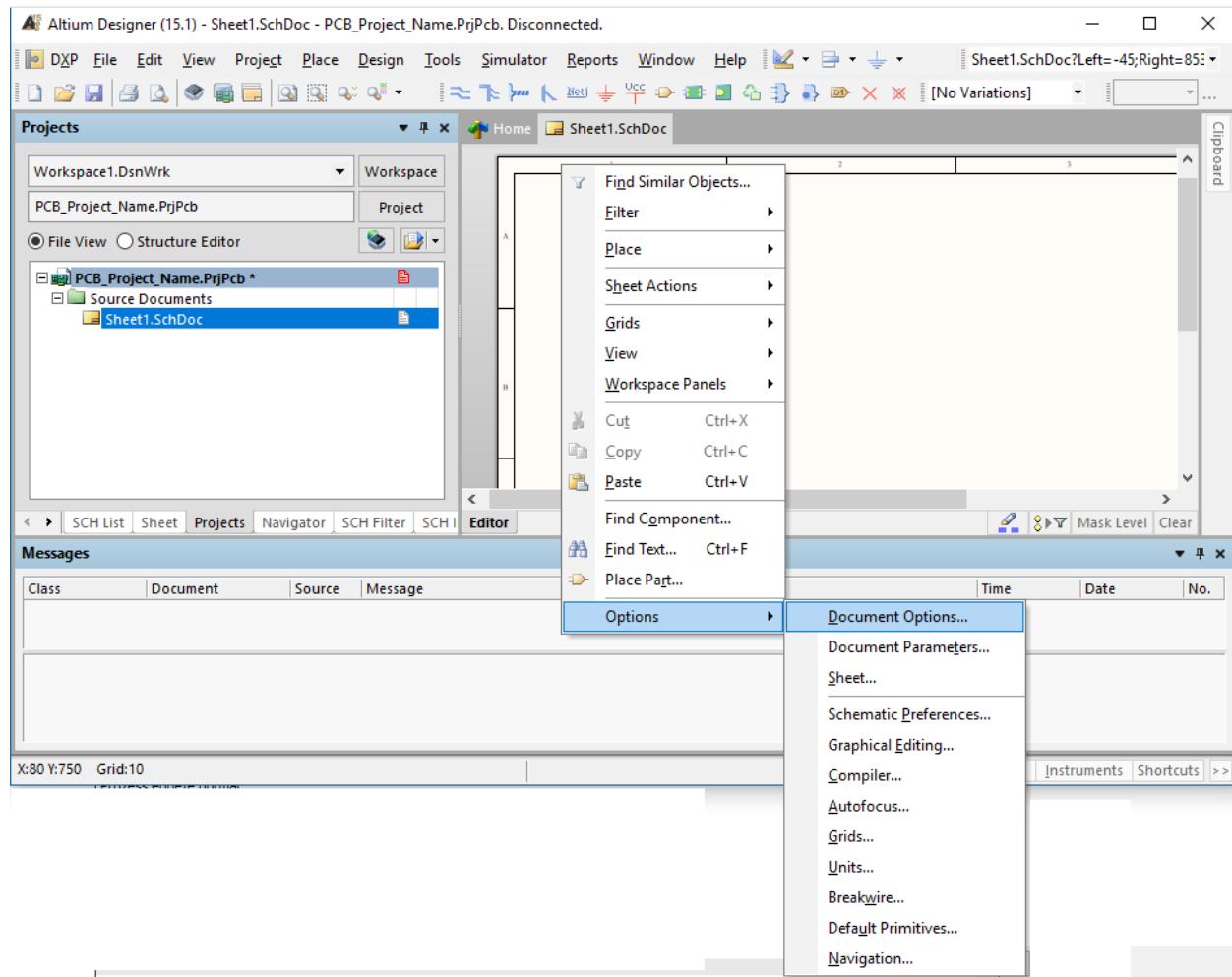


Figure 16: Altium change options of the generated Document in this case a schematic sheet.

9. In the Document options Dialog you can define the layout parameters for the specific document. For now we only will change or ensure that the paper format is set to US Letter format. Therefore, under Standard Style chose Letter, click OK.

Hint: Format A refers to the European paper format. In Europe a common format is A4 which is similar to US Letter or A3 which is twice the size of A4 so similar to US tabloid format.

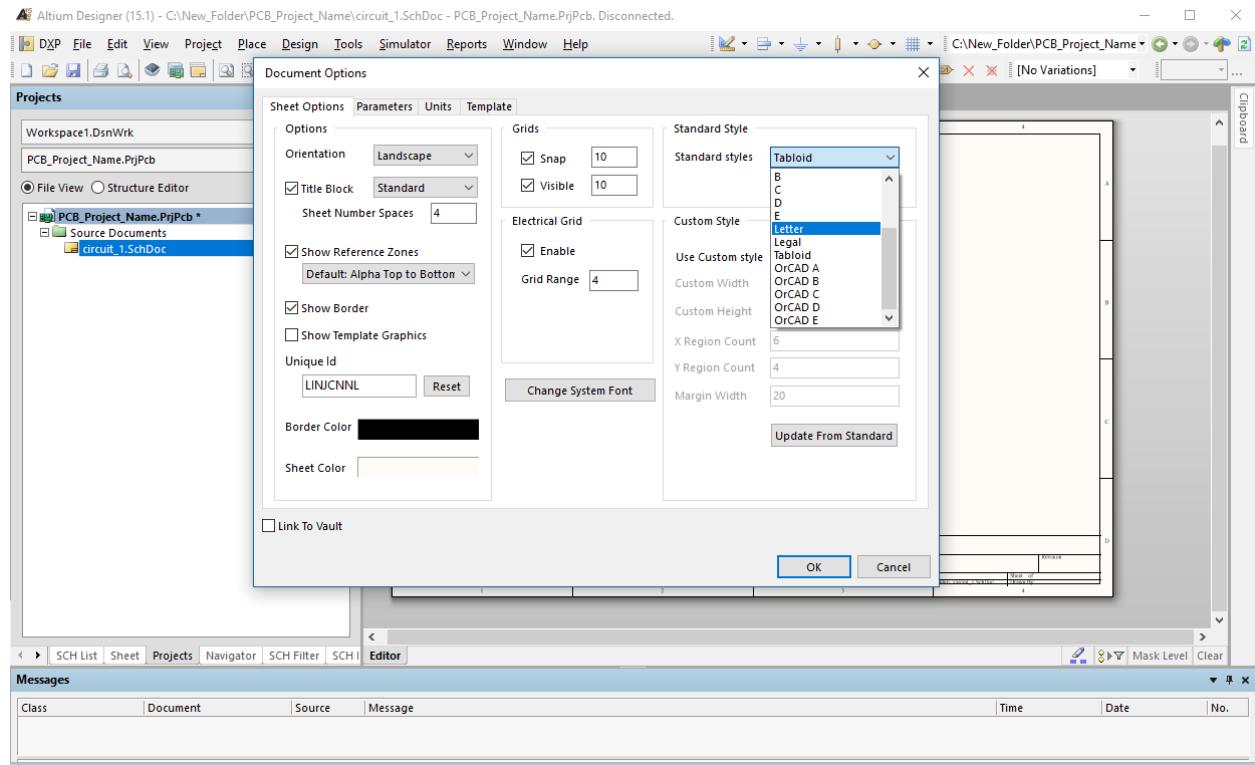


Figure 17: Altium Document Options Dialog.

10. To set the Document Parameters just change the register on top from sheet options to Parameters. The dialog will show all default parameters that are assigned to this sheet. Now fill out all the parameters that you can fill out or make sense to fill out as the Engineer, Date, Title, Drawn by, etc., as shown in Figure 18. In addition the dialog allows you to add parameters so if your organization requires an email address or an phone number as parameter use the "Add..." button.

NOTE: to show a parameter in the sheet place a string and use the = sign to allocate the parameter that shall be placed.

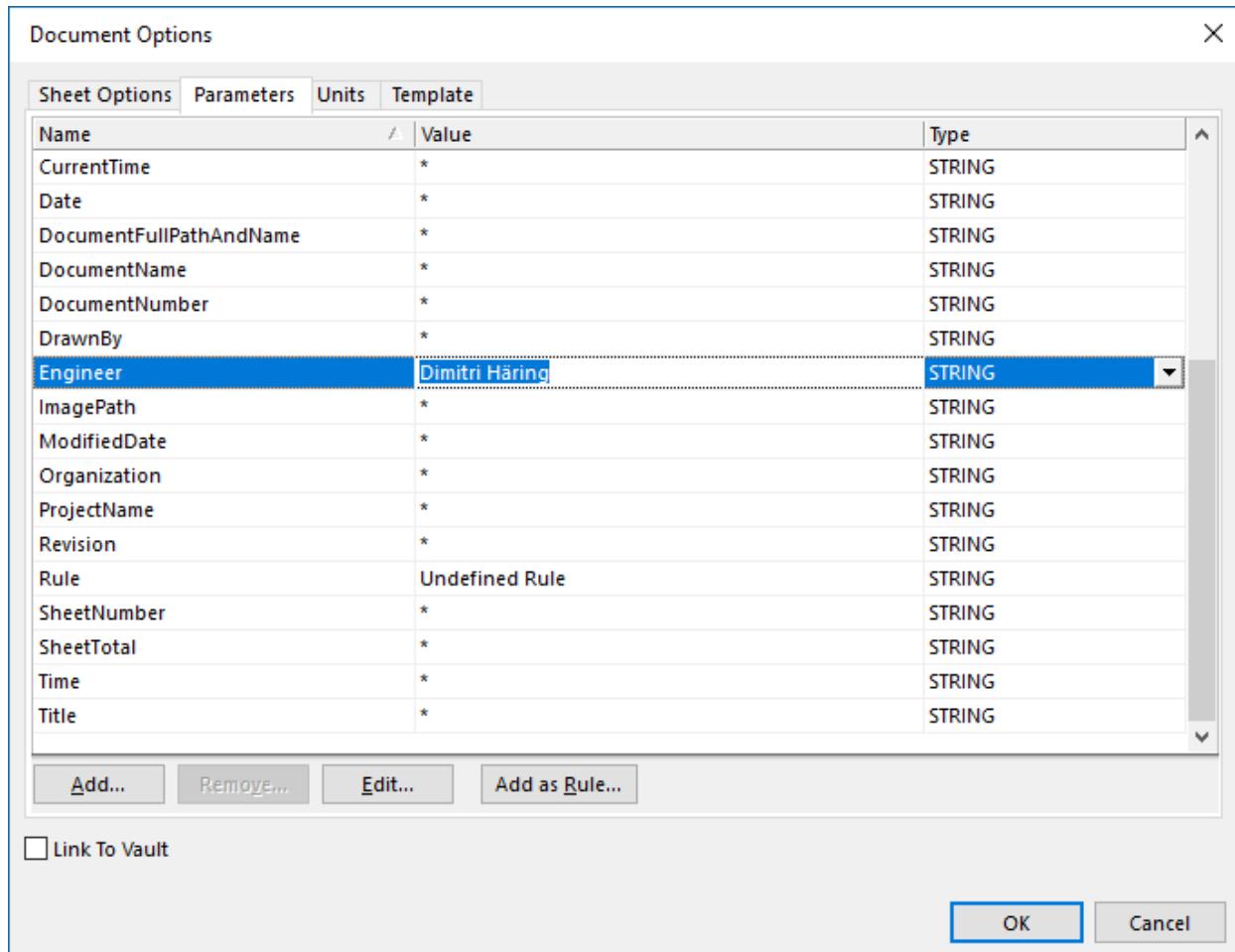


Figure 18: Altium Document Parameters Dialog.

11. Lets explain how you navigate the sheet. To move the sheet on the screen right click on int and hold which allows you to drag the sheet around the screen. To zoom into a document press CTRL and scroll on the mouse wheel back and forth. Now zoom in on the legend on the bottom right of the document as shown in figure19.

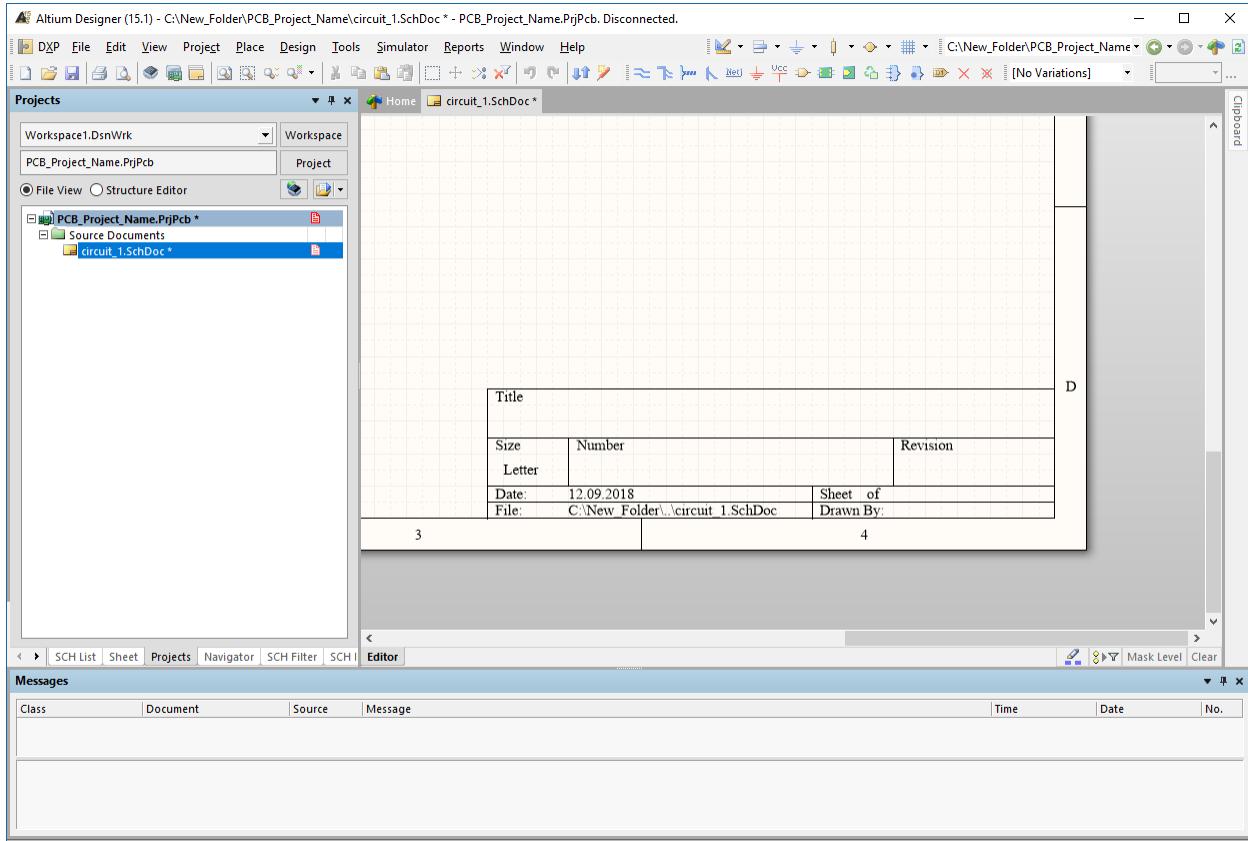


Figure 19: Altium schematic sheet zoomed in on legend.

12. To place the title that we defined in the previous step press P and then T to set a Text String. The Text String dialog pops up and allows you to define the string. To select a parameter start the string with an = sign as shown in Figure 20. Then press ok and place the string under the title. As you noticed now Altium keeps the string so you can place it as many times as you wish, to change the parameter press TAB which brings you back to the Text String dialog so you can change the string. If you have placed all strings press ESC to leave the mode or cancel in the Text String dialog. It should look now similar to Figure 21. Notice that we did not assign a sheet number or sheet total because under menu bar Tools → Number Schematic Sheets.. that will do the job for you or redo it if you expand the number of sheets. I think its important at this place to show you the in build shortcut help which is on the right lower edge of the software highlighted in Figure 21.

Note: The tutorial provides a shortcut table of the most common short cuts at the end might be handy to print that out now and have it beside.

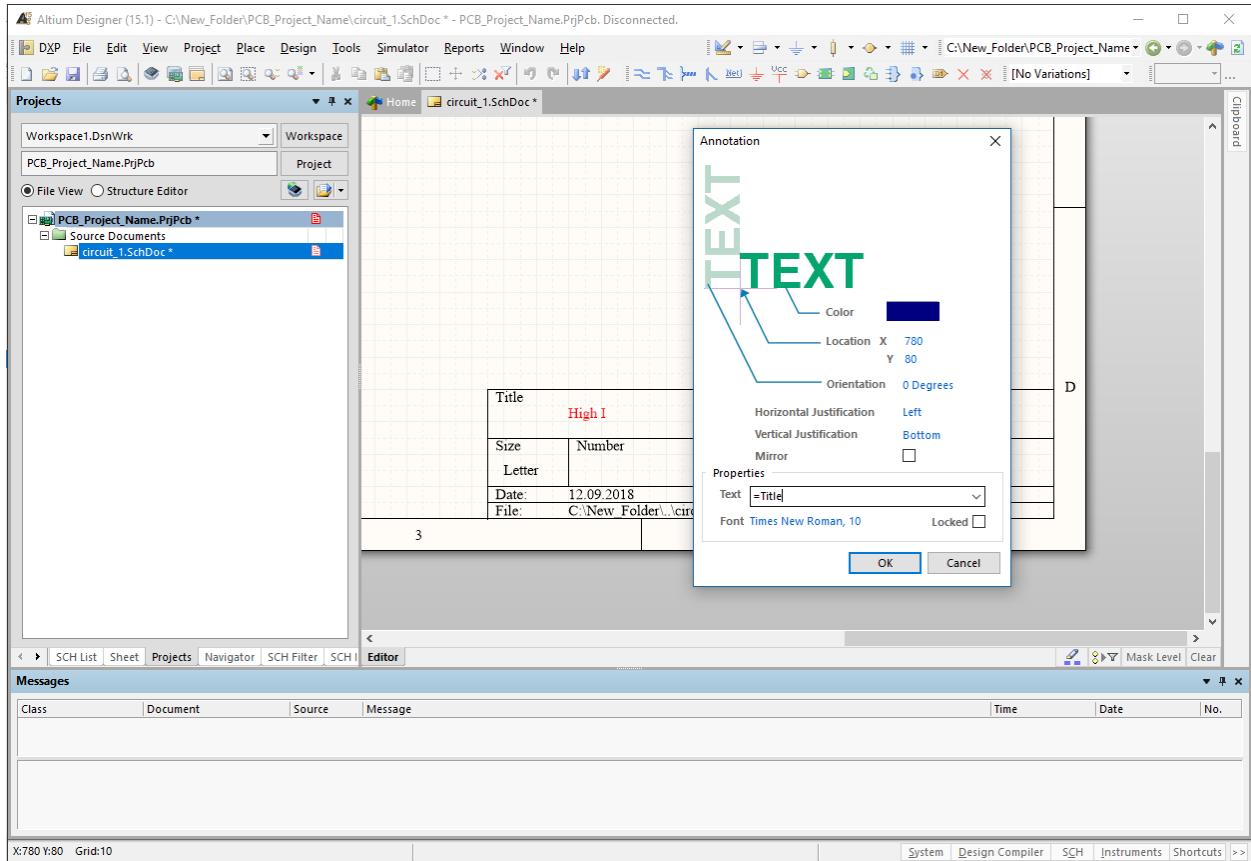


Figure 20: Altium schematic sheet zoomed in on legend.

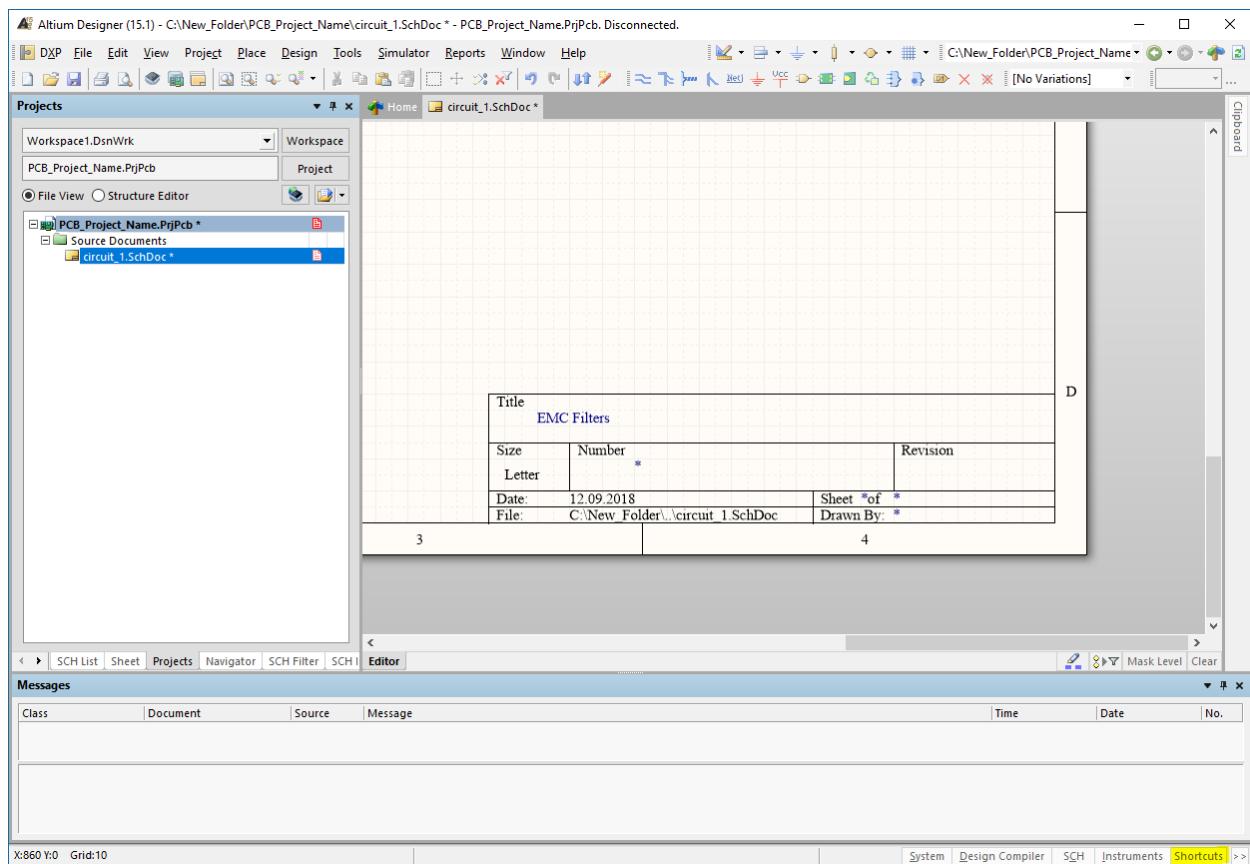


Figure 21: Altium schematic sheet zoomed in on legend and highlighted shortcut menu.

3.1 Integrated Library

13. Now that we have set up the parameters lets make a library which will allow us to create our own components. Altium has a limited standard library so you will probably need to create your own components. In menu bar go to **File → New... → Project...** and chose Integrate Library as you did to open a new project in a prior step. And give here a name like myLib and press OK.

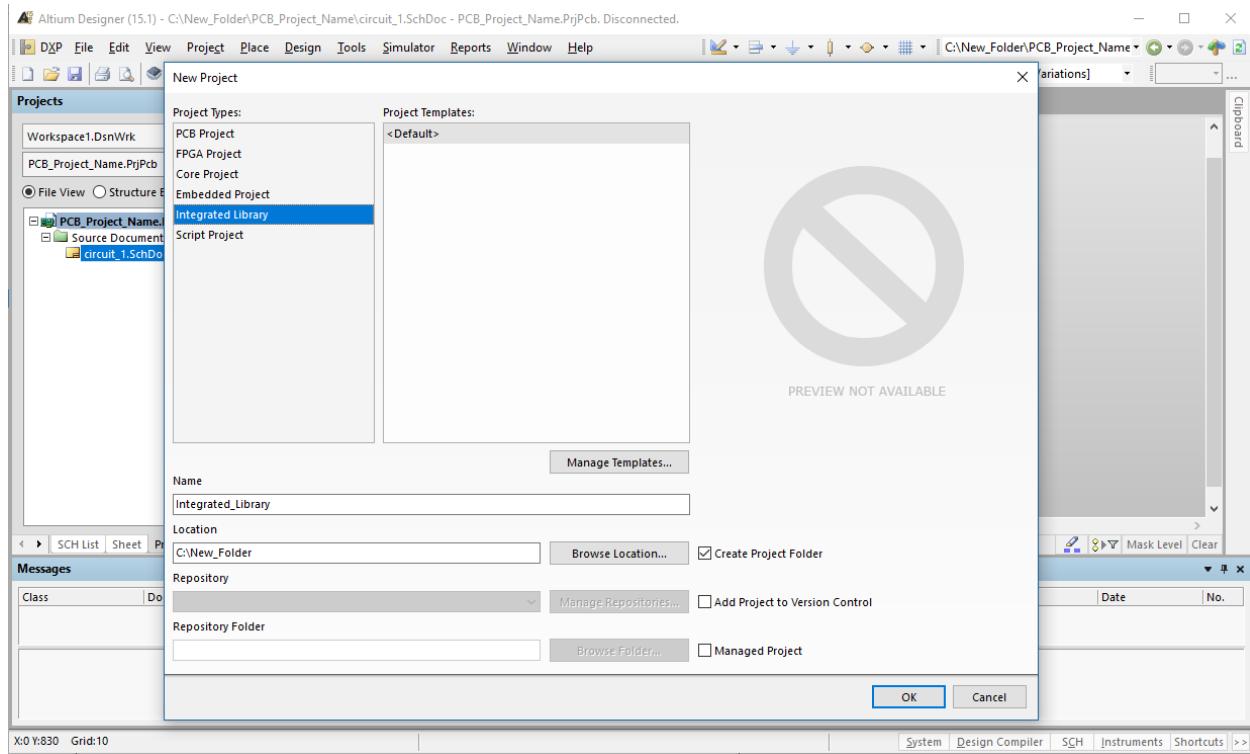


Figure 22: Altium new Integrated Library.

14. Figure 23 shows the generated Integrated Library similar to an empty project documents as schematic library and PCB library need to be added named and saved.

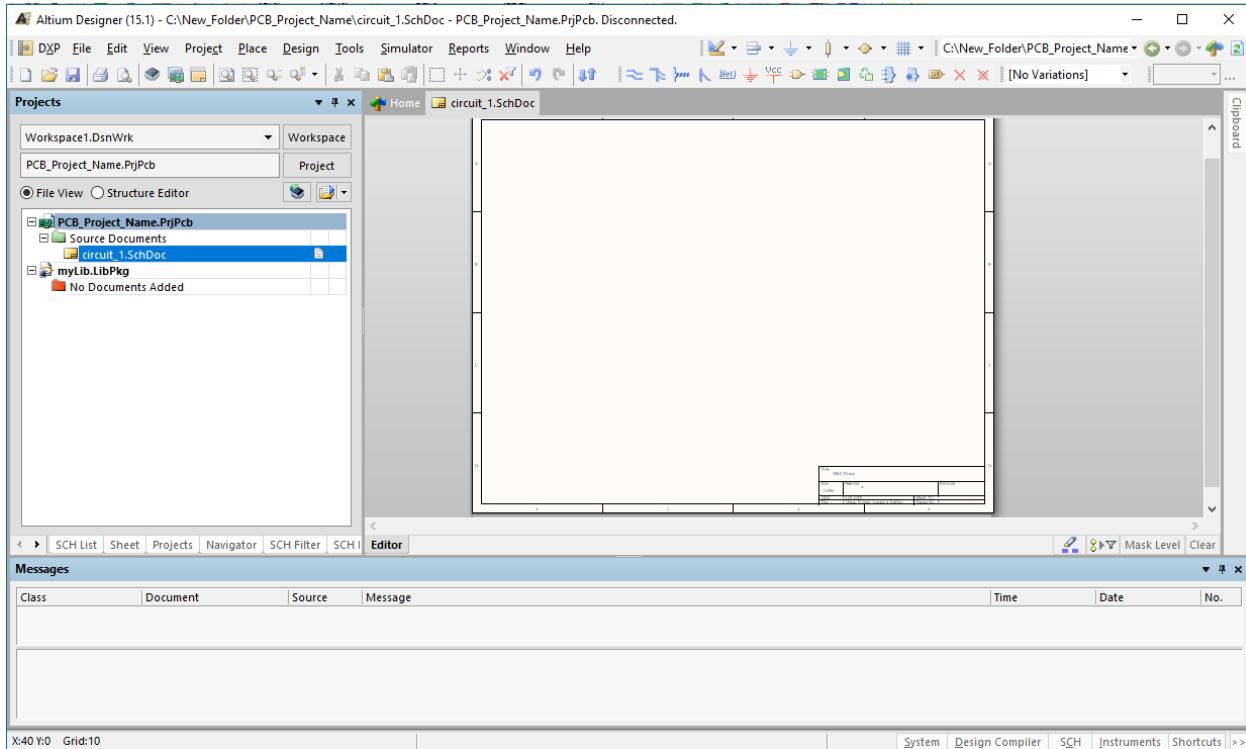


Figure 23: Altium empty Integrated Library.

3.1.1 Schematic (SCH) Library

15. After the Integrated Library is generated it has to be populated with a SCH Library Document and a PCB Library document. Therefor, right click on the Integrated Library Project and chose Add to New Project... → Schematic Library, as shown in Figure 24. And repeat this step to add the PCB Library. By double clicking on the document you can open it, as shown in Figure 25 which shows the added PCB and schematic library as Source Documents of the Integrated Library named myLib.

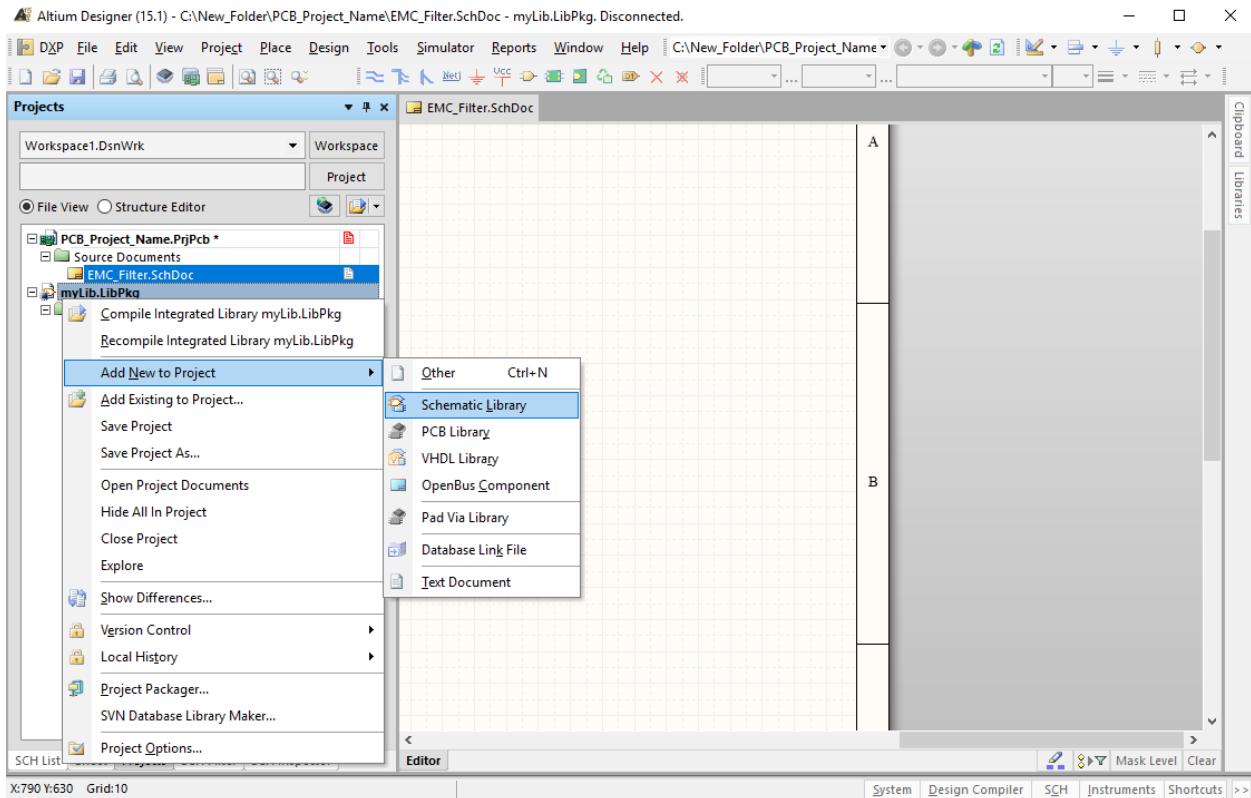


Figure 24: Altium add a SCH Library and a PCB Library document.

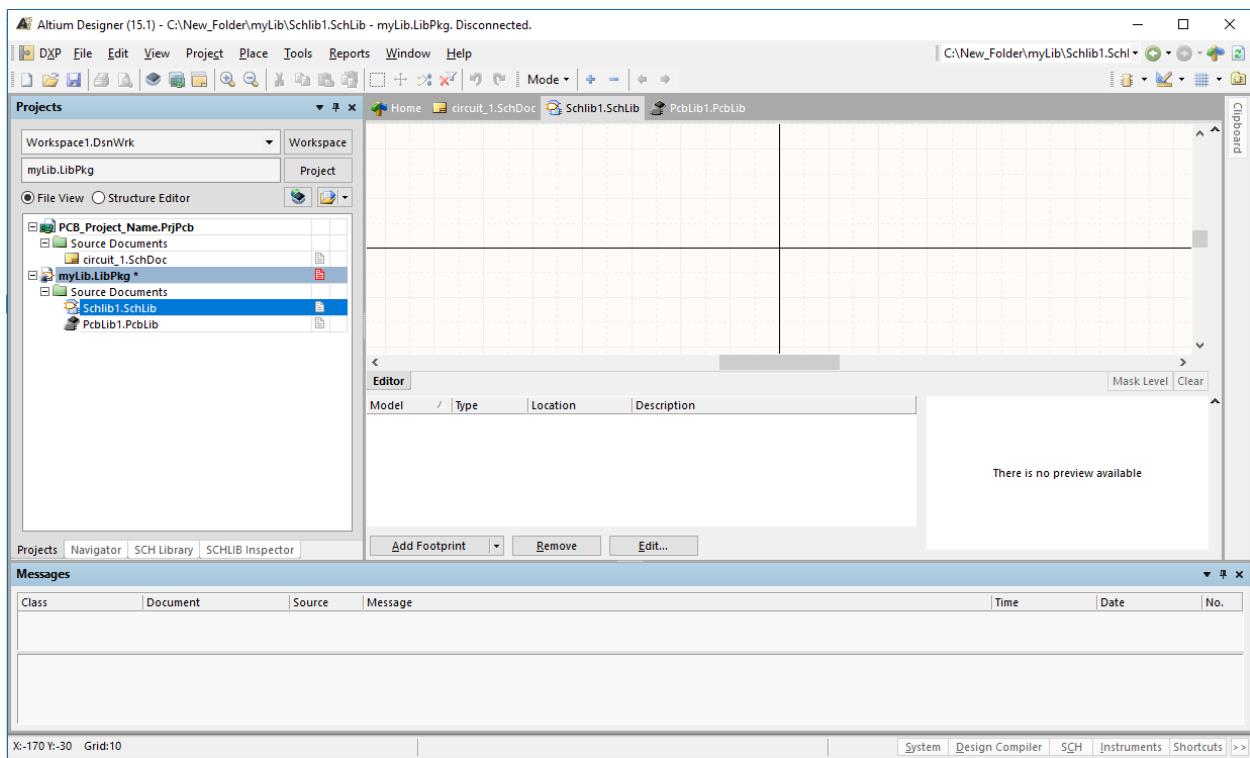


Figure 25: Altium SCH Library and PCB Library.

16. Figure 26 shows the generated open schematic library with two placed pins and blue line drawn in form of a resistor. to place the pins you press P than P and than **TAB** to edit the pin to your needs, which is shown in Figure 27. In this dialog settings of number of the pin which is used to link the pin to the footprint can be made as well as visual properties. So take some time and maybe try one or another thing out by changing it and placing a pin. To place a line hit p to open the place menu and press L or chose Line... as by the pin by hitting **TAB** the line properties dialog pops up and the lane can be changed according to your need, not shown in figure.

IMPORTANT: With G the grid can be selected by placing a pin take care that a 10 mil grid is selected as while you draw a symbol most likely a 5 mil grid is selected or even a 1 mil grid. The grid can be changed by hitting G multiple times.

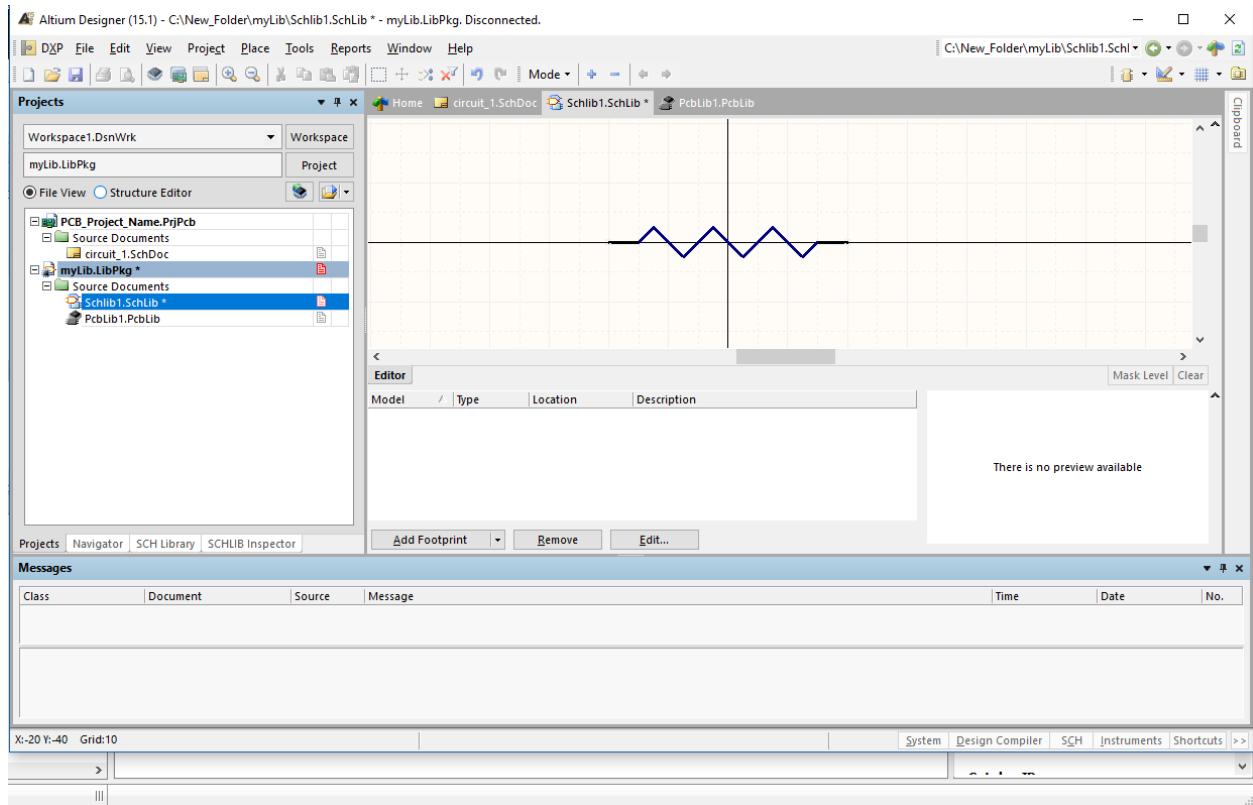


Figure 26: Altium schematic (SCH) library open with an drawn resistor symbol.

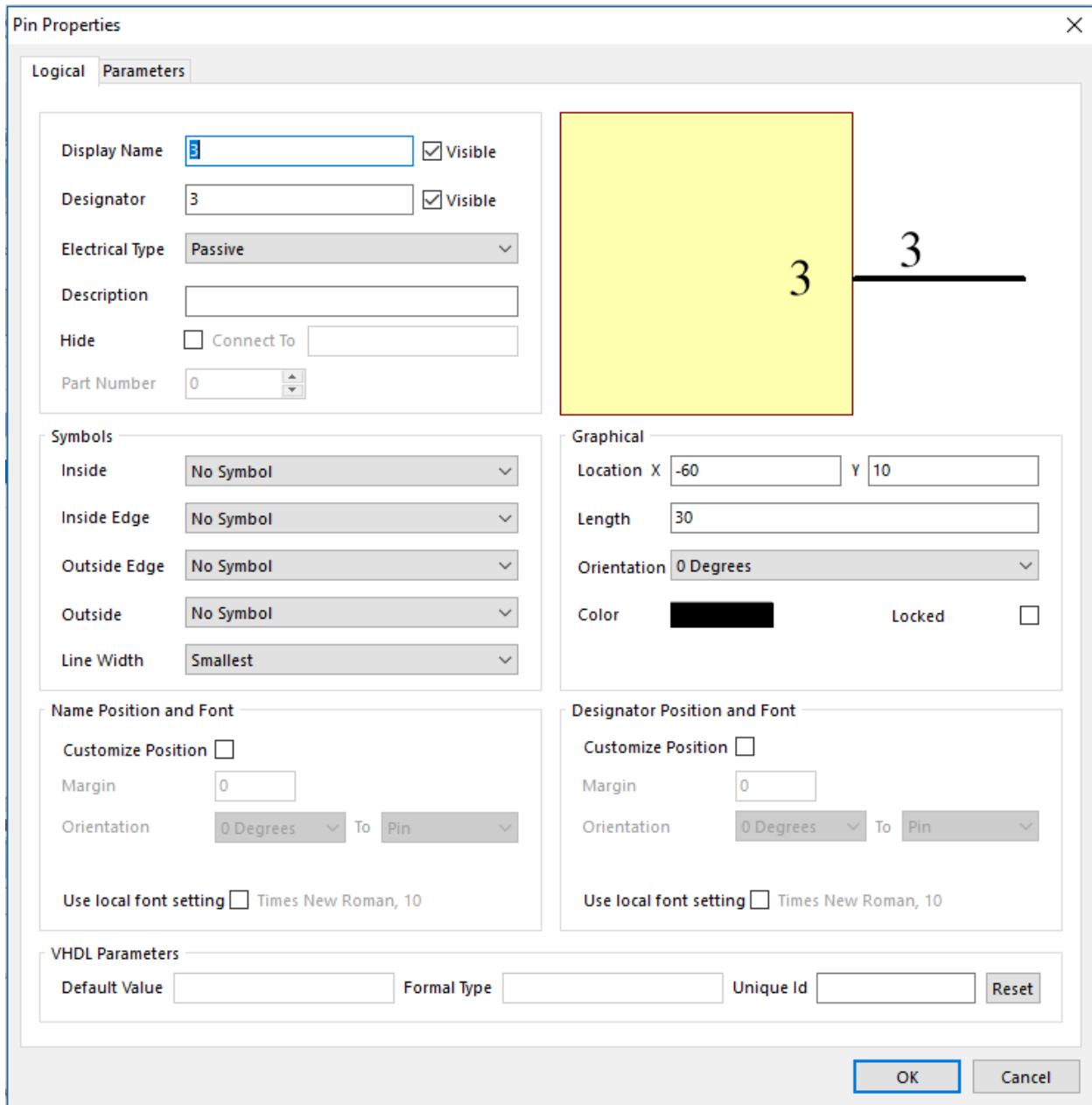


Figure 27: Altium Pin Properties.

17. Figure 28 shows the SCH Library view on the left side of the image and the Library Component Properties as a pop up dialog which shows up by doing a double left mouse click one the Component_1 in the SCH Library Components section which is highlighted blue. As parameters could be added for a document parameters can be added to a component as well Which is shown in the pop up as Value, Footprint, Power Rating, Manufacturer, and Manufacturer No. Those properties can be made visible later on in the Schematic after placing a component and can be changed any time. Special care has to be taken by the Default Designator which will be the reference designator shown in the schematic the ? symbol serves there as a place holder for the Annotation tool that can be found under Tools as you are looking at a Schematic document not a Schematic Library Document. A large compendium of reference designators can be found under this link Graphic Symbols for Electrical and Electronics Diagrams [IEEERefDes]. If a specific part is used a supplier can be added with the exact part number which has direct access, online, to suppliers database. Furthermore, you can add spice models which would allow a tool in Altium to perform signal integrity analysis or more common add a footprint which has to be created first. Don't forget to save.

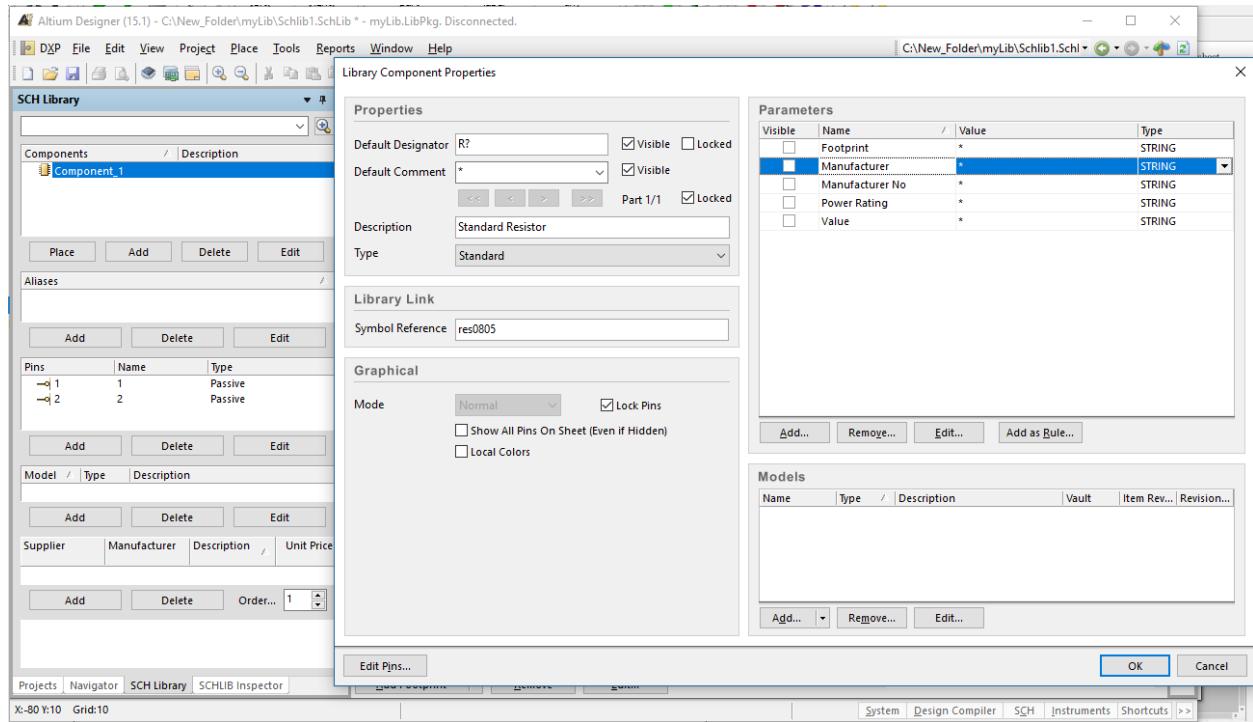


Figure 28: Altium SCH Library Properties.

3.1.2 Printed Circuit Board (PCB) Library

18. Open the PCB Library document to layout a footprint for the resistor for what you made the symbol, the empty PCB Library should look similar to Figure 29. First place a pad by pressing P for place than P again for selecting pad than press **TAB** to open the pad dialog, which is shown in Figure 30. The pad dialog allows you to customize the pad, because a pad can have different shapes, a hole, and much more. For now because we make the footprint of an 0805 surface mount resistor according to the recommended land pattern from Vishay, shown in Figure 31 and we will design it for reflow and not wave soldering. Note, that the units are metric not imperial. Altium is able to handle that so most values you will use are in mil and are by default used as mil but you can use any unit so in this case millimeter (mm) to do so just write the unit behind the value you wish to set as shown in Figure 32 in the part Size and Shape. As long as you not have placed the pad onto the document don't change anything under location, rather close the dialog and place the pad press escape than double left click on the placed pad to open the dialog again and set the location according to the Vishay land pattern. Take your time by doing so and calculate the correct values where to place the pad that saves you time because the second pad is symmetrical to the first one and you will use copy and place to make the second pad. Select pad no. 1 by one left mouse click and press **CTRL+C** after that you will see a cross appearing as your mouse and the next one left mouse click sets a reference point that is used for rotation of the selected object. Set the reference point onto the center point($x = 0, y = 0$, usually shown somewhere on the top but can be modified as well if not the with shortcuts) and do one left mouse click, most of the time it helps as you zoom in (**CTRL+Mouse wheel**) or change the grid size (Press **G** and chose **grid** out of pop up menu, notice the grid option is different in PCB Library document then in an SCH Library document). Now use **CTRL+V** to paste the copied pad, you will notice the offset to the mouse position as you set the reference not in the middle of the part but in the center of the sheet. To rotate the pad around the reference point hit **SPACE**, each stroke will rotate counter clockwise by 90° angle. Next you change the Designator of the copied pad by opening the pad dialog and change it to 2, if you did everything right and calculated the right position according to the Vishay land pattern it should look as shown in Figure 33. By the way the reason why the package 0805 is called so is that 08 refers to the length in deka mils so 80 mils in length and 05 refers to the width in deka mils so 50 mils, be aware that there is a similar naming convention for the same package in metric units and not imperial units.

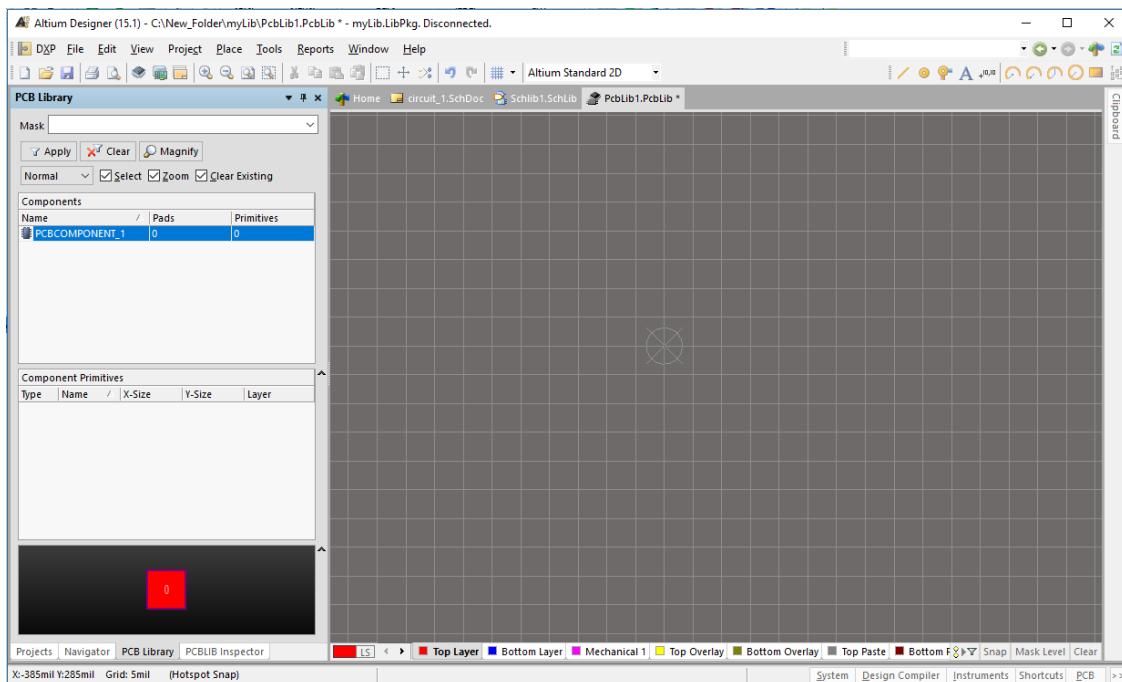


Figure 29: Altium empty PCB Library.

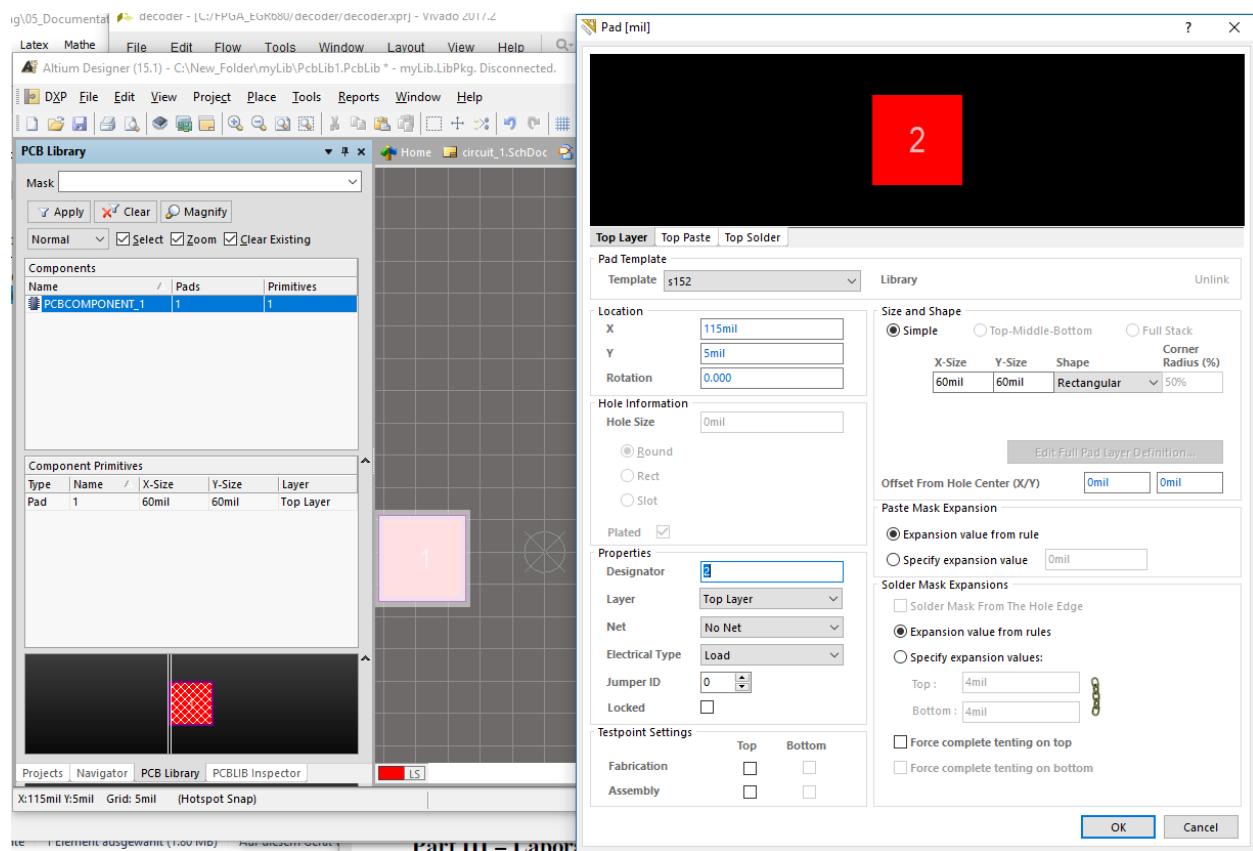


Figure 30: Altium PCB Library view to the left and Pad Dialog to the right.

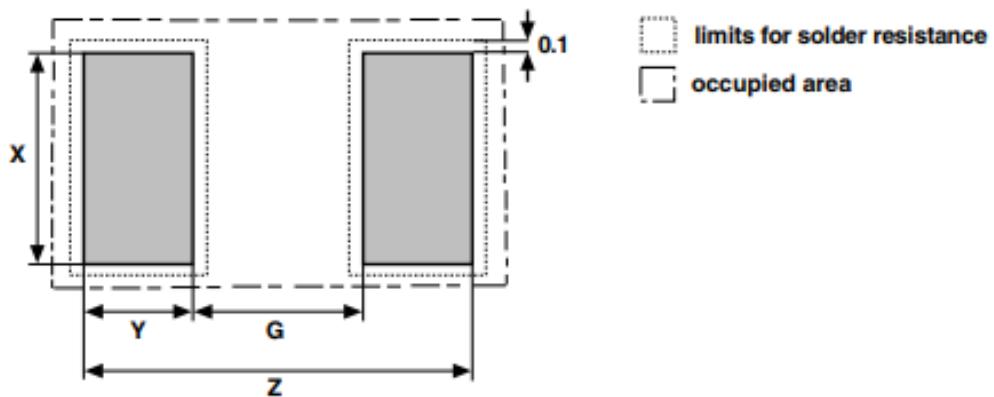


Recommended Solder Pad Dimensions

Surface Mount Resistors

Vishay Beyschlag

PATTERN STYLES FOR SMD RESISTORS



Dimensions in mm

TYPE	WAVE SOLDERING				REFLOW SOLDERING			
	G (mm)	Y (mm)	X (mm)	Z (mm)	G (mm)	Y (mm)	X (mm)	Z (mm)
MCS 0402	-	-	-	-	0.25	0.6	0.55	1.45
MCT 0603	0.5	1.2	1.1	2.9	0.5	0.95	0.95	2.4
MCU 0805	0.65	1.4	1.5	3.45	0.65	1.1	1.4	2.85
MCA 1206	1.5	1.6	1.9	4.7	1.5	1.25	1.75	4.0
MMU 0102	0.65	1.4	1.5	3.45	0.65	1.1	1.4	2.85
MMA 0204	1.5	1.6	1.9	4.7	1.5	1.25	1.75	4.0
MMB 0207	2.8	2.3	2.5	7.4	2.8	2.2	2.2	7.2

Figure 31: Vishay Recommended Land Pattern for surface mount resistors [VishayLandPattBeyschlag].

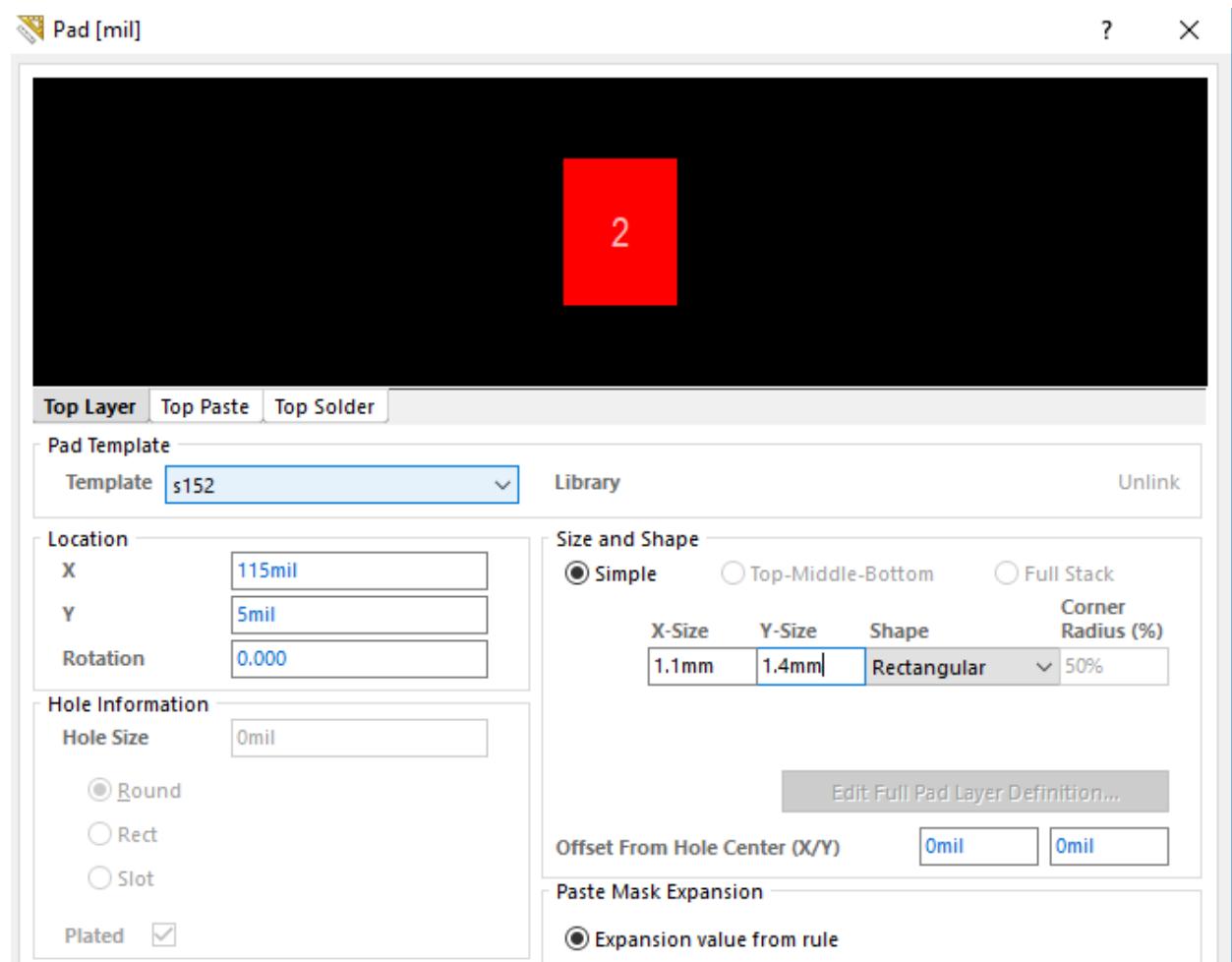


Figure 32: Altium Pad Dialog used with metric units.

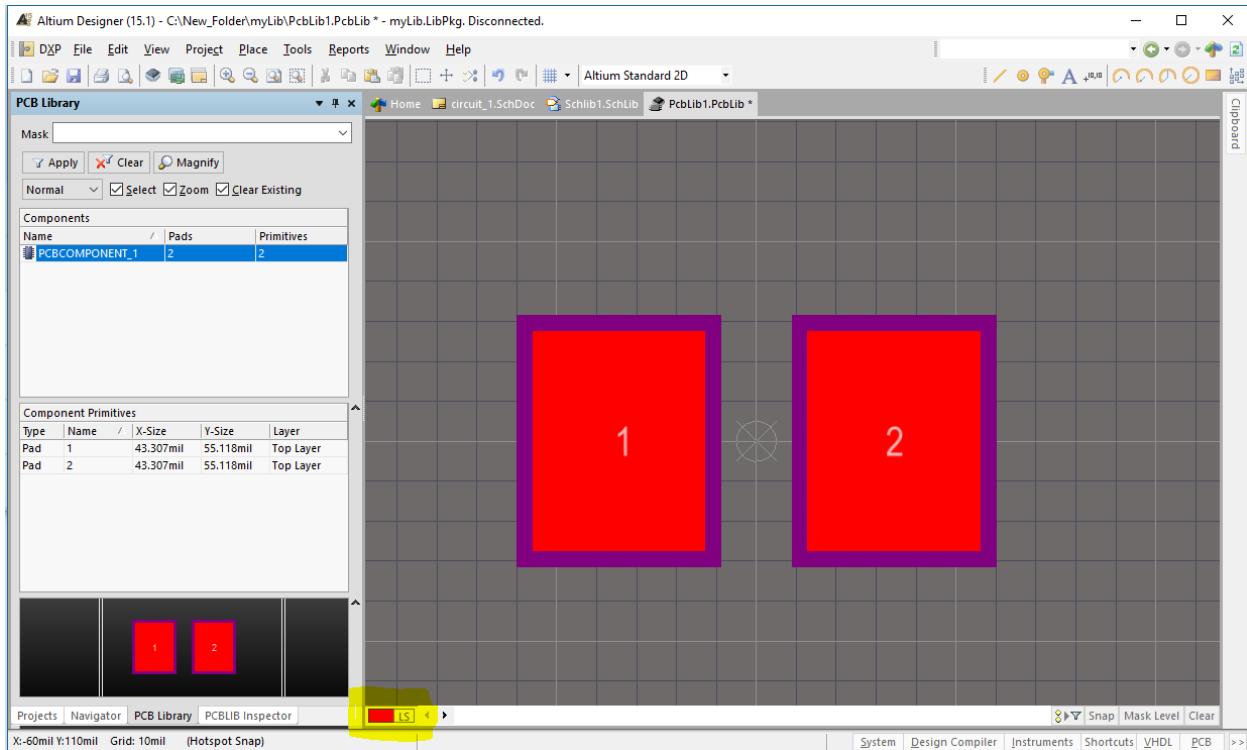


Figure 33: Altium Pad Placed according to Vishay recommended land pattern for a 0805 SMD resistor.

- Now change the naming of the footprint to res0805 and add a component height, which can be found in a data sheet, for now we will use 18 mil as height. As description use the following string "Standard SMD resistor, Vishay recommended land pattern for **Reflow**.". Additionally, add a silk screen that will aide pick and place machines and the design process latter on. So far, you only used the top layer. To add silk screen we introduce the Layer Manager, press **L** or the highlighted Current Layer field button **LS**, shown in Figure 33. The View Configuration dialog will pop up which allows you to show ()enable) different layers. Multiple layers together are known as layer stack up which will be introduced later on in more details.

Ensure that the top silk screen layer, named Top Overlay, is shown and configure the View Configuration as shown in Figure 35. At this point I like to introduce an important shortcut that allows to highlight a specific layer, because layers are sometimes overlapping and due to that not visible. Press **CTRL** and hold it, select the Top Paste layer on the bottom of the screen, it should look similar as shown in Figure 36. To reverse the effect hold **CTRL** and perform one left mouse click somewhere in the document where no layer is shown.

Select the Top Overlay, press **P** than press **L** to draw a line onto the Top overlay with a grid selected of 10 mils. Keep a equal or greater distance of the outer edge of the silkscreen to the Top Solder mask (Top Solder mask is an negative layer and defines an cut out of the Solder Mask!), the minimal distance is defined by the manufacturer that you will give the contract to produce your PCB board. Choose a line width of 6 mils to draw the surroundings of the SMD component. To check that you have a distance between Top Paste and Silkscreen use **CTRL+M** to change to measurement mode and change the grid to 1 mil so you can measure the distance between and ensure rule conformance. The applied Silkscreen should look similar to Figure 37. It might be a good time to use the measure tool **CTRL+M** to double check that the top layer is according to the recommended land pattern!

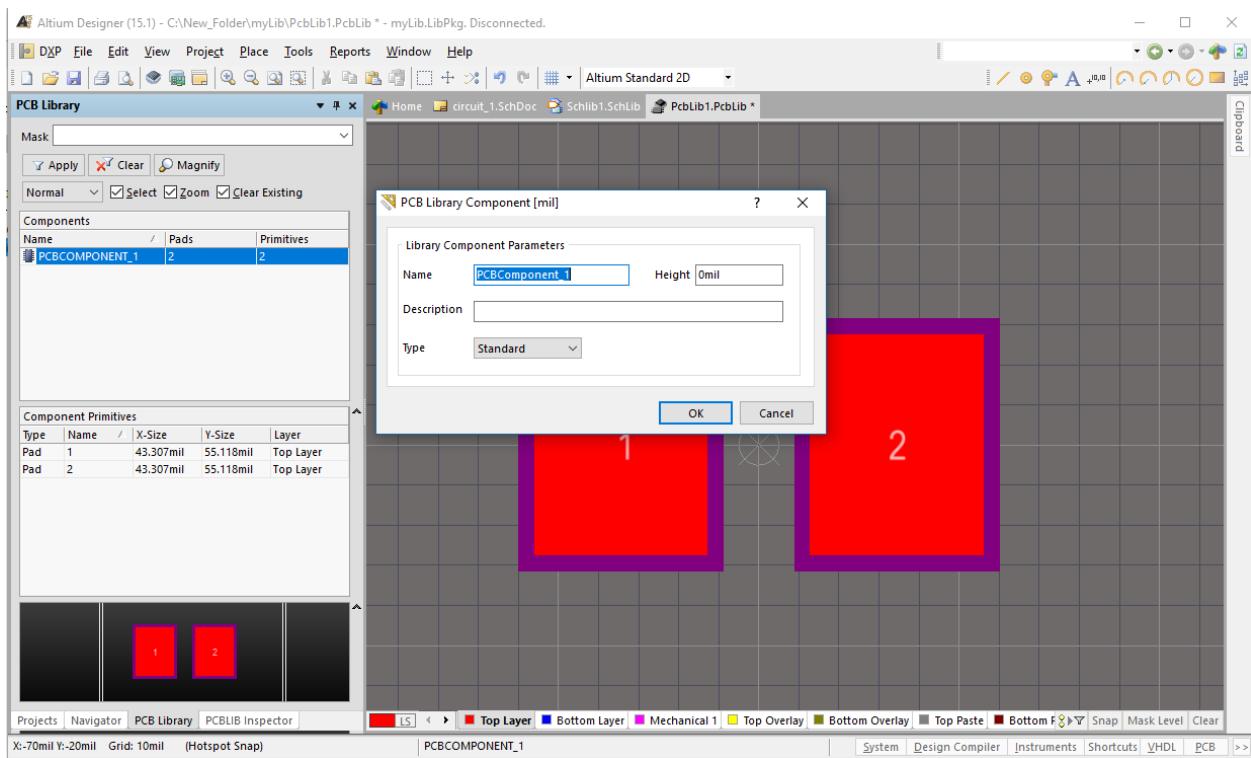


Figure 34: Altium footprint name, height, and description.

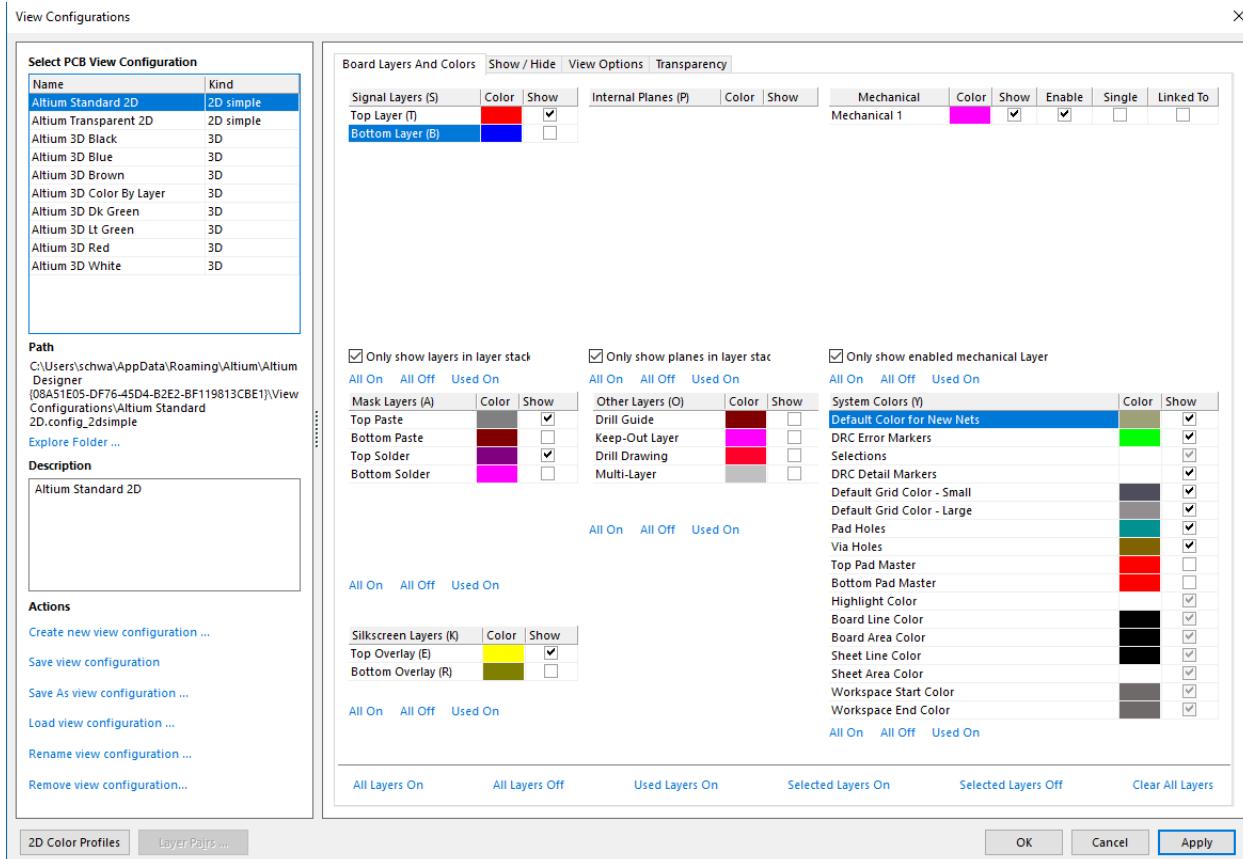


Figure 35: Altium View Configuration that shows Top Layer, Mechanical 1, Top Overlay, Top Paste, Top Solder.

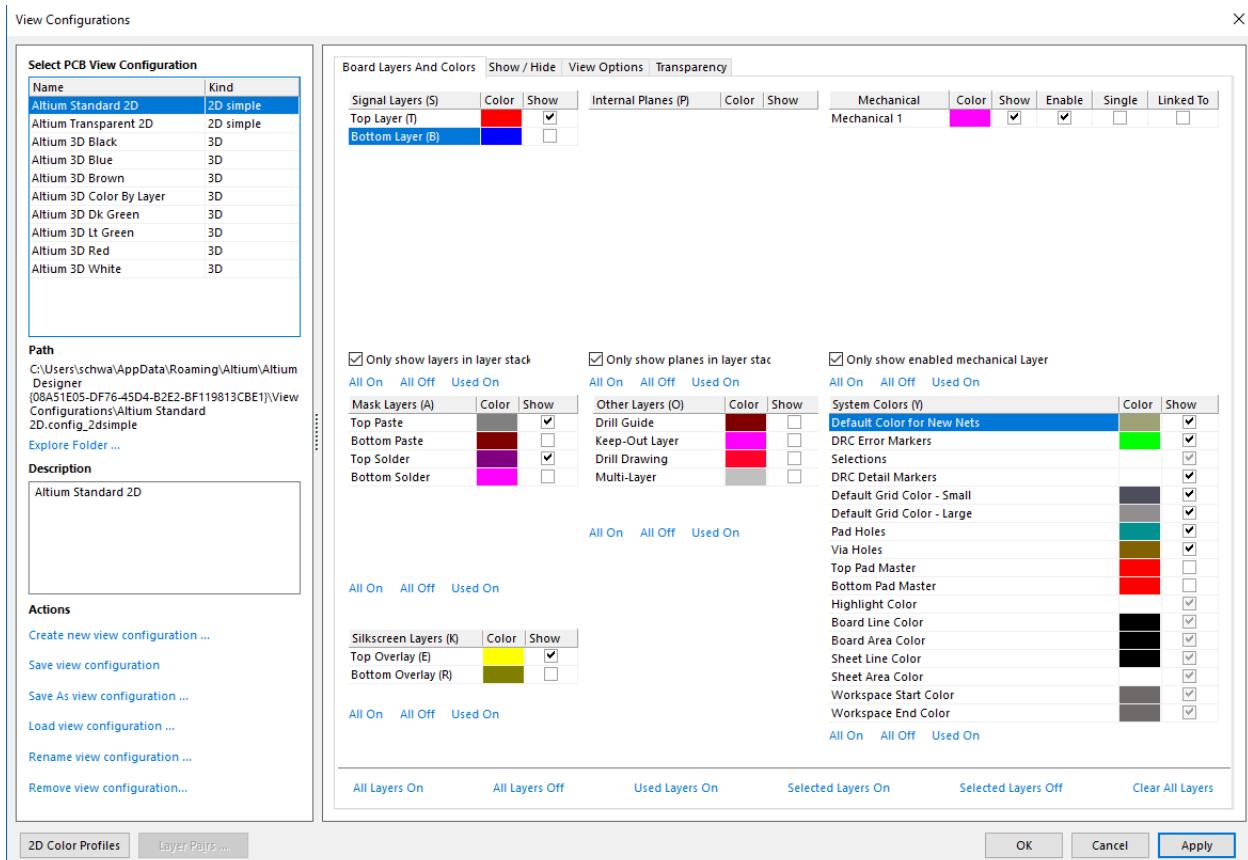


Figure 36: Altium View Configuration that shows Top Layer, Mechanical 1, Top Overlay, Top Paste, Top Solder.

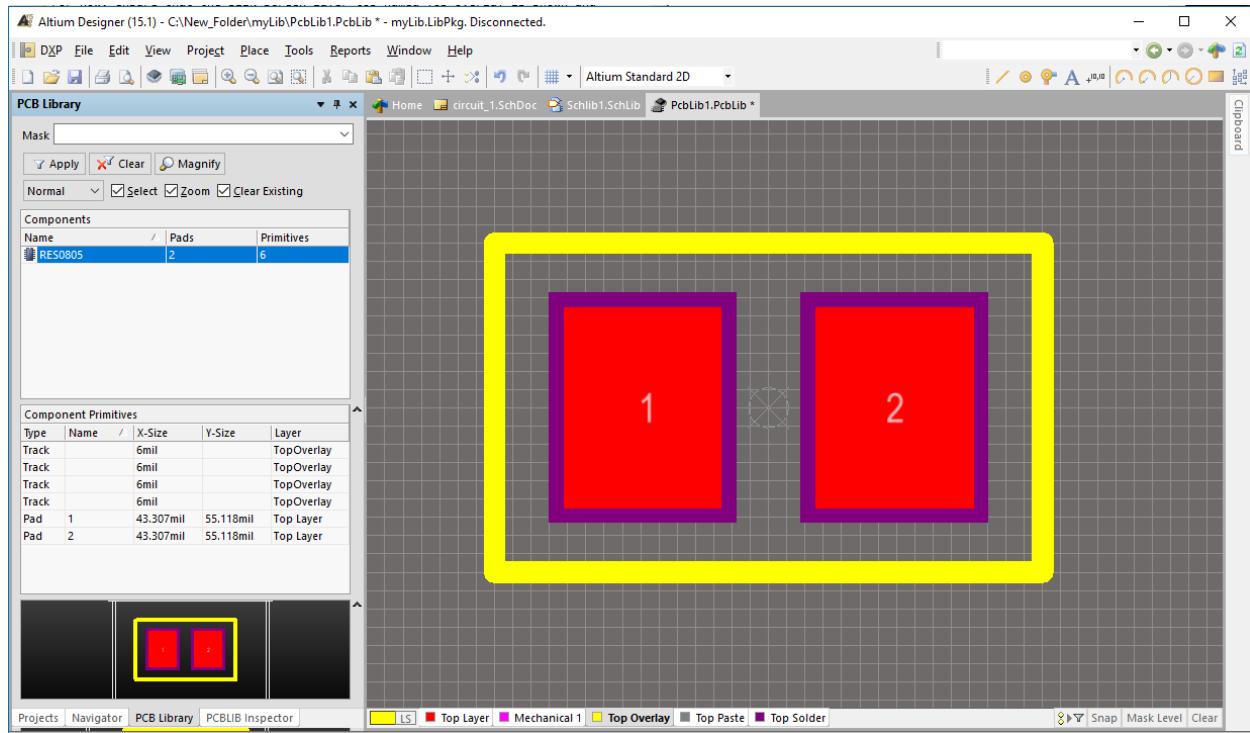


Figure 37: Altium View Configuration that shows Top Layer, Mechanical 1, Top Overlay, Top Paste, Top Solder.

20. Modern computer aided-design (CAD) software is not confined to 2D drawings rather uses 3D drawings. So lets build an body that shows in 3D the resistor. To do so press **P** and **B** which opens the 3D Body dialog. The 3d Body dialog is shown in 38. Here you specify the hight and the color of the body that shall be extruded while the length and the width of the body is defined by using your mouse and a **smart choice of grid size**.

To properly design a resistor we need three body parts, two contacts and a middle ceramic part. As we recall the height of a SMD 0805 resistor is ≈ 18 mils and we assume for now there is 1 mil standoff, most likely it will have a small standoff because solder will be in between the coper and the part. The drawing in 2D is shown in Figure 39. The part can also be viewed in 3D view mode which you can change by pressing **3** on the keyboard, to return to the 2D view mode press **2** on the keyboard. To change the angle of view in 3D mode **hold SHIFT pressed and hold right mouse button clicked** to change the angle of view with perspective reference set at the place where the mouse was, as you hold SHIFT. The 3D view of the resistor is shown in Figure 40.

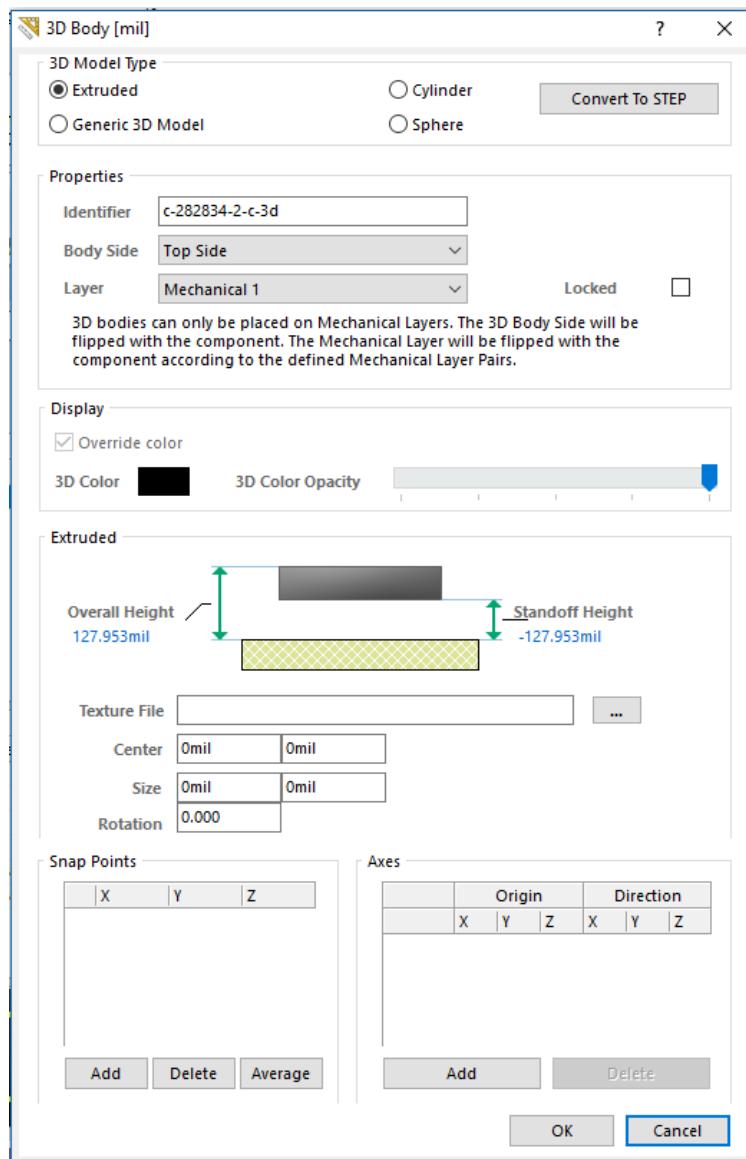


Figure 38: Altium 3D Body dialog.

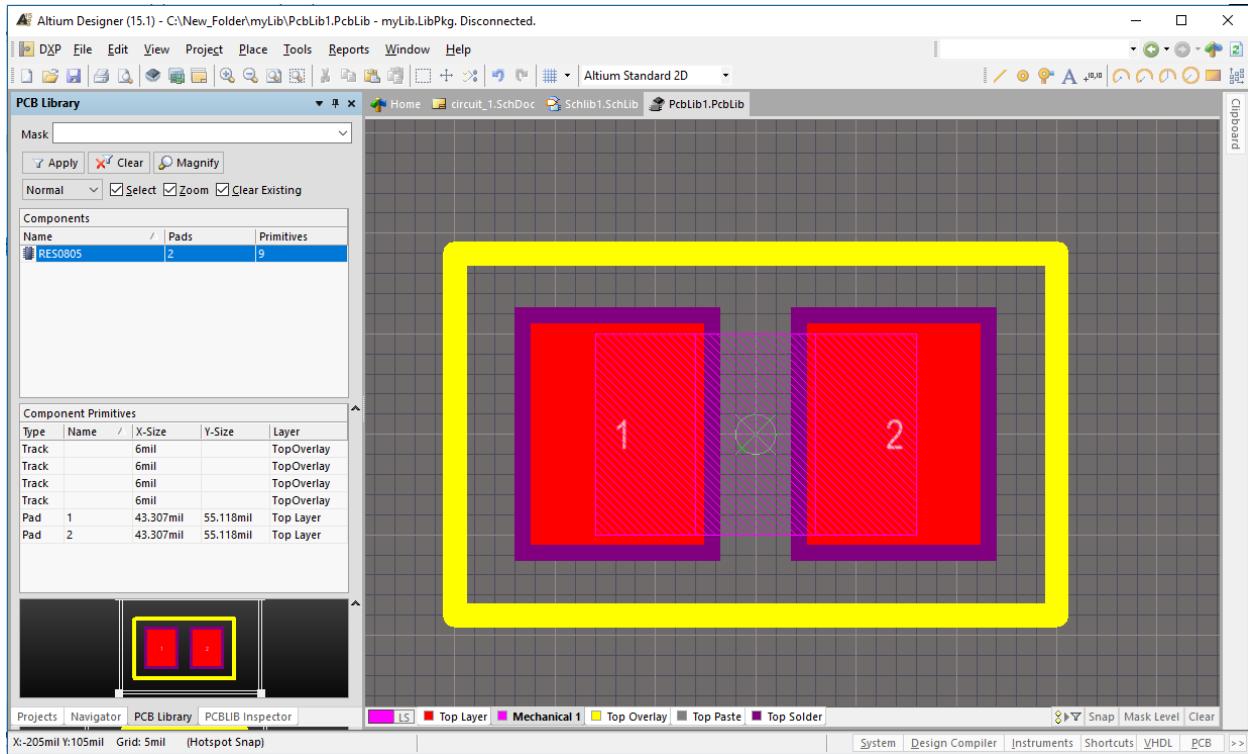


Figure 39: Altium 3D Body placed as 3 parts in the 2D view mode for a 0805 SMD resistor.

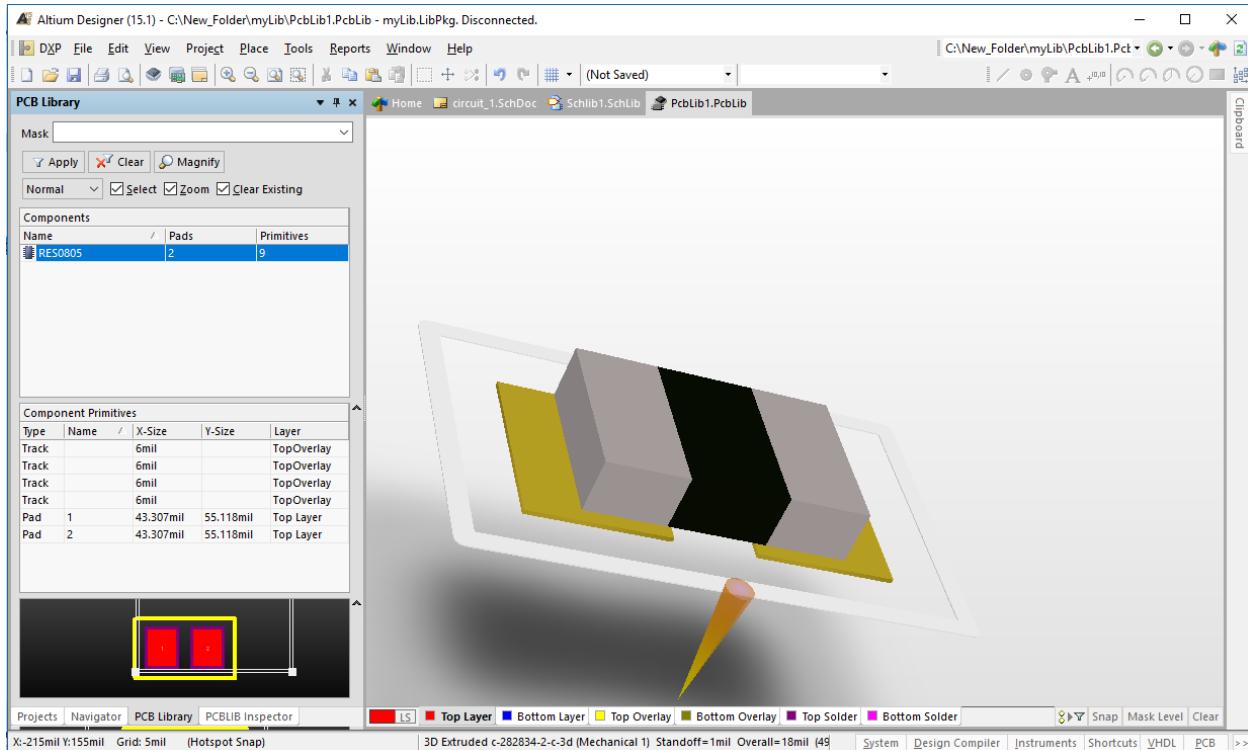


Figure 40: Altium 3D Body placed as 3 parts in the 3D view mode for a 0805 SMD resistor.

21. Before we add the footprint to the schematic component in the library, lets check if our footprint is manufacturer rule conform. A good way to do this is to choose a cheap mainstream manufacturer as example PCBway from China and use their standard rules to confirm that the footprint is according to the rules, which you can find under the following link <https://www.pcbway.com/capabilities.html>. Watch out especially for hole diameter min. max., silk screen distance, trace width, and gaps. By default try not to have a smaller trace width than 10 mils and a gap of 10 mils which is often seen as 10/10 mils width. Don't think too much because it's a tutorial and you can still change your footprint at any time, if there is an issue! **Now, save all CTRL+S!**

IMPORTANT: You really want now what your manufacturer can do. Otherwise, you design something that will be super expansive to manufacturer or even worse, not possible at all!

22. Now go back to the SCH library document open the Library Component Properties dialog of the drawn resistor symbol and add the drawn footprint under model, which should look like in Figure 41. Press OK to close the dialog and notice the changes that have been made in the SCH Library View on the left side of the software, where the pins are mapped and the footprint is added, as shown in Figure 42. **Save with CTRL+S.**

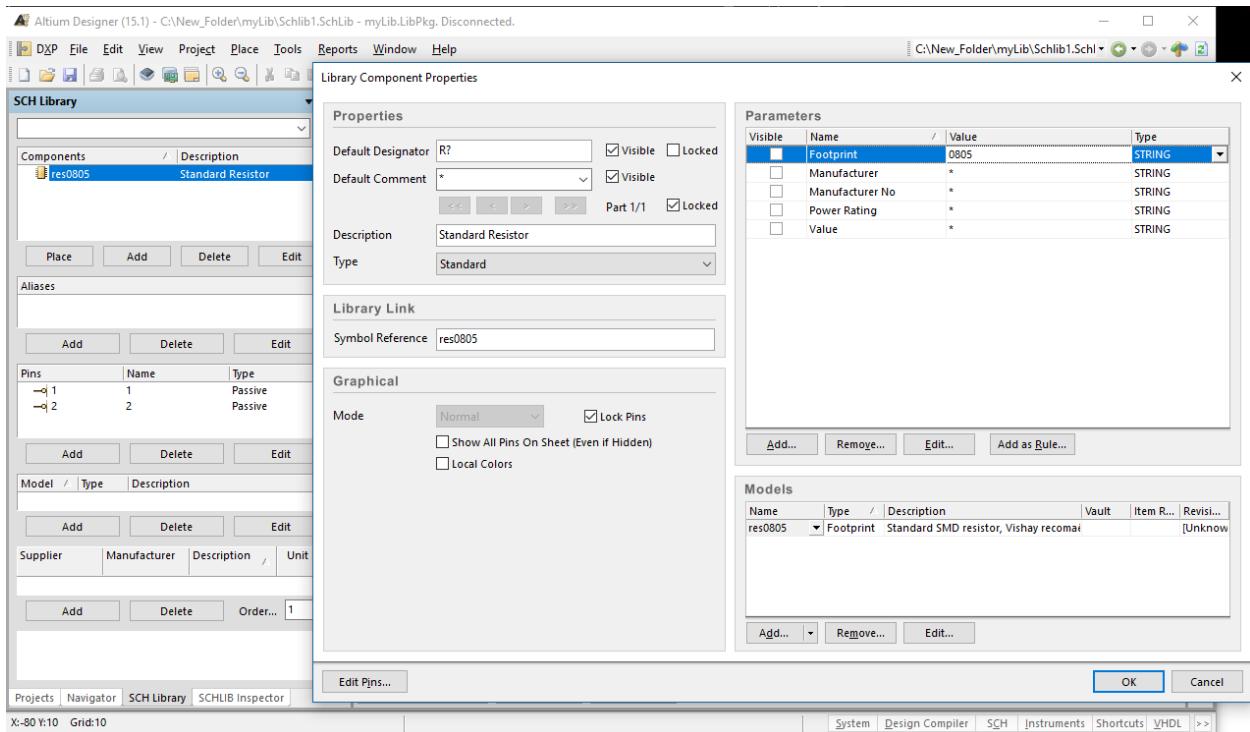


Figure 41: Altium SCH Library add a footprint to component.

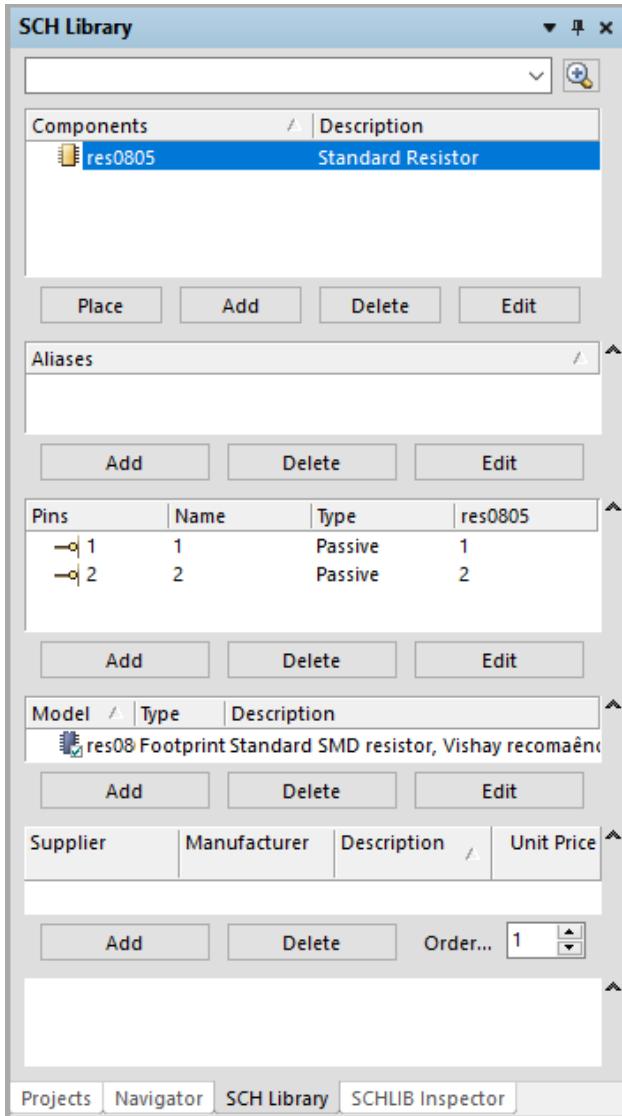


Figure 42: Altium SCH Library footprint added to component.

23. To use a Integrated Library the library needs to be compiled first. Save the Integrated Library than right click on it in the Project View, and click Compile Integrated Library myLib.LibPkg, if there are errors a Message view will pop up. To check if the Integrated Library compilation is successful open the message view and check for the message
"Class Document Source Message Time Date No. [Info] myLib.LibPkg Compiler Compile successful, no errors found. 12:16:16 13.09.2018 1"
To open the Message view use the highlighted bar and click on System, and select Message as shown in Figure 44.

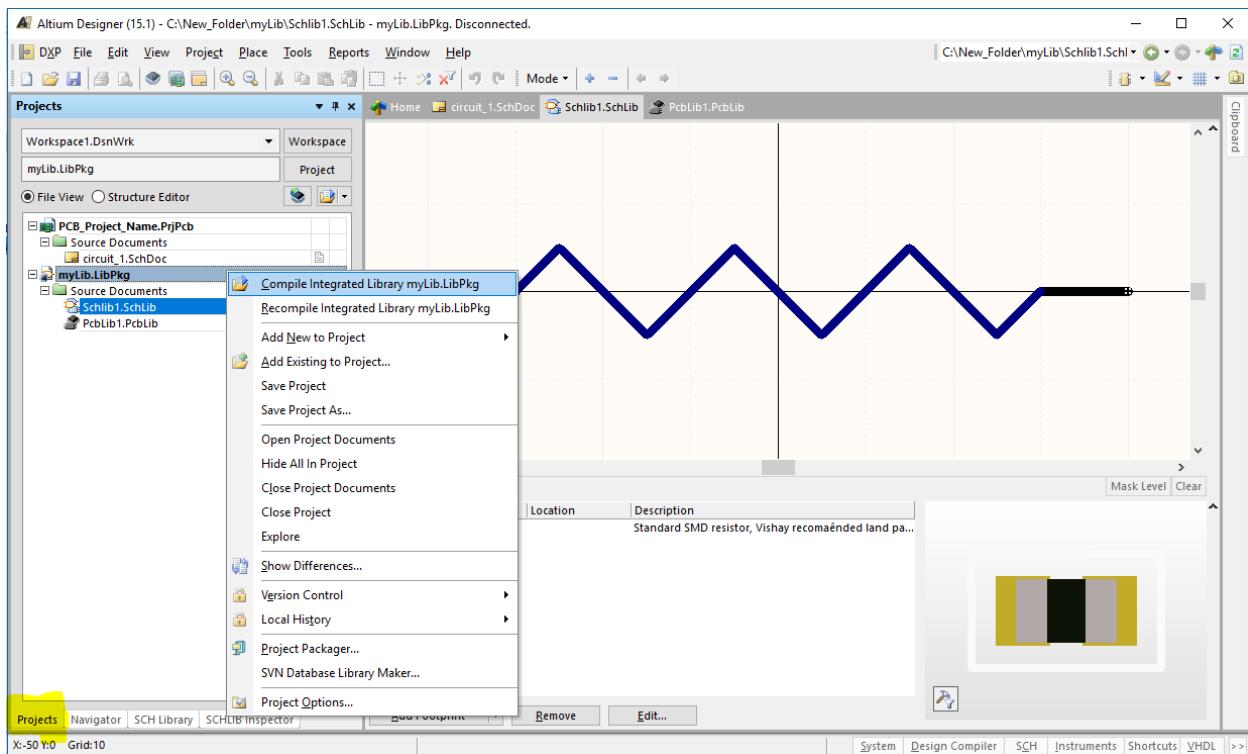


Figure 43: Altium Project View compile Integrated Library.

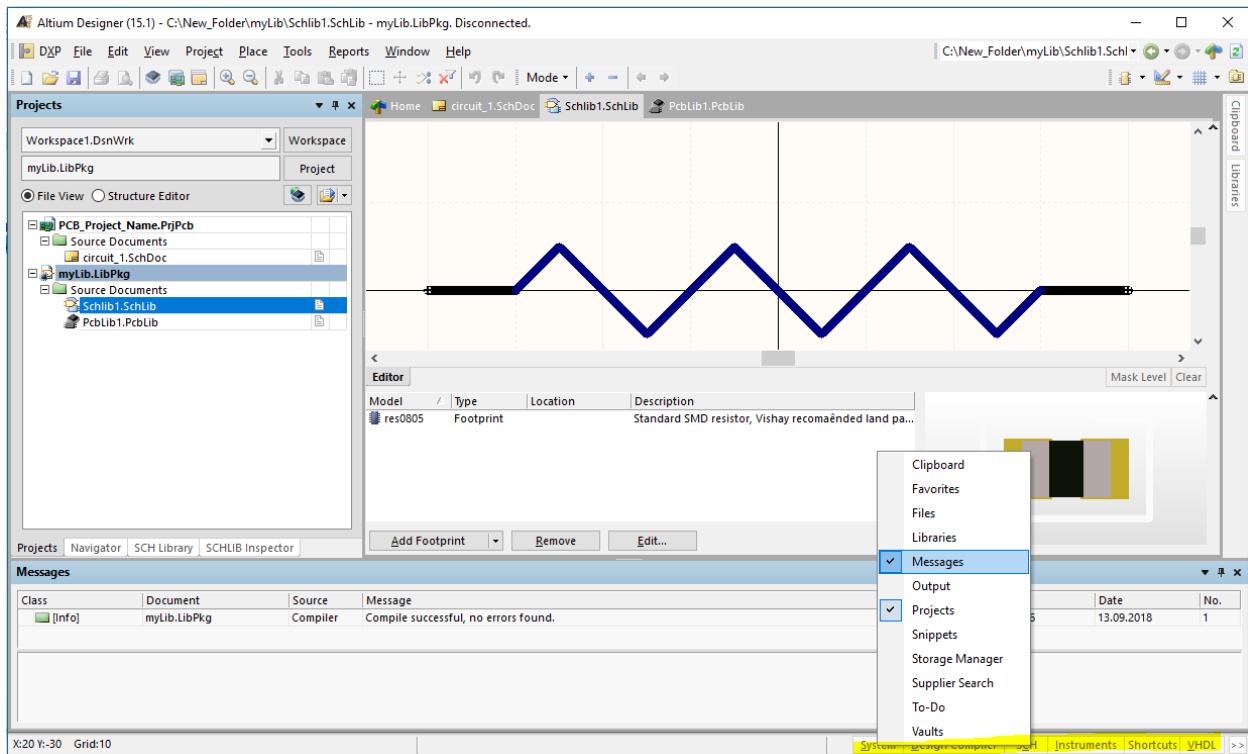


Figure 44: Altium Message View that shows the message output of the compiler.

24. Unfortunately, most of the schematics are not drawn by using a single component. Go ahead and add a 0805 capacitor, 2525 inductor, and a 1616 inductor component to your Integrated Library. The data sheets are in the Appendix 4 under sub-sections 4.4, and 4.5. The components can also be found on digi-key by using the following two links:
<https://www.digikey.com/products/en?keywords=ihlp1616>,
<https://www.digikey.com/products/en?keywords=ihlp2525>
25. **IMPORTANT:** Footprints and schematic symbols can be copied and pasted from one integrated library to another this avoids a lot of redundant work! So, try to split the work with your class mates so that each one does a inductor and another does an capacitor and copy the components instead of drawing all by your own. Keep in mind every copied component has to be verified which means you open the data sheet and remeasure the footprint and check the pin out for correctness.

Hint: If you do not see the copied components in your library in the schematic sheet, ask yourself "Did I save and compile the Integrated Library?".

3.2 Schematic

After the library has been created start drawing a schematic. Notice, most of the shortcuts you learned so far are valid also for a schematic document.

In this tutorial we will design an EMC Filter that allows to equip different values and perform measurements on it to learn the different impacts and effects around the EMC Filter.

Open the schematic document that we prepared prior in this tutorial. As you might have noticed previously, the title of the document is not the name of the file. To change the name of the file open the Storage Manager dialog by left clicking System, on the menu lower left corner and select Storage manager with left mouse click. Right click on the file which should be renamed and chose Rename, as shown in Figure 45, the content is from the following web page [[RenameAltiumDoc](#)]. After doing so and closing the dialog your screen should be looking similar to Figure 46.

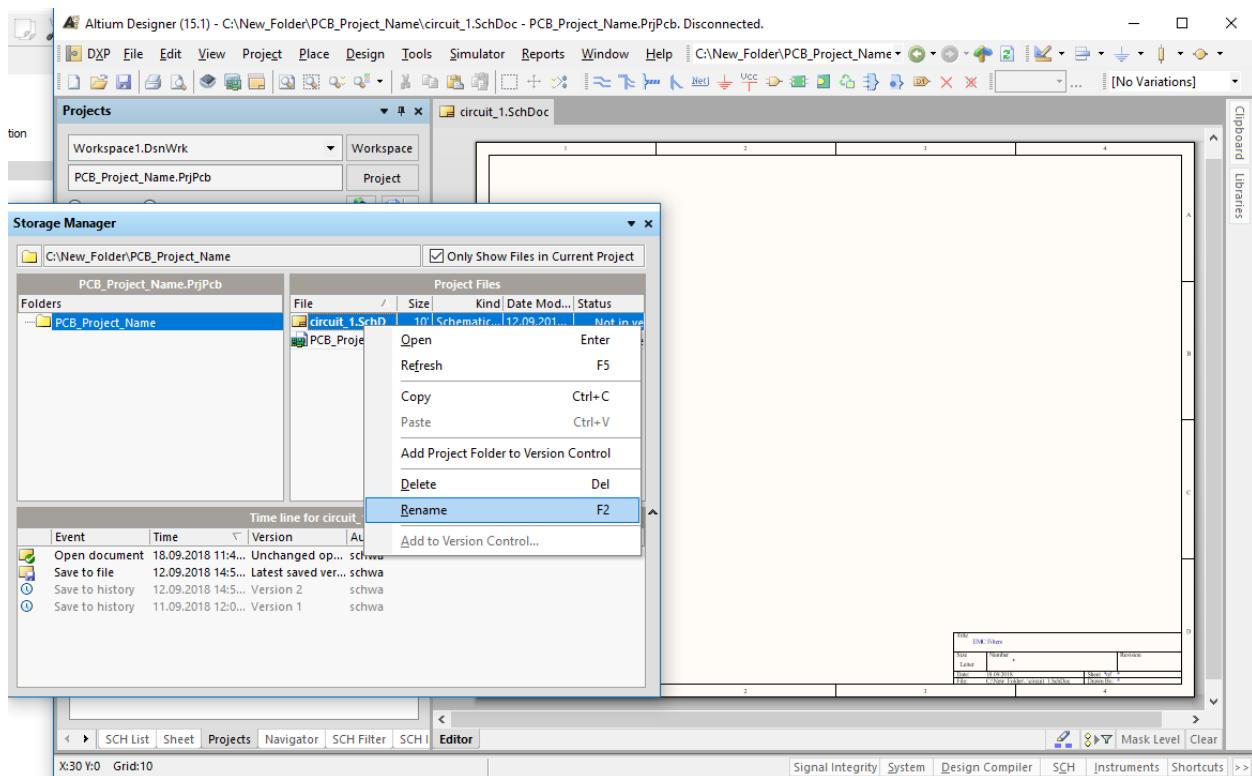


Figure 45: Altium Rename a file without Save As... by using the Storage Manager.

26. Your screen should look similar to what is shown in Figure 46.

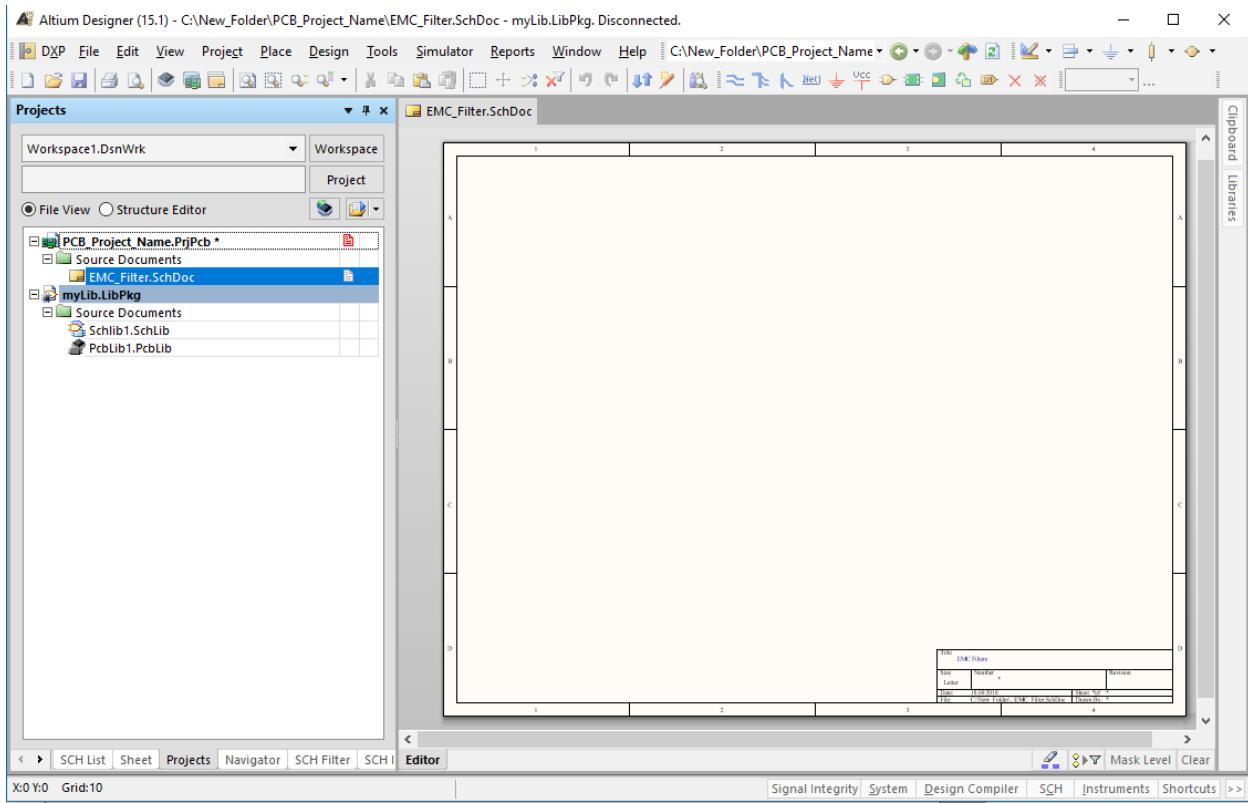


Figure 46: Altium empty schematic document EMC_Filter.

27. The goal is now to build a basic EMC Filter board according to the following LTSpice schematic shown in Figure 47. Figure 48 shows how the LTSpice model is used to simulate a 1_{th} order LC filter which builds the basis for a filter design that can be validated with your designed hardware. As you may notice there are no footprints in neither of one of the two LTSpice figures or chosen components.

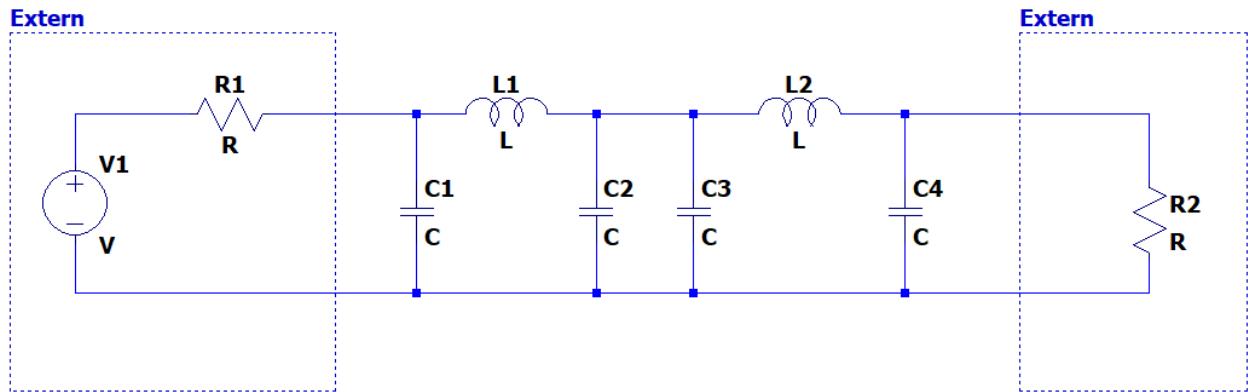


Figure 47: Altium LTSpice schematic generic EMC_Filter.

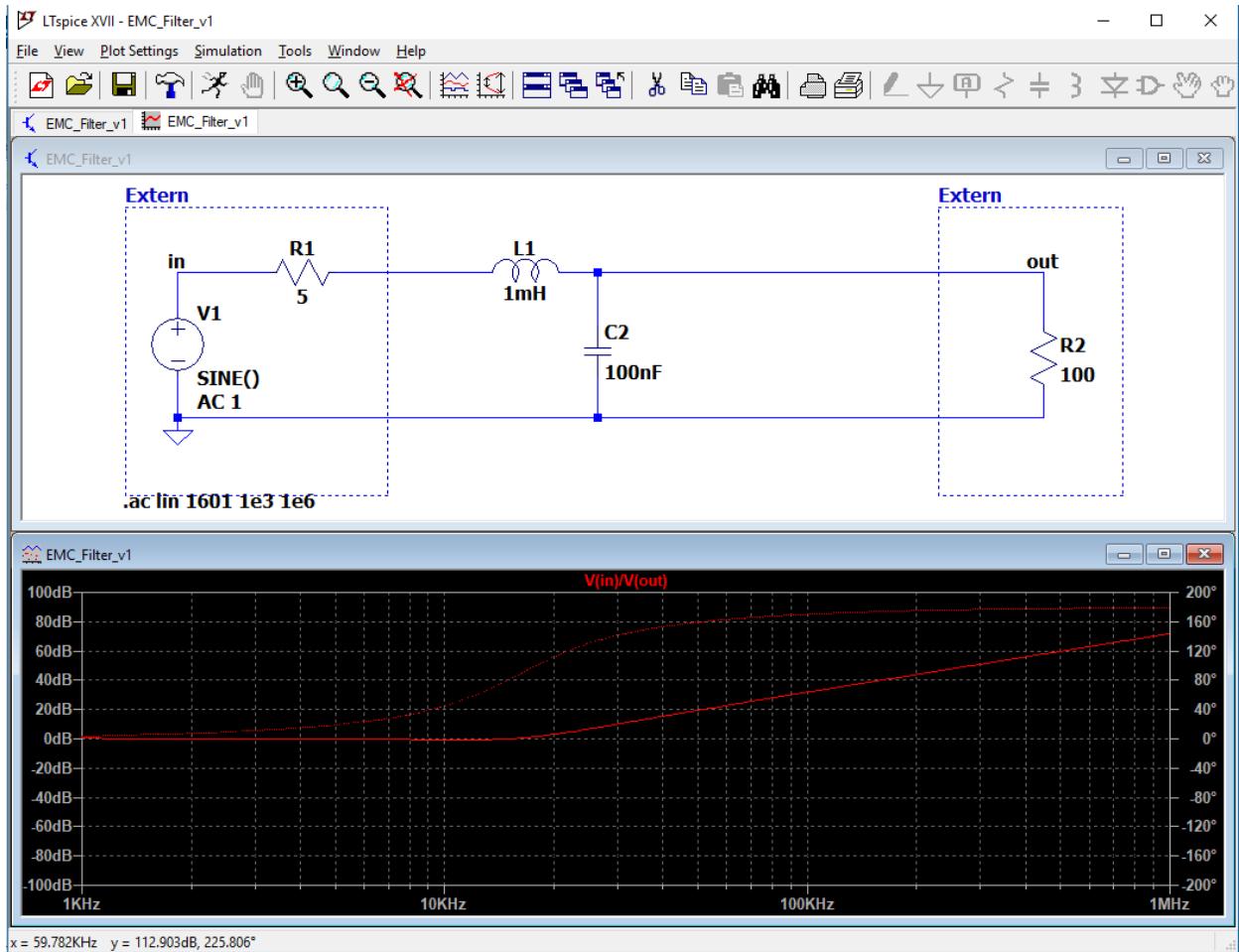


Figure 48: LTSpice EMC Filter - 1th order LC Filter [Adamczyk2017].

28. This means that the first big design decision has to be made which is the decision what package size makes the most sense and gives the most freedom of choice according to the design specifications. To make it extra hard we basically specify nothing here but the author of this document assumes that you gone use the previous created components.

In real world the engineer knows what to do out of personal experience, or knows somebody that has the experience and ask those (this was what the author of the this document did), or you start searching on digi-key and mouser (what the author of this document did too), mouser filter for induc-tors shown in Figure 49.

Hint: If your workstation has only one screen, it is helpful to print the circuit shown in Figure 47 so you can make nodes on paper which helps extremely to make design decisions and you can spare a second screen (the author of this document prints most of the schematics in paper form).

Search results for inductor:

Manufacturer	Shielding	Tolerance	Maximum DC Current	Maximum DC Resistance	Self Resonant Frequency	Minimum Operating Temperature	Maximum Operating Temperature	Q Minimum	Test Frequency	Mounting Style	Length	Width	Height	Application	Series
--- Most Popular ---	Shielded	5%	30 mA	10 Ohms	1.9 MHz	-55 C	+85 C	20	1 kHz 100 kHz 0.25 MHz 0.525 MHz 0.252 kHz 0.79 MHz 0.796 MHz	PCB Mount	4.5 mm	3.2 mm	2.6 mm	Power	1812LS
Bourns	Unshielded	10%	50 mA	16 Ohms	2 MHz	-40 C	+100 C	28		4.8 mm	3.5 mm	3.2 mm	RF	1812PS	
Colcraft			66 mA	25 Ohms	2.3 MHz	-25 C	+105 C	30		4.95 mm	3.81 mm	3.43 mm		AISM-1812	
Murata			70 mA	30 Ohms	2.5 MHz		+125 C	40		5.87 mm	4.98 mm	3.5 mm		B82432T	
Würth Electronics			40 Ohms	44 Ohms	7 MHz									CM45	
Vishay														IMC	
EPCOS / TDK														ISC-1812	

Figure 49: Altium Mouser filter for a inductor with 1mH inductance in an 1812 package.

- To start with your schematic press **P** for place and **P** again for Part. Chose the components according to your prior made design decisions and placed the C and L onto the schematic sheet.

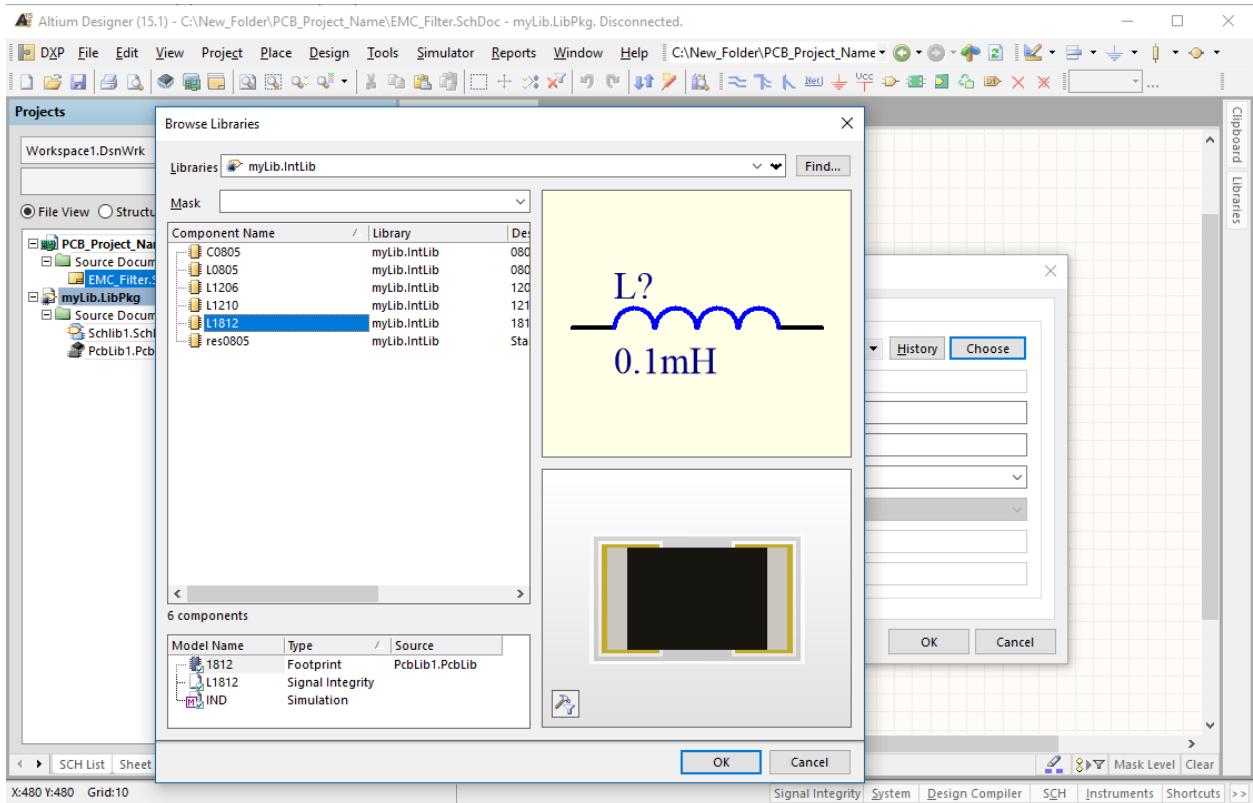


Figure 50: Altium place a component, an inductor 1812 package, chosen from myLib library.

30. Your schematic sheet should look similar to Figure 51. At this point we introduce a new dialog the SCH Inspector which comes into really handy by changing a lot or a group of components as well as the SCH Filter which is not discussed further because we will discuss the PCB filter which provides similar functionalities later on.

Select all placed components at the same time with a **drag of the left mouse**. Open the SCH Inspector view, if not opened yet. The SCH Inspector view shows you all the properties and similar properties and parameters of the selected components. Make a single left click on the parameter Footprint which is highlighted. This opens the parameter menu for the specific parameter that is commonly shared by all of this components.

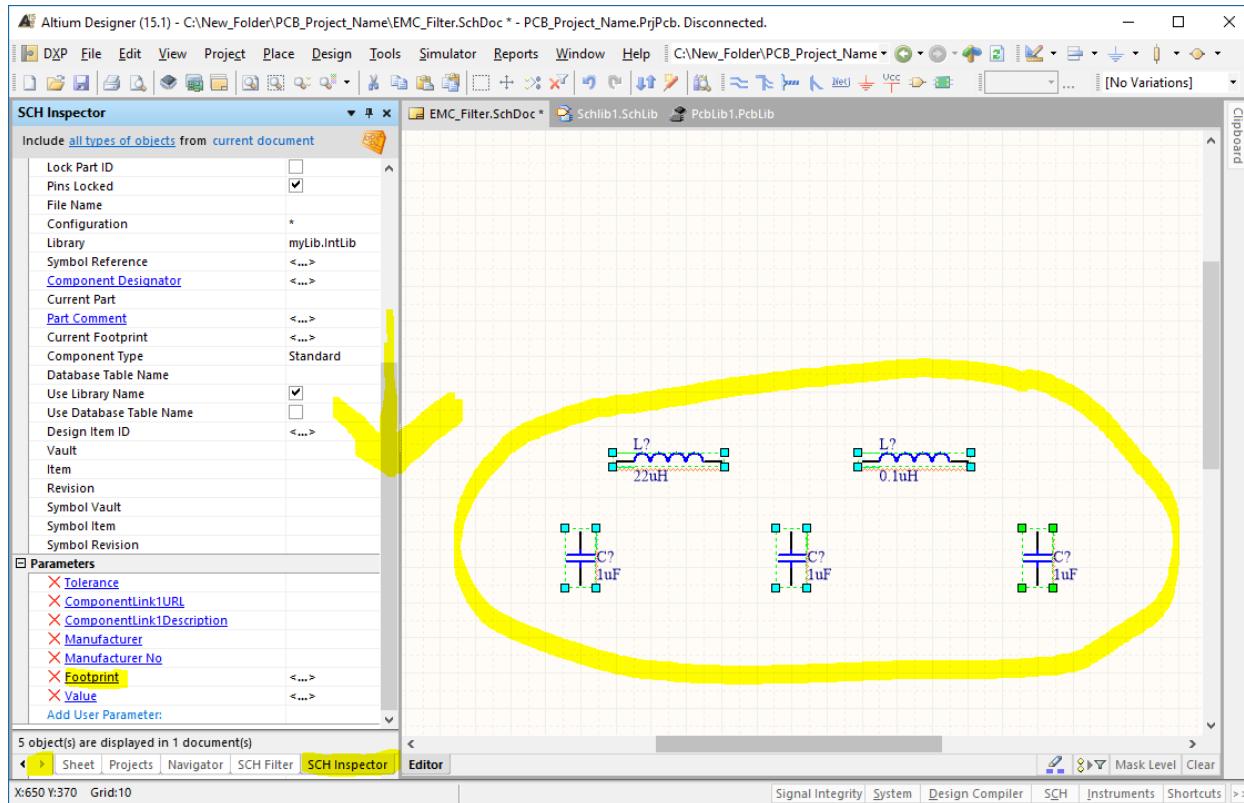


Figure 51: Altium Schematic placed C and L components.

31. Change the Hide property from True to False, which shows the footprint of each component in the schematic as shown in Figure 52.

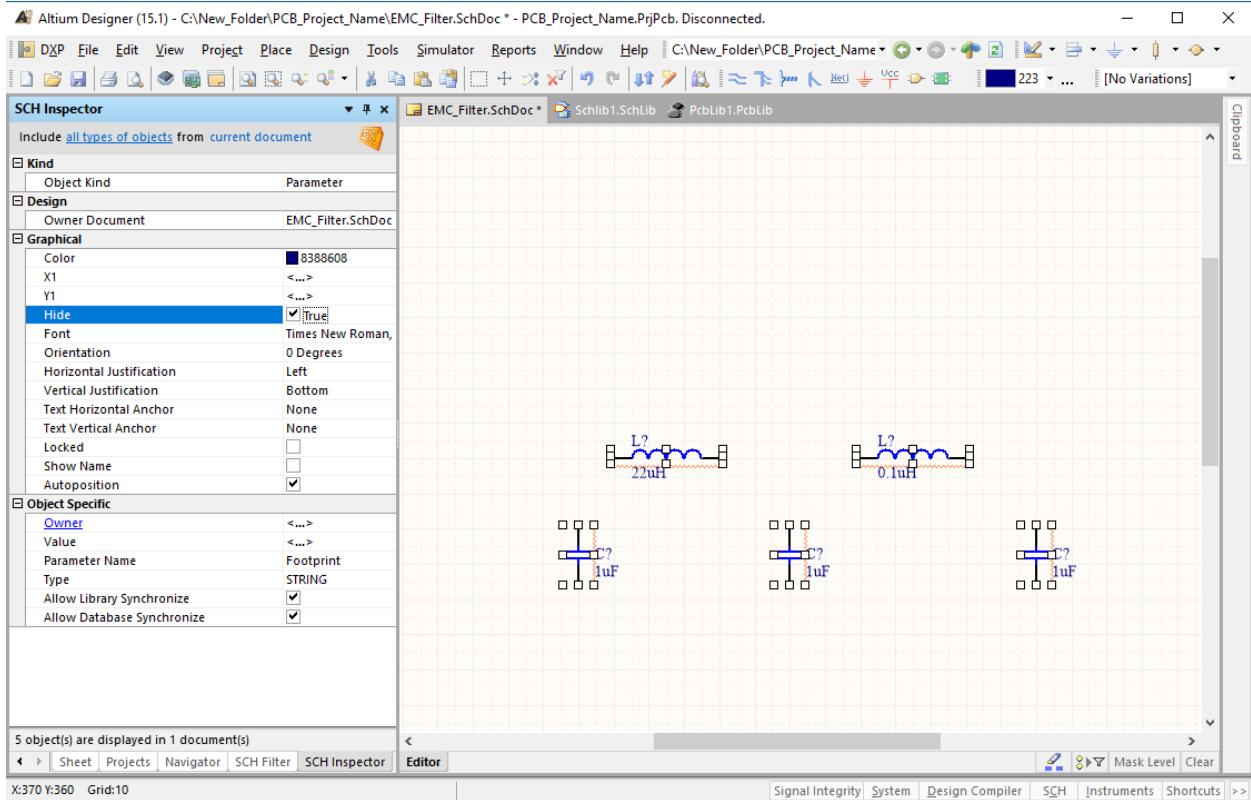


Figure 52: Altium SCH Inspector parameter Footprint.

32. Next chose connectors, to save you time and work, the SMA Connector parts are provided as an Integrated Library and can be downloaded from the following GitHub repository https://github.com/haringd/SMA_Con_Altium_IntegratedLibrary. Figure 53 shows the schematic with the added SMA connectors left and right side.

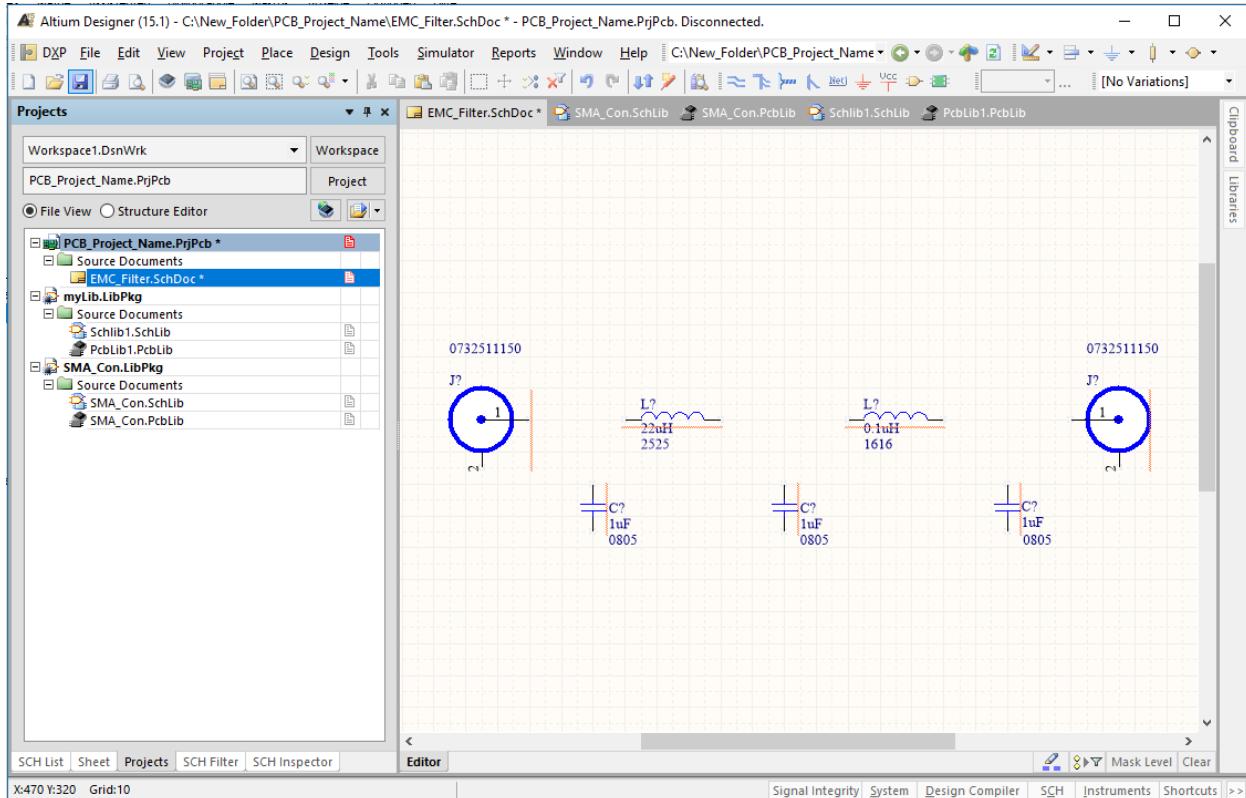


Figure 53: Altium Schematic SMA parts added.

33. Next step is to wire the schematic so press **P** for place and **W** for wire. Draw the wires between the components as shown in Figure 54. To make the Power Port 'GND' use the highlighted symbol on top of the screen as shown in Figure ???. By pressing **TAB** you open the the Power Port dialog that allows you changes to the style of the port and the Net Name.

IMPORTANT: Altium does connect nets with names which are case sensitive. Nets can be globally connected or locally connected. Locally connected means that there are on the same hierarchy level only connected, and do not change the hierarchy level. Globally connected means that the nets are connected trough out hierarchy levels. A power port is always globally connected! This tutorial will not discuss hierarchy level layout schematic design which is often used in a multi-sheet project, for further reference see this link [https://www.altium.com/documentation/18.0/display/ADES/\(\(Multi-Sheet+and+Multi-Channel+Design\)\)_AD](https://www.altium.com/documentation/18.0/display/ADES/((Multi-Sheet+and+Multi-Channel+Design))_AD)

+Design))_AD.

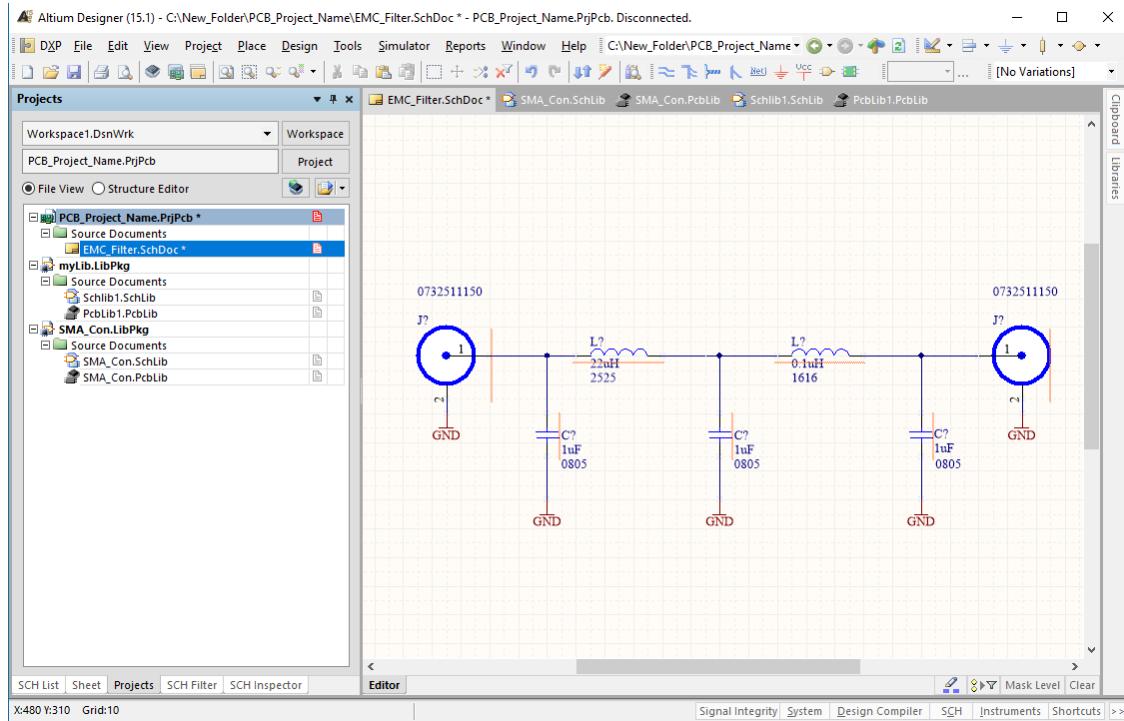


Figure 54: Altium Schematic wire.

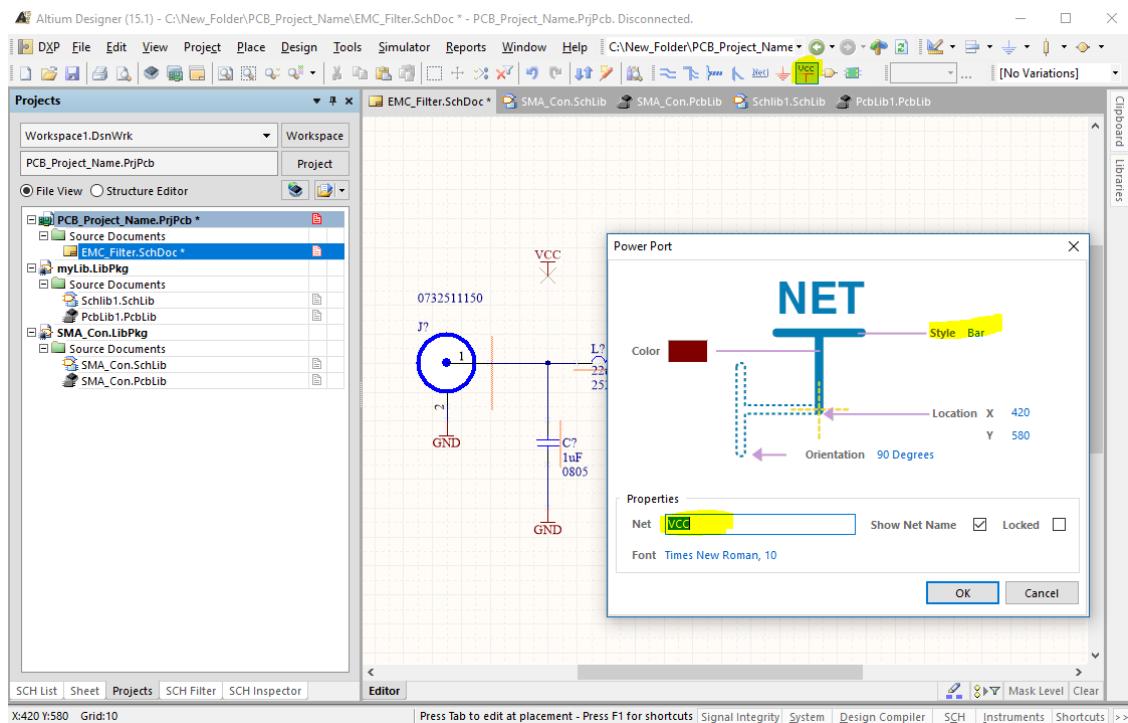


Figure 55: Altium Schematic power bar.

34. Figure 54 shows that each component has a red curly line which means there is an error that has not been resolved yet. In this case the error is that all the components on the sheet have the same reference designators. Use the Annotation Tool as followed **Tools** → **Annotate Schematic** the Annotate dialog opens as shown in Figure 57.

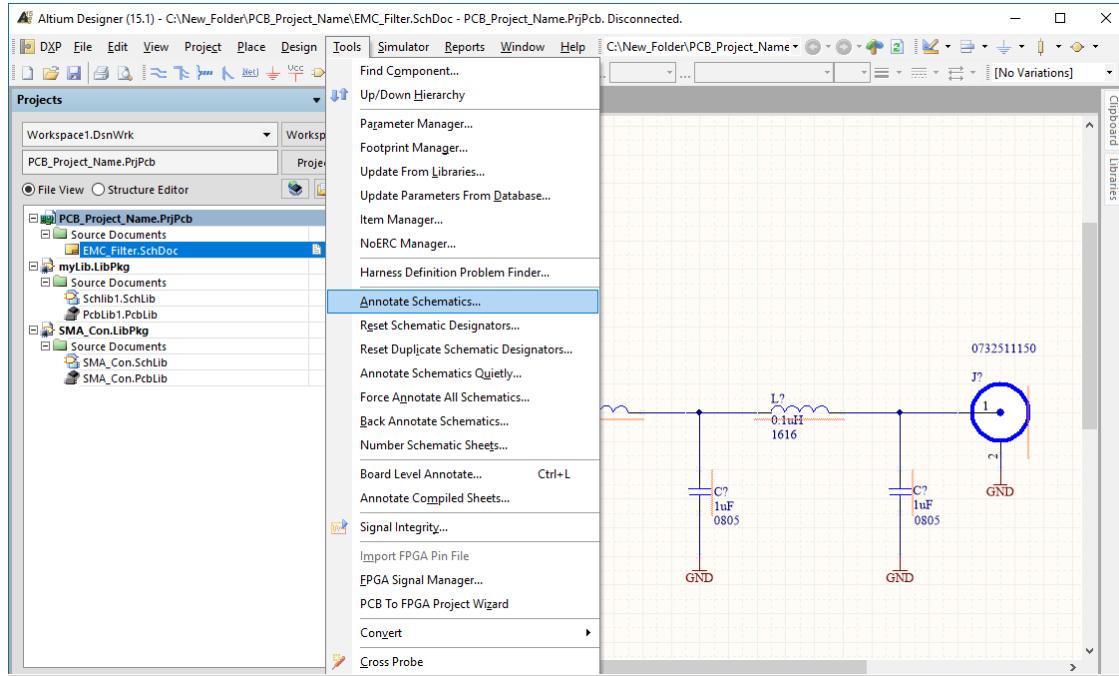


Figure 56: Altium Schematic Annotation Tool.

35. The Annotate dialog is shown in Figure 57. First, click button **Update Change List** which updates the Current Designator to the Proposed Designator. This does not make any changes yet in the schematic as you would see if you close the dialog. To execute the changes into the schematic document press **Accept Changes: (Create ECO)** which opens an Engineering Change Order dialog.

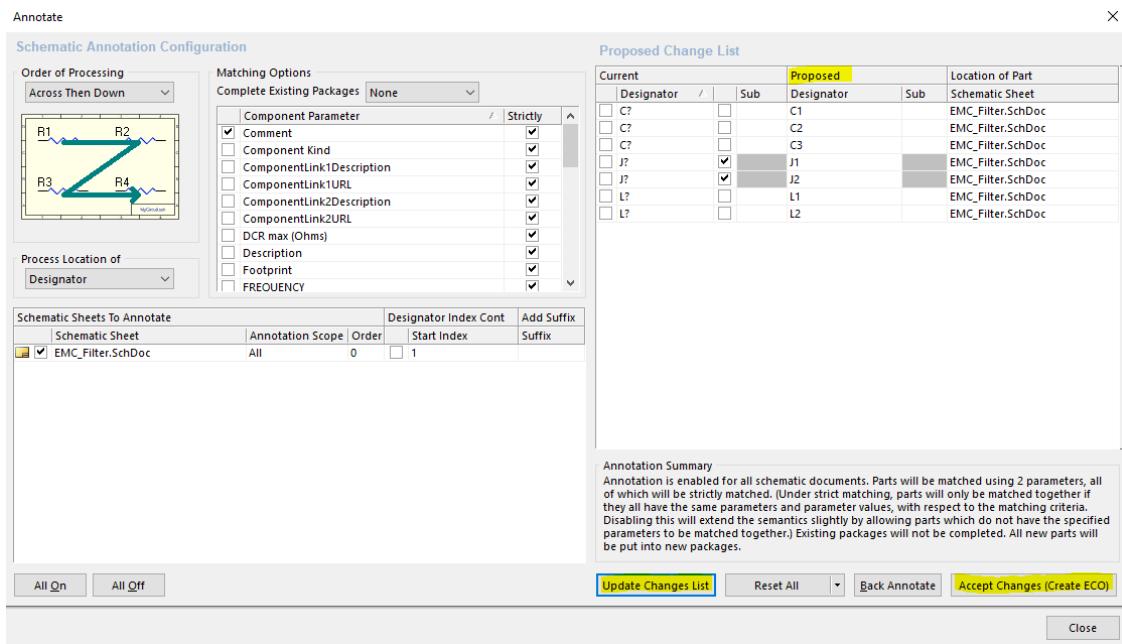


Figure 57: Altium Schematic Annotate Dialog.

36. The Engineering Change dialog is shown in Figure 58 which gives the engineer a list of the modifications that were made and allows to select them independently if not wanted. First, press **Validate Changes**. This is like a dry run and evaluates errors that may occur without making a real change in your documents, Figure 59 shows the dialog after validation, notice the change of status. Now that the validation show no sign of trouble press **Execute Changes**, which is shown in Figure 60. The Engineering Change dialog is a general concept of Altium and you will see it many times later on. This dialog will not be explained further on in the tutorial.

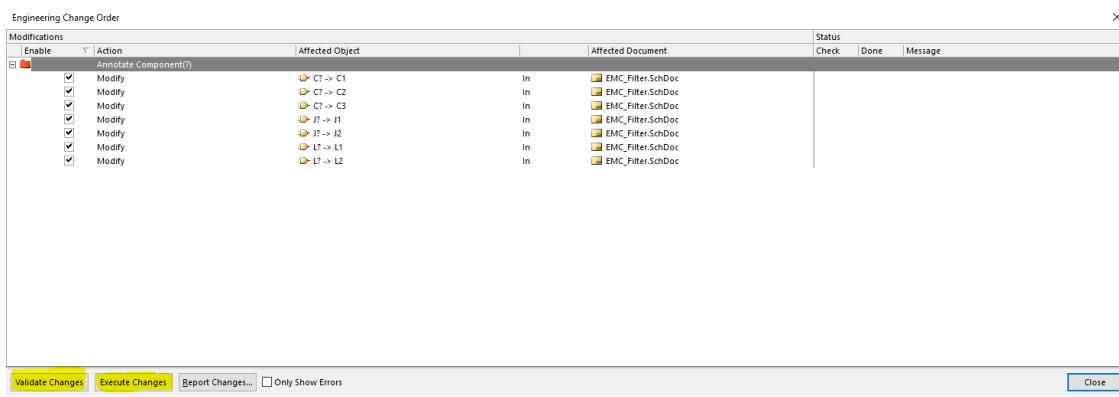


Figure 58: Altium Annotate Tool Engineering Change Order.

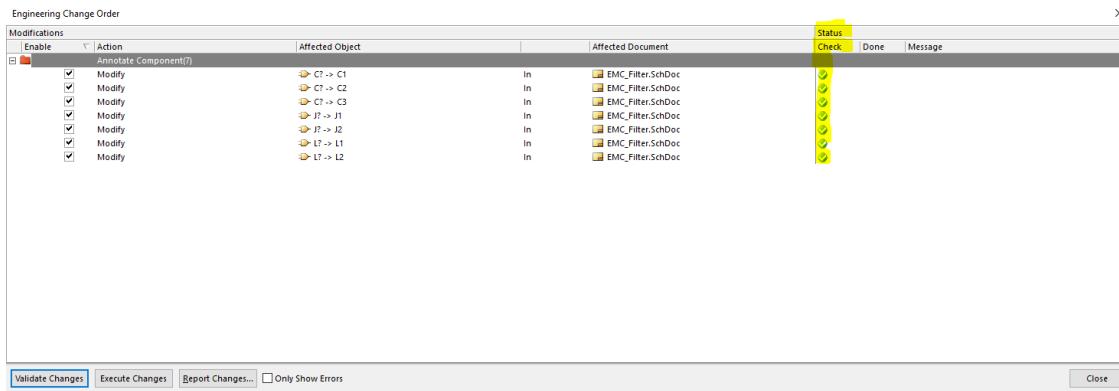


Figure 59: Altium Annotate Tool Engineering Change Order validated.

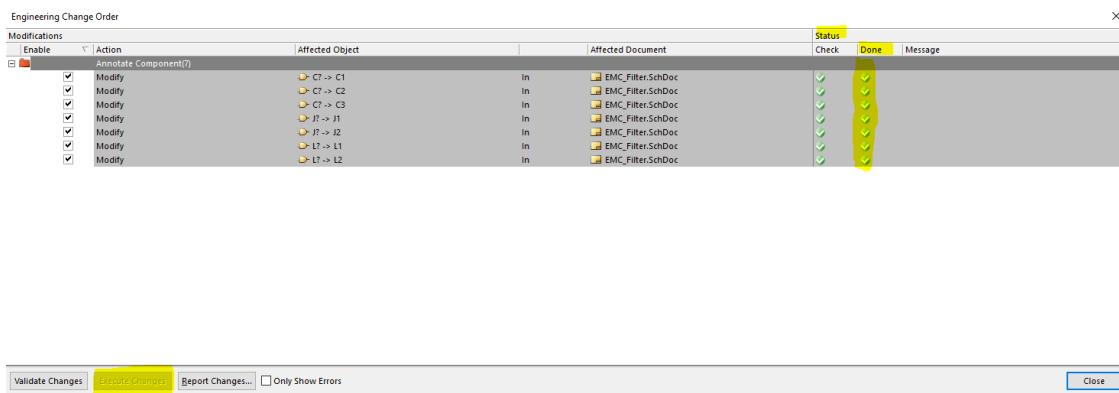


Figure 60: Altium Annotate Tool Engineering Change Order executed.

37. Your screen should now look similar to Figure 61, notice that the schematic is fully annotated and that the red curly lines that indicated errors are disappeared.

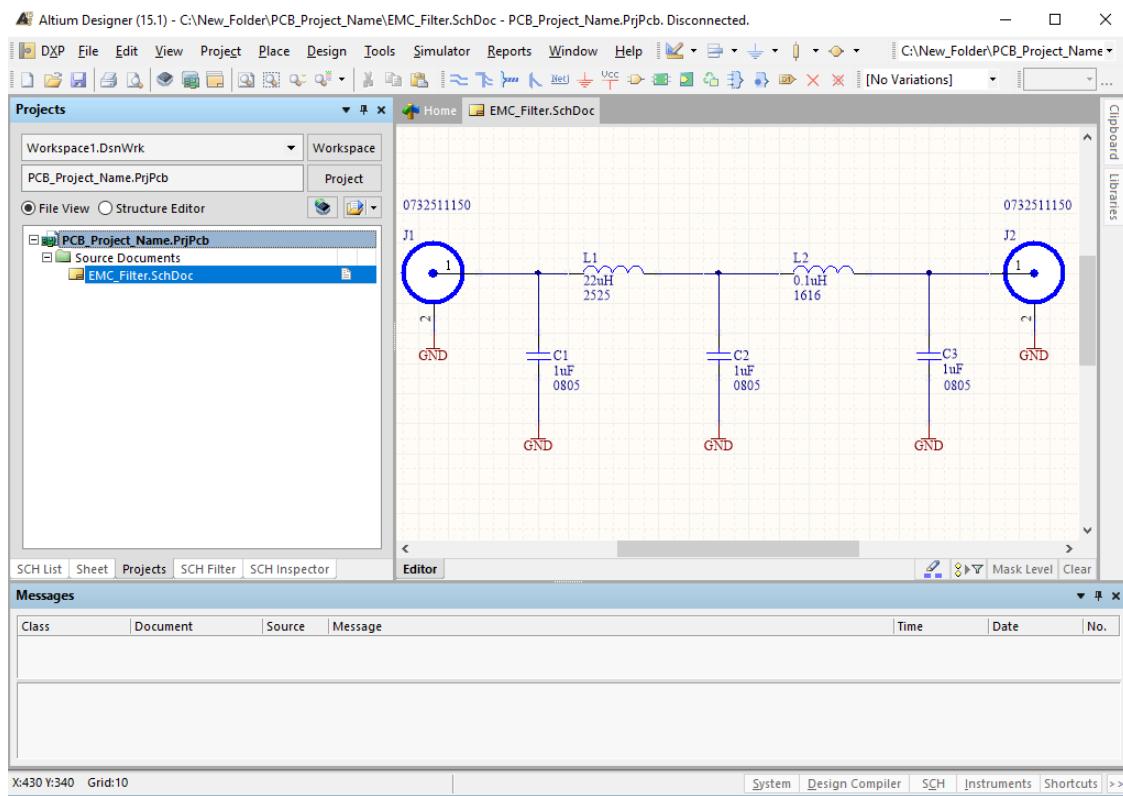


Figure 61: Altium Schematic annotated.

3.2.1 Directives

38. A wire is most of the time just a wire, but sometimes it serves a special purpose as example a RF transmission line or differential bus lines as commonly used for USB. Therefor, directives are used to define additional information for those wires most commonly used in form of a **Net Class**. Figure 62 shows how to select a **directive**. The most general is net class so chose **Net Class** and then press **TAB** to open the Parameters Dialog shown in Figure 63. The Parameters dialog shows under Properties Name the name which you see in the schematic. The **ClassName** under column Name is a **Altium specific identifier or key word** that has to be precious like that! under the column Value is the actual class name in this case **TML_cn** which stands for transmission line class name. The class name can be used to create rules for the assigned wires as example a 50Ohm impedance micro strip trace that needs a controlled width and distance to the objects in the PCB document. Class names are a general concept in Altium. Figure 64 shows the placed directives for the transmission line.

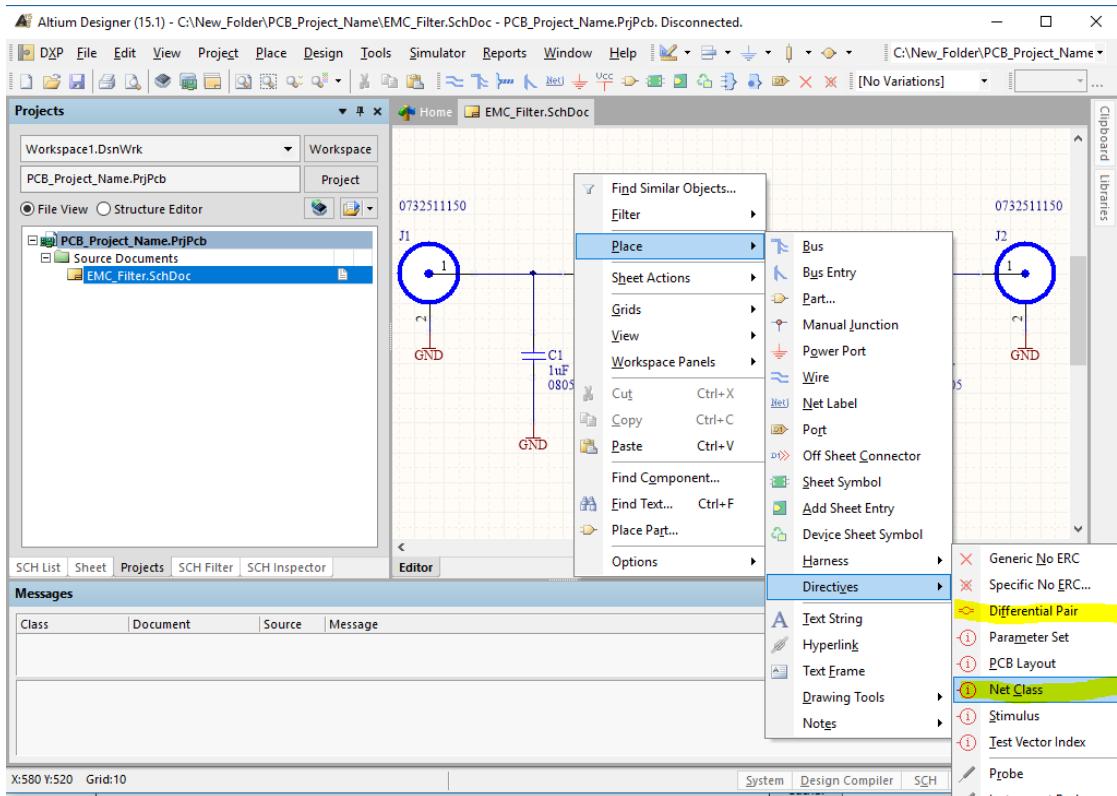


Figure 62: Altium Schematic Directives.

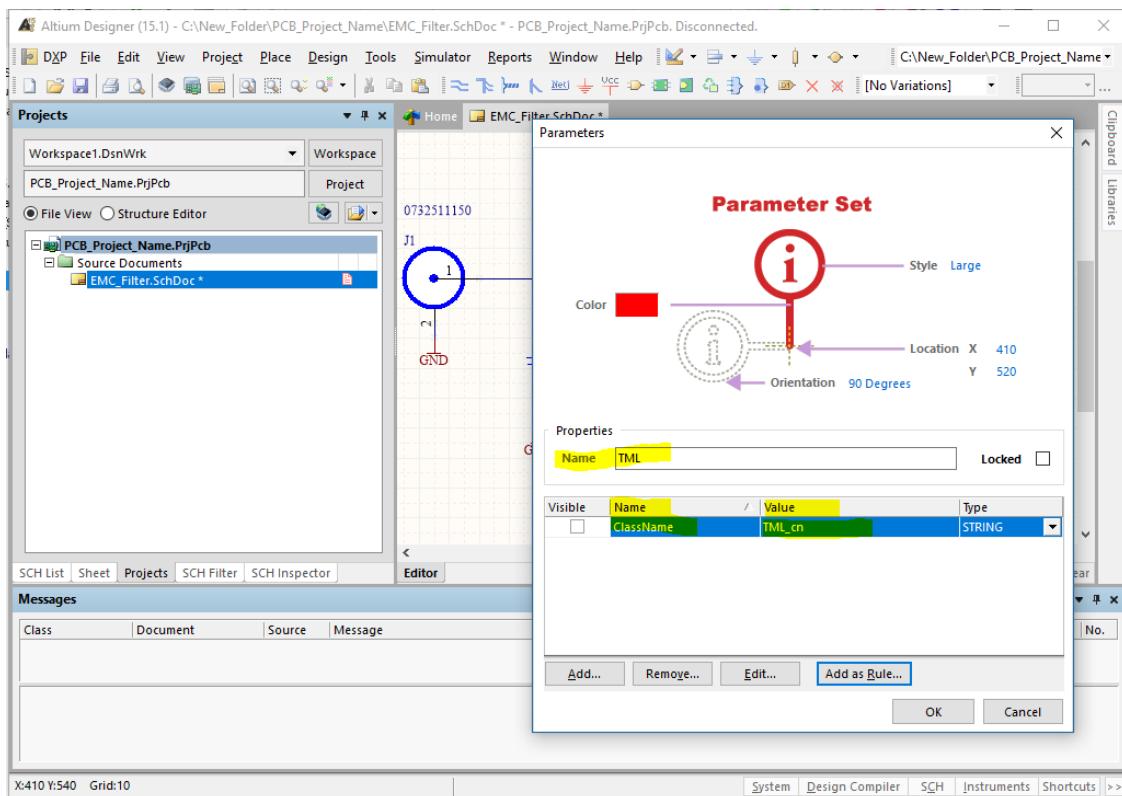


Figure 63: Altium Directives Net Class parameter dialog.

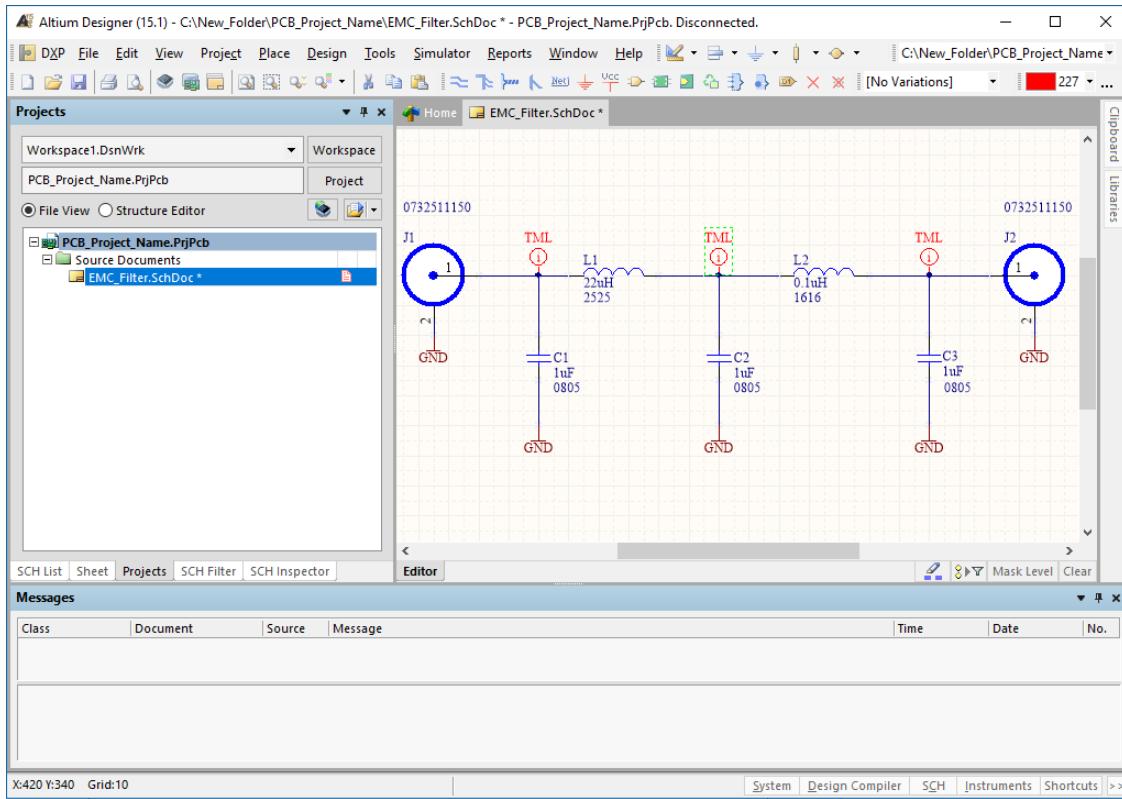


Figure 64: Altium Directives Net Class TML.

39. Altium has a build in compiler that checks for rules violations as wire shorts or wires they would act as an antenna because they are not connected to, as examples. Press **CTRL+S** to save your schematic document. Press right click on the schematic sheet document chose **Compile Document** [**your Document name**] to compile the document. The compiler out put is shown in the Message view as shown in Figure 66. With a successful compile process the schematic is finished proceed with the PCB Layout sub section 3.3

NOTICE: If the message view is not shown and the compiler message is successful the Message view will not pop up. If there is a compiler error the Message view will pop up and inform you about the error.

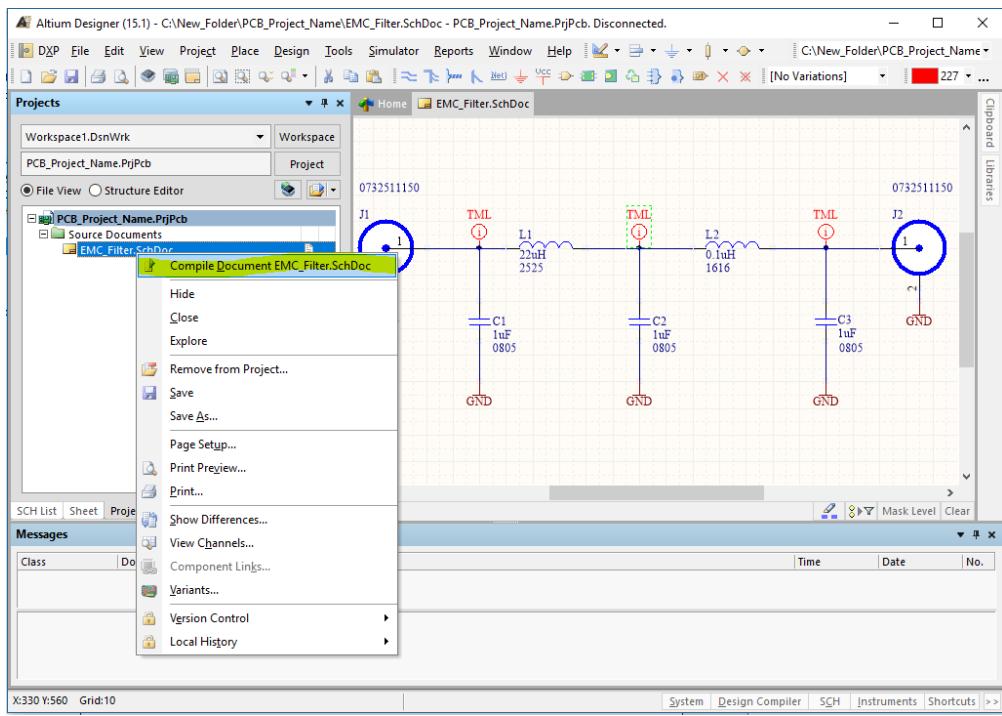


Figure 65: Altium Compile schematic document.

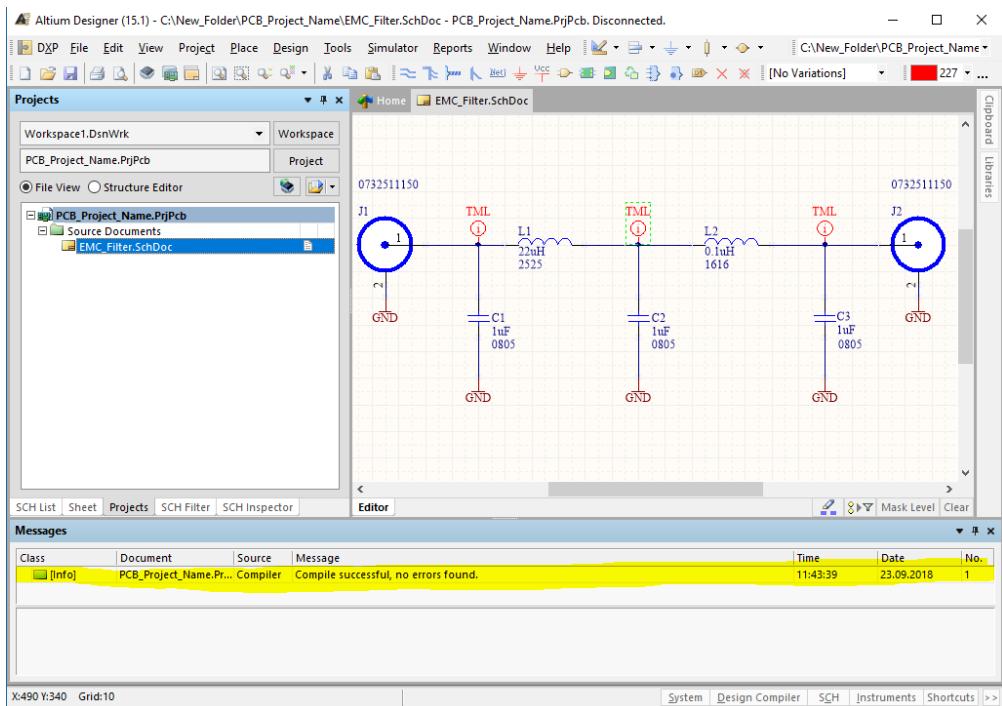


Figure 66: Altium Compile schematic document Message output.

3.3 PCB Layout

40. First, add a new document to your project of type PCB by right click on project and select **Add New to Project...** than **PCB**, as shown in Figure 67.

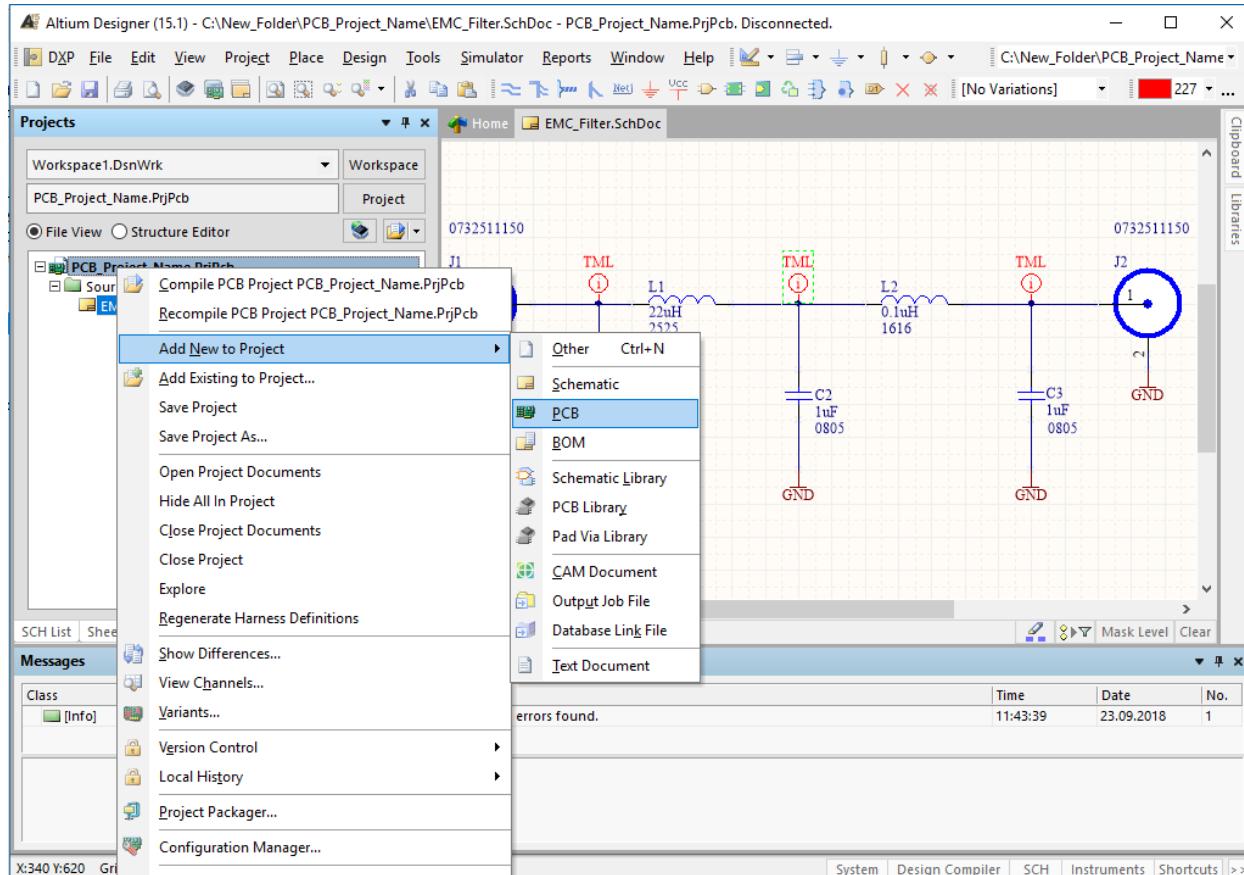


Figure 67: Altium PCB add new PCB document.

41. Next, save the document with an appropriate name by pressing CTRL+S as suggestion because you design an EMC filter chose EMC Filter and your screen should look as shown in Figure 68. Notice the yellow highlighted features, as the heads up display with short cuts shown on the top left of the PCB document. On the bottom left there is the Project view which aids to open and close documents. Right next to it is PCB Filter View as well as PCB Inspector which works the same as the SCH Inspector discussed in previous section. Below of those are the X and Y courser position measured from the reference point. Left to that one of the more important ones the grid selection which is recommended to set to **10 mils** as minimum which helps to avoid unnecessary rule violations. Right to that is a field highlighted **LS** which stands for **Layer Set** by clicking on it the View Configuration opens as introduced previously in the PCB library document.

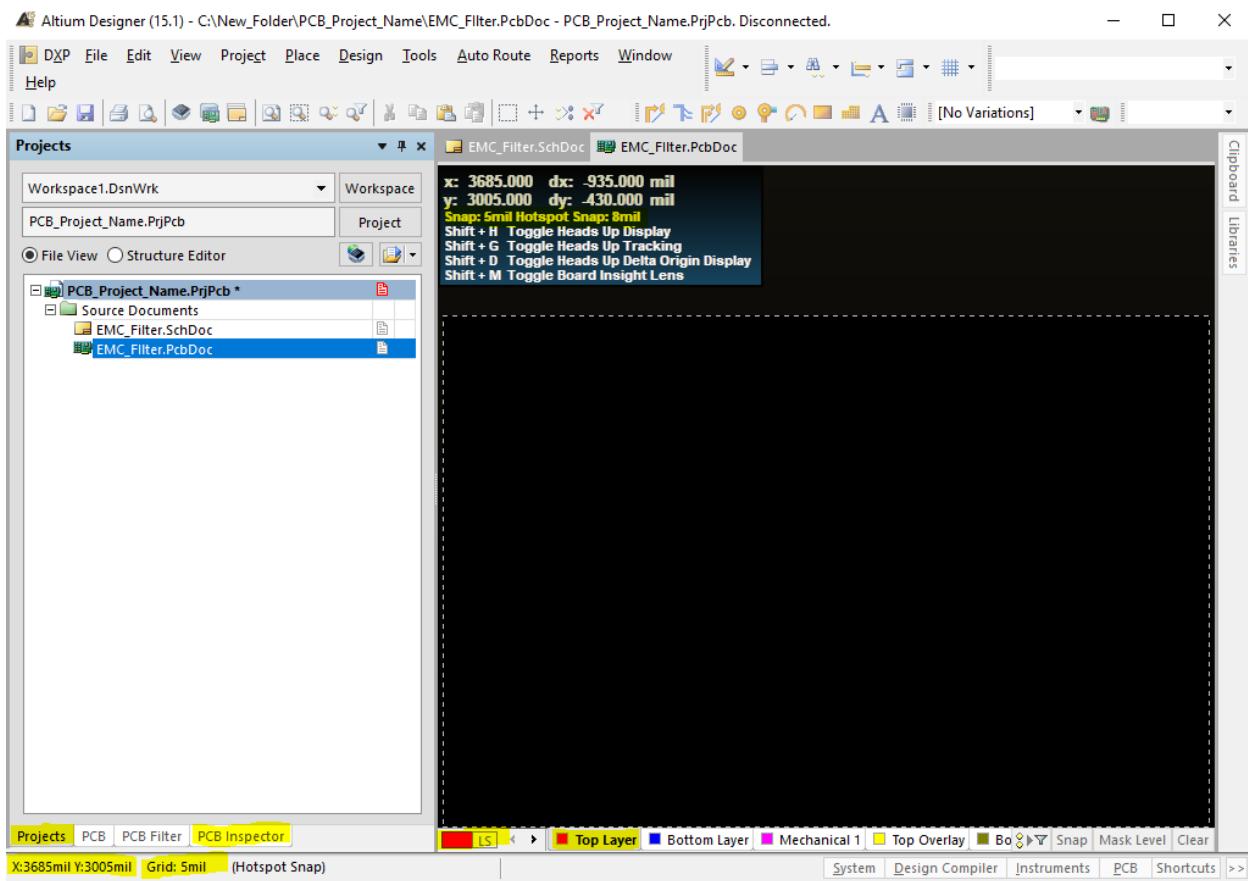


Figure 68: Altium PCB empty PCB document.

42. First, and **very important**, zoom out and set the reference point on the lower left edge of the PCB board. To do so change the grid by press **G** and choose **100 mils**. Then in menu bar chose **Edit → Origin → Set**, as shown in Figure 69. Place the Origin of measurement to the lower left corner of the PCB board outline. as shown in Figure 70.

IMPORTANT: The origin is used as the point of reference for all measurements of the design in x and y axis!

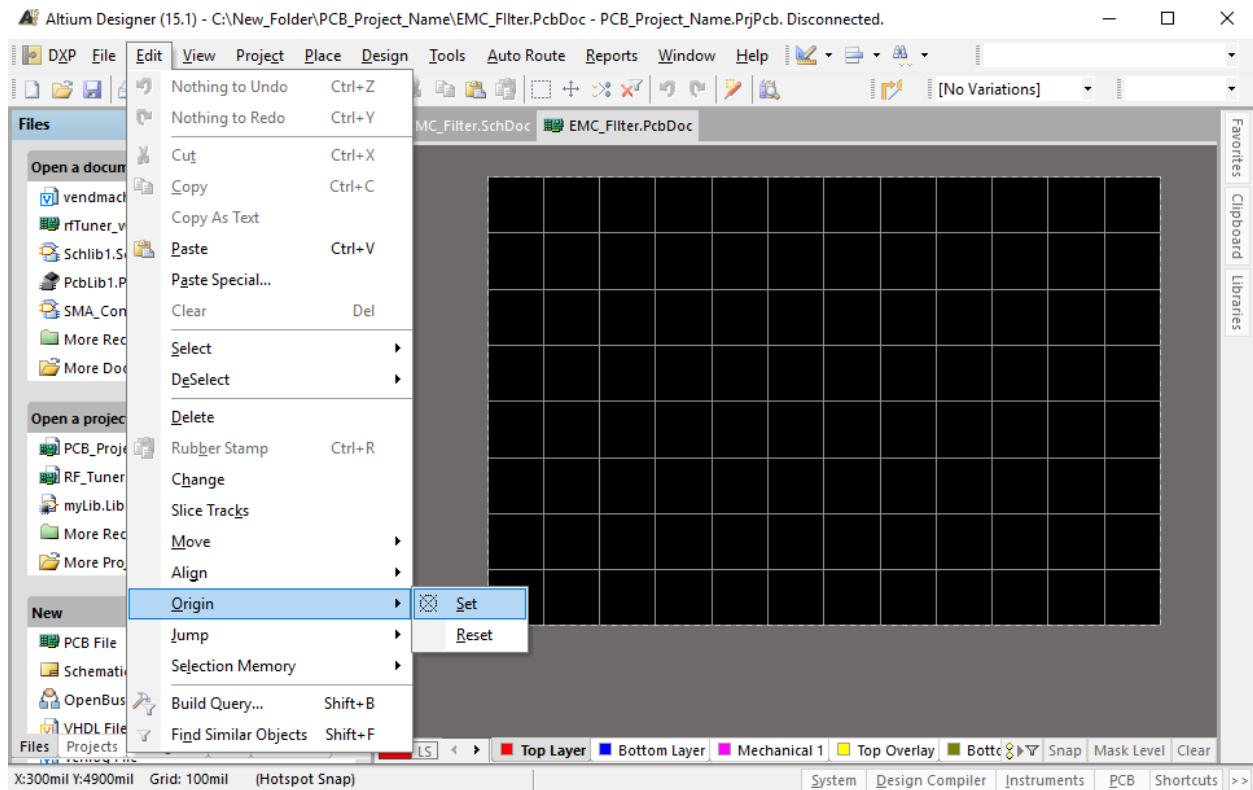


Figure 69: Altium PCB set Origin.

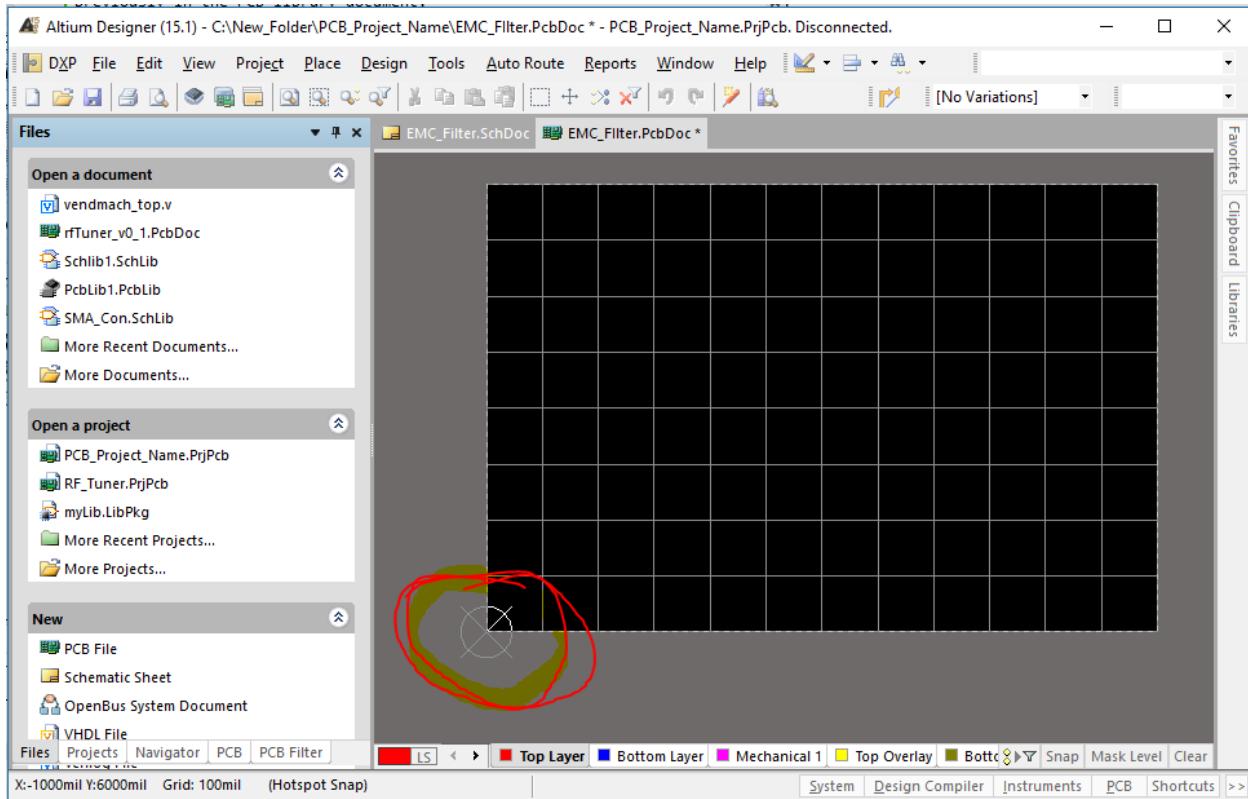


Figure 70: Altium PCB Origin set to bottom left corner.

43. Defined the size of the PCB. Therefore, it is good to know what the biggest PCB size is to the lowest price. Use the web calculator of PCBway.com to determine the biggest possible board size for a 2-layer board that has a cost of \$ 5.

Board size: _____

Delivery cost to US: _____

Silkscreen color highest cost: _____

Cost of a stencil: _____

Location of Production: _____

3.3.1 PCB Board Outline

44. The board outline is commonly defined in **Mechanical layer 3**. Note, this is not a standard, this is a de facto standard that is widely used by making a list for your manufacturer you could redefine that as Mechanical layer 16 for your board outline. Change the layer set so that only Mechanical layer 3 is on and turn the other layers off. There for use the View Configurations dialog **L** to first turn All Layers Off on the bottom highlighted than un-check Only show enabled mechanical layer highlighted below Mechanical Layers column to show Mechanical layer 3. Check Enable **Mechanical 3 Enable and Show** check box as highlighted and press **Apply** and **Close**.

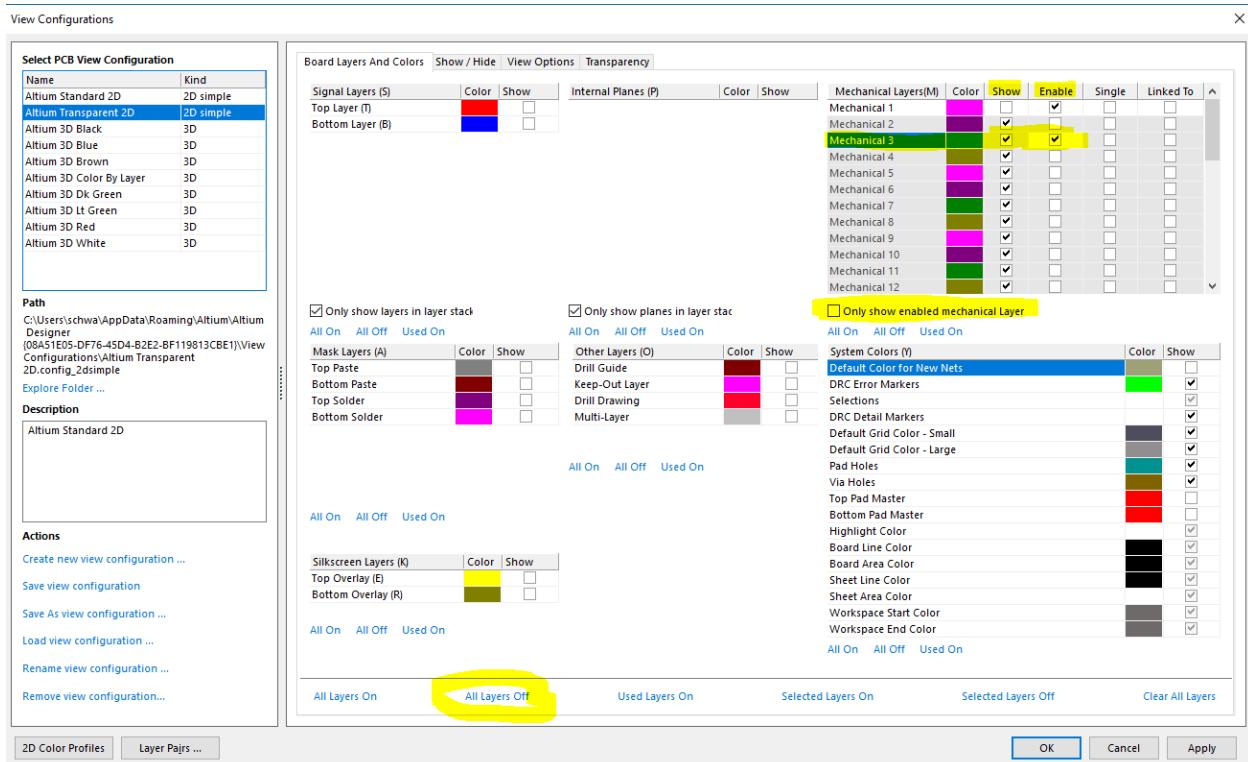


Figure 71: Altium PCB Layer Set Mechanical Layer 3 only.

45. The board outline is defined by a line, so press **P** for place and **L** for Line. Draw the desired board outline started by the point of origin. The board board size chosen is **3” x 2”** inches. use the Heads up display to see how many mills you draw the line which has a delta function that calculates the length of line in x and y direction for you. The board layout should look similar to Figure 72. To define the drawn lines as board shape select all lines than in menu bar chose **Design** → **Board Shape** → **Define from selected objects**. Your screen should look similar as Figure 74.

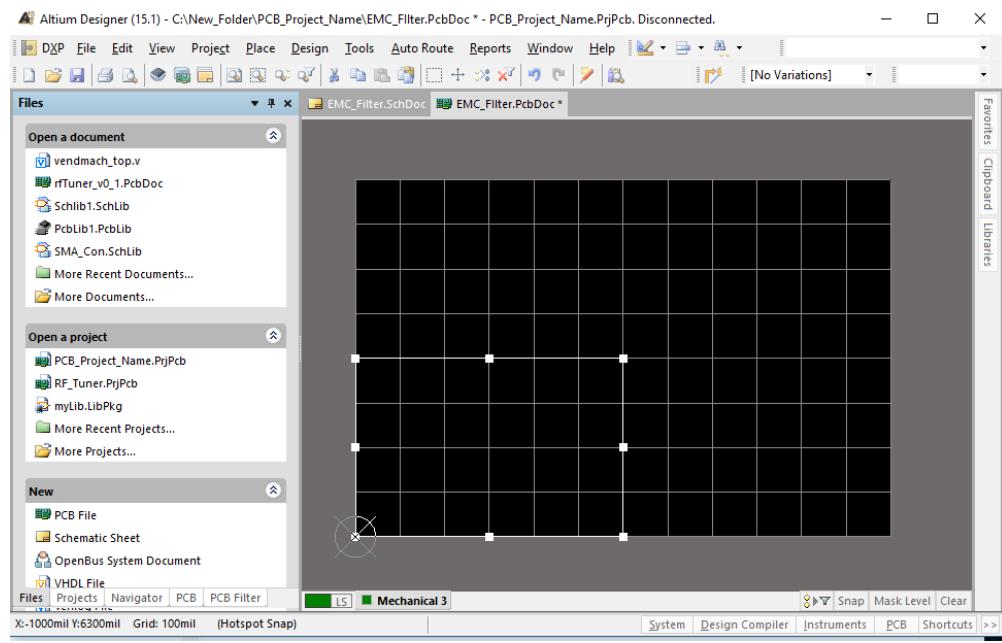


Figure 72: Altium PCB board outline selected.

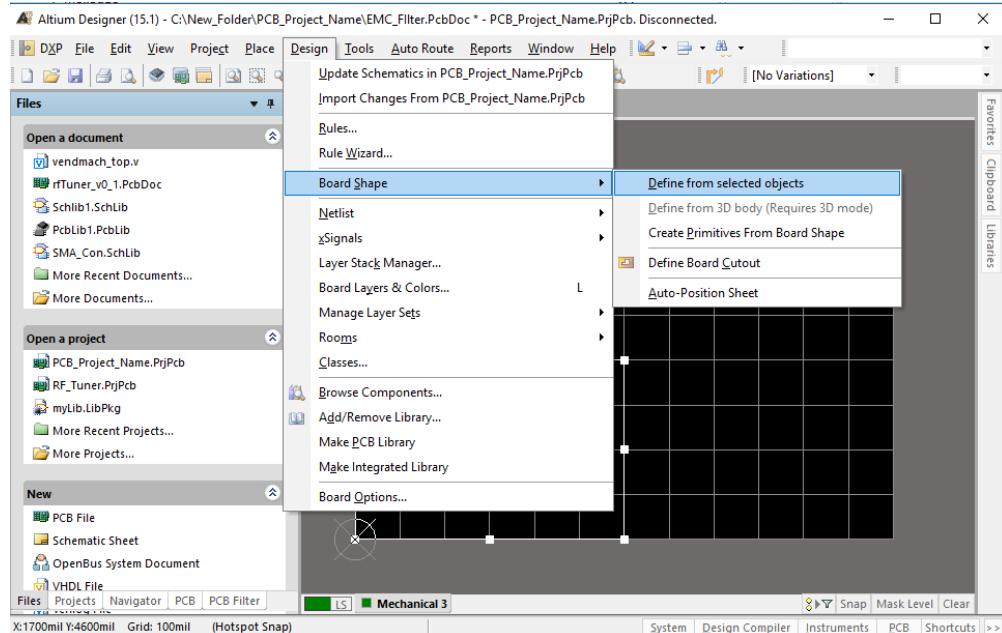


Figure 73: Altium PCB board outline Define form selected objects.

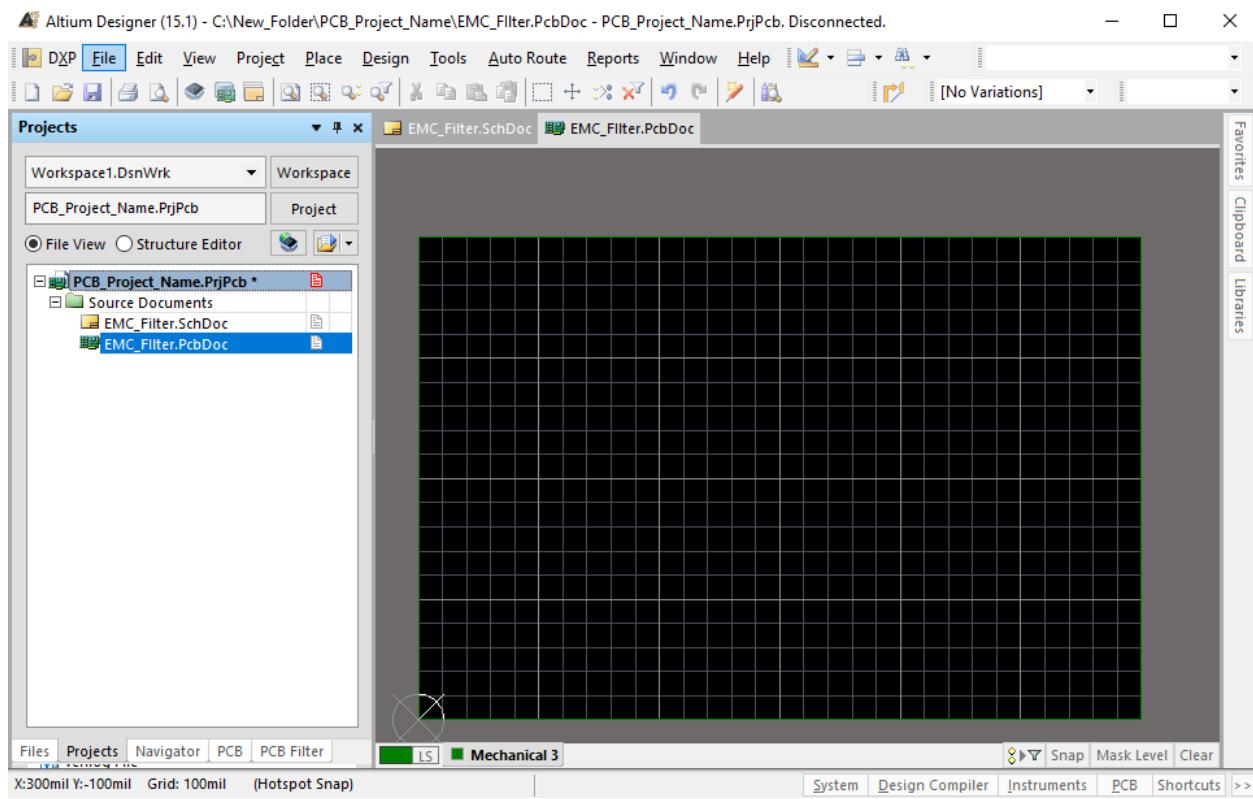


Figure 74: Altium PCB board defined board outline or board shape.

3.4 PCB Design Rules

46. After defining the board shape it might be a good idea to check on the PCB Design Rules and cross check those with the Design capabilities of your manufacturer which is PCBway.com because they are cheap, PCBway Design Capabilities Link. The most important rules to start with are the minimum clearance, the minimum track width, and the minimum hole size. The Altium Design rules can be changed by **menu bar chose Design → Rules...**, the opened dialog is shown in Figure 75. Highlighted are the most important rules to check on and to edit according to the manufacturer capabilities. In general, to start with a design chose big clearance and width, as minimum settings because its simpler to make it smaller at the end then to expand objects where no space is available.

If you do not know yet what each rule means do not worry to much and carry on. Rules can be changed at any time, and most of the rules start making sense while designing the PCB. Due the vast amount of rules a deeper discussion will be done as we use them or run into trouble and we have to use them.

IMPORTANT: The engineer has to follow those rules simply because that it what defines what is physically possible to manufacturer. Otherwise, you may end up with a great design that can not be manufactured. So, try **not to design smaller then 10 mils!**

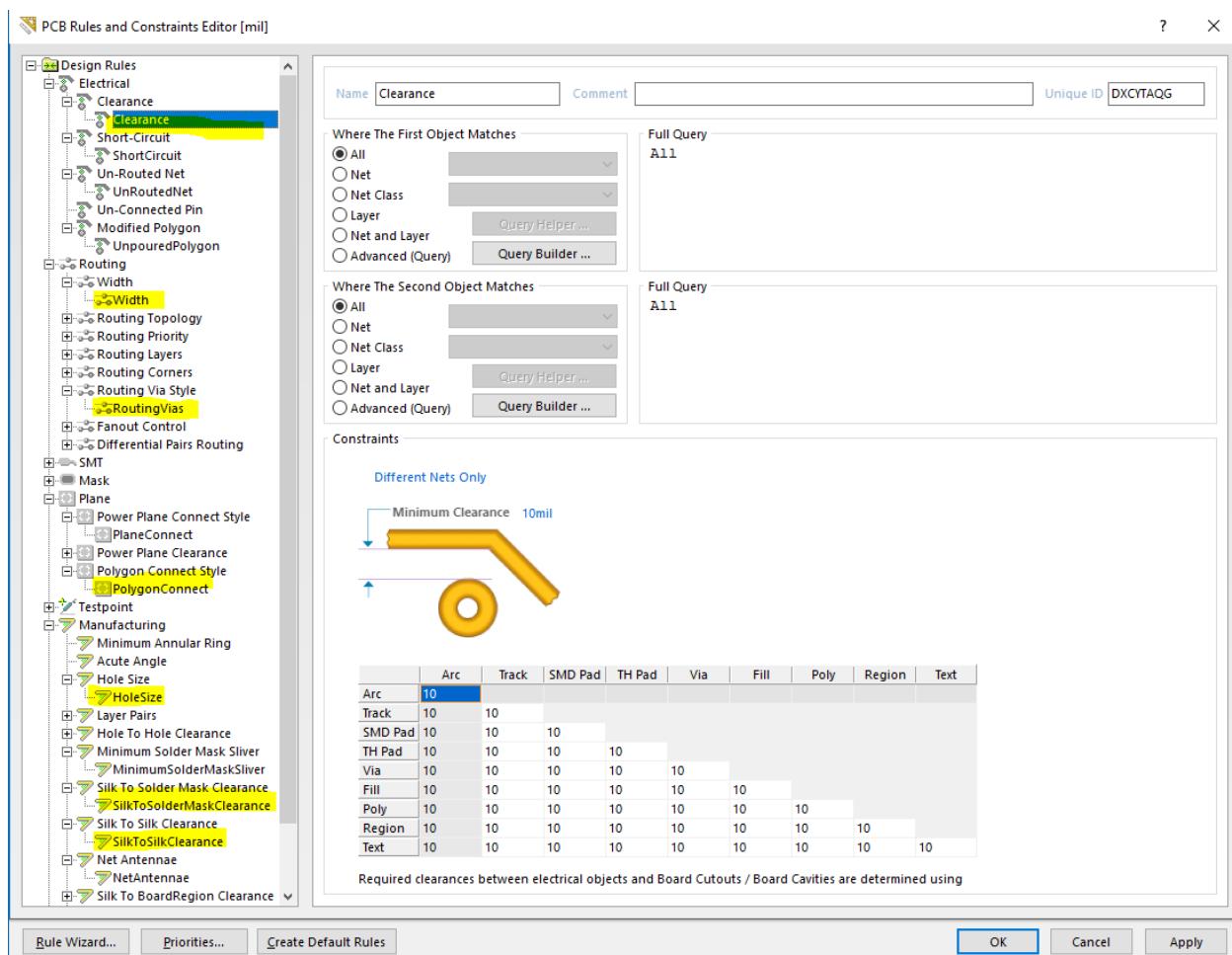


Figure 75: Altium PCB Rules and Constraints Editor dialog.

3.5 PCB Layer Stack Manager

47. A second feature that is important to know is the Layer Stack Manager that can be found under menu bar chose **Design → Layer Stack Manager...** that allows you to define your layer stack up. The layer stack up is defined by your manufacturer and needs to be requested or looked up on the Internet, for PCBway the layer stack up can be found under Multi Layer Laminated Structure. Due to the fact that tracks or traces can be routed over the bottom or top layer or on an layer in-between it is important to define the layer stack, especially if you have an RF trace. For an RF trace the impedance control is vital and can only be calculated if the height from a ground plane is known.

Which rises the question how are layer heights calculated? The most common manufacturer of Core and Prepreg material is a firm named Isola and it is there product Isola FR-406 ISOLA FR406 or commonly known as FR-4 with a dielectric constant of 4.6. Isola provides a slight set that nicely shows and explains the most important knowledge around the used PCB material which can be found here Understanding-Laminate-Prepreg-Manufacturing.pdf[[Isola](#)] and should be studied closely due to his importance. A further reference is <https://www.4pcb.com/pcb-stack-ups-0.062.html> and <https://www.4pcb.com/media/prepreg-thickness-chart.pdf> because the thickness of Prepreg depends on multiple factors. As you can see this topic is an lecture himself for now just use a standard 62 mill 2 layer board stack up with 1 oz copper. which results in an 59.2 mil core thickness as shown in Figure 77.

Dielectric Constant ϵ_r for Isola FR406 Prepreg 2116 Sheet @ 500 MHz: _____

Resin Content % for Isola FR406 Prepreg 2116 Sheet: _____

Glass Transition Temperature (Tg) for Isola FR406: _____

Cooper weight and thickness options for Isola FR406: _____

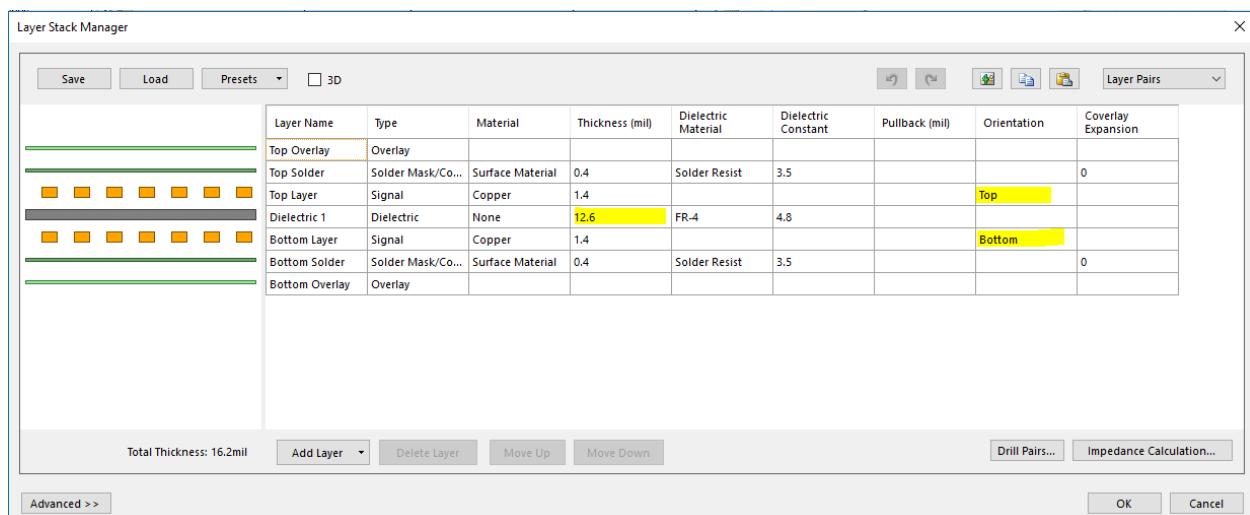


Figure 76: Altium PCB Layer Stack Manager dialog.

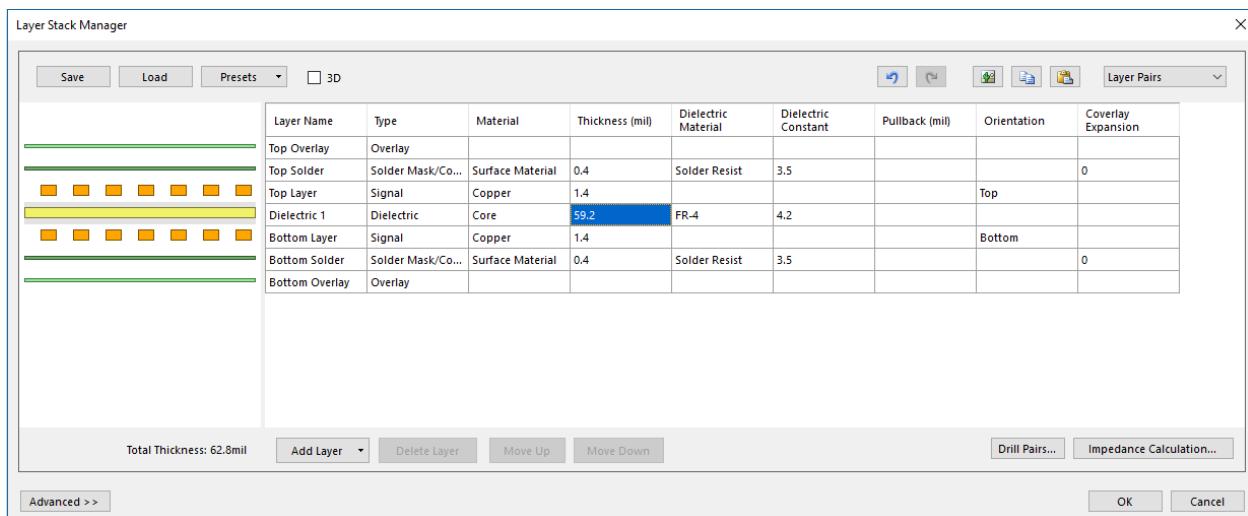


Figure 77: Altium PCB 2-Layer Stack up 1 oz copper 62 mil in height.

48. After, touching slightly rules and layer stacks lets import the schematic drawn previously in menu bar chose Design → Import Changes from [Project name] ..., as shown in Figure 78. The Engineering Change Order dialog appears as shown in Figure 79. First un-check the Room so it will not be added to the PCB document, a room is used only in PCB design document and is useful for bigger designs and repeated designs. Further more notice the added Component class and the added Net Class named TML_cn which was created with a class name directive in the schematic. Each component or net that has been drawn in in the schematic will be imported to do so press Validate Changes and then Executed Changes assuming no error occurs. Close the dialog and your screen should look as shown in Figure 80, notice that you do not see much because most layers are disabled to show them press L and turn All Layers On and hide the Mechanical 3 layer because it is not longer used except you want to change the board shape.

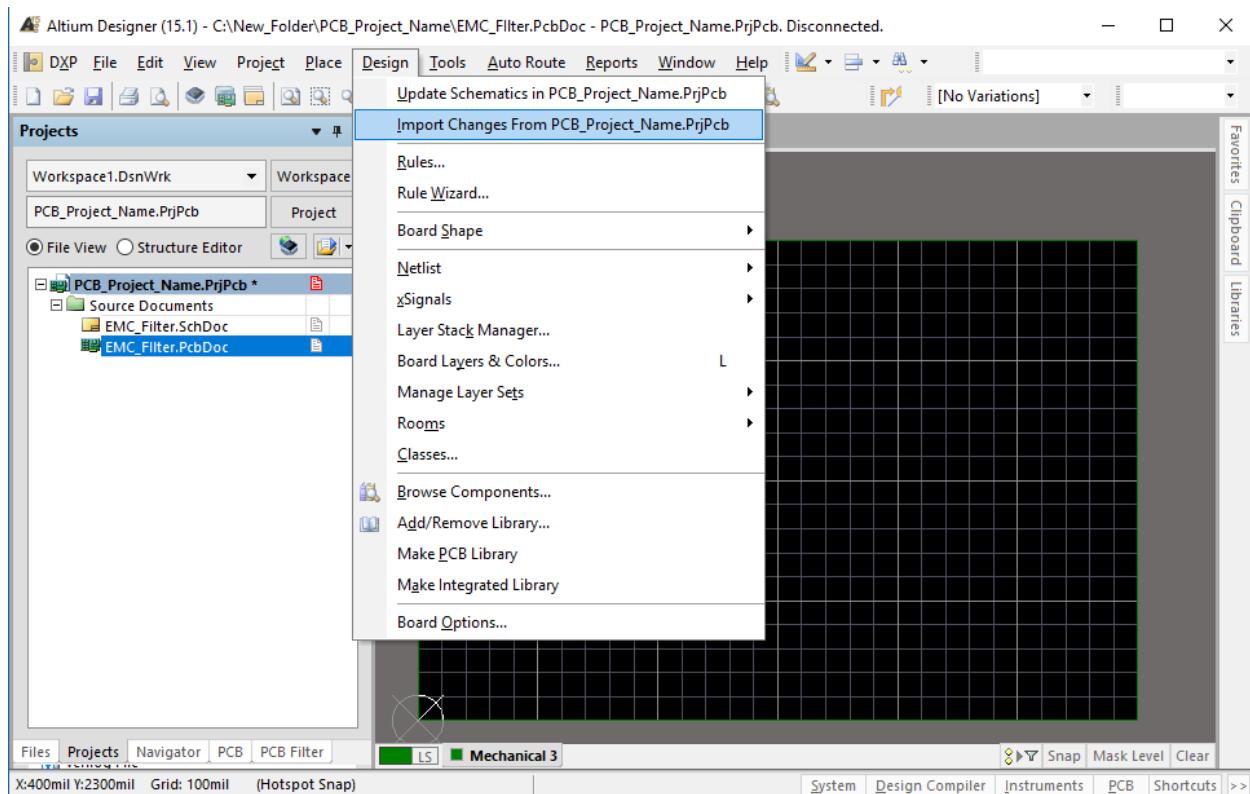


Figure 78: Altium PCB Import Changes From PCB Project.

Engineering Change Order				Status
Modifications	Action	Affected Object	Affected Document	Check Done Message
Enable	Add Components(7)	C1 C2 C3 J1 J2 L1 L2	To To To To To To To	EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc
Add Nets(4)	Add	GND NetC1_2 NetC2_2 NetC3_2	To To To To	EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc EMC_Filter.PcbDoc
Add Component Classes(1)	Add	EMC_Filter	To	EMC_Filter.PcbDoc
Add Net Classes(1)	Add	TM_U_cn	To	EMC_Filter.PcbDoc
Add Rooms(1)	Add	Room EMC_Filter (Scope=inComponentClass(EMC_Fi	To	EMC_Filter.PcbDoc

Validate Changes | Execute Changes | Report Changes... | Only Show Errors | Close

Figure 79: Altium PCB Import Changes From PCB Project Engineering Change Order.

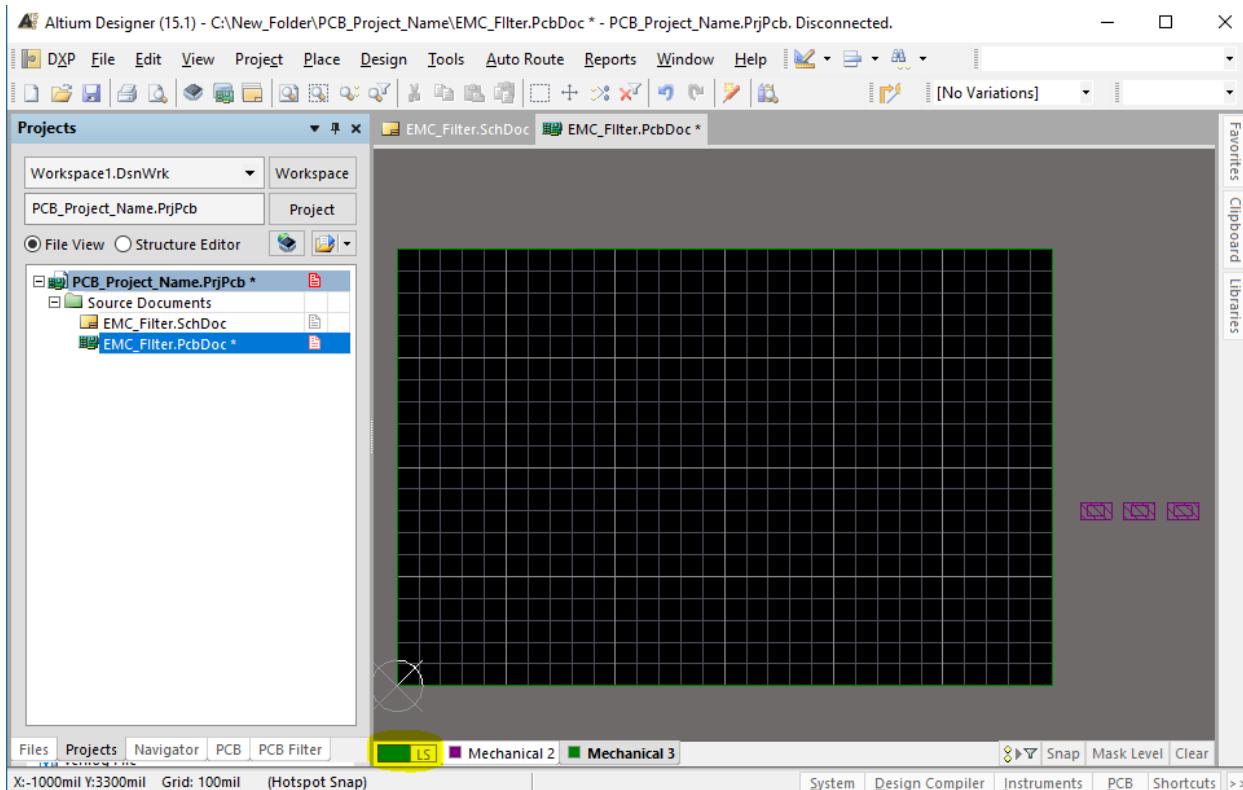


Figure 80: Altium PCB Imported wires and nets.

3.6 General Design Process (GDP)

49. After you enabled the layers you are ready to place the components, as shown in Figure 81 proceed with general design process.

General Design Process (GDP):

- (a) Place components according to design specs, try to avoid components on the bottom, tat safes one step in manufacturing 3.6.1.
- (b) After all components are in place rout the board by using tracks (press P than T), Regions (Preferred, press P than R), Pours (not that often used), and polygon pours (used for signals between tracks, press P than G, check option remove dead cooper)3.6.2.
- (c) Add additional information to Silkscreen layer like (In, Out, and 3V3 texts as example).
- (d) Add further information to Drill Drawing Layer as instructions for manufacture 4.2, Layer stack up and Drill Table).
- (e) Run Design Rule Check (DRC) by menu bar chose Tools... → Design Rule Check... 3.6.5.
- (f) Resolve all violations.
- (g) Create a Output Job and generate documentation, Gerber Files and NC Drill Files according to your manufacturers specifications 3.6.6.
- (h) Review by second engineer.
- (i) If OK send to production, after you got the quote and budget approval (time line for budget approval, if it is a university assume a month).

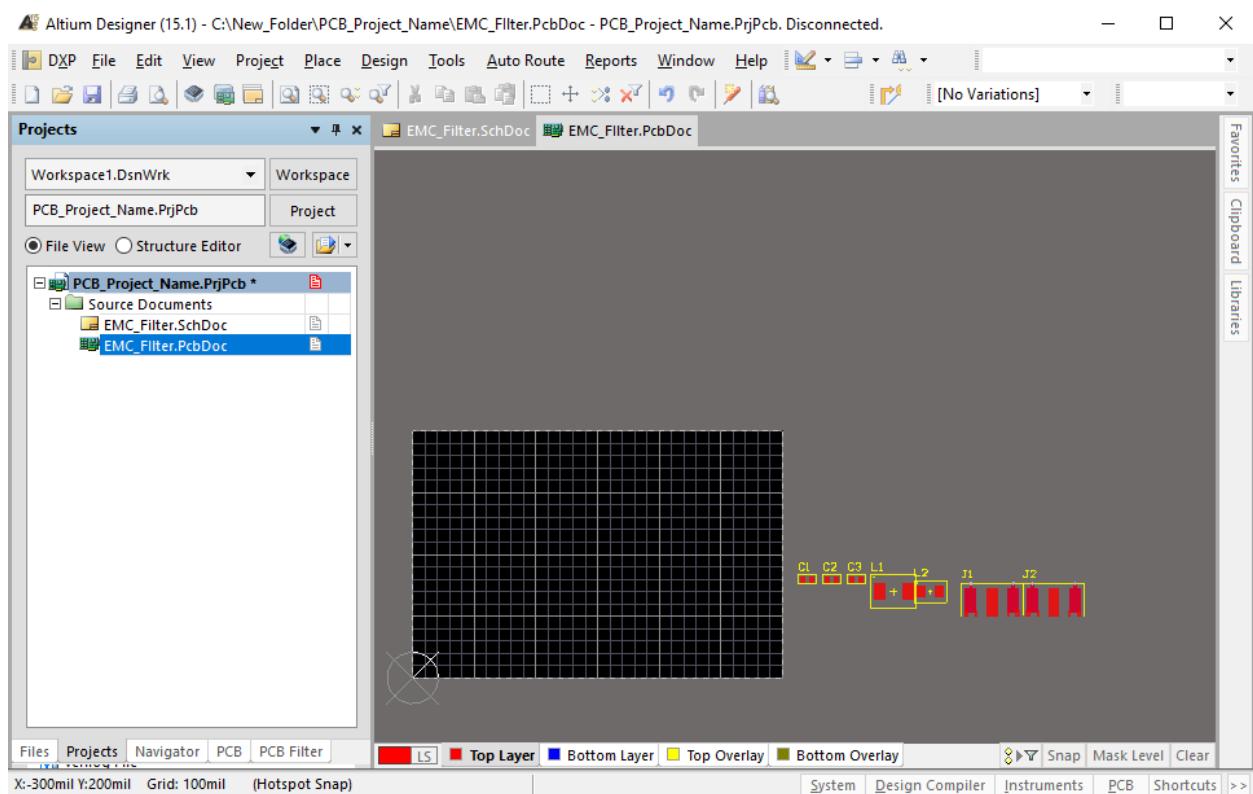


Figure 81: Altium PCB Imported wires and nets.

3.6.1 GDP Place Components

Figure 82 shows how the components have been placed or arranged by drag and drop them and using **Space** to rotate a component. Notice the alignment of the capacitors reference designators, reference designators are aligned the long side of the component if possible. As the zoom is increased on a component it the net name is displayed in the pad see Figure 83.

Furthermore, by holding **CTRL** and click on a net with a single mouse left click nets can be highlighted and de-highlighted by hold **CTRL** and click **not** on a net. It is highly encouraged to thick the routing trough before starting routing tracks and so on. For a larger design it is through normal that arranging of components alone can take up to 16h of work and more.

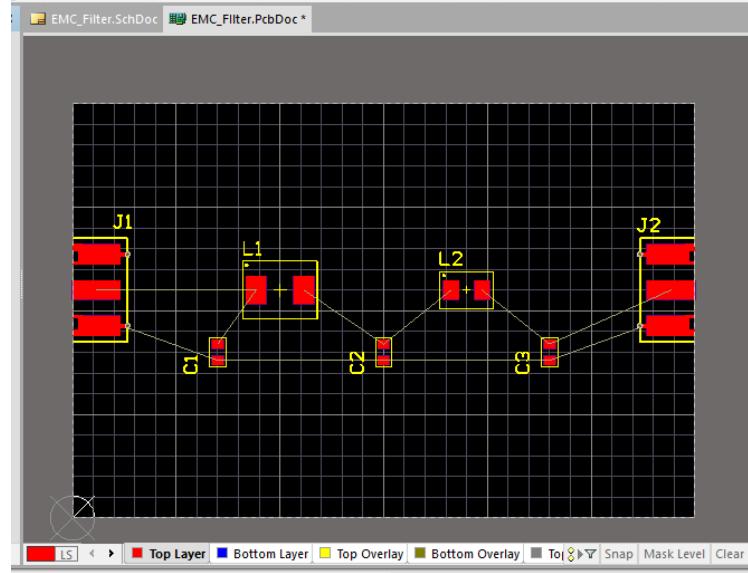


Figure 82: Altium PCB placed or arranged components.

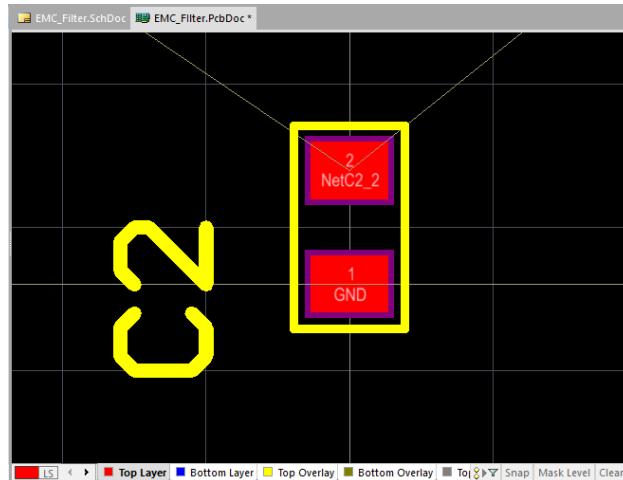


Figure 83: Altium PCB zoomed components which allows to read the net name.

3.6.2 GDP Routing

Routing is a bit like solving an integral equation less calculus more art, you do not know if there is a solution or not. The NetC2_2 is routed with solid regions which are just defined polygons of copper. As you can see the GND net is not routed yet. Therefore, a polygon pour is used that will cover the entire board and decrease the overall ground impedance.

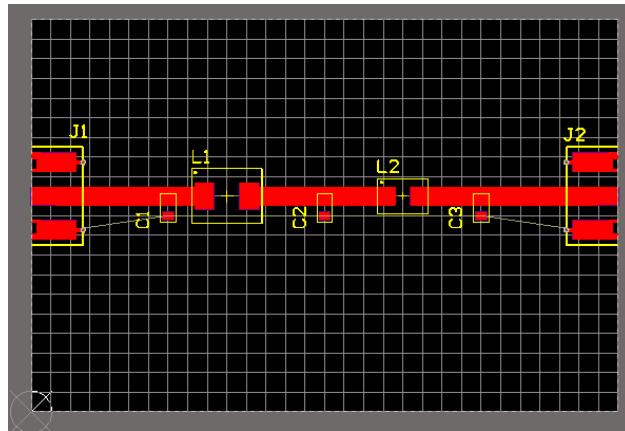


Figure 84: Altium PCB routed components with regions.

50. A Polygon Pour can be placed by pressing P than G which opens the Polygon Pour dialog as shown in Figure 85. There you can specify a Name the Layer applied to Connected to what Net in this case GND, select Pour Over All Same Net Objects, and check Remove Dead Copper which is really important! Place a polygon pour on the top layer and one on the bottom layer.

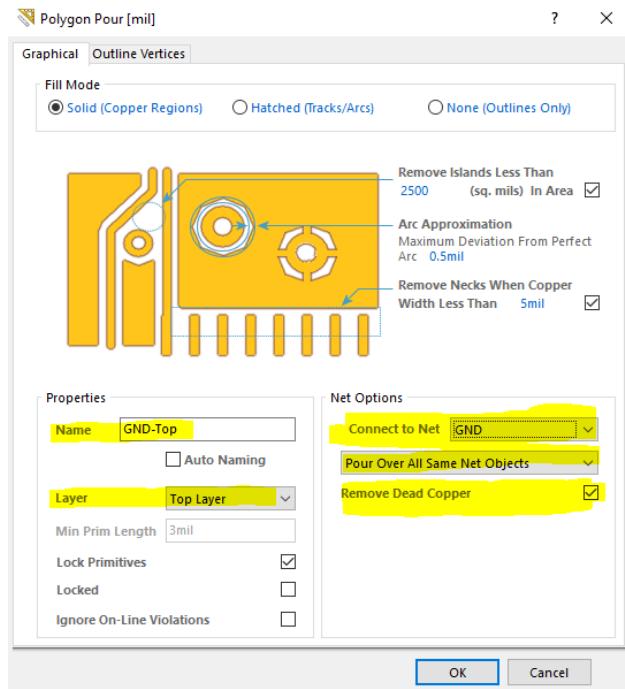


Figure 85: Altium PCB Polygon Pour Dialog.

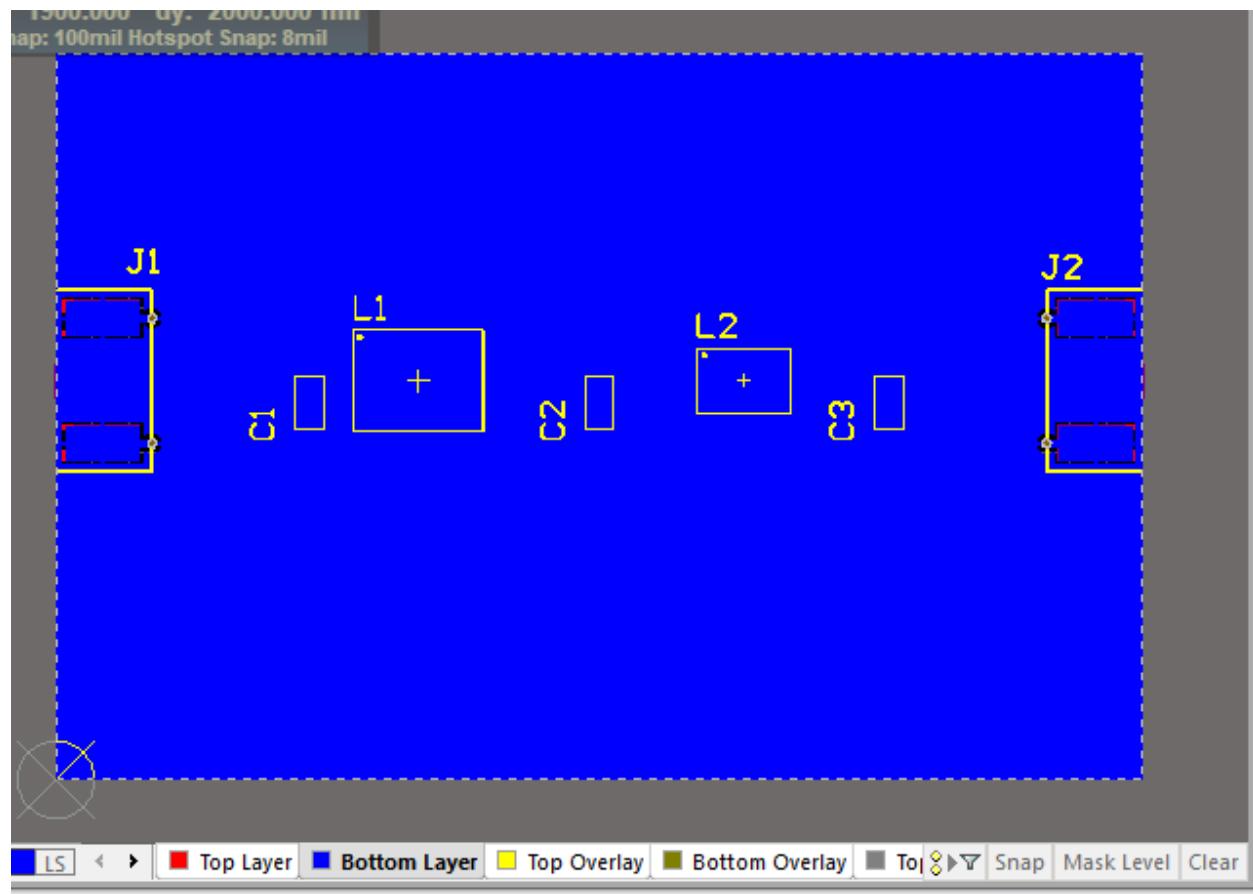


Figure 86: Altium PCB Polygon Pour placed on the Bottom Layer with net GND.

51. To connect the top and bottom layer vias are used. A via can be placed by pressing P than V first press **TAB** to set up the right parameters as shown in 87. The parameter Force complete tenting on top or bottom means that the via is not open the solder mask will cover it. Notice the drill hole size which is the minimum size possible by PCBway. Take care that the angular ring (Ar) is greater then the via hole. Place vias by hand and adjust grid resolution to simplify the task, as shown in Figure 88. Notice the thermal relieves around the pads which help by soldering but increase impedance. The thermal relieve could be eliminated by writing a rule if the engineer thinks it is a favorable design choice which you have to make and argue why.

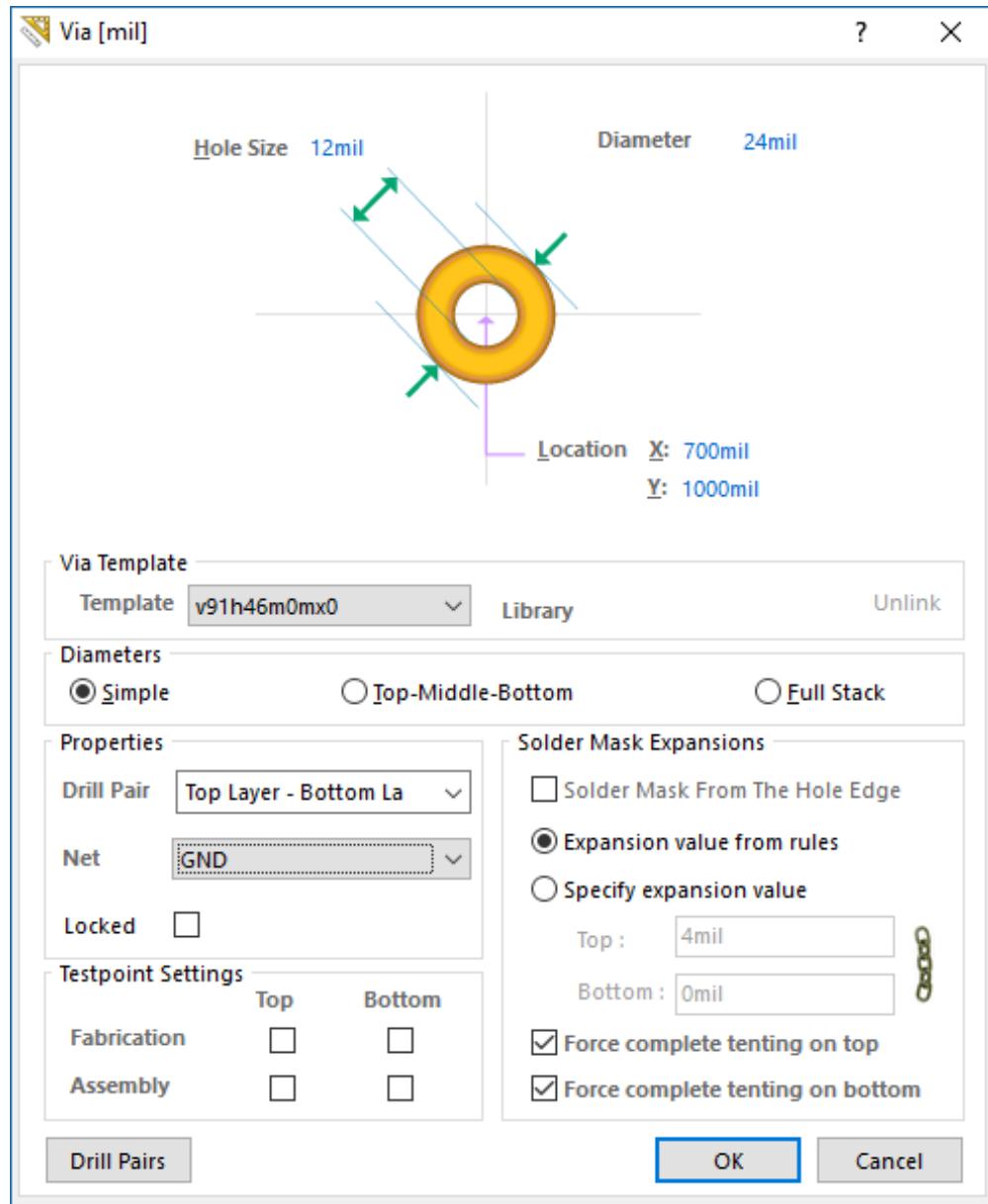


Figure 87: Altium PCB GDP Via Dialog.

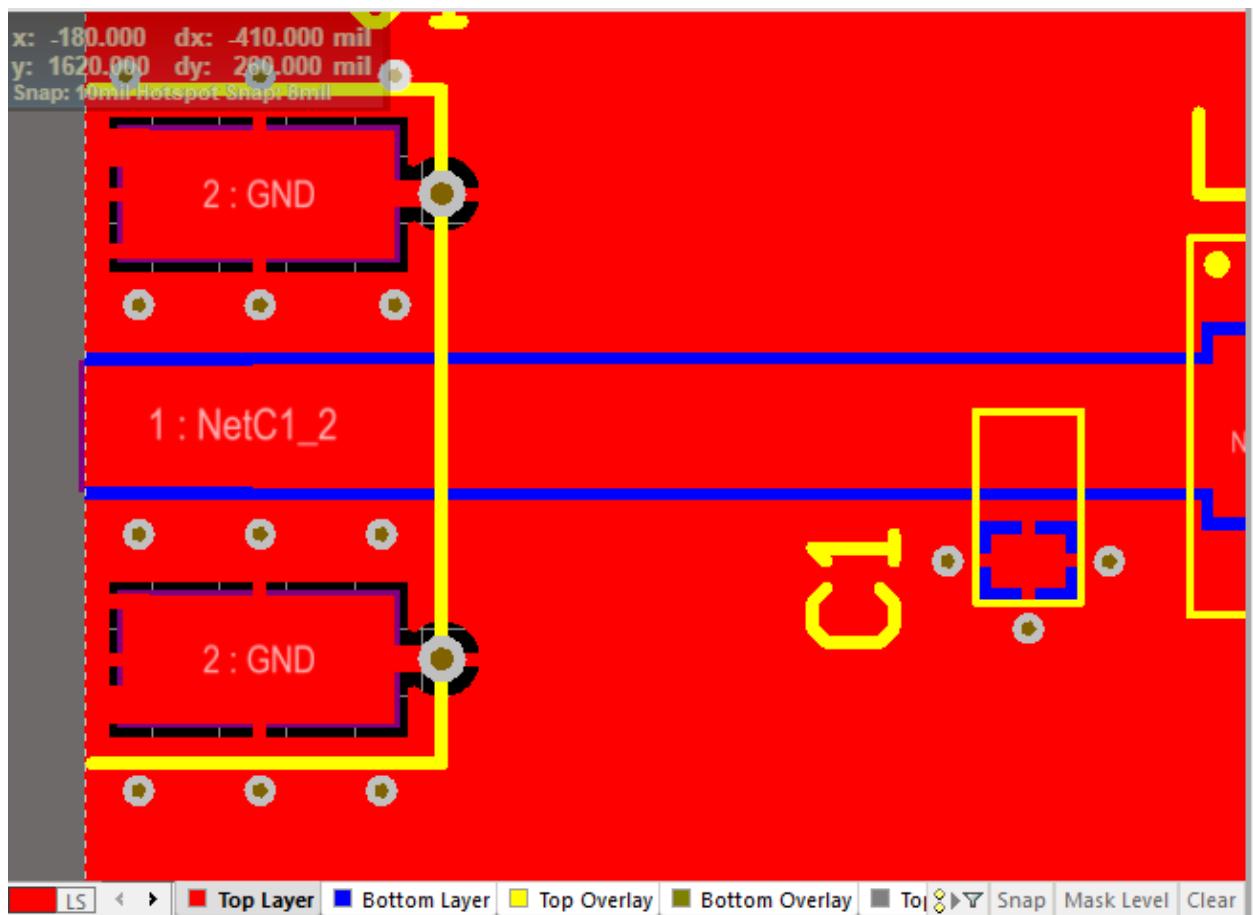


Figure 88: Altium PCB GND Via placement and thermal reliefs.

52. After polygons are placed you want to get it way temporarily because it prevents you from moving components. This can be done multiple ways but the polygon manager is the way that gives you the most flexibility. The polygon manager can be opened in menu bar **Tools** → **Polygon Pours**→ **Polygon Manager** which opens the **Polygon Manager** dialog shown in Figure 89. To shelf the polygons check the highlighted Shelfe boxes and press apply. Furthermore, you can use the polygon manager to change the rule for thermal relieves on pads. This can be done by press the button Create Polygon Connection Style Rule... which opens the Edit PCB Rule - Polygon Connect Style, as shown in Figure 90. This dialog lets you change the Connect Style which is now set to Relief Connect but you can set it to Direct Connector No Connect. Furthermore, There are Query that you can write an two are already generated for you. First Object Matches is set to All objects and Second Objects Matches is set to IsNamedPolygon('GND-Bottom'). This means the rule will be valid for all objects that are in the polygon named GND-Bottom.

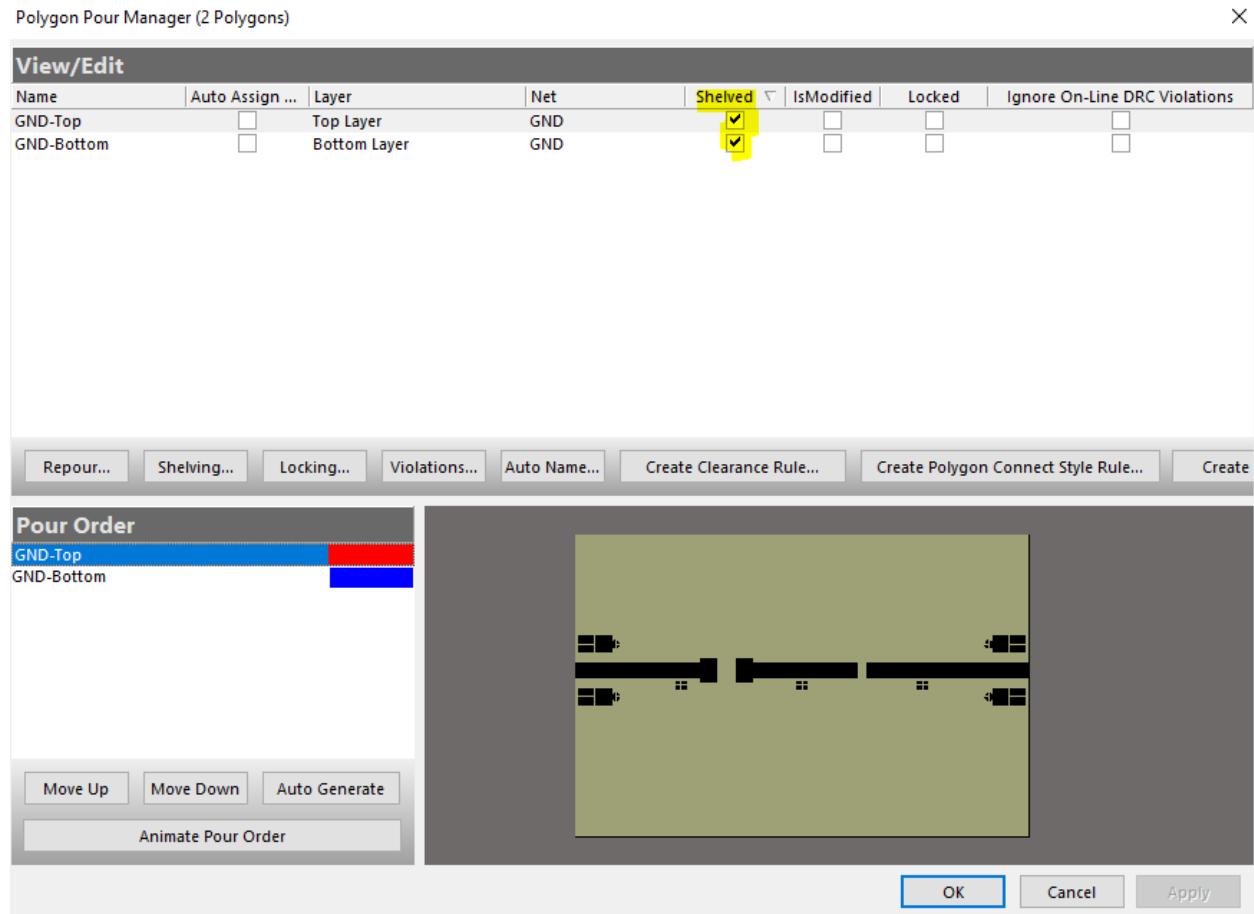


Figure 89: Altium PCB GDP Polygon Manager Dialog.

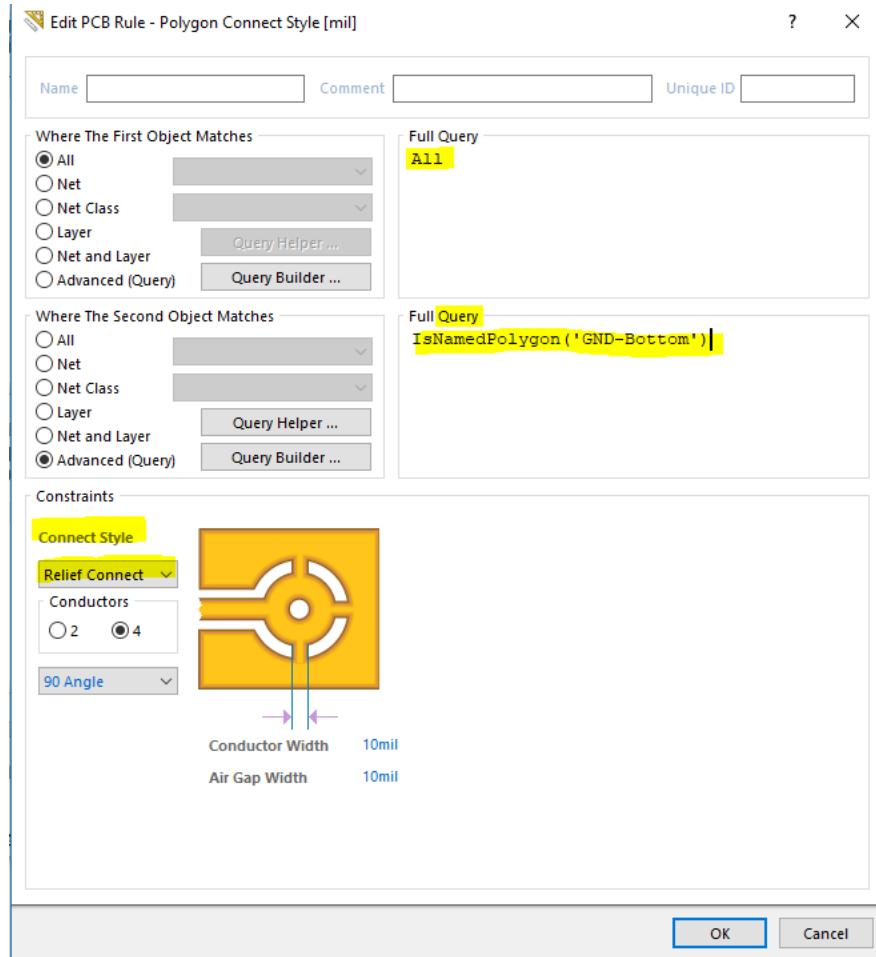


Figure 90: Altium PCB GND Polygon Connection Style Rule Dialog.

53. In terms of building query's which is one of the most important concepts of Altium take a look at the PCB filter view which allows you to use querys or design querys that can be used to build rules. Therefore we will use our predefined Net Class named TML_cn an filter for that. To do so you can use the query InNetClass('TML_cn'), as shown in Figure 91, and write that into the PCB Filter and press the button Apply to All. The nets that are in the net class TML_cn are highlighted. Now you can make a rule out of it by press Create Rule button and chose Clearance Constraint, as shown in Figure 92. Press OK which opens the PCB Rules and Constraints Editor in which you see there is a new clearance rule named Clearance_1 which you will rename to Clearance_TML.cn. You can see that the query defined in the PCB Filter is here written into the First Object Matches. Now the clearance distance is the same right now as the the general rule for all objects. To change the clearance between region and Pour polygons set the highlighted number from 10 mil clearance to 30 mil clearance. Press Apply and OK to close the dialog. In PCB Filter view press the Clear button to clear the filter selection. Now un-shelf the polygons with the polygon manager and repour (re-calculate the polygon shape with the new rules or changes made to it) the top polygon. Your screen should look similar to Figure 94, notice the blue marked via that is connected to ground while the rest of the board edge distributed vias is not connected to ground. This happens because a via that is copied does not have a net and if it does not hit a net while it is pasted into the document it will remain as no net. This happened because as I copied the vias the bottom and top polygon was shelfed.

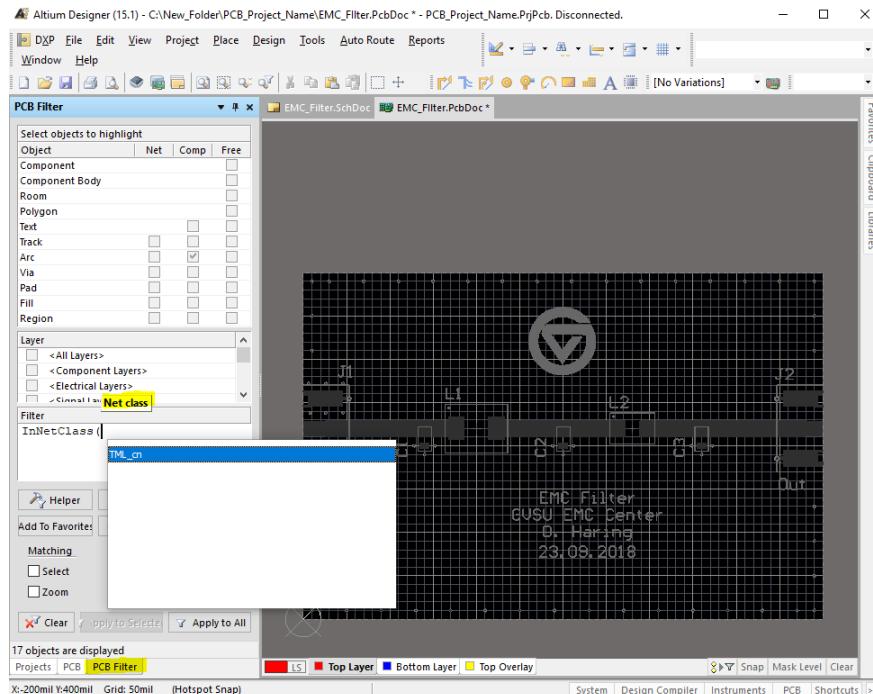


Figure 91: Altium PCB GDP Polygon Manager Dialog.

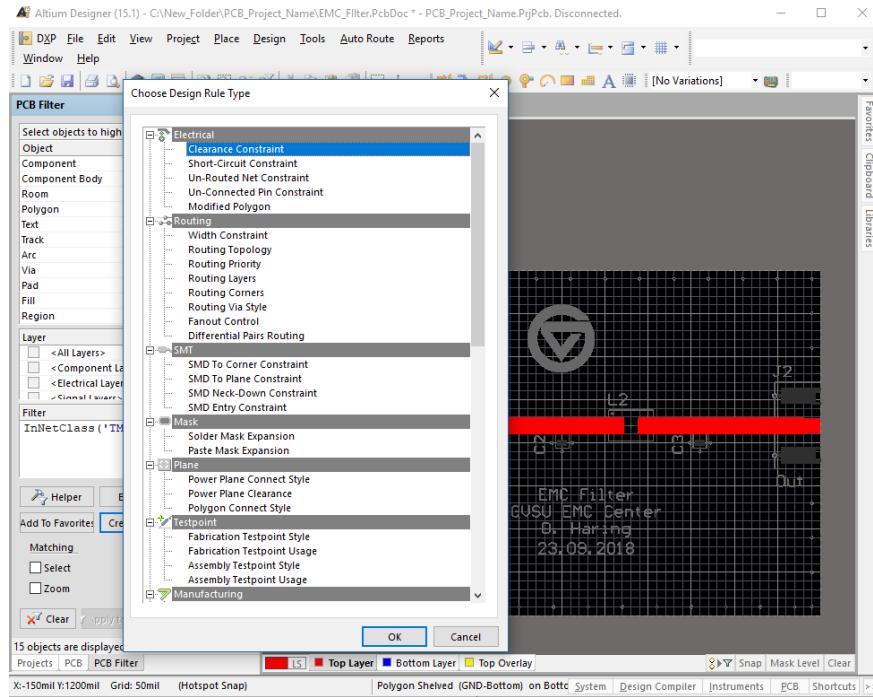


Figure 92: Altium PCB GDP PCB Filter Create Rule

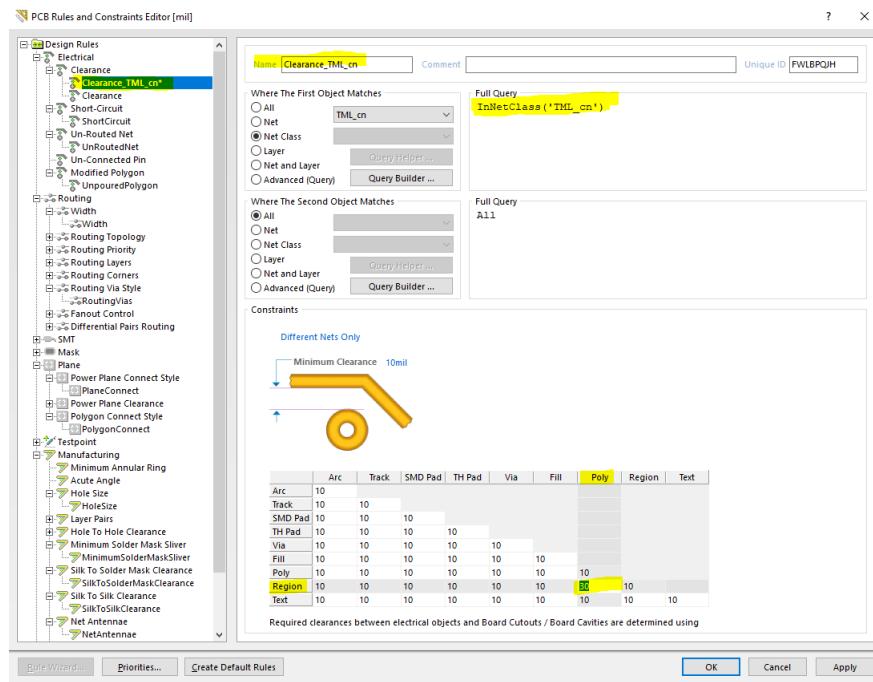


Figure 93: Altium PCB GDP PCB Filter Create Rule

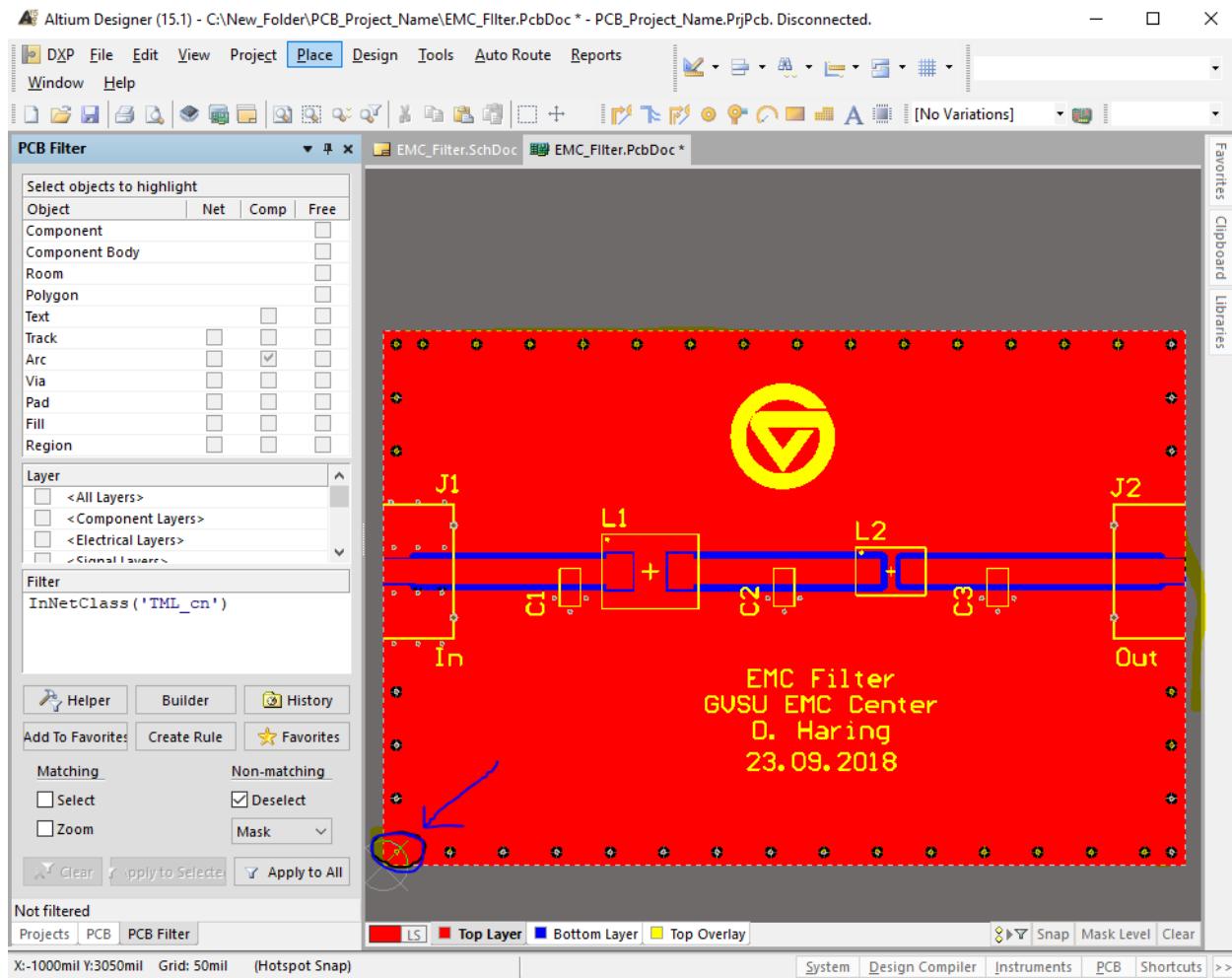


Figure 94: Altium PCB GDP Created Clearance Rule for TMF_cn net class.

54. To avoid single double click on each via and change the net use the Find similar objects tool in combination with the **PCB Inspector** view. The **Find Similar Object** tool is used by selecting a via with no net then right click on it and select Find Similar Object as shown in Figure 95. The Find Similar Objects dialog will appear where you see that the object kind is via, the Net is No Net, and we search for all objects that are via and have no net that's why both lines have instead of selected Any, selected Same. To search you have to press first the button Apply and then OK to close the dialog. To the left in the same figure you see the PCB Inspector view which can be found if not opened to the left bottom by clicking on the highlighted PCB. In the PCB Inspector you can now change once the net from No Net to GND for all selected objects. Now you have to repour the polygons both bottom and top to connect the vias to the GND net. This can be done by **right click on the board chose Polygon Actions and chose Repour All**.

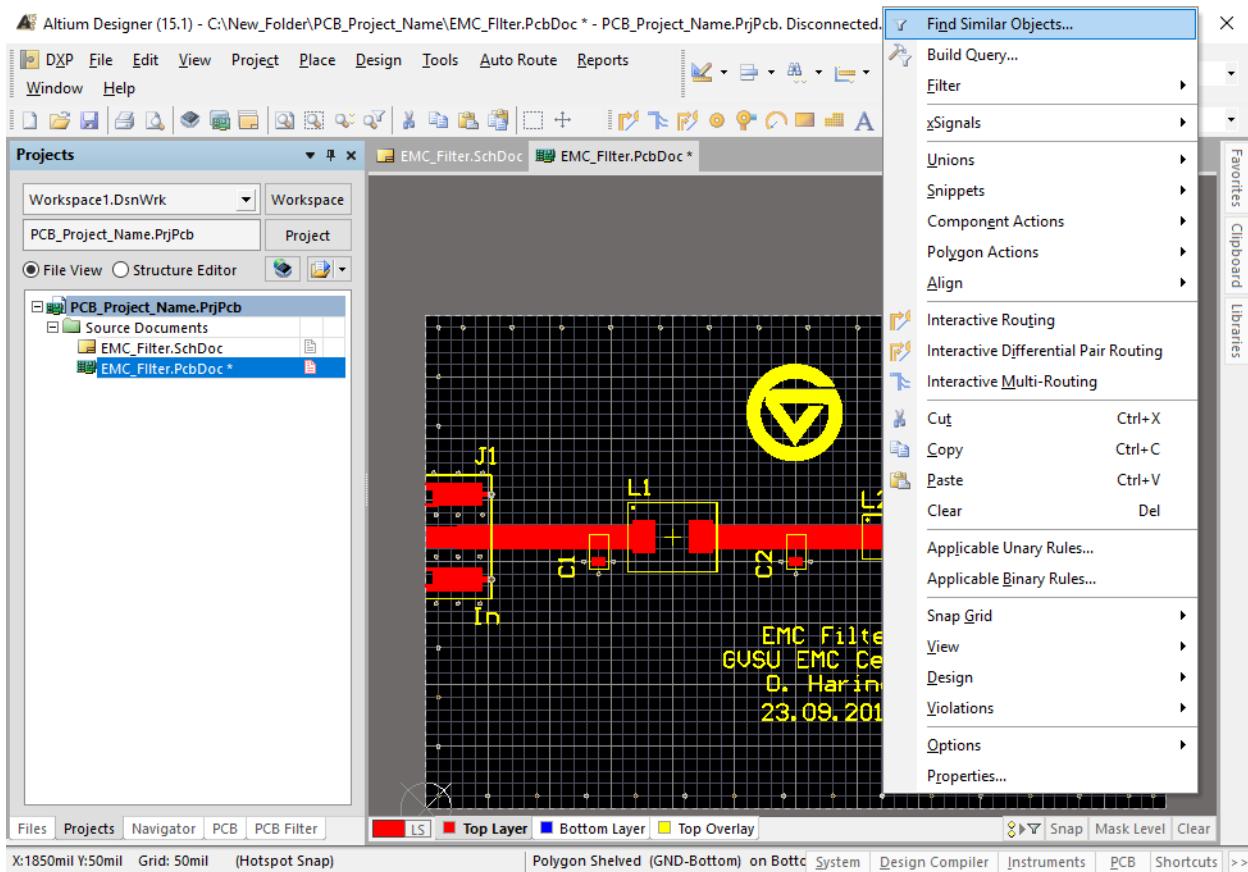


Figure 95: Altium PCB GND Placed vias around the edge, and Find Similar Objects...

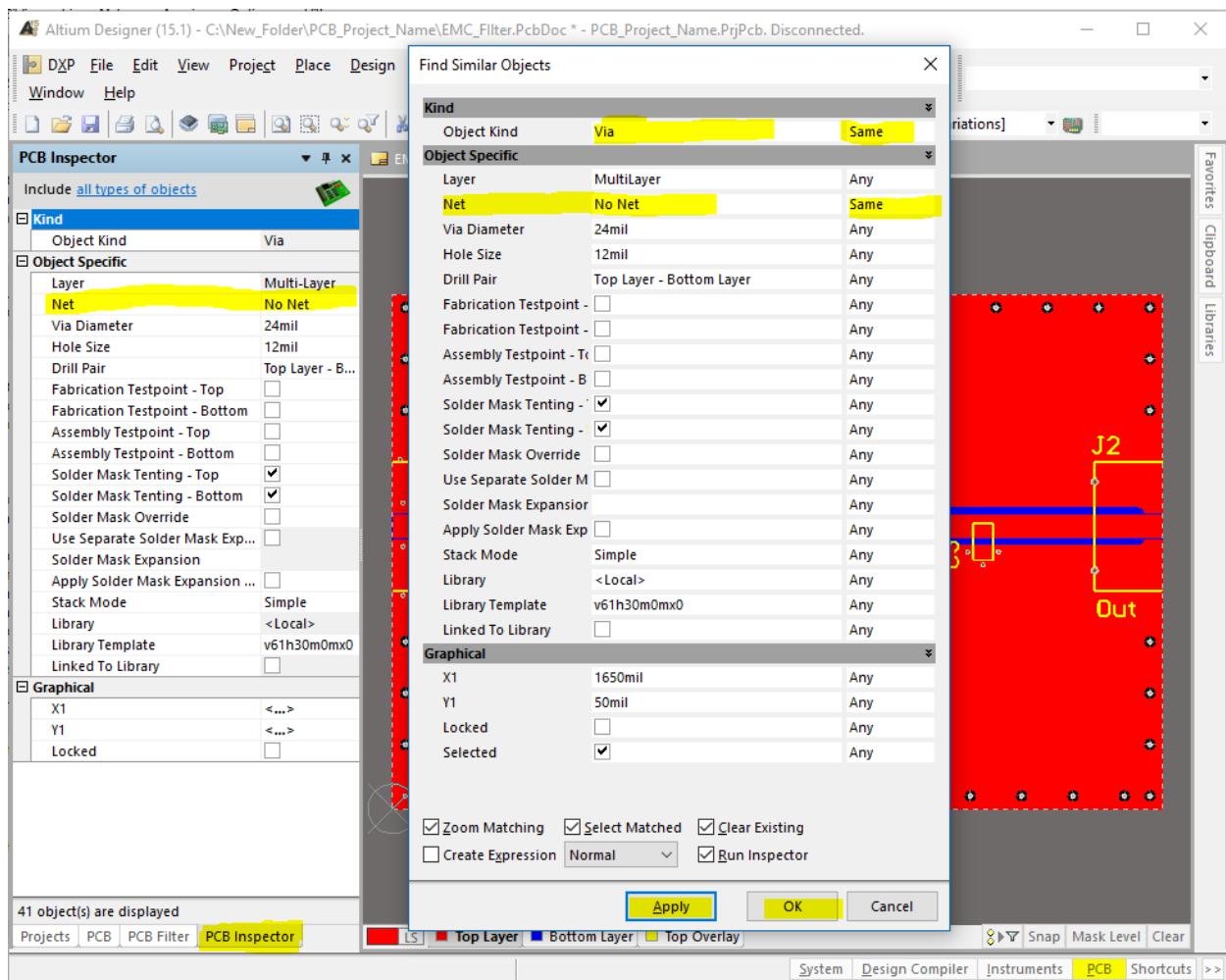


Figure 96: Altium PCB GDP Find Similar Objects... and PCB Inspector.

55. To improve the ground impedance use the Via Stitching tool by chose in menu bar Tools → Via Stitching/Shielding → Add Stitching to Net... which opens the dialog Add Stitching to Net. Use 200 mil as grid distance and a12724 mil via dimension, check Force tenting top and bottom and connect the Stitching to net GND than press OK. It will pop up a Window that informs you about how many vias got placed. Do not chose a too dense grid p bother wise you may achieve the opposite of what you want to achieve and blocking the return current with holes.

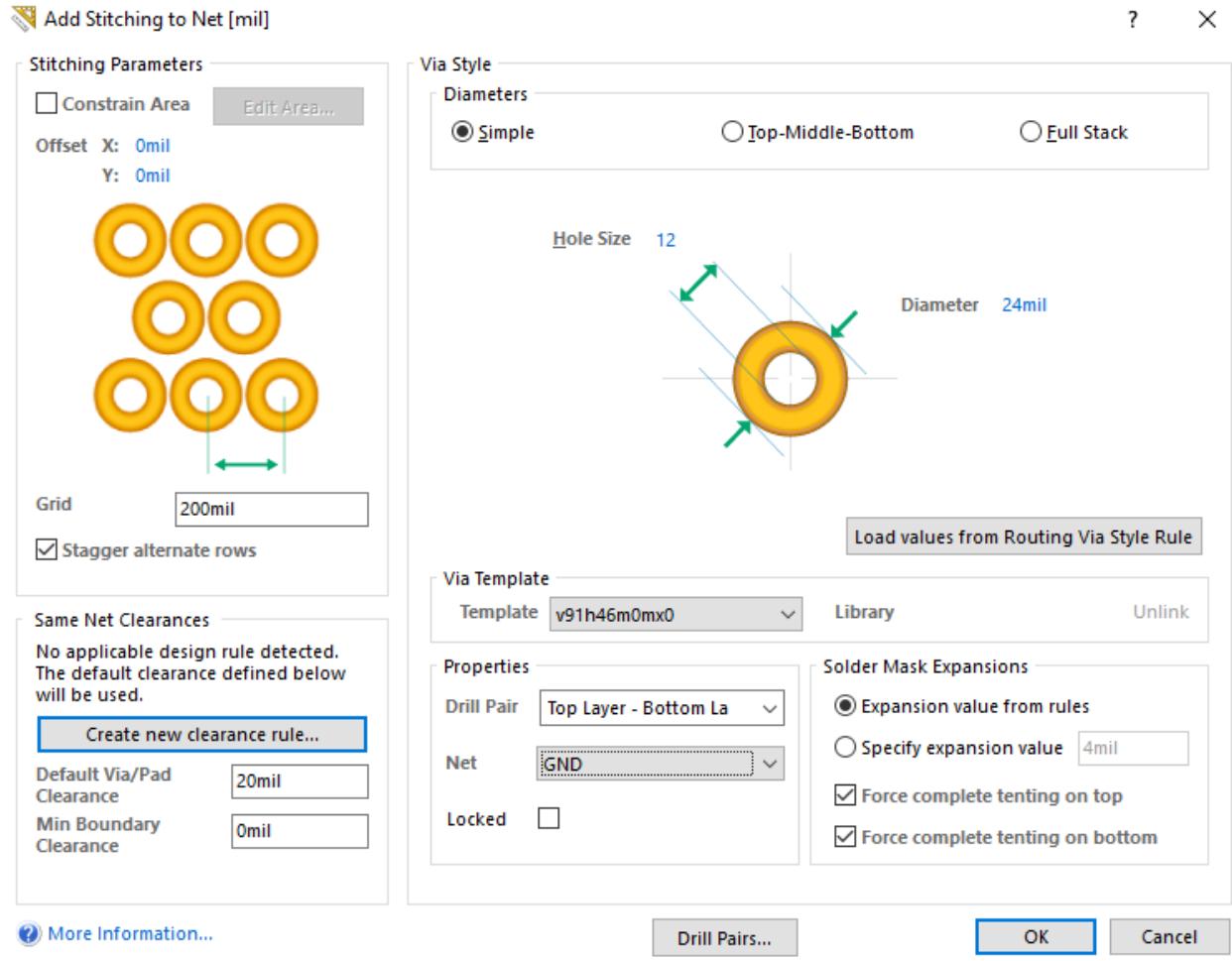


Figure 97: Altium PCB GDP Via Stitching dialog.

3.6.3 GDP Silkscreen

56. After the routing is finished place additional text onto the silkscreen layer top and bottom if necessary, Figure 98 shows the top silkscreen. A text string is placed by pressing P then press S. Furthermore, the layer stack can be placed as well as example on the bottom silkscreen. Press P and then chose Layer Stack Table from the tool tip menu. Press Tab to open the Layer Stack Table dialog and un-check Draw Board Map and change text width to 6 mil and text height to 36 mil, press OK. It is important to place the layer stack table first on the top silkscreen than drag and hold it and press L which mirrors the component onto the bottom layer. To check if it is mirrored correctly switch the view to 3D view by press 3 and flip the board to check that the layer stack is shown correctly, as shown in Figure 99. To flip the board in 3D view right click on the highlighted place to open the shown menu and click Flipped. The 3D view is a very effective tool to proof that the design is correct. The concept of mirroring from top to bottom is important if a component an integrated chip (IC) is only flipped to the bottom sight the footprint will be wrong so take special care that the part is it should be.

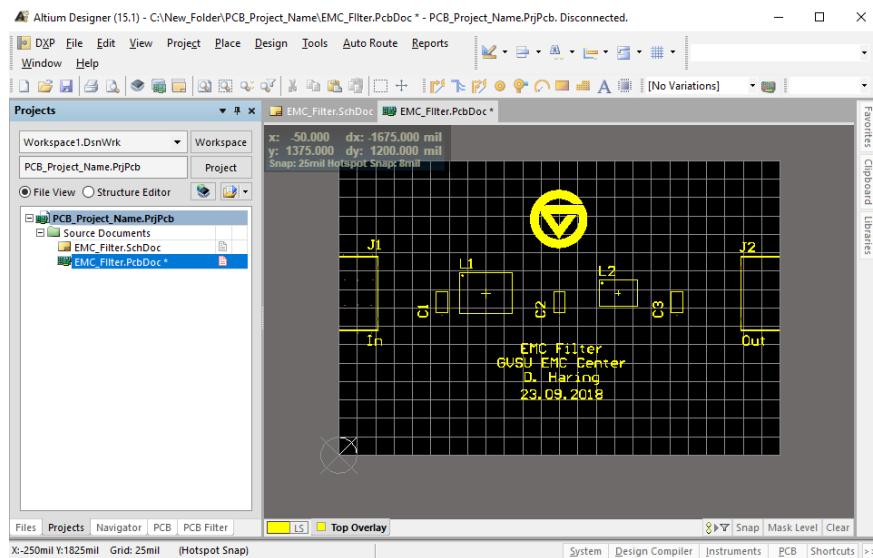


Figure 98: Altium PCB GDP Silkscreen.

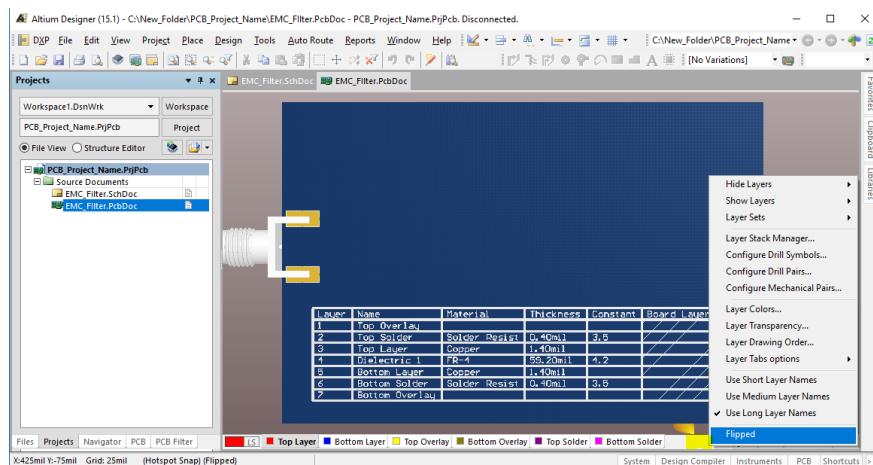


Figure 99: Altium PCB GDP Layer Stack Table bottom silkscreen.

3.6.4 GDP Drill Drawing Layer add additional info for manufacturer

57. A simple and effective way to present documentation needed for the manufacturer is to put additional information into the Drill Drawing Layer. Common are the Drill Table, Layer Stack Table and Manufacturer Instructions 4.2, as well as mechanical measurements. In Altium version 17 an additional document type was introduced called Draftsman document that allows to import the design and measure it out in older Altium versions a Mechanical layer or Drill drawing layer is used to.

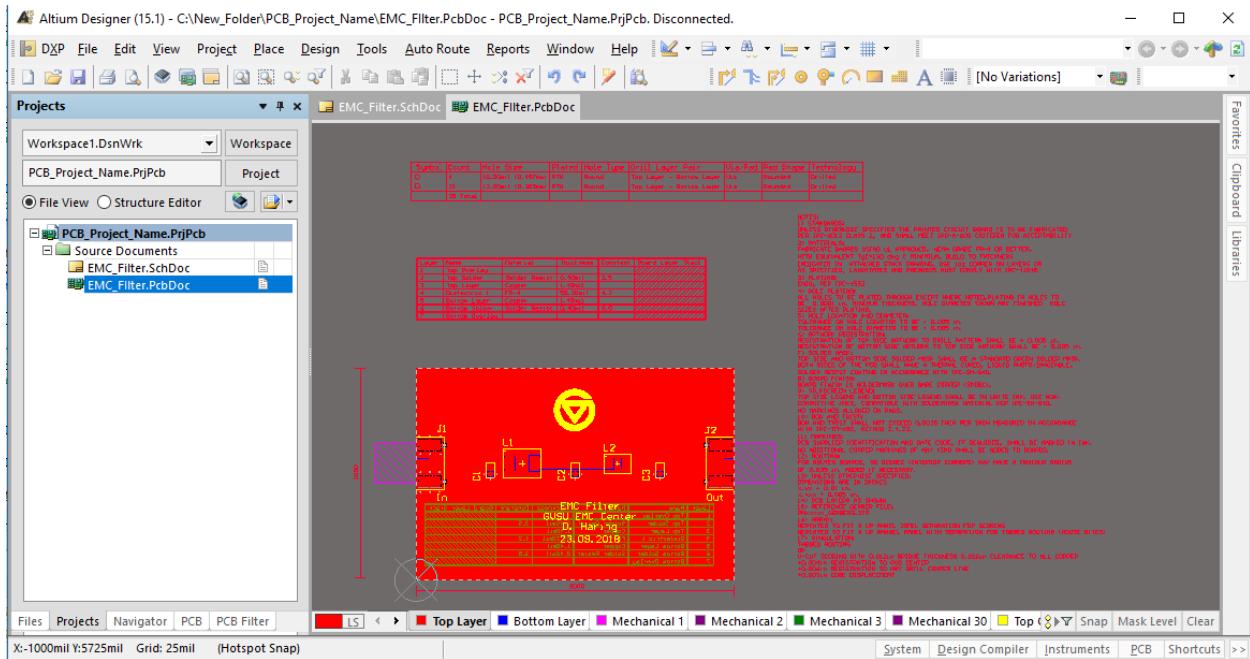


Figure 100: Altium PCB GDP Drill Drawing.

3.6.5 GDP Design Rule Check (DRC)

To perform a design rule check (DRC) in menu bar chose **Tools → Design Rules Check...** which opens the Design Rule Check dialog. To perform the DRC simply press the button to lower left side of the dialog named **Run Design Rule Check...**. The generated output should look similar to what is shown in Figure 101. The DRC generates a report file that pops up as well if there are violations those are shown in the Message view. To resolve the issues open the PCB design file and double click on an violation in message view, the screen will jump to spot where the violation occurred. Sometimes, it is necessary to increase the zoom to encounter the problem. As example a Silk To Solder Mask Clearance Constraint Violation was double clicked in the Messenger view and is shown in Figure 102. Now it seems kind of clear that the foot print himself is the issue which yields two options to resolve the issue, first change the footprint in the integrate library and updated it. Second, check on the manufacturer rules what is the minimum value for this rule and change the clearance rule accordingly. The clearance rule can be changed by using the filter and make a separate rule for all components footprints or just change the rule for all objects. Altium v17 would present a third option where violations can be simply waved. The author decided to check on the manufacturer rules are he could not find one on PCBway but knowing that the minimum line width for silkscreen is 6 mil leads to the assumption that the spacing to a different object would be equal or not smaller then 6 mil. Therefore, He changed all silk screen rules to 7 mil minimum value. Now you run the DRC again and there are only 10 rule violations left which belongs all to the bottom layer stack. Know that we ensured that no footprint is involved actually we do not care if the bottom layer stack is not that nice so the silk to silk clearance rule can be now set to 0 mils which leads in the worst that some lines are overlapping. After running the DRC again following output was achieved see Figure 103 which shows zero violations. After successfully proofed that the design is OK you can give it into review.

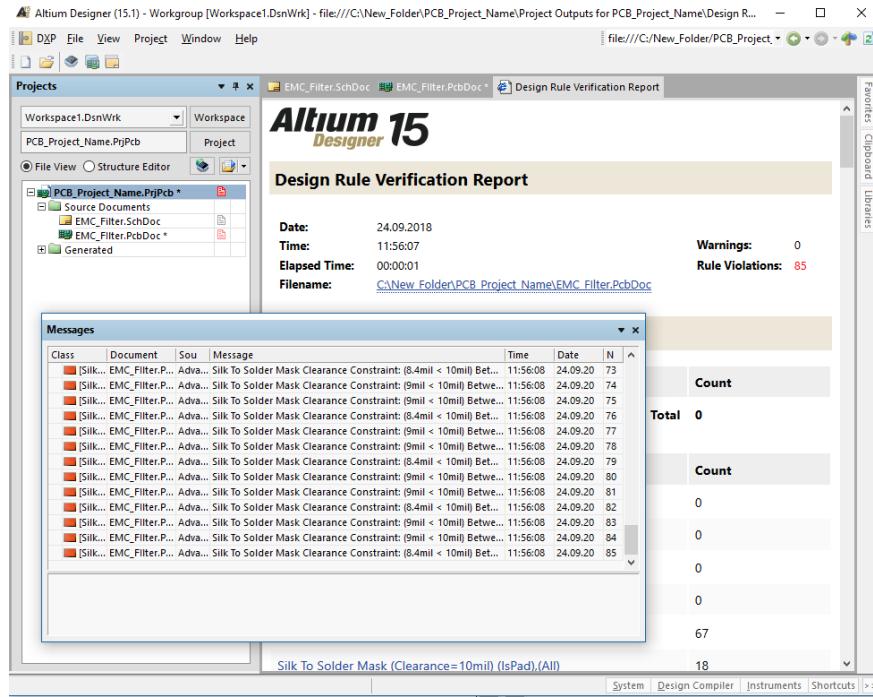


Figure 101: Altium PCB GDP Design Rule Check results.

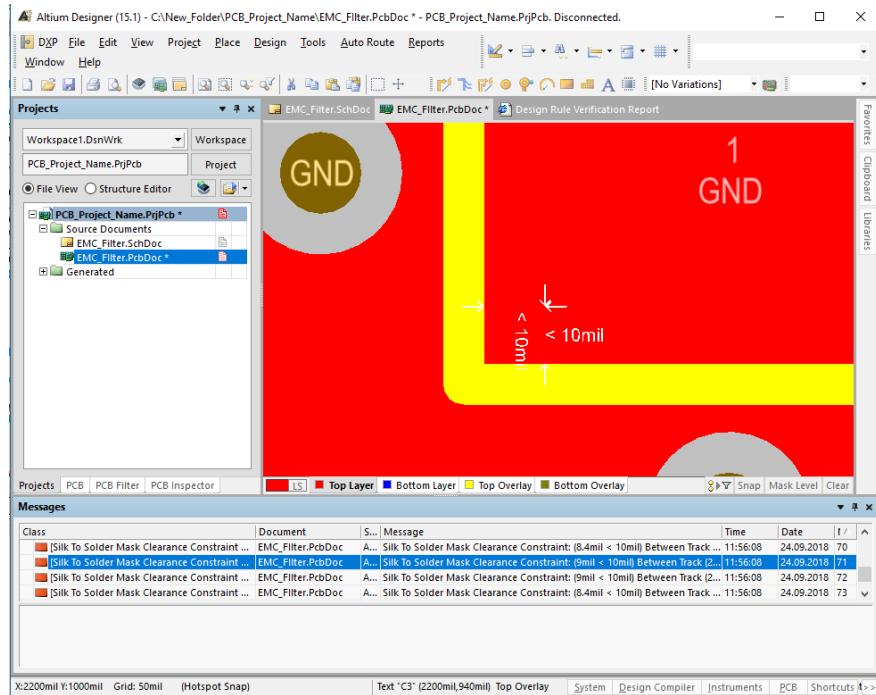


Figure 102: Altium PCB GDP Silk To Solder Mask Clearance Constraint Violation.

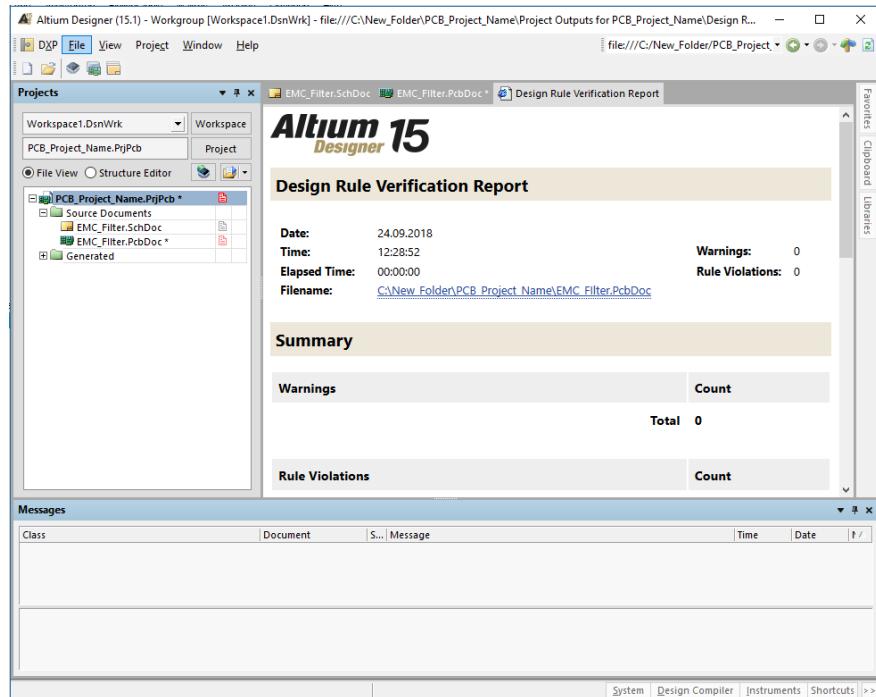


Figure 103: Altium PCB GDP DRC shows no violation.

3.6.6 GDP Output Job

A good design software usually provides tools for documentation, in Altium it is an OutJob file that is used to generate reports in form of organized ordering of your documents. Go ahead and add an Output Job file to your project by right click on project and chose **Add New to Project → Output Job File**. After the output job file is generated you have to add documents which you would like to add to the pdf generator on the right, see Figure 104. The order of documents is indicated with the small green numbers how the documents will be ordered in the pdf file. Altium provides a huge variety of different files that can be generated, the most common are schematic, assembly view, 3D view, Drill Drawing, DRC report, and Bill of Material. Altium can also generate fabrication outputs as Gerber files and NC Drill files which are the ones sent to a manufacturer for production. Those documents need review before sending to the manufacturer, just in case something was wrong generated as example! Good manufacturer houses send sometimes their edited Gerber and drill files back to you for review and final approval. The output files are generated and stored into a folder as shown in Figure 105.

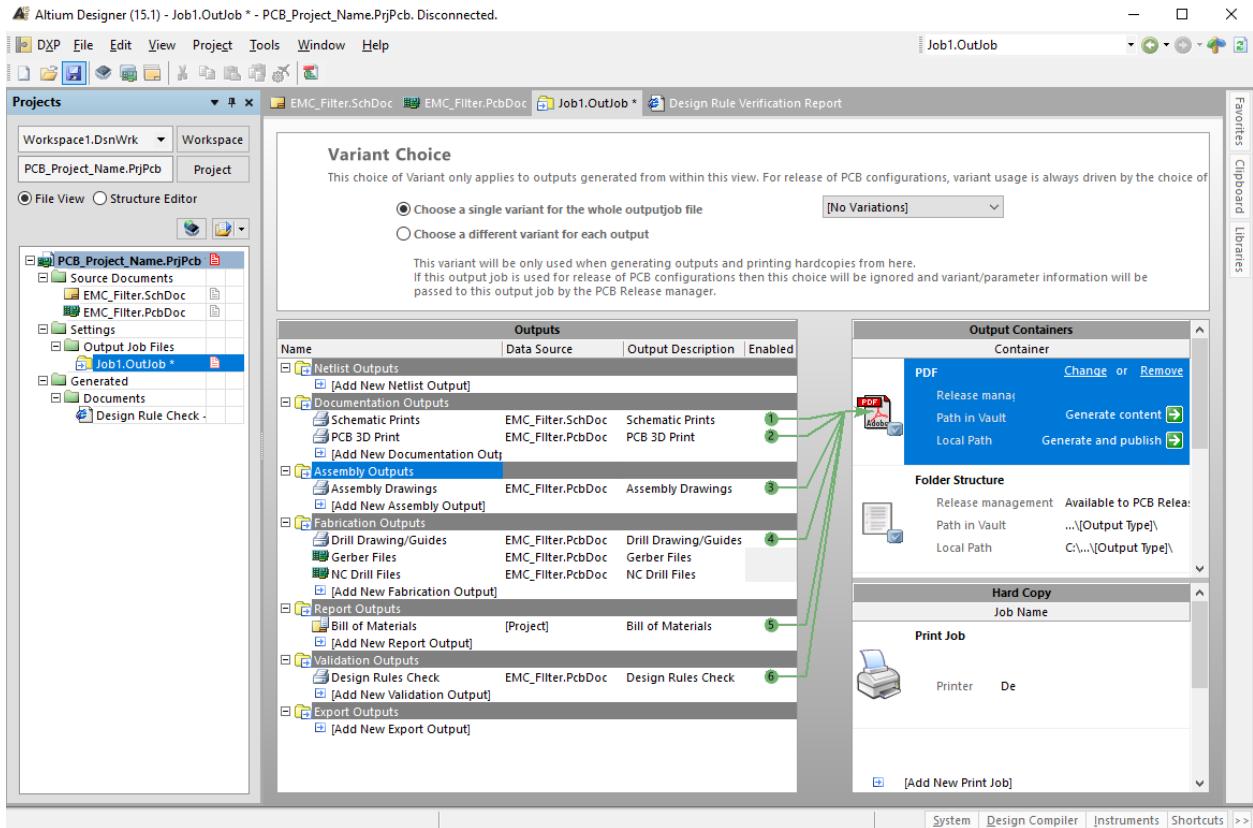


Figure 104: Altium PCB GDP Output job pdf.

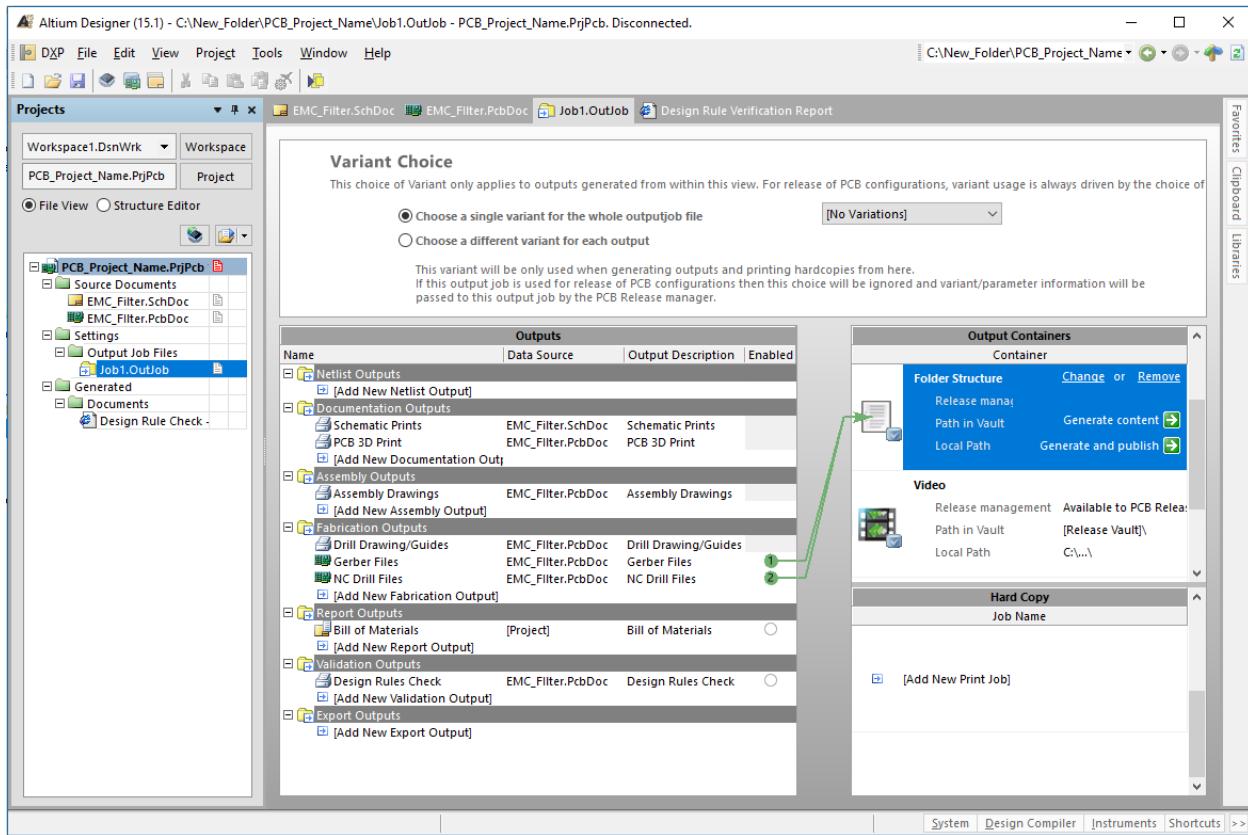


Figure 105: Altium PCB GDP Output job fabrication.

58. Gerber files are used as interface to the manufacturer. Each layer in the stack up will generate one Gerber file that is used for fabrication. By double click on the Gerber file the Gerber File dialog opens and the General register should look as shown in picture 106. Which should be the default setting. Be aware that the manufacturer you chose may have different demands and guidelines so double check on those. The next register is the Layer where you can independently choose which layer shall be generated and which not. A simple recommendation is to use the Plot Layers button and choose Used On. Which enables all layers that contain data in it.

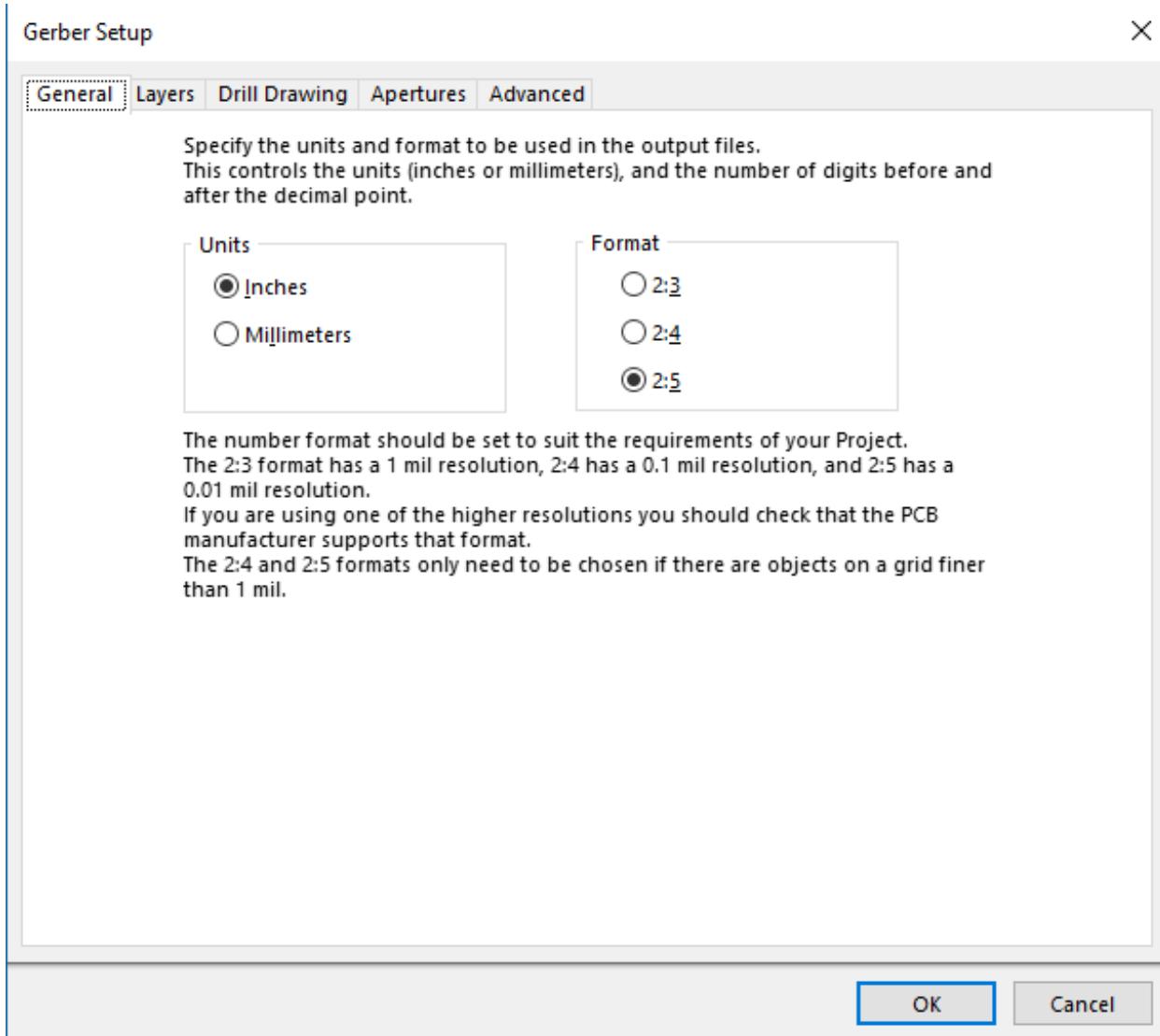


Figure 106: Altium PCB GDP Gerber Setup General.

Gerber Setup

X

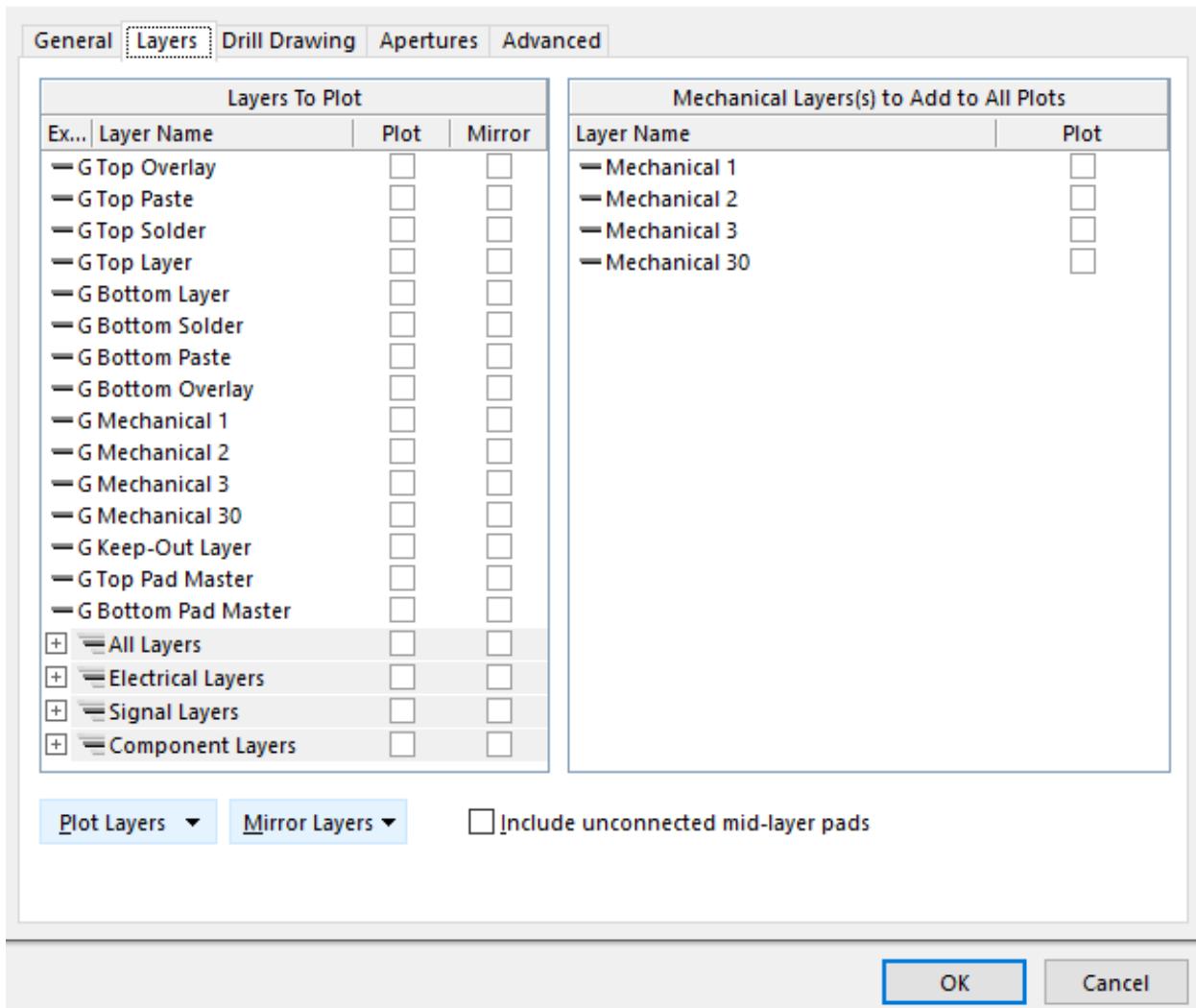


Figure 107: Altium PCB GDP Gerber Setup Layers.

59. The NC Drill files set up can be left default in most cases if not otherwise demanded by your board manufacturer. Figure 108 shows the default settings and your setup should look similar to that. The NC Drill file is a *.txt file.

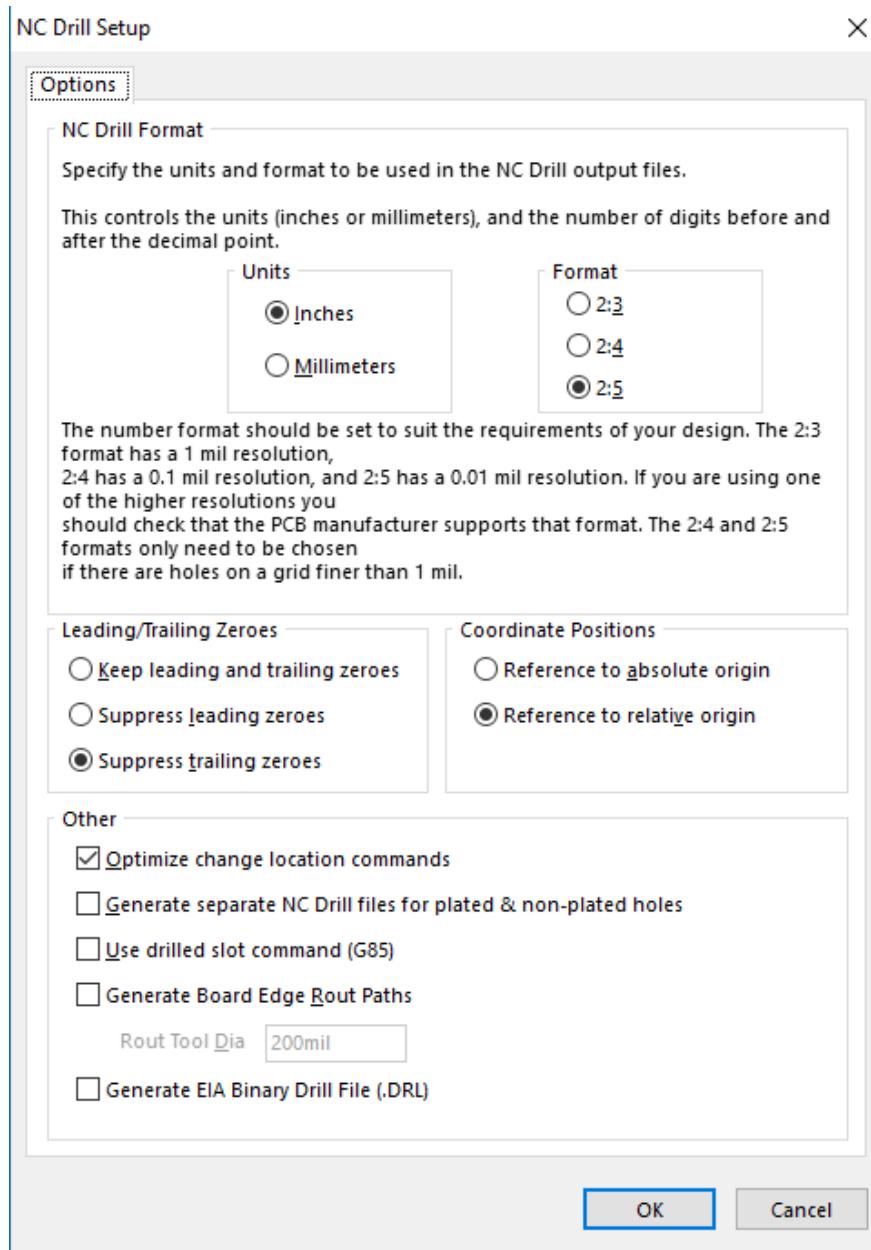


Figure 108: Altium PCB GDP NC Drill files.

60. The generated output files should look as shown in Figure 109. Notice the *.TXT file and when it is open it shows the drill holes while the rest of the files are named in a short abbreviation of the layer name. By comparison of the naming of this figure with Figure 107 it is clear while there are named in this way.

Hint: Altium has not the best CAM file viewer there are other products then Altium which make more sense to check the Gerber file output as example ViewMate which has a free ware version.

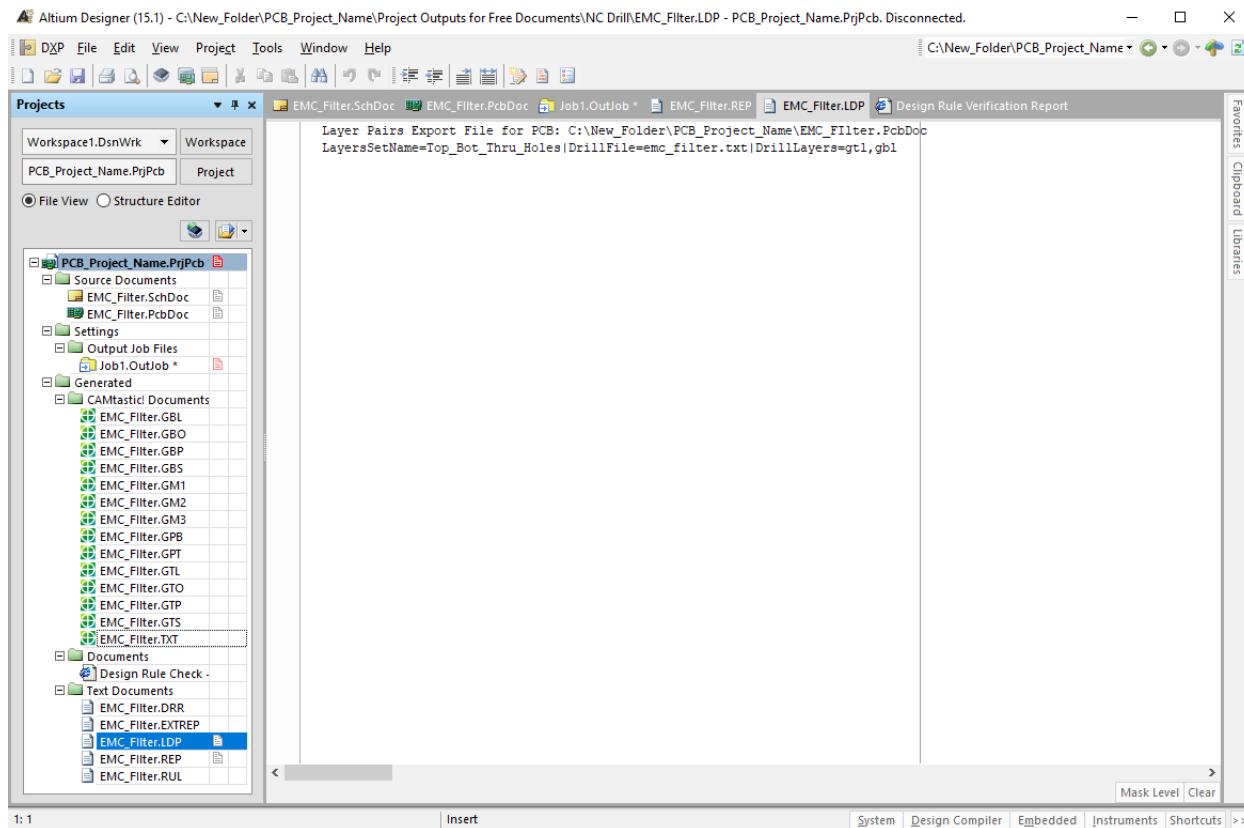


Figure 109: Altium PCB GDP CAM files.

61. Review of the Gerber files in View mate shows that the bottom layers thermal relieves where not changed to direct connect which does not make a lot of sense especially for the vias because there is nothing soldered. This how important it is to review your own work and search for bugs that can be easily corrected before fabrication!

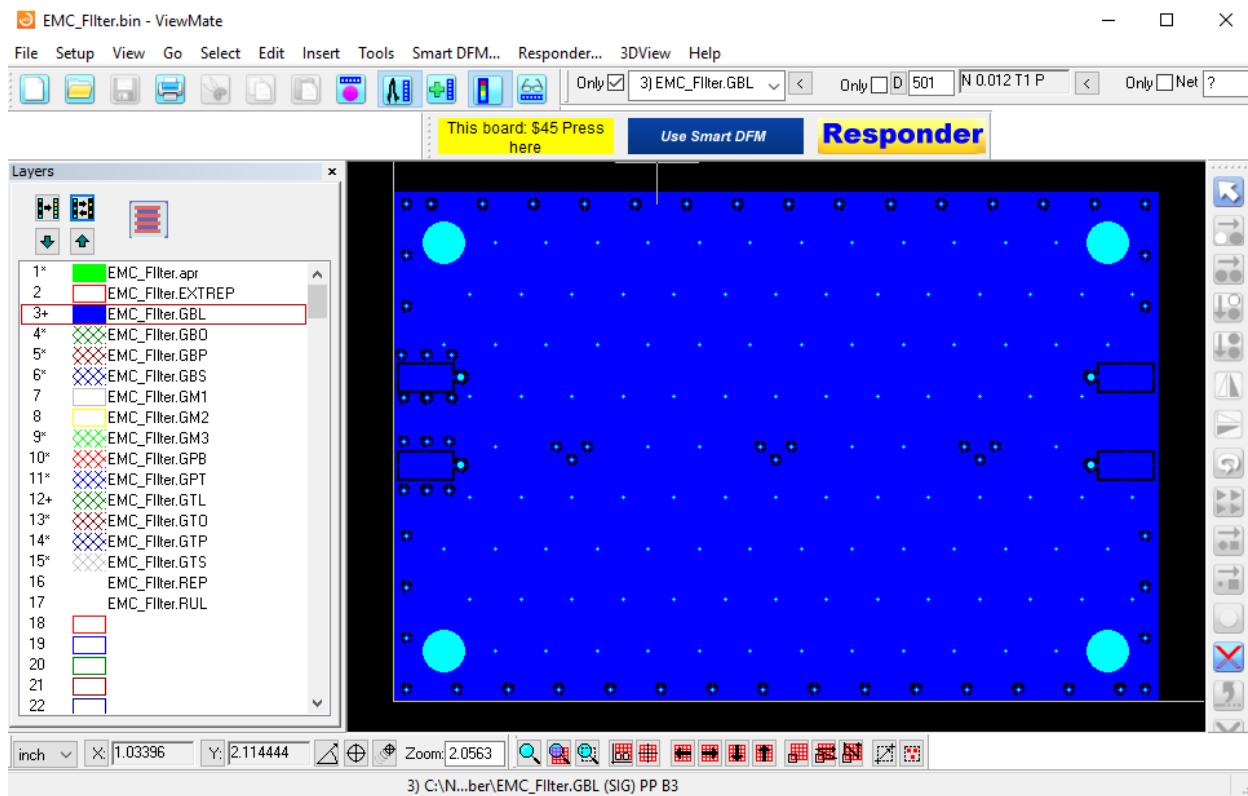


Figure 110: Altium PCB GDP Gerber files and Drill file loaded in View Mate.

62. The BOM is an important part as soon as it comes to ordering parts and optimizing number of parts to reduce costs in production. Therefore, generate an Excel file and use appropriate columns and group the components in a way it makes sens, an example is shown in Figure 111.

Bill of Materials For Project [PCB_Project_Name.PjPcb] (No PCB Document Selected)

The dialog shows a table of components with columns: Designator / Value, Description, Footprint, and Quantity. Below the table are sections for Grouped Columns, All Columns, Source Options, Supplier Options, Export Options, and Excel Options. The 'File Format' is set to Microsoft Excel Worksheet (*.xls; *.xlsx; *.xlsm). Buttons at the bottom include Menu, Export..., OK, and Cancel.

Designator / Value	Description	Footprint	Quantity
C1, C2, C3	1uF 0805 Ceramic Chip Capacitor - Standard	0805CAP	
J1, J2	0732511150 Molex CONN SMA RCPT STR 500OHM EDGE MNT 18 GHz	SMA_Molex_board_edge	
L1	22uH 2525 VISHAY IHLP Automotive Inductors	2525IND	
L2	0.1uH 1616 VISHAY IHLP Automotive Inductors	1616IND	

Grouped Columns

All Columns

- FREQUENCY
- Height(Mil)
- Height(mm)
- Ibis Model
- ImagePath
- Index
- Irms
- ItemGUID
- Library Name
- Library Reference
- LibRef
- CanonicalDesignator

Source Options

- Include Not Fitted Components
- Include Parameters From PCB
- Include Parameters From Vault
- Include Parameters From Database
- Include in Component Variations

Supplier Options

- <none>
- Production Quantity 1
- Round up Supplier Order Qty to cheaper price break
- Use cached pricing data in parameters if offline

Export Options

File Format Microsoft Excel Worksheet (*.xls; *.xlsx; *.xlsm)

- Add to Project
- Open Exported

Excel Options

Template:

- Rglative Path to Template File

OK Cancel

Figure 111: Altium PCB GDP BOM.

4 Appendix

4.1 Newer file formats from version 15.1 to 17.1

File in Newer Format	
Version	Warning
Release 15.1	CAUTION - Support Multi-line PCB Text added.
Release 16.0	CAUTION - Pad/Via hole size tolerance value added.
Release 17.0	CAUTION - Component parameters added.
Release 17.0	CAUTION - Supports of backdrilling
Release 17.1	CAUTION - Support of waived violations
Release 17.1	CAUTION - Support of object specific keepouts

This file was generated by a later version of the software

Figure 112: Altium changes and added features of different Altium versions.

4.2 Manufacturer Instructions Drill Drawing Layer

NOTES:

1) STANDARDS:

UNLESS OTHERWISE SPECIFIED THE PRINTED CIRCUIT BOARD IS TO BE FABRICATED PER IPC-6012 CLASS 2, AND SHALL MEET IPC-A-600 CRITERIA FOR ACCEPTABILITY

2) MATERIALS:

FABRICATE BAORDS USING UL APPROVED, NEMA GRADE FR-4 OR BETTER, WITH EQUIVALENT $T_{gE}=130$ deg C MINIMUM. BUILD TO THICKNESS INDICATED IN ATTACHED STACK DRAWING. USE 1oz COPPER ON LAYERS OR AS SPECIFIED, LAMINTATES AND PREPREGS MUST COMPLY WITH IPC-4104B

3) PLATING:

ENIG, PER IPC-4552

4) HOLE PLATING:

ALL HOLES TO BE PLATED THROUGH EXCEPT WHERE NOTED. PLATING IN HOLES TO BE 0.0001 in. MINIMUM THICKNESS. HOLE DIAMETER SHOWN ARE FINISHED HOLE SIZES AFTER PLATING.

5) HOLE LOCATION AND DIAMETER:

TOLERANCE ON HOLE LOCATION TO BE + 0.005 in.

TOLERANCE ON HOLE DIAMETER TO BE + 0.005 in.

6) ARTWORK REGISTRATION:

REGISTRATION OF TOP SIDE ARTWORK TO DRILL PATTERN SHALL BE + 0.005 in.

REGISTRATION OF BOTTOM SIDE ARTWORK TO TOP SIDE ARTWORK SHALL BE + 0.005 in.

7) SOLDER MASK:

TOP SIDE AND BOTTOM SIDE SOLDER MASK SHALL BE A STANDARD GREEN SOLDER MASK. BOTH SIDES OF THE PCB SHALL HAVE A THERMAL CURED, LIQUID PHOTO-IMAGEABLE, SOLDER RESIST COATING IN ACCORDANCE WITH IPC-SM-840.

8) BOARD FINISH:

BOARD FINISH IS SOLDERMASK OVER BARE COPPER (SMOBC).

9) SILKSCREEN LEGEND:

TOP SIDE LEGEND AND BOTTOM SIDE LEGEND SHALL BE IN WHITE INK. USE NON-CONDUCTIVE INKS, COMPATIBLE WITH SOLDERMASK MATERIAL PER IPC-SM-840.

NO MARKINGS ALLOWED ON PADS.

10) BOW AND TWIST:

BOW AND TWIST SHALL NOT EXCEED 0.0035 INCH PER INCH MEASURED IN ACCORDANCE WITH IPC-TM-650, METHOD 2.4.22.

11) MARKINGS:

PCB SUPPLIER IDENTIFICATION AND DATE CODE, IF REQUIRED, SHALL BE MARKED IN INK. NO ADDITIONAL COPPER MARKINGS OF ANY KIND SHALL BE ADDED TO BOARDS.

12) ROUTING:

FOR ROUTED BOARDS, 90 DEGREE (INTERIOR CORNERS) MAY HAVE A MAXIMUM RADIUS OF 0.039 in. ADDED IF NECESSARY.

13) UNLESS OTHERWISE SPECIFIED:

DIMENSIONS ARE IN INCHES

x.xx + 0.01 in.

x.xxx + 0.005 in.

14) PCB LAYERS AS SHOWN:

15) REFERENCE GERBER FILE:

PNxxxxx_GERBERS.ZIP

16) ARRAY:

REPEATED TO FIT X UP PANEL 20MIL SEPARATION FOR SCORING

REPEATED TO FIT X UP PANNEL PANEL WITH SEPARATION FOR TABBED ROUTING (MOUSE BITES)

17) SINGULATION:

TABBED ROUTING

OR

V-CUT SCORING WITH 0.012in BRIDGE THICKNESS 0.020in CLEARANCE TO ALL COPPER
+0.004in REGISTRATION TO PCB CENTER
+0.006in REGISTRATION TO ANY DRILL CENTER LINE
+0.003in EDGE DISPLACEMENT

4.3 Shortcuts

Shortcut	Description
CTRL+Mouse Wheel	Zoom into document
CTRL+S	Save selected document
G	Press "G" to change the grid
P	Press "P" as your mouse is over an open document to open placement options.
TAB	Component properties while placing the component.
S	Menu for selection to chose selection options.
SPACE	Rotates component while hovering it with mouse or placing it.

Table 1: Shortcuts for the schematic document.

Shortcut	Description
CTRL+Mouse Wheel	Zoom into document
CTRL+Select Layer	Highlight specific layer
CTRL+S	Save selected document
G	Press "G" to change the grid it rotates 10 mil, 5 mil, 1 mil
P	Press "P" as your mouse is over an open document to open placement options.
Q	Press "Q" to Toggle Units.
TAB	Component properties while placing the component.
SPACE	Rotates component while hovering it with mouse or placing it.

Table 2: Shortcuts for the PCB document.

Shortcut	Description
CTRL+Click on Net	Highlight net
CTRL+Mouse Wheel	Zoom into document
CTRL+S	Save selected document
G	Press "G" to change the grid
L	Press "L" to change the layer stack
P	Press "P" as your mouse is over an open document to open placement options.
Q	Press "Q" to Toggle Units.
TAB	Component properties while placing the component.
SPACE	Rotates component while hovering it with mouse or placing it.

Table 3: Shortcuts for the PCB document.

Unit A	Unit B
1 mm	39.37 mil \approx 40 mil
1 inch	1000 mil

Table 4: Shortcuts for the PCB document.

4.4 Vishay inductor data sheet lp16ab11



www.vishay.com

IHLP-1616AB-11

Vishay Dale

IHLP® Commercial Inductors, Low DCR Series



DESIGN SUPPORT TOOLS click logo to get started



FEATURES

- Shielded construction
- Lowest DCR/ μ H, in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- Excellent DC/DC energy storage up to 1.0 MHz to 2.0 MHz. Filter inductor applications up to SRF (see "Standard Electrical Specifications" table)
- IHLP design. PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

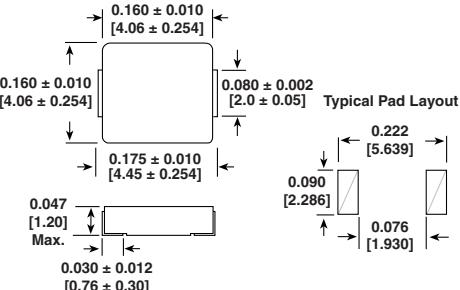


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- PDA / notebook / desktop / server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

DIMENSIONS in inches [millimeters]



Notes

- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +125 °C
- The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.
- Rated operating voltage (across inductor) = 40 V
- (1) DC current (A) that will cause an approximate ΔT of 40 °C
- (2) DC current (A) that will cause L_0 to drop approximately 20 %

DESCRIPTION

IHLP-1616AB-11	2.2 μ H	$\pm 20\%$	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC® LEAD (Pb)-FREE STANDARD

GLOBAL PART NUMBER

I	H	L	P	1	6	1	6	A	B	E	R	2	R	2	M	1	1
PRODUCT FAMILY				SIZE				PACKAGE CODE		INDUCTANCE VALUE				TOL.		SERIES	

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

Revision: 12-Oct-17

1

Document Number: 34194

For technical questions, contact: magnetics@vishay.com

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4.5 Vishay inductor data sheet lp25cz8a



www.vishay.com

IHLP-2525CZ-8A

Vishay Dale

IHLP® Automotive Inductors, High Temperature (180 °C) Series



DESIGN SUPPORT TOOLS click logo to get started



Design Tools Available

FEATURES

- High temperature, up to 180 °C
- Shielded construction
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up to the SRF (see Standard Electrical Specifications table).
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- AEC-Q200 qualified
- IHLP design. PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE



Pb-free

RoHS

COMPLIANT

HALOGEN FREE

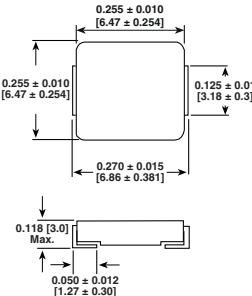
GREEN

(IS-2008)

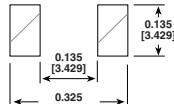
APPLICATIONS

- Engine and transmission control units
- Diesel injection drivers
- Noise suppression for motors: windshield wipers / power seats / power mirrors / heating and ventilation blower / HID lighting
- LED drivers

DIMENSIONS in inches [millimeters]



Typical Pad Layout (Min.)



STANDARD ELECTRICAL SPECIFICATIONS					
L ₀ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (μH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) ⁽¹⁾	SATURATION CURRENT DC TYP. (A) ⁽²⁾	SRF TYP. (MHz)
0.47	3.87	4.14	20.0	14.0	79.6
0.68	5.38	5.76	16.5	17.0	62.8
0.82	6.75	7.22	13.8	16.8	72.9
1.0	7.90	8.45	12.0	13.0	59.1
1.5	12.3	13.2	10.6	11.6	45.9
2.2	17.10	18.30	8.1	10.8	34.3
3.3	26.50	28.40	6.8	8.3	28.3
4.7	35.90	38.40	5.6	5.6	25.5
5.6	42.60	45.60	5.3	4.8	23.0
6.8	53.80	57.60	4.4	4.4	16.0
10	71.90	76.90	4.0	2.9	13.9
15	118.0	127.0	2.9	2.8	11.0
22	163.0	174.0	2.8	2.2	8.76

Notes

- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +180 °C
- The part temperature (ambient + temp. rise) should not exceed 180 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application
- Rated operating voltage (across inductor) = 75 V

⁽¹⁾ DC current (A) that will cause an approximate ΔT of 40 °C

⁽²⁾ DC current (A) that will cause L₀ to drop approximately 20 %

DESCRIPTION

IHLP-2525CZ-8A	22 μH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC® LEAD (Pb)-FREE STANDARD

GLOBAL PART NUMBER

I	H	L	P	2	5	2	5	C	Z	E	R	2	2	0	M	8	A
MODEL				SIZE				PACKAGE CODE		INDUCTANCE VALUE		TOL.		SERIES			

PATENT(S): www.vishay.com/patents

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Revision: 23-Oct-17

1

Document Number: 34362

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