Altium Tutorial v15.1

EGR 643 - PCB Design and EMC

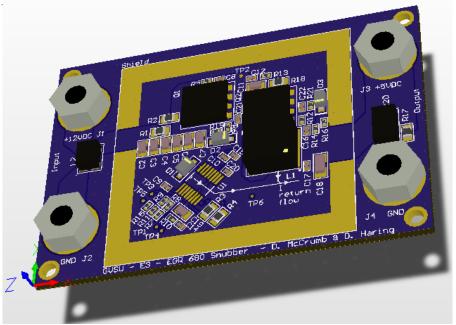
Dimitri Häring



Overview

- Mechanical drawings
- Layer stack up
- Cost approximation
- Snubber
- Schematic
- Layout
- Q&A



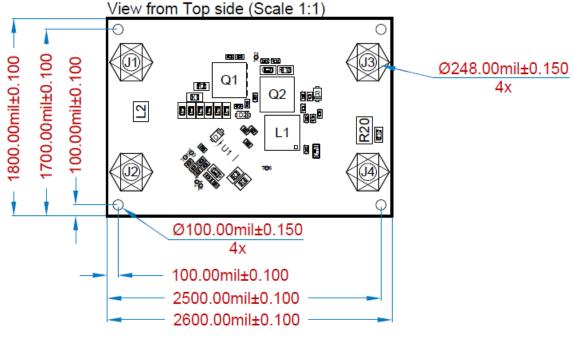


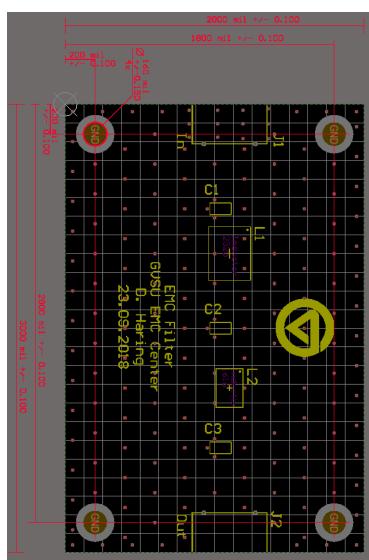
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Mechanical drawings

- Draftsman in Altium v17
- DrillDrawing Layer v15







Layer stack up

Layer		Material	Thickness	Constant	
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	10/0/0/0/0/0
3	Component Side	Copper	1.40mil		
4	Dielectric 1	FR-4	59.00mil	4.2	
5	Bottom Layer		1.40mil		
6	Solder Side	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2		Solder Resist			4
3			1.38mil		
4	Dielectric 1	1x 7628 ATO5 47% Resin TG130			
5			1.38mil		
6	Dielectric 2	6x 7628M 43% Resin TG150	44.49mil		
7	Signal Layer 1		1.38mil		
8	Dielectric 3	1x 7628 ATO5 47% Resin TG130			
9	GND Bottom		1.38mil		
10		Solder Resist			
11	Bottom Overlay				



Layer stack up

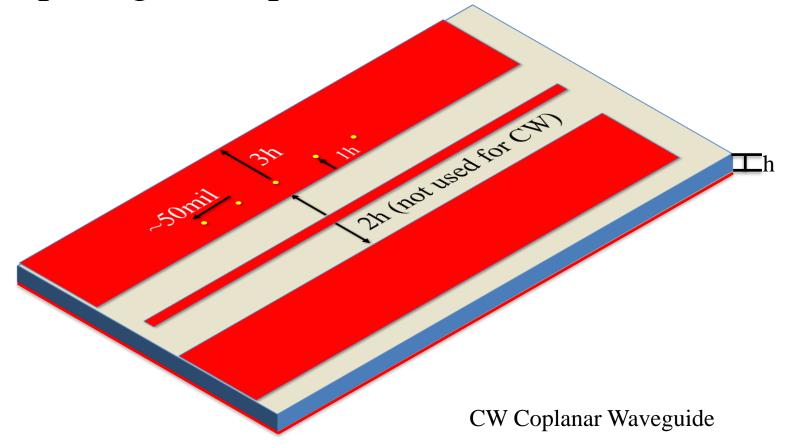
Check Gerbers from Manufacturer





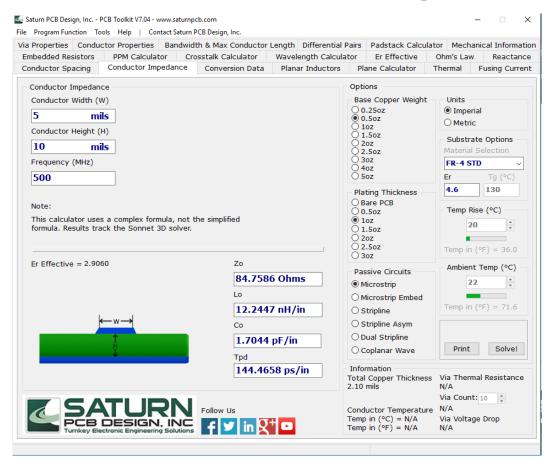
RF Grounded Microstrip or Coplanar Waveguide (CW)

spacing for impedance control





Saturn PCB Design Toolkit



A microstrip line with 50 Ohm impedance and a dielectric height of 10 mil, fc = 866 MHz, BW = 2 MHz, and 70 um copper, calculate;

Width:

Calculate the width and distance of CW for the same properties mentioned above:

Wi	A	+ 1	h	
vvı	(1			

Distance:

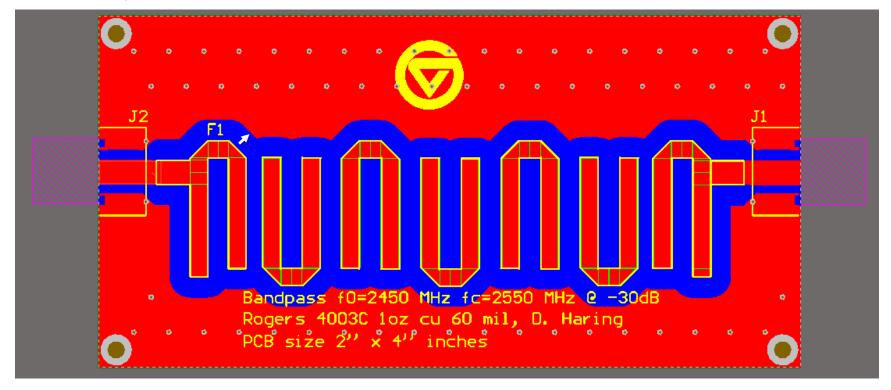
Link Saturn PCB Toolkit



10/3/2018

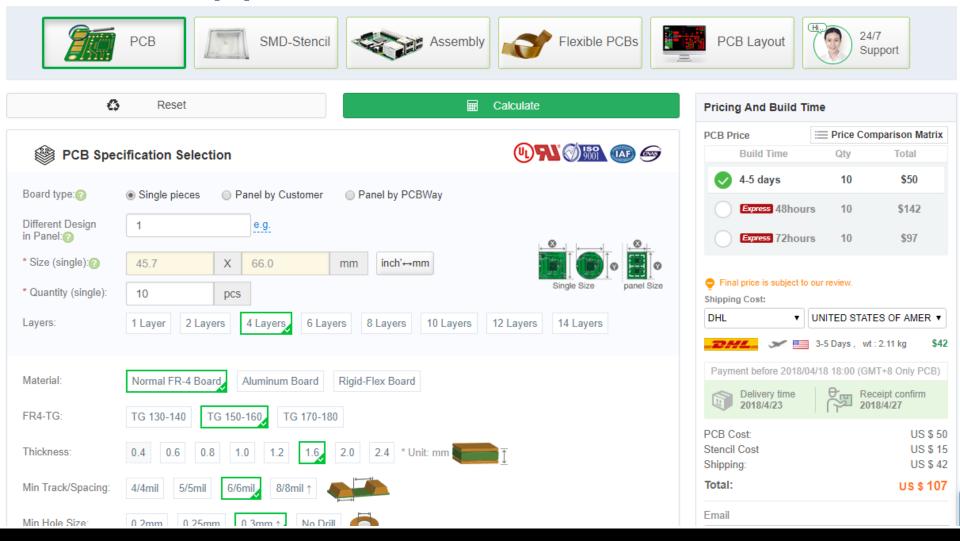
Filter with Microstrip design

Distance between coupled elements is the same as the 2h distance for the microstrip line. In this case, the distance rule of 2h is not valid.





Cost approximation \$62 -> \$107





10/3/2018

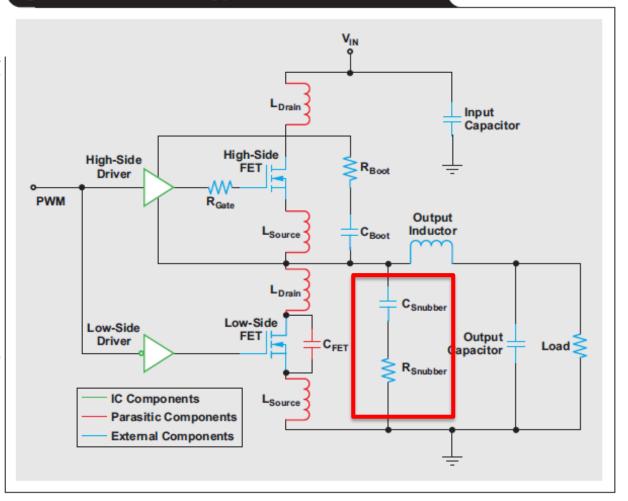
Snubber

Figure 1. Schematic showing parasitics of a buck converter

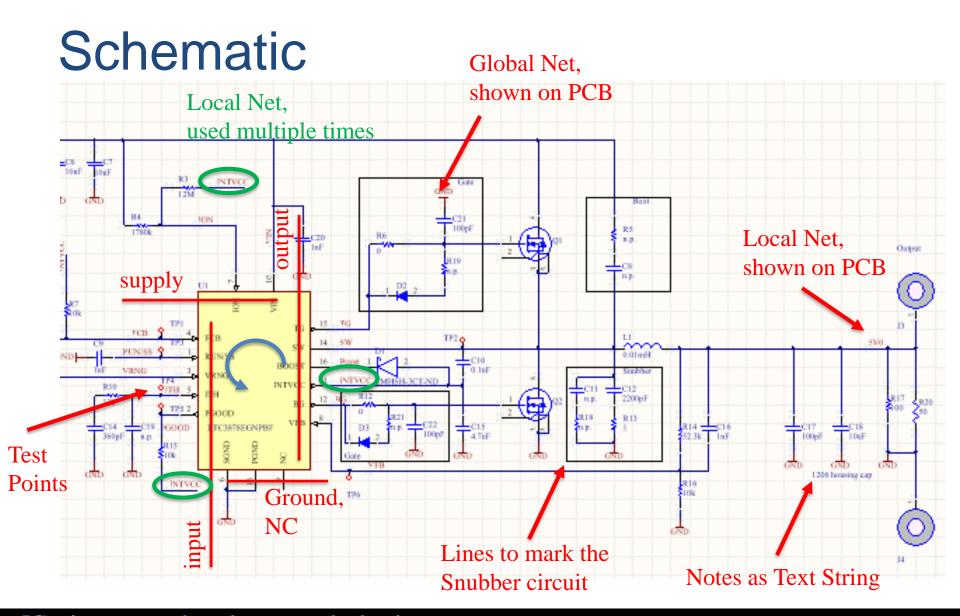
Using a snubber

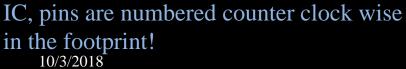
The third option to consider for reducing ringing is a snubber. The snubber circuit consists of a resistor and capacitor that are connected in series from the switch node to ground. The snubber circuit is used to damp the parasitic inductances and capacitances during the switching transitions. This circuit reduces the ringing voltage and frequency and also reduces the number of ringing cycles. This helps to reduce the EMI emitted by the system.

The procedure for choosing the capacitor and resistor components starts with measuring the ringing frequency of the original circuit. Once the frequency is determined, a capacitor is put in parallel with the low-side FET to change the ringing frequency to half the original value. When the frequency is half the original value, the parallel capacitor is equal to three times the parasitic capacitance of the original circuit. With the capacitance and frequency known, the parasitic inductance can be calculated by using the formula $f = \frac{1}{2}\pi\sqrt{LC}$, where f is the original ringing frequency and C is the parasitic capacitance. The resistor to critically damp the circuit is calculated from the equation $R = \sqrt{L/C}$. This resistor may or may not provide the necessary ringing reduction. Increasing the resistance results in an underdamped system, which allows more ringing but decreases power dissipation. Increasing the capacitance reduces the ringing but increases power dissipation. For the example, using a 2200-pF capacitor and a $1-\Omega$ resistor reduced ringing to 19.1 V.











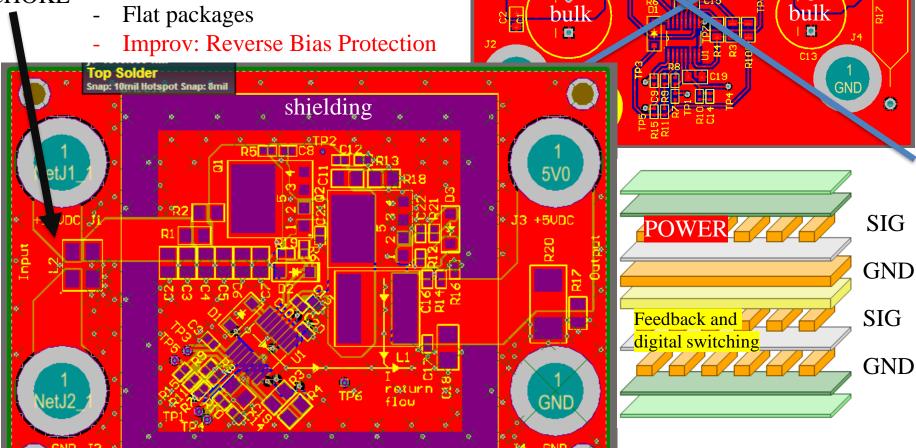
SMPS

Switched Mode Power Supply

- Shielding, Top Paste

CHOKE

- 45° degree angel safes space



%680/Snubber *-∞0. McCrumb & D. Waring.



5V0

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Bottom Layer

The bottom overlay can be used for additional information or to safe space on the top layer.





Questions





Thank you for your attention.



References

[1] "File:Overview icon.svg - Wikimedia Commons." [Online]. Available: https://commons.wikimedia.org/wiki/File:Overview_icon.svg. [Accessed: 10-Apr-2018].

